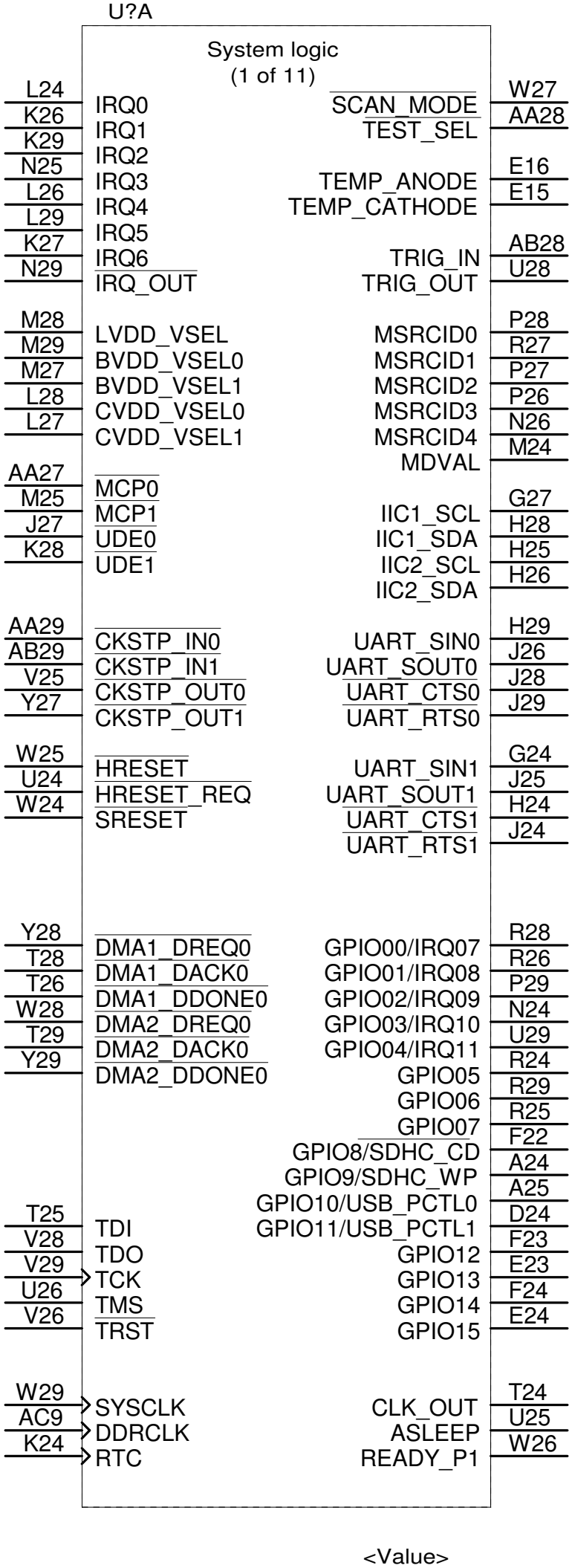
U?A
System logic
(1 of 11)
L24 IRQ0
K26 IRQ1
K29 IRQ2
N25 IRQ3
L26 IRQ4
L29 IRQ5
K27 IRQ6
N29 IRQ_OUT
M28 LVDD_VSEL
M29 BVDD_VSEL0
M27 BVDD_VSEL1
L28 CVDD_VSEL0
L27 CVDD_VSEL1
AA27 MCP0
M25 MCP1
J27 UDE0
K28 UDE1
AA29 CKSTP_IN0
AB29 CKSTP_IN1
V25 CKSTP_OUT0
Y27 CKSTP_OUT1
W25 HRESET
U24 HRESET_REQ
W24 SRESET
Y28 DMA1_DREQ0
T28 DMA1_DACK0
T26 DMA1_DDONE0
W28 DMA2_DREQ0
T29 DMA2_DACK0
Y29 DMA2_DDONE0
T25 TDI
V28 TDO
V29 TCK
U26 TMS
V26 TRST
W29 SYSCLK
AC9 DDRCLK
K24 RTC
W27 SCAN_MODE
AA28 TEST_SEL
E16 TEMP_ANODE
E15 TEMP_CATHODE
AB28 TRIG_IN
U28 TRIG_OUT
P28 MSRCID0
R27 MSRCID1
P27 MSRCID2
P26 MSRCID3
N26 MSRCID4
M24 MDVAL
G27 IIC1_SCL
H28 IIC1_SDA
H25 IIC2_SCL
H26 IIC2_SDA
H29 UART_SIN0
J26 UART_SOUT0
J28 UART_CTS0
J29 UART_RTS0
G24 UART_SIN1
J25 UART_SOUT1
H24 UART_CTS1
J24 UART_RTS1
R28 GPIO00/IRQ07
R26 GPIO01/IRQ08
P29 GPIO02/IRQ09
N24 GPIO03/IRQ10
U29 GPIO04/IRQ11
R24 GPIO05
R29 GPIO06
R25 GPIO07
F22 GPIO8/SDHC_CD
A24 GPIO9/SDHC_WP
A25 GPIO10/USB_PCTL0
D24 GPIO11/USB_PCTL1
F23 GPIO12
E23 GPIO13
F24 GPIO14
E24 GPIO15
T24 CLK_OUT
U25 ASLEEP
W26 READY_P1
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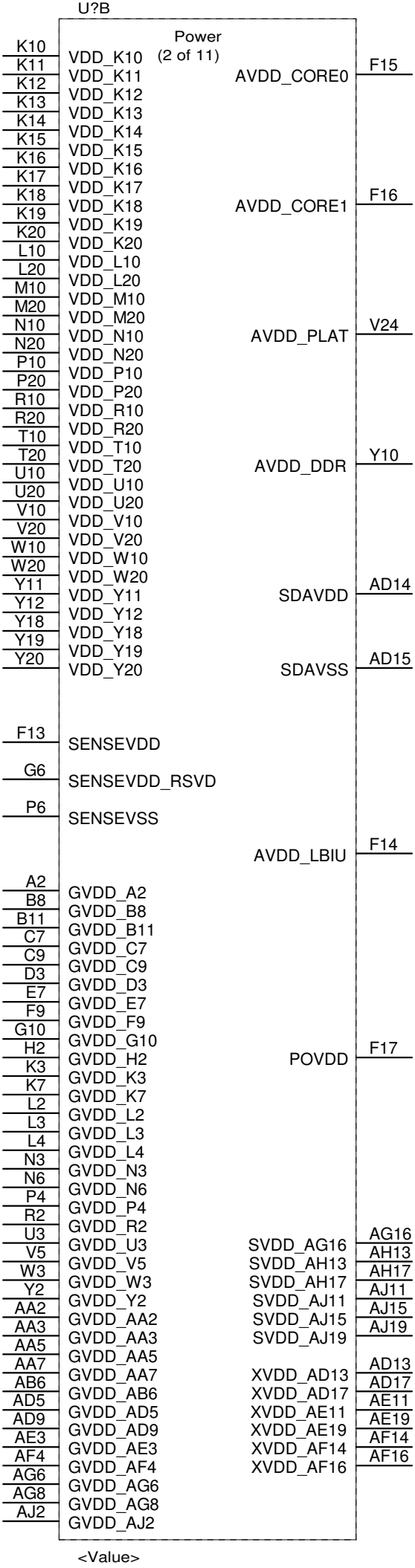
U?B
Power
(2 of 11)
K10 VDD_K10
K11 VDD_K11
K12 VDD_K12
K13 VDD_K13
K14 VDD_K14
K15 VDD_K15
K16 VDD_K16
K17 VDD_K17
K18 VDD_K18
K19 VDD_K19
K20 VDD_K20
L10 VDD_L10
L20 VDD_L20
M10 VDD_M10
M20 VDD_M20
N10 VDD_N10
N20 VDD_N20
P10 VDD_P10
P20 VDD_P20
R10 VDD_R10
R20 VDD_R20
T10 VDD_T10
T20 VDD_T20
U10 VDD_U10
U20 VDD_U20
V10 VDD_V10
V20 VDD_V20
W10 VDD_W10
W20 VDD_W20
Y11 VDD_Y11
Y12 VDD_Y12
Y18 VDD_Y18
Y19 VDD_Y19
Y20 VDD_Y20
AVDD_CORE0 F15
AVDD_CORE1 F16
AVDD_PLAT V24
AVDD_DDR Y10
SDAVDD AD14
SDAVSS AD15
F13 SENSEVDD
G6 SENSEVDD_RSVD
P6 SENSEVSS
AVDD_LBIU F14
A2 GVDD_A2
B8 GVDD_B8
B11 GVDD_B11
C7 GVDD_C7
C9 GVDD_C9
D3 GVDD_D3
E7 GVDD_E7
F9 GVDD_F9
G10 GVDD_G10
H2 GVDD_H2
K3 GVDD_K3
K7 GVDD_K7
L2 GVDD_L2
L3 GVDD_L3
L4 GVDD_L4
N3 GVDD_N3
N6 GVDD_N6
P4 GVDD_P4
R2 GVDD_R2
U3 GVDD_U3
V5 GVDD_V5
W3 GVDD_W3
Y2 GVDD_Y2
AA2 GVDD_AA2
AA3 GVDD_AA3
AA5 GVDD_AA5
AA7 GVDD_AA7
AB6 GVDD_AB6
AD5 GVDD_AD5
AD9 GVDD_AD9
AE3 GVDD_AE3
AF4 GVDD_AF4
AG6 GVDD_AG6
AG8 GVDD_AG8
AJ2 GVDD_AJ2
POVDD F17
SVDD_AG16 AG16
SVDD_AH13 AH13
SVDD_AH17 AH17
SVDD_AJ11 AJ11
SVDD_AJ15 AJ15
SVDD_AJ19 AJ19
XVDD_AD13 AD13
XVDD_AD17 AD17
XVDD_AE11 AE11
XVDD_AE19 AE19
XVDD_AF14 AF14
XVDD_AF16 AF16
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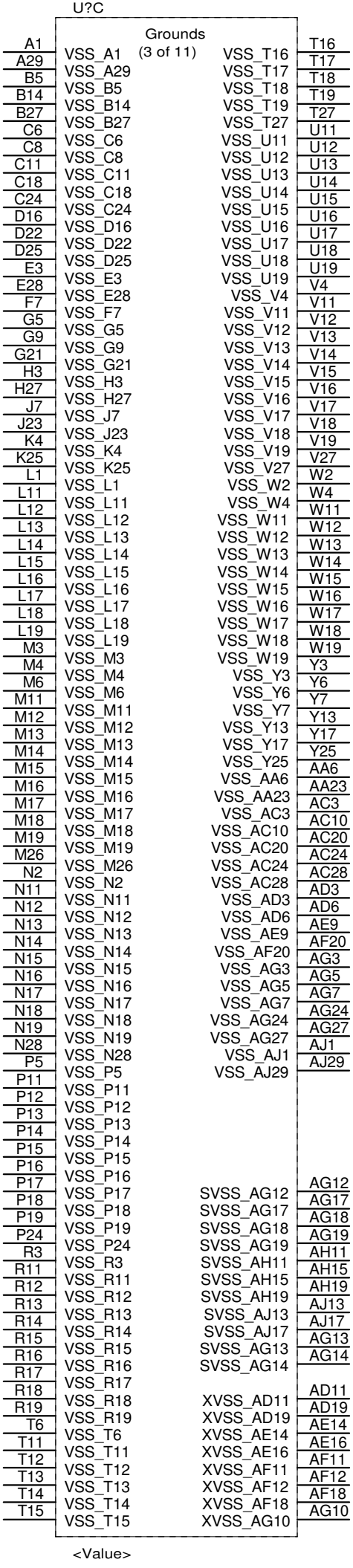
U?C
Grounds
(3 of 11)
A1 VSS_A1
A29 VSS_A29
B5 VSS_B5
B14 VSS_B14
B27 VSS_B27
C6 VSS_C6
C8 VSS_C8
C11 VSS_C11
C18 VSS_C18
C24 VSS_C24
D16 VSS_D16
D22 VSS_D22
D25 VSS_D25
E3 VSS_E3
E28 VSS_E28
F7 VSS_F7
G5 VSS_G5
G9 VSS_G9
G21 VSS_G21
H3 VSS_H3
H27 VSS_H27
J7 VSS_J7
J23 VSS_J23
K4 VSS_K4
K25 VSS_K25
L1 VSS_L1
L11 VSS_L11
L12 VSS_L12
L13 VSS_L13
L14 VSS_L14
L15 VSS_L15
L16 VSS_L16
L17 VSS_L17
L18 VSS_L18
L19 VSS_L19
M3 VSS_M3
M4 VSS_M4
M6 VSS_M6
M11 VSS_M11
M12 VSS_M12
M13 VSS_M13
M14 VSS_M14
M15 VSS_M15
M16 VSS_M16
M17 VSS_M17
M18 VSS_M18
M19 VSS_M19
M26 VSS_M26
N2 VSS_N2
N11 VSS_N11
N12 VSS_N12
N13 VSS_N13
N14 VSS_N14
N15 VSS_N15
N16 VSS_N16
N17 VSS_N17
N18 VSS_N18
N19 VSS_N19
N28 VSS_N28
P5 VSS_P5
P11 VSS_P11
P12 VSS_P12
P13 VSS_P13
P14 VSS_P14
P15 VSS_P15
P16 VSS_P16
P17 VSS_P17
P18 VSS_P18
P19 VSS_P19
P24 VSS_P24
R3 VSS_R3
R11 VSS_R11
R12 VSS_R12
R13 VSS_R13
R14 VSS_R14
R15 VSS_R15
R16 VSS_R16
R17 VSS_R17
R18 VSS_R18
R19 VSS_R19
T6 VSS_T6
T11 VSS_T11
T12 VSS_T12
T13 VSS_T13
T14 VSS_T14
T15 VSS_T15
VSS_T16 T16
VSS_T17 T17
VSS_T18 T18
VSS_T19 T19
VSS_T27 T27
VSS_U11 U11
VSS_U12 U12
VSS_U13 U13
VSS_U14 U14
VSS_U15 U15
VSS_U16 U16
VSS_U17 U17
VSS_U18 U18
VSS_U19 U19
VSS_V4 V4
VSS_V11 V11
VSS_V12 V12
VSS_V13 V13
VSS_V14 V14
VSS_V15 V15
VSS_V16 V16
VSS_V17 V17
VSS_V18 V18
VSS_V19 V19
VSS_V27 V27
VSS_W2 W2
VSS_W4 W4
VSS_W11 W11
VSS_W12 W12
VSS_W13 W13
VSS_W14 W14
VSS_W15 W15
VSS_W16 W16
VSS_W17 W17
VSS_W18 W18
VSS_W19 W19
VSS_Y3 Y3
VSS_Y6 Y6
VSS_Y7 Y7
VSS_Y13 Y13
VSS_Y17 Y17
VSS_Y25 Y25
VSS_AA6 AA6
VSS_AA23 AA23
VSS_AC3 AC3
VSS_AC10 AC10
VSS_AC20 AC20
VSS_AC24 AC24
VSS_AC28 AC28
VSS_AD3 AD3
VSS_AD6 AD6
VSS_AE9 AE9
VSS_AF20 AF20
VSS_AG3 AG3
VSS_AG5 AG5
VSS_AG7 AG7
VSS_AG24 AG24
VSS_AG27 AG27
VSS_AJ1 AJ1
VSS_AJ29 AJ29
SVSS_AG12 AG12
SVSS_AG17 AG17
SVSS_AG18 AG18
SVSS_AG19 AG19
SVSS_AH11 AH11
SVSS_AH15 AH15
SVSS_AH19 AH19
SVSS_AJ13 AJ13
SVSS_AJ17 AJ17
SVSS_AG13 AG13
SVSS_AG14 AG14
XVSS_AD11 AD11
XVSS_AD19 AD19
XVSS_AE14 AE14
XVSS_AE16 AE16
XVSS_AF11 AF11
XVSS_AF12 AF12
XVSS_AF18 AF18
XVSS_AG10 AG10
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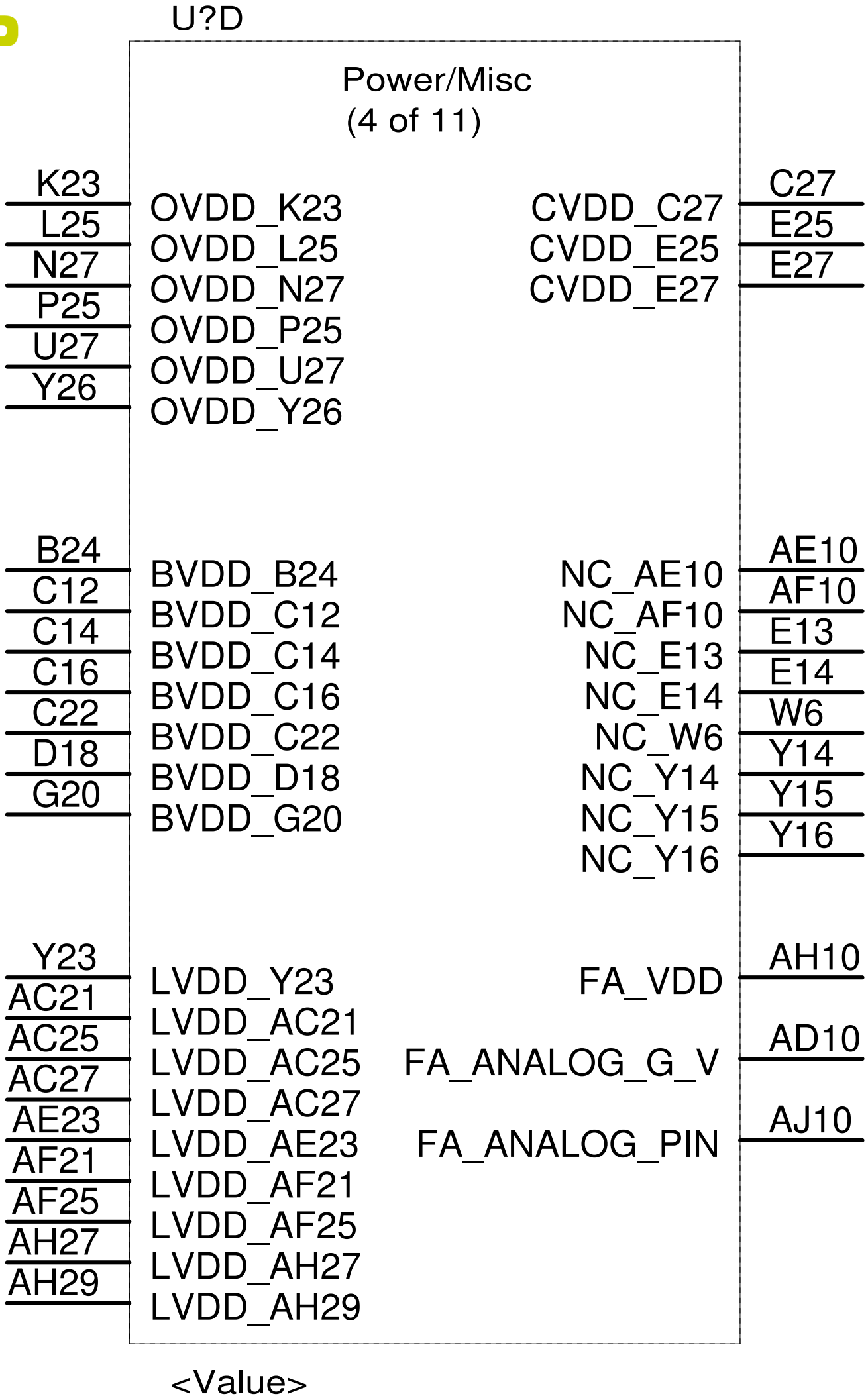
U?D
Power/Misc
(4 of 11)
K23
L25
N27
P25
U27
Y26
OVDD_K23
OVDD_L25
OVDD_N27
OVDD_P25
OVDD_U27
OVDD_Y26
CVDD_C27
CVDD_E25
CVDD_E27
C27
E25
E27
B24
C12
C14
C16
C22
D18
G20
BVDD_B24
BVDD_C12
BVDD_C14
BVDD_C16
BVDD_C22
BVDD_D18
BVDD_G20
NC_AE10
NC_AF10
NC_E13
NC_E14
NC_W6
NC_Y14
NC_Y15
NC_Y16
AE10
AF10
E13
E14
W6
Y14
Y15
Y16
Y23
AC21
AC25
AC27
AE23
AF21
AF25
AH27
AH29
LVDD_Y23
LVDD_AC21
LVDD_AC25
LVDD_AC27
LVDD_AE23
LVDD_AF21
LVDD_AF25
LVDD_AH27
LVDD_AH29
FA_VDD
FA_ANALOG_G_V
FA_ANALOG_PIN
AH10
AD10
AJ10
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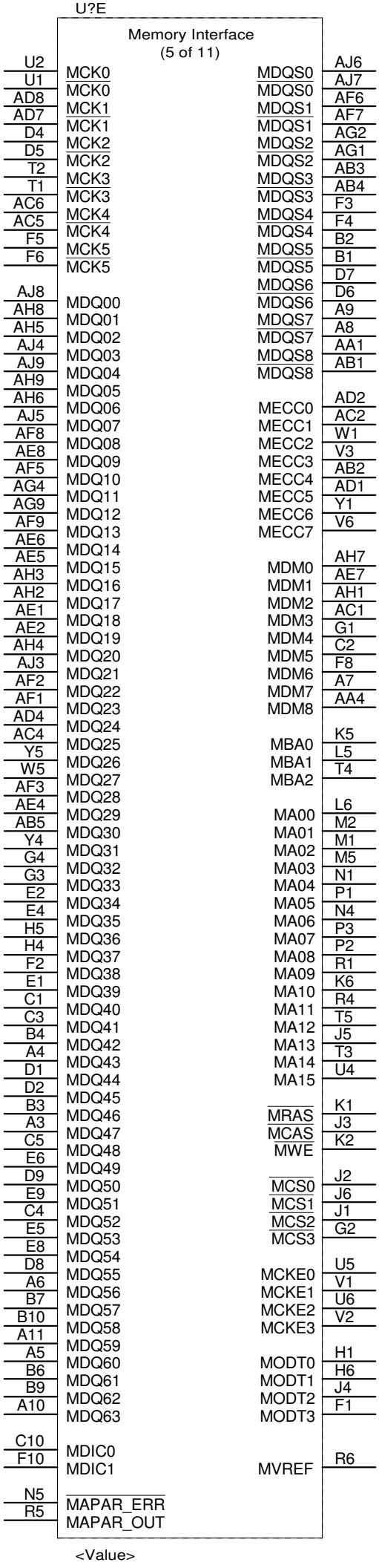
U?E
Memory Interface
(5 of 11)
U2 MCK0
U1 MCK0
AD8 MCK1
AD7 MCK1
D4 MCK2
D5 MCK2
T2 MCK3
T1 MCK3
AC6 MCK4
AC5 MCK4
F5 MCK5
F6 MCK5
AJ8 MDQ00
AH8 MDQ01
AH5 MDQ02
AJ4 MDQ03
AJ9 MDQ04
AH9 MDQ05
AH6 MDQ06
AJ5 MDQ07
AF8 MDQ08
AE8 MDQ09
AF5 MDQ10
AG4 MDQ11
AG9 MDQ12
AF9 MDQ13
AE6 MDQ14
AE5 MDQ15
AH3 MDQ16
AH2 MDQ17
AE1 MDQ18
AE2 MDQ19
AH4 MDQ20
AJ3 MDQ21
AF2 MDQ22
AF1 MDQ23
AD4 MDQ24
AC4 MDQ25
Y5 MDQ26
W5 MDQ27
AF3 MDQ28
AE4 MDQ29
AB5 MDQ30
Y4 MDQ31
G4 MDQ32
G3 MDQ33
E2 MDQ34
E4 MDQ35
H5 MDQ36
H4 MDQ37
F2 MDQ38
E1 MDQ39
C1 MDQ40
C3 MDQ41
B4 MDQ42
A4 MDQ43
D1 MDQ44
D2 MDQ45
B3 MDQ46
A3 MDQ47
C5 MDQ48
E6 MDQ49
D9 MDQ50
E9 MDQ51
C4 MDQ52
E5 MDQ53
E8 MDQ54
D8 MDQ55
A6 MDQ56
B7 MDQ57
B10 MDQ58
A11 MDQ59
A5 MDQ60
B6 MDQ61
B9 MDQ62
A10 MDQ63
C10 MDIC0
F10 MDIC1
N5 MAPAR_ERR
R5 MAPAR_OUT
AJ6 MDQS0
AJ7 MDQS0
AF6 MDQS1
AF7 MDQS1
AG2 MDQS2
AG1 MDQS2
AB3 MDQS3
AB4 MDQS3
F3 MDQS4
F4 MDQS4
B2 MDQS5
B1 MDQS5
D7 MDQS6
D6 MDQS6
A9 MDQS7
A8 MDQS7
AA1 MDQS8
AB1 MDQS8
AD2 MECC0
AC2 MECC1
W1 MECC2
V3 MECC3
AB2 MECC4
AD1 MECC5
Y1 MECC6
V6 MECC7
AH7 MDM0
AE7 MDM1
AH1 MDM2
AC1 MDM3
G1 MDM4
C2 MDM5
F8 MDM6
A7 MDM7
AA4 MDM8
K5 MBA0
L5 MBA1
T4 MBA2
L6 MA00
M2 MA01
M1 MA02
M5 MA03
N1 MA04
P1 MA05
N4 MA06
P3 MA07
P2 MA08
R1 MA09
K6 MA10
R4 MA11
T5 MA12
J5 MA13
T3 MA14
U4 MA15
K1 MRAS
J3 MCAS
K2 MWE
J2 MCS0
J6 MCS1
J1 MCS2
G2 MCS3
U5 MCKE0
V1 MCKE1
U6 MCKE2
V2 MCKE3
H1 MODT0
H6 MODT1
J4 MODT2
F1 MODT3
R6 MVREF
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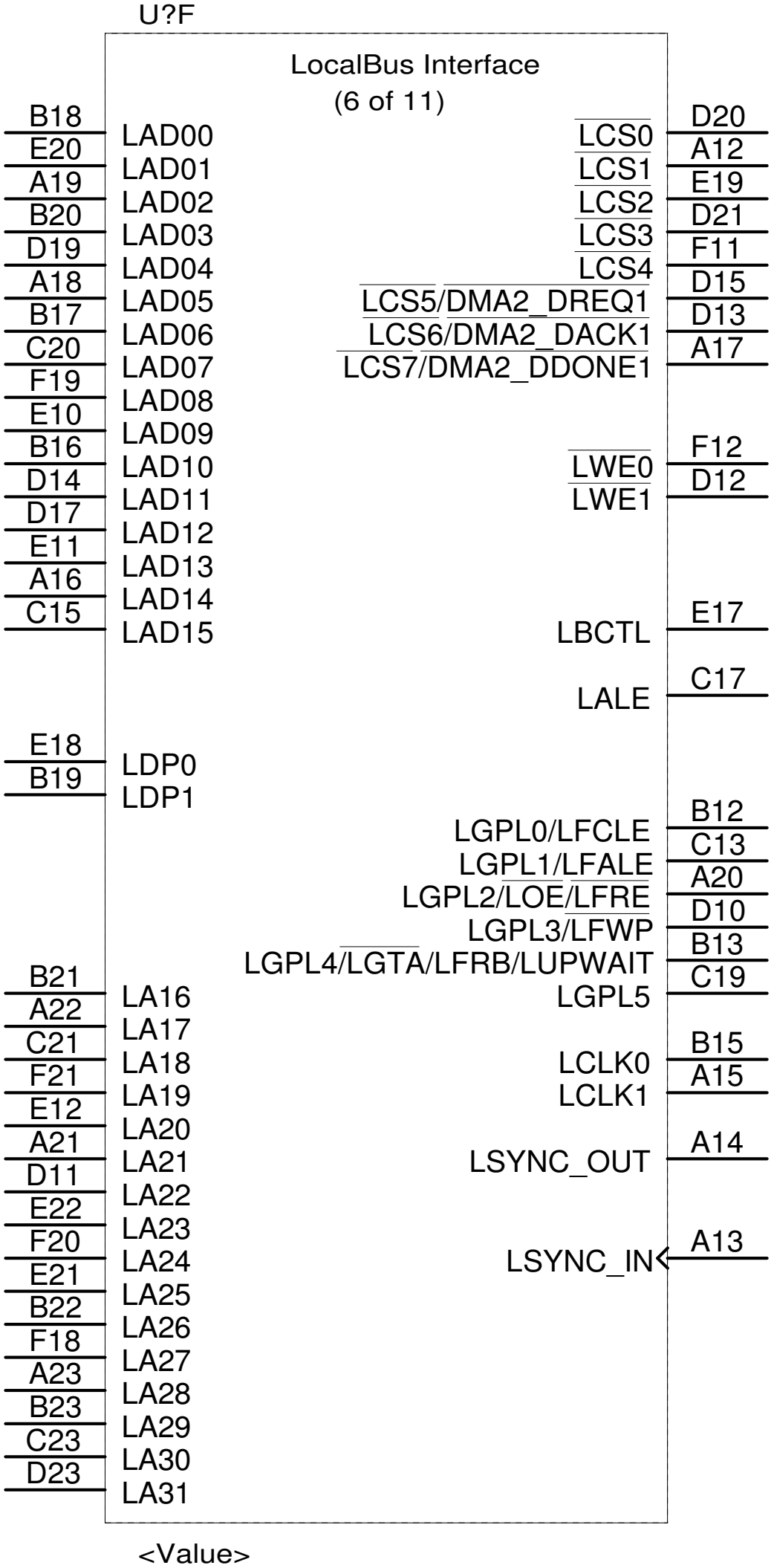
U?F
LocalBus Interface
(6 of 11)
B18 LAD00
E20 LAD01
A19 LAD02
B20 LAD03
D19 LAD04
A18 LAD05
B17 LAD06
C20 LAD07
F19 LAD08
E10 LAD09
B16 LAD10
D14 LAD11
D17 LAD12
E11 LAD13
A16 LAD14
C15 LAD15
E18 LDP0
B19 LDP1
B21 LA16
A22 LA17
C21 LA18
F21 LA19
E12 LA20
A21 LA21
D11 LA22
E22 LA23
F20 LA24
E21 LA25
B22 LA26
F18 LA27
A23 LA28
B23 LA29
C23 LA30
D23 LA31
LCS0 D20
LCS1 A12
LCS2 E19
LCS3 D21
LCS4 F11
LCS5/DMA2_DREQ1 D15
LCS6/DMA2_DACK1 D13
LCS7/DMA2_DDONE1 A17
LWE0 F12
LWE1 D12
LBCTL E17
LALE C17
LGPL0/LFCLE B12
LGPL1/LFALE C13
LGPL2/LOE/LFRE A20
LGPL3/LFWP D10
LGPL4/LGTA/LFRB/LUPWAIT B13
LGPL5 C19
LCLK0 B15
LCLK1 A15
LSYNC_OUT A14
LSYNC_IN A13
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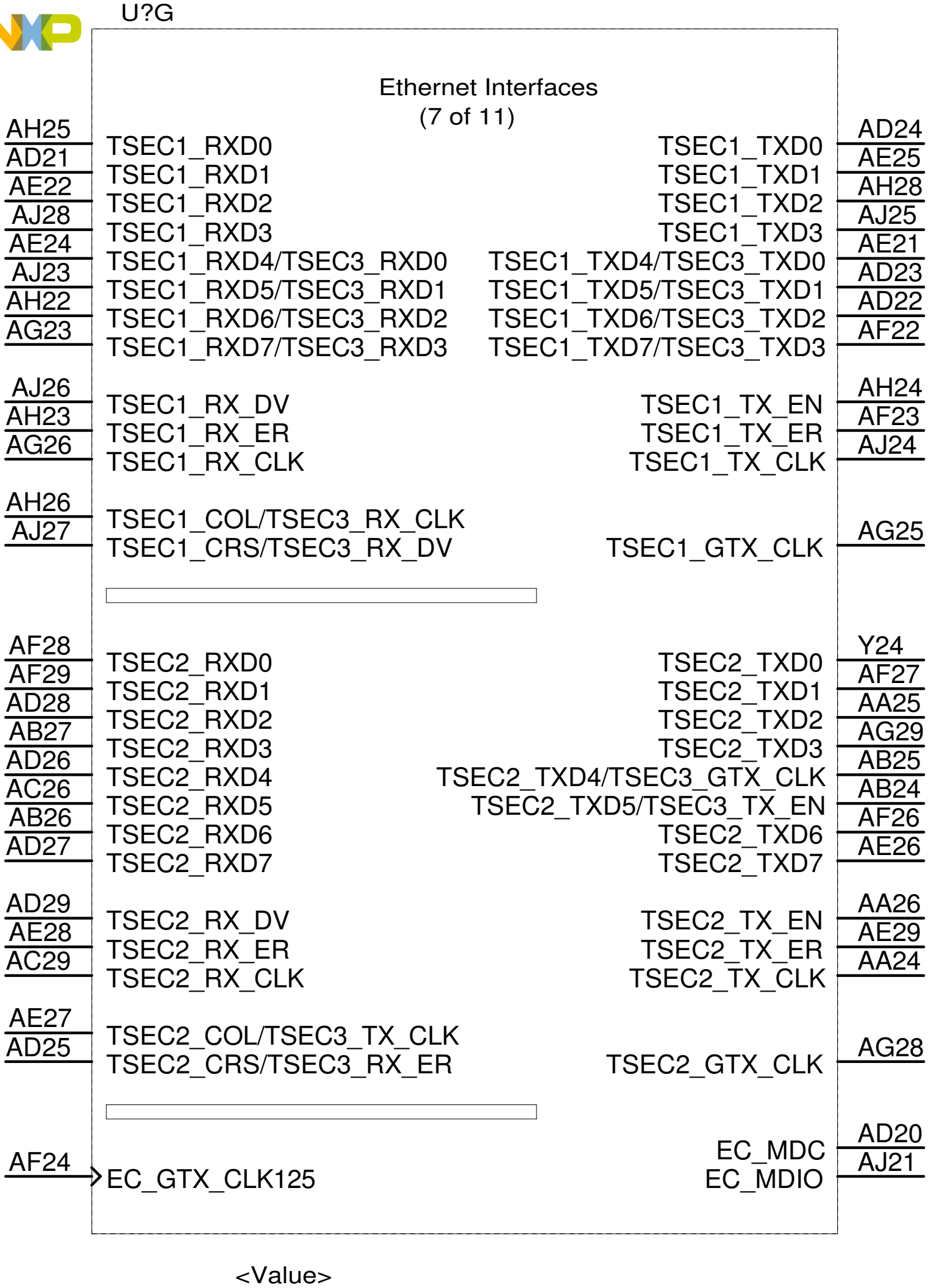
U?G
Ethernet Interfaces
(7 of 11)
AH25 TSEC1_RXD0
AD21 TSEC1_RXD1
AE22 TSEC1_RXD2
AJ28 TSEC1_RXD3
AE24 TSEC1_RXD4/TSEC3_RXD0
AJ23 TSEC1_RXD5/TSEC3_RXD1
AH22 TSEC1_RXD6/TSEC3_RXD2
AG23 TSEC1_RXD7/TSEC3_RXD3
AJ26 TSEC1_RX_DV
AH23 TSEC1_RX_ER
AG26 TSEC1_RX_CLK
AH26 TSEC1_COL/TSEC3_RX_CLK
AJ27 TSEC1_CRS/TSEC3_RX_DV
TSEC1_TXD0 AD24
TSEC1_TXD1 AE25
TSEC1_TXD2 AH28
TSEC1_TXD3 AJ25
TSEC1_TXD4/TSEC3_TXD0 AE21
TSEC1_TXD5/TSEC3_TXD1 AD23
TSEC1_TXD6/TSEC3_TXD2 AD22
TSEC1_TXD7/TSEC3_TXD3 AF22
TSEC1_TX_EN AH24
TSEC1_TX_ER AF23
TSEC1_TX_CLK AJ24
TSEC1_GTX_CLK AG25
AF28 TSEC2_RXD0
AF29 TSEC2_RXD1
AD28 TSEC2_RXD2
AB27 TSEC2_RXD3
AD26 TSEC2_RXD4
AC26 TSEC2_RXD5
AB26 TSEC2_RXD6
AD27 TSEC2_RXD7
AD29 TSEC2_RX_DV
AE28 TSEC2_RX_ER
AC29 TSEC2_RX_CLK
AE27 TSEC2_COL/TSEC3_TX_CLK
AD25 TSEC2_CRS/TSEC3_RX_ER
TSEC2_TXD0 Y24
TSEC2_TXD1 AF27
TSEC2_TXD2 AA25
TSEC2_TXD3 AG29
TSEC2_TXD4/TSEC3_GTX_CLK AB25
TSEC2_TXD5/TSEC3_TX_EN AB24
TSEC2_TXD6 AF26
TSEC2_TXD7 AE26
TSEC2_TX_EN AA26
TSEC2_TX_ER AE29
TSEC2_TX_CLK AA24
TSEC2_GTX_CLK AG28
AF24 EC_GTX_CLK125
EC_MDC AD20
EC_MDIO AJ21
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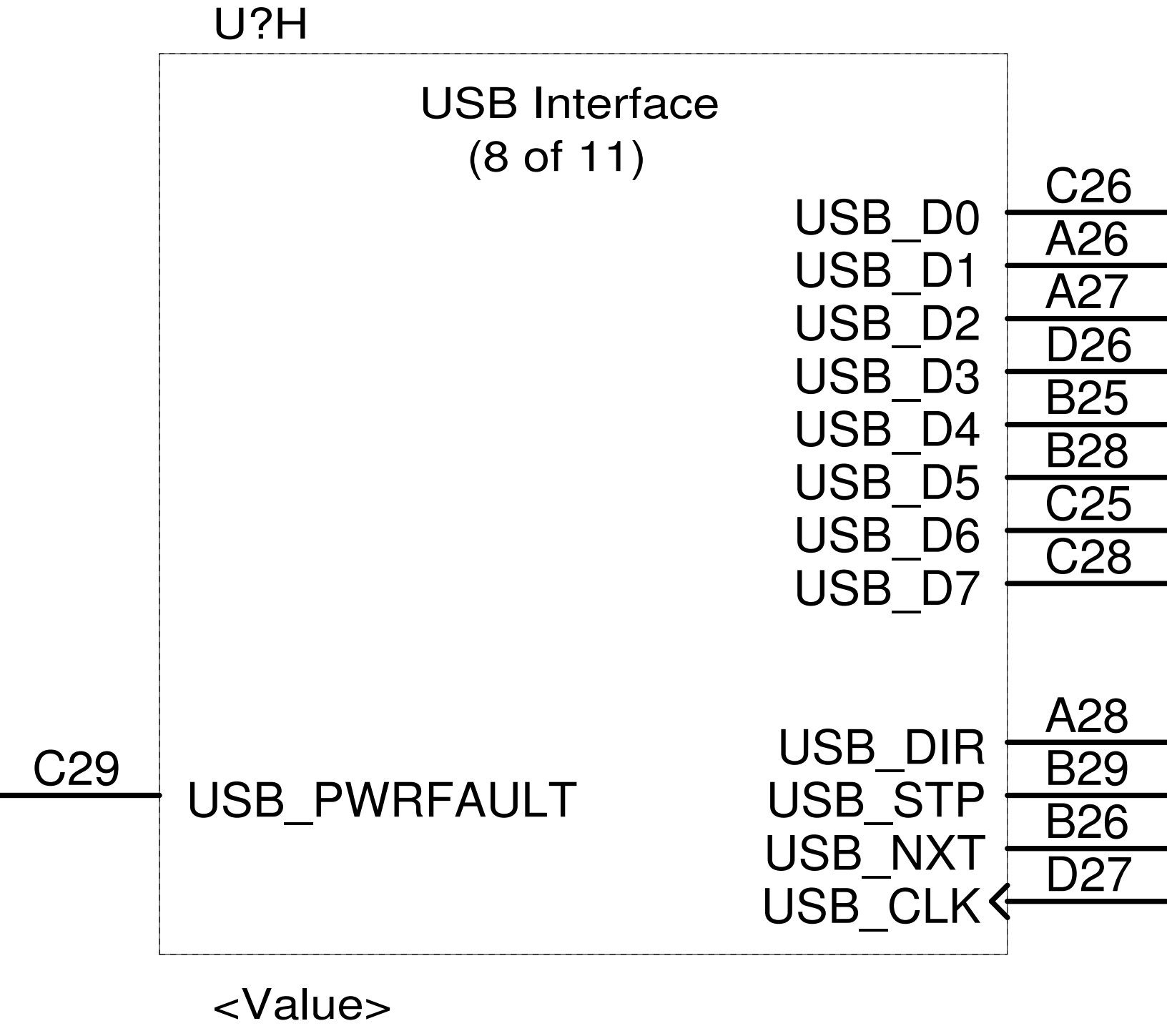
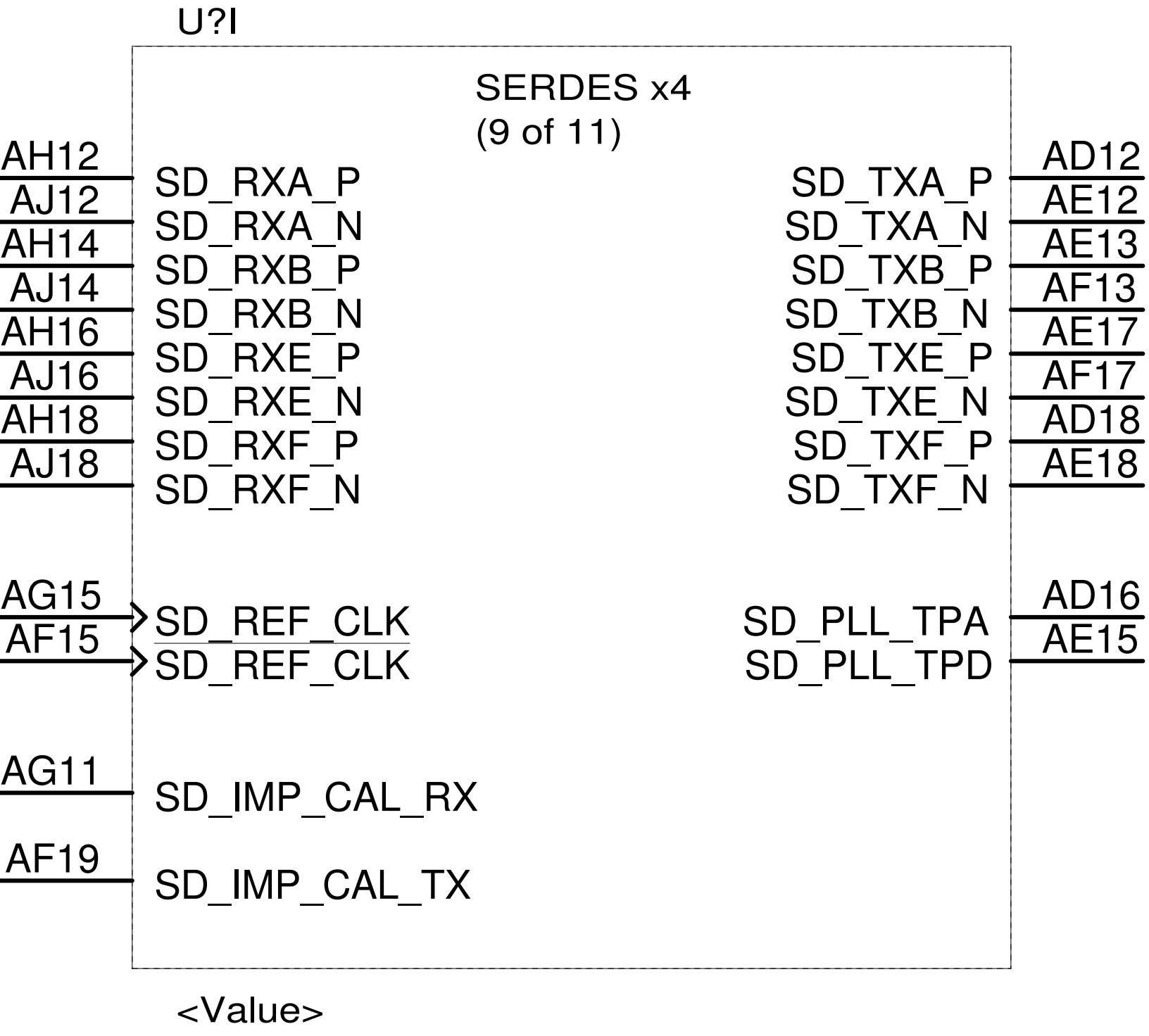

U?H
USB Interface
(8 of 11)
USB_D0
USB_D1
USB_D2
USB_D3
USB_D4
USB_D5
USB_D6
USB_D7
C26
A26
A27
D26
B25
B28
C25
C28
C29
USB_PWRFAULT
USB_DIR
USB_STP
USB_NXT
USB_CLK
A28
B29
B26
D27
<Value>


U?I
SERDES x4
(9 of 11)
AH12
SD_RXA_P
AJ12
SD_RXA_N
AH14
SD_RXB_P
AJ14
SD_RXB_N
AH16
SD_RXE_P
AJ16
SD_RXE_N
AH18
SD_RXF_P
AJ18
SD_RXF_N
AG15
SD_REF_CLK
AF15
SD_REF_CLK
AG11
SD_IMP_CAL_RX
AF19
SD_IMP_CAL_TX
SD_TXA_P
AD12
SD_TXA_N
AE12
SD_TXB_P
AE13
SD_TXB_N
AF13
SD_TXE_P
AE17
SD_TXE_N
AF17
SD_TXF_P
AD18
SD_TXF_N
AE18
SD_PLL_TPA
AD16
SD_PLL_TPD
AE15
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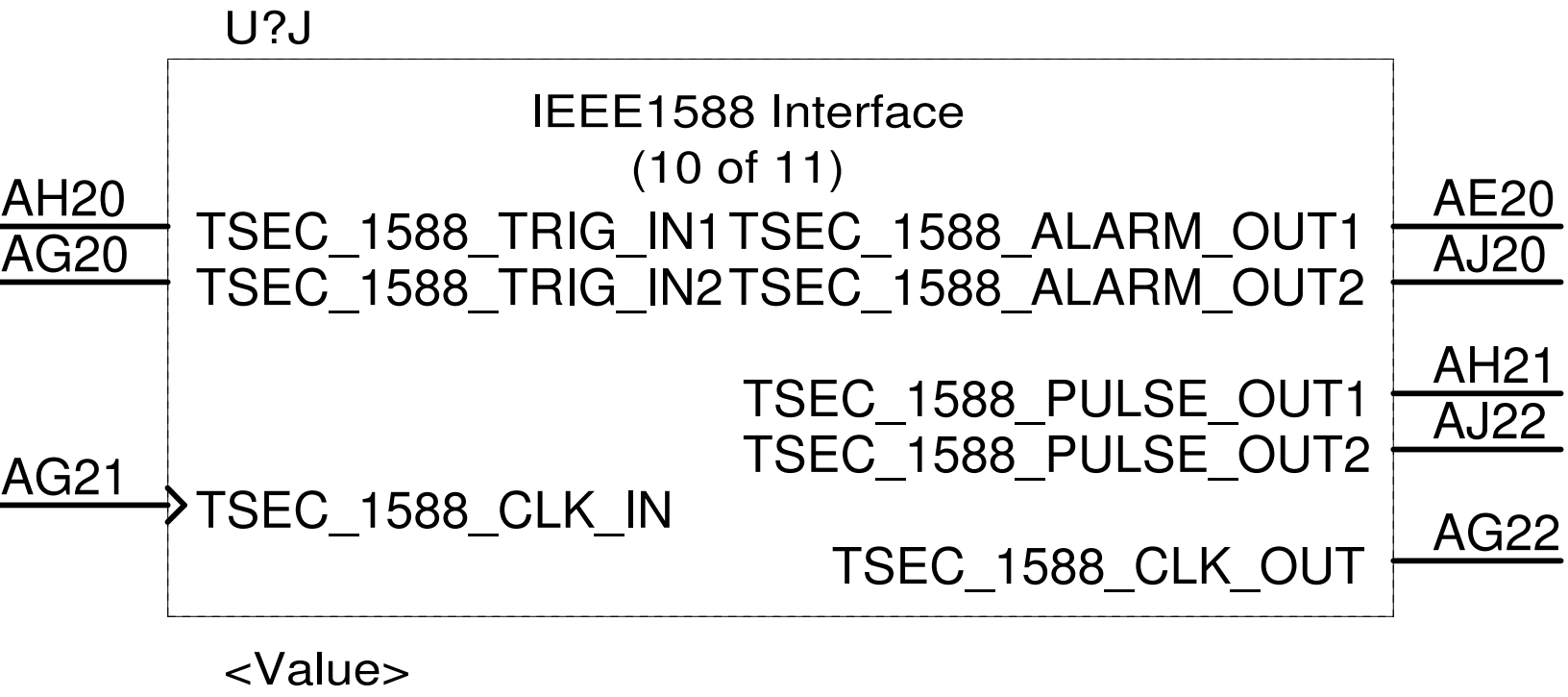
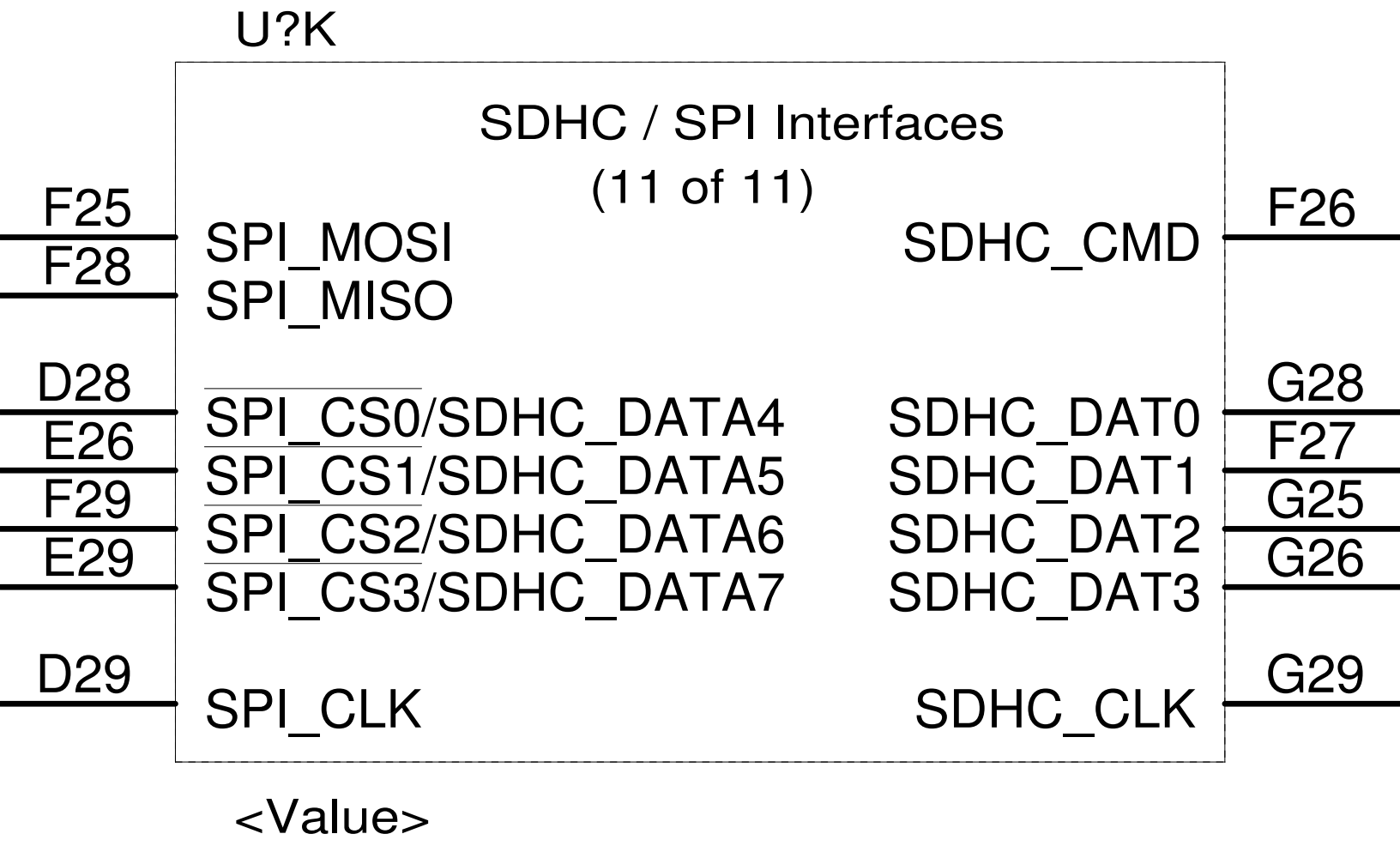

U?J
IEEE1588 Interface
(10 of 11)
AH20
AG20
TSEC_1588_TRIG_IN1
TSEC_1588_TRIG_IN2
TSEC_1588_ALARM_OUT1
TSEC_1588_ALARM_OUT2
AE20
AJ20
AH21
AJ22
TSEC_1588_PULSE_OUT1
TSEC_1588_PULSE_OUT2
AG21
TSEC_1588_CLK_IN
TSEC_1588_CLK_OUT
AG22
<Value>


U?K
SDHC / SPI Interfaces
(11 of 11)
F25
SPI_MOSI
F28
SPI_MISO
D28
SPI_CS0/SDHC_DATA4
E26
SPI_CS1/SDHC_DATA5
F29
SPI_CS2/SDHC_DATA6
E29
SPI_CS3/SDHC_DATA7
D29
SPI_CLK
F26
SDHC_CMD
G28
SDHC_DAT0
F27
SDHC_DAT1
G25
SDHC_DAT2
G26
SDHC_DAT3
G29
SDHC_CLK
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