

Valis*

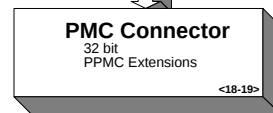
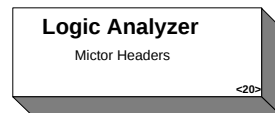
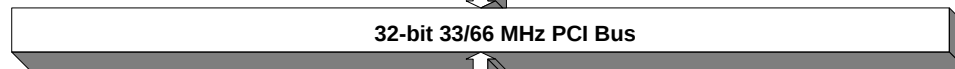
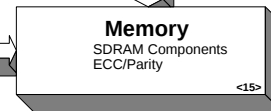
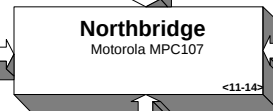
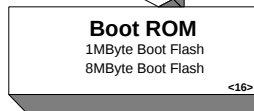
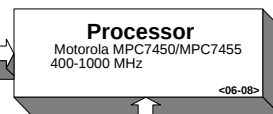
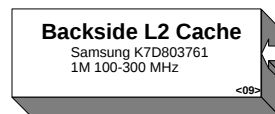
MPC7450

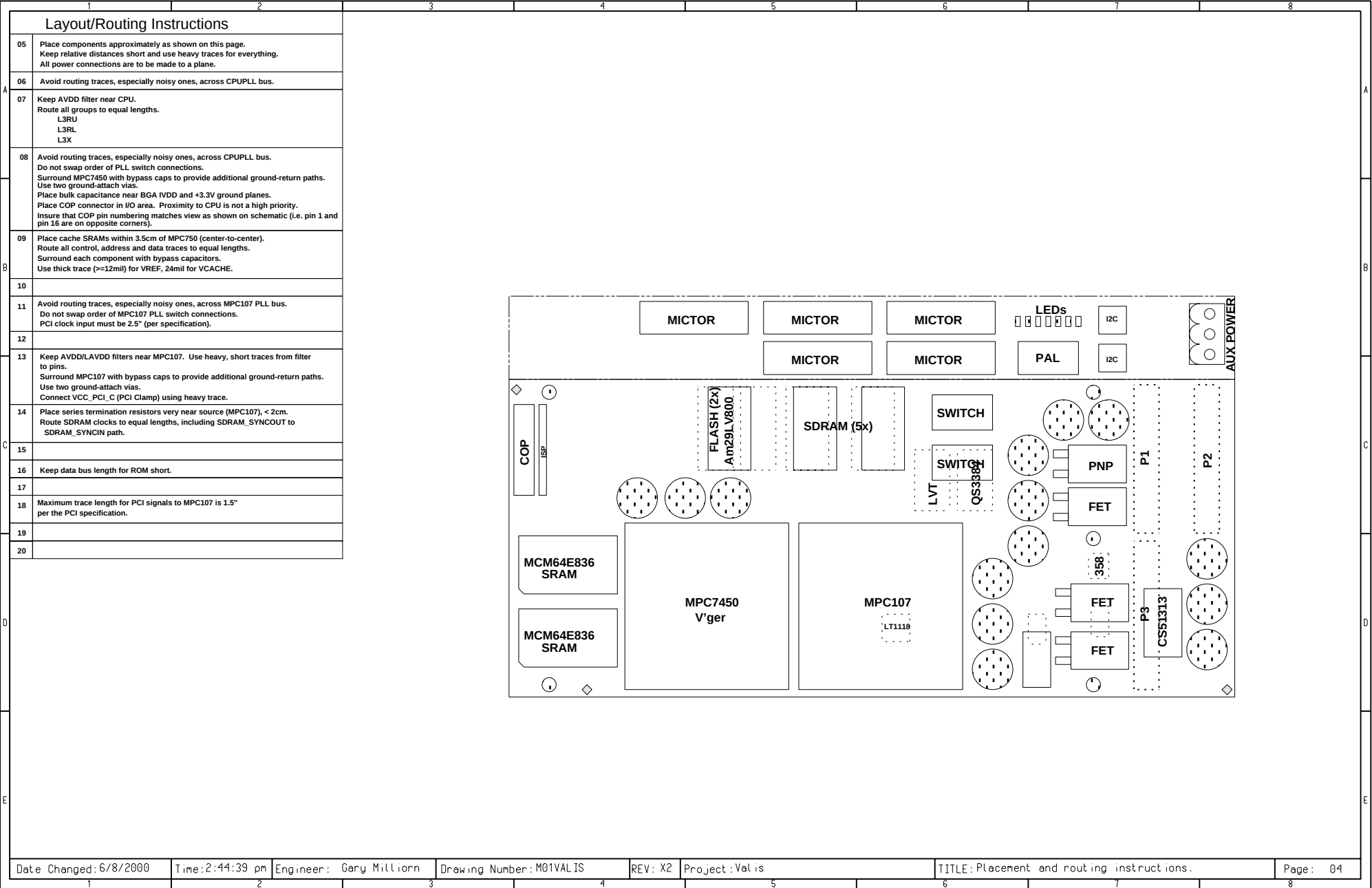
MPC7455

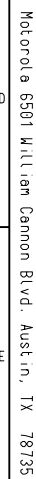
intelligence  **everywhere**

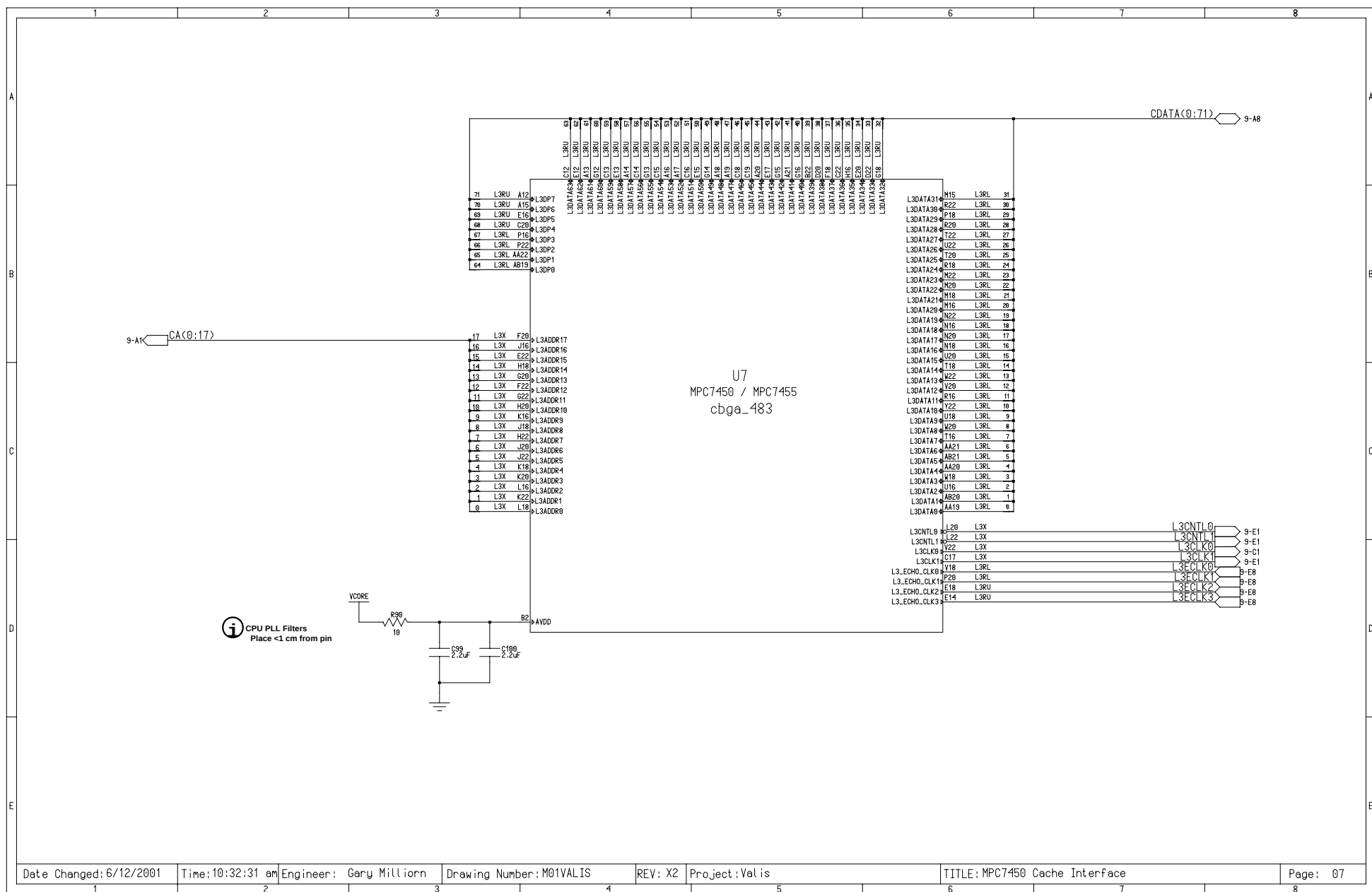
***Digital DNA**
from Motorola

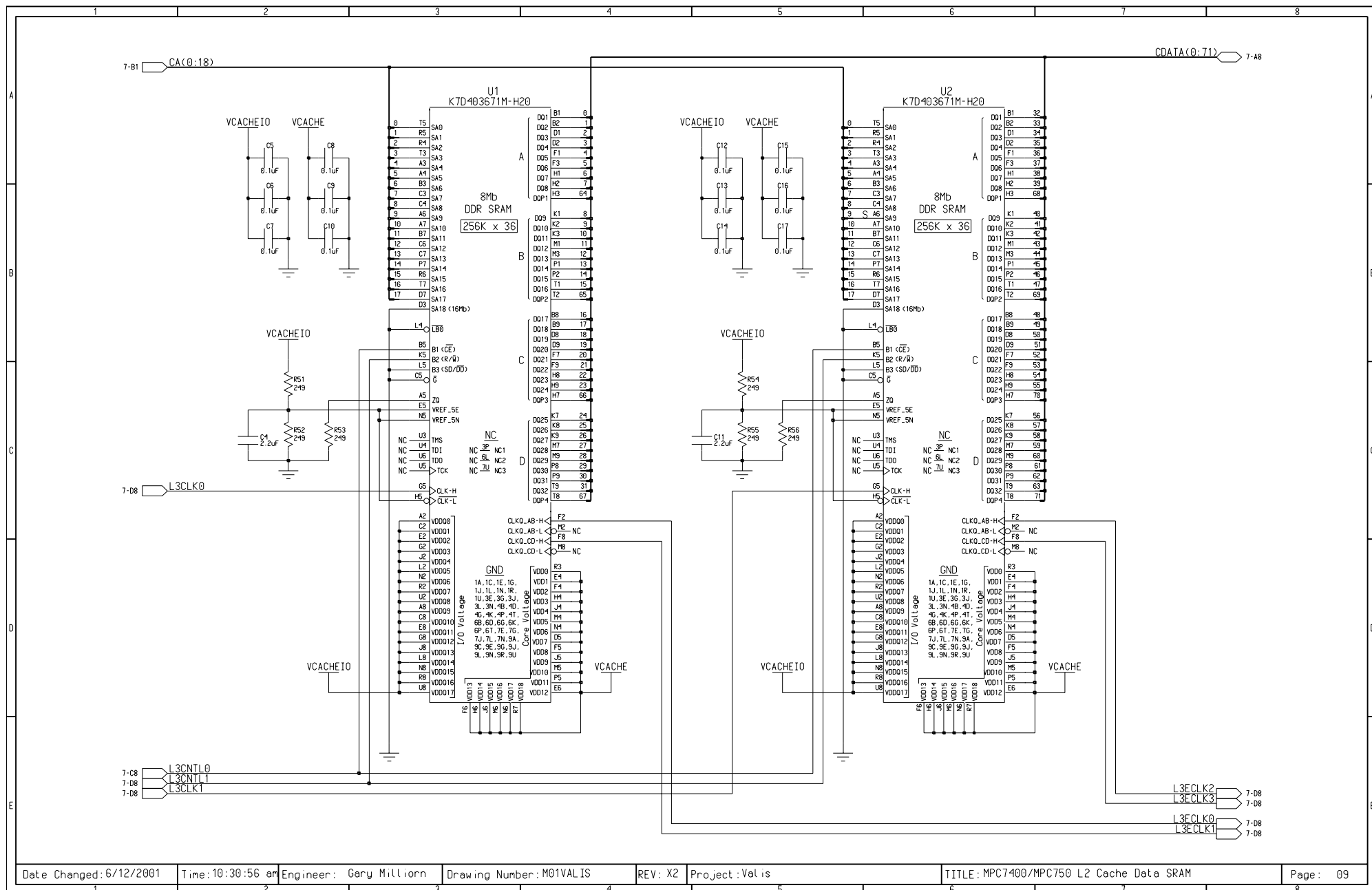
1		2		3		4		5		6		7		8													
A	Schematic Notes											Page	Contents														
	1. Unless otherwise specified: All resistors are SMD0603, in ohms, 0.08W, +/-5% All capacitors are SMD0603, in microfarads (uF), +/-20%. All inductances are in microhenries (uH). All ferrites are Z=50 ohms at 100 MHz. All fuses are self-resetting polyswitch (PTC) devices. Board impedance is 55 +/- 5 ohms.											01	Cover Page														
	2. Integrated circuits have default connections to power and ground unless explicitly shown otherwise. Global power connections are: GND VCCACHE VCCACHE_IO VCC_3.3 VCC_2.5 OVDD VCC_5 VCCORE VCC_12											02	General Information														
	3. Part numbers used are for reference only; compatible parts may be used; refer to the bill of materials.											03	Block Diagram														
	4. Motorola and the Motorola logo are registered trademarks of Motorola. PowerPC is a trademark of IBM. Other trademarks are the respective property of their respective copyright holders. There is no spoon. All rights reserved. No warranty is made, express or implied.											04	Routing and Layout Information														
	5. The sheet-to-sheet cross reference format is: Sheet "" VertZoneLetter HorizZoneNumber											05	Power Supply														
	6. Components with the visible property "NO STUFF" are not to be installed by default; they are for test or manufacturing purposes only. 											06	MPC7450 System Logic														
	7. All buses follow big-endian bit numbering order (bit 0 is the most-significant bit), except where industry standards apply (i.e. PCI). Little-endian numbering is noted at the source component.											07	MPC7450 Cache Interface														
B	8. Team Valis is: Cindy Callis.....CAD/Layout Ivan Erickson.....Program Manager Gary Million.....Hardware Design Tony Saucedo.....Purchasing Margarito Trevino.....Tech/Debug Gary Wojcik.....Grand Poobah											08	MPC7450 Power/Options														
												09	L2 Cache SRAM														
												10	Reserved														
												11	MPC107: System Logic														
												12	MPC107: Processor Interface														
												13	MPC107: PCI Interface														
												14	MPC107: Memory Interface														
												15	SDRAM SODIMM Socket														
16												Local Boot ROM															
C												17	Configuration Logic / LEDs														
												18	PMC Connectors.														
												19	PMC Connector														
												20	Analyzer Headers														



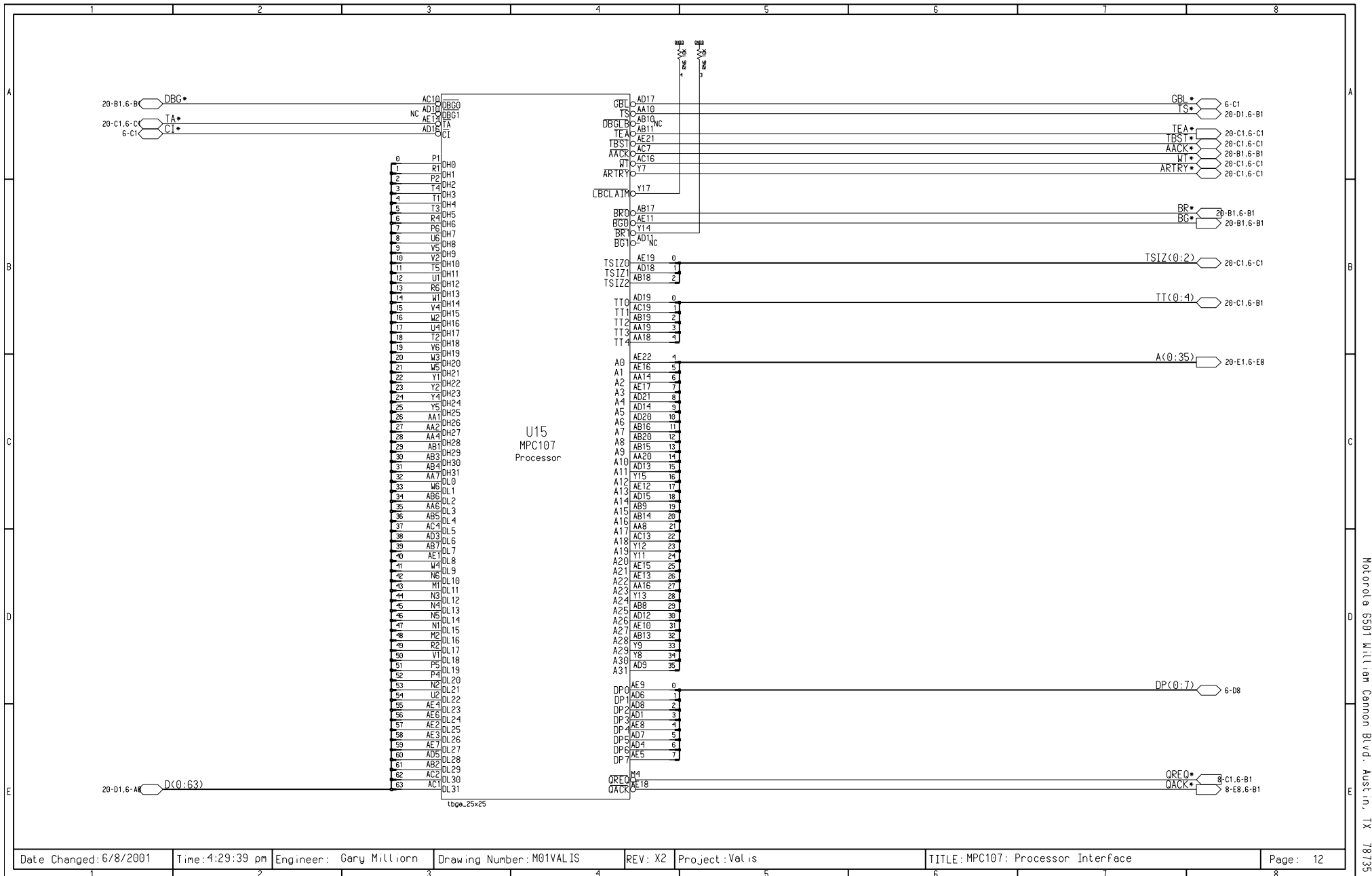




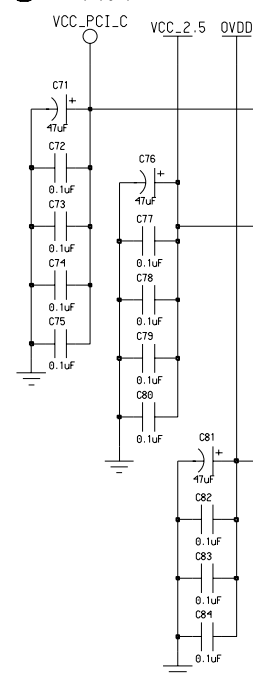




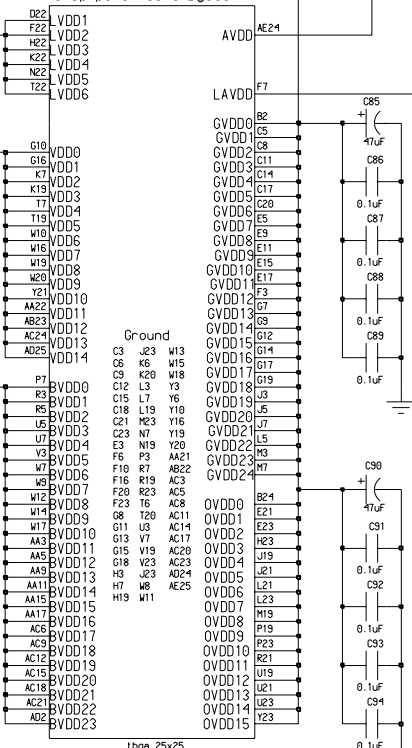
	1	2	3	4	5	6	7	8	
A									A
B									B
C									C
D									D
E									E
Date Changed: 6/8/2001 Time: 3:56:13 pm Engineer: Gary Million Drawing Number: M01VALIS REV: X2 Project: Valis TITLE: Reserved Page: 10									
	1	2	3	4	5	6	7	8	



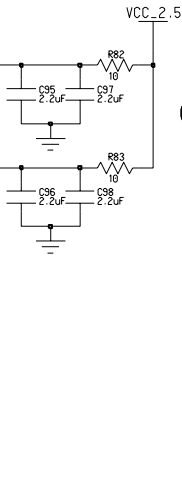
PCI Clamp Voltage 3.3V or 5V depending upon VCO selection (see page 15).



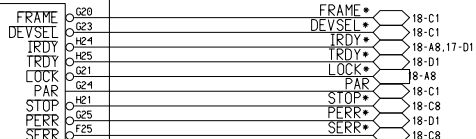
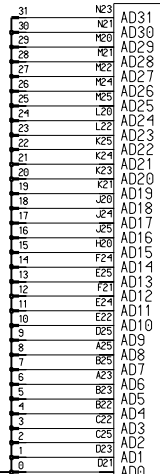
U15
MPC107
chap.power.3of5.bga504



PLL Filters Use 15 mil traces and keep them short.

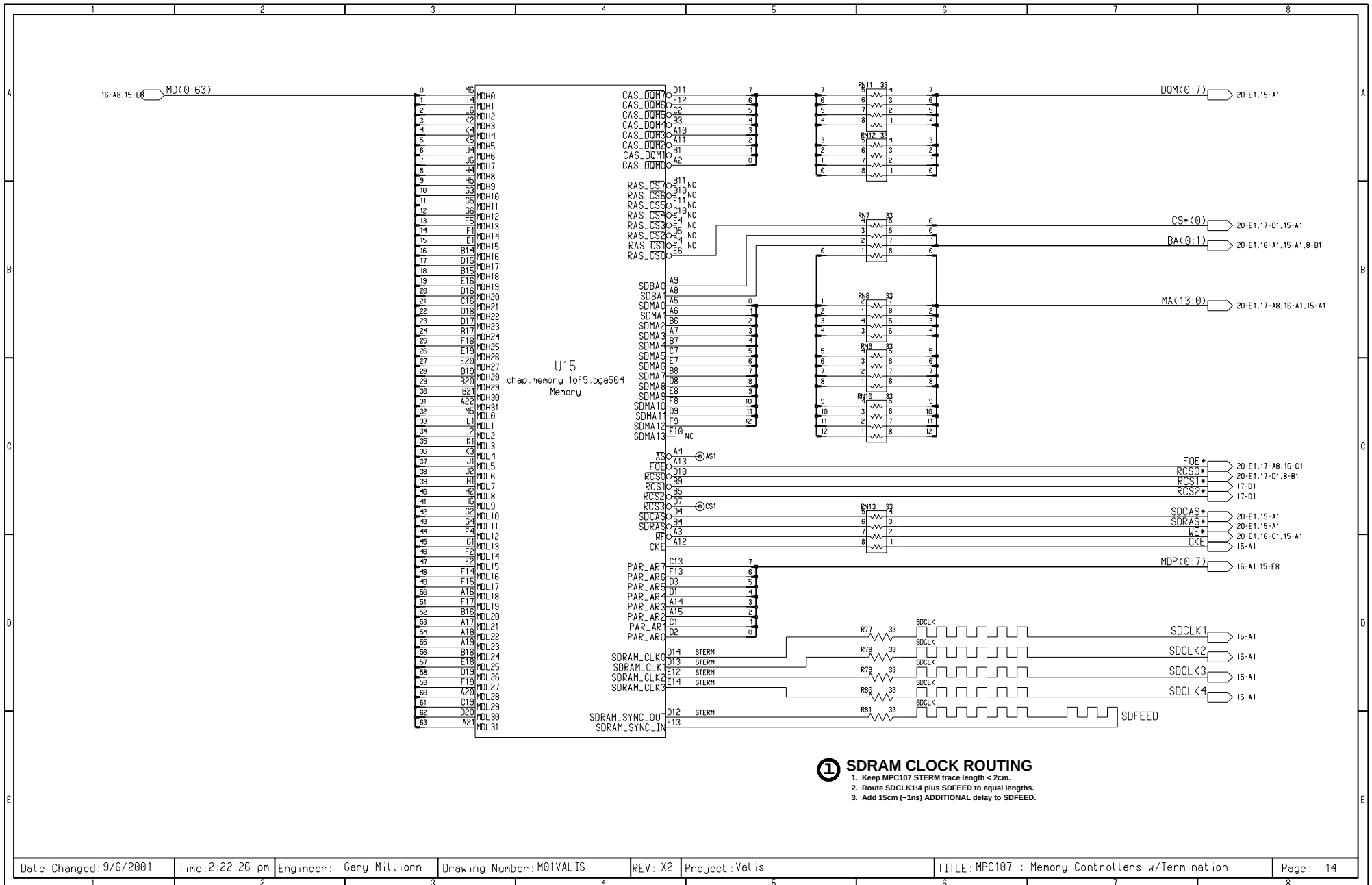


U15
MPC107
chap.pc1.2of5.bga504



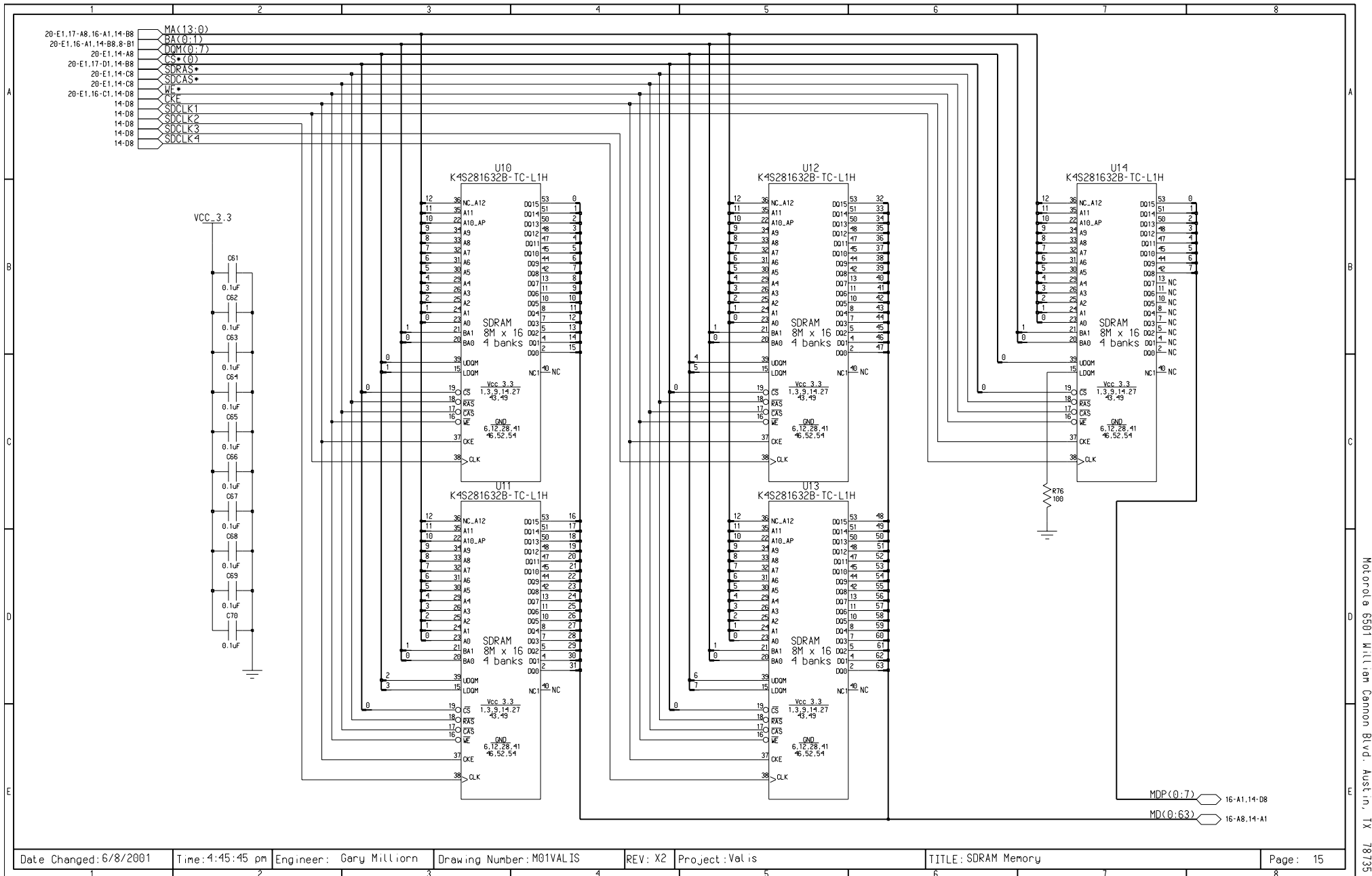
PCI Clock Trace Must equal exactly 2.5" from connector pin to MPC107 pin, per specifications. Route aux-clock to connector pin.

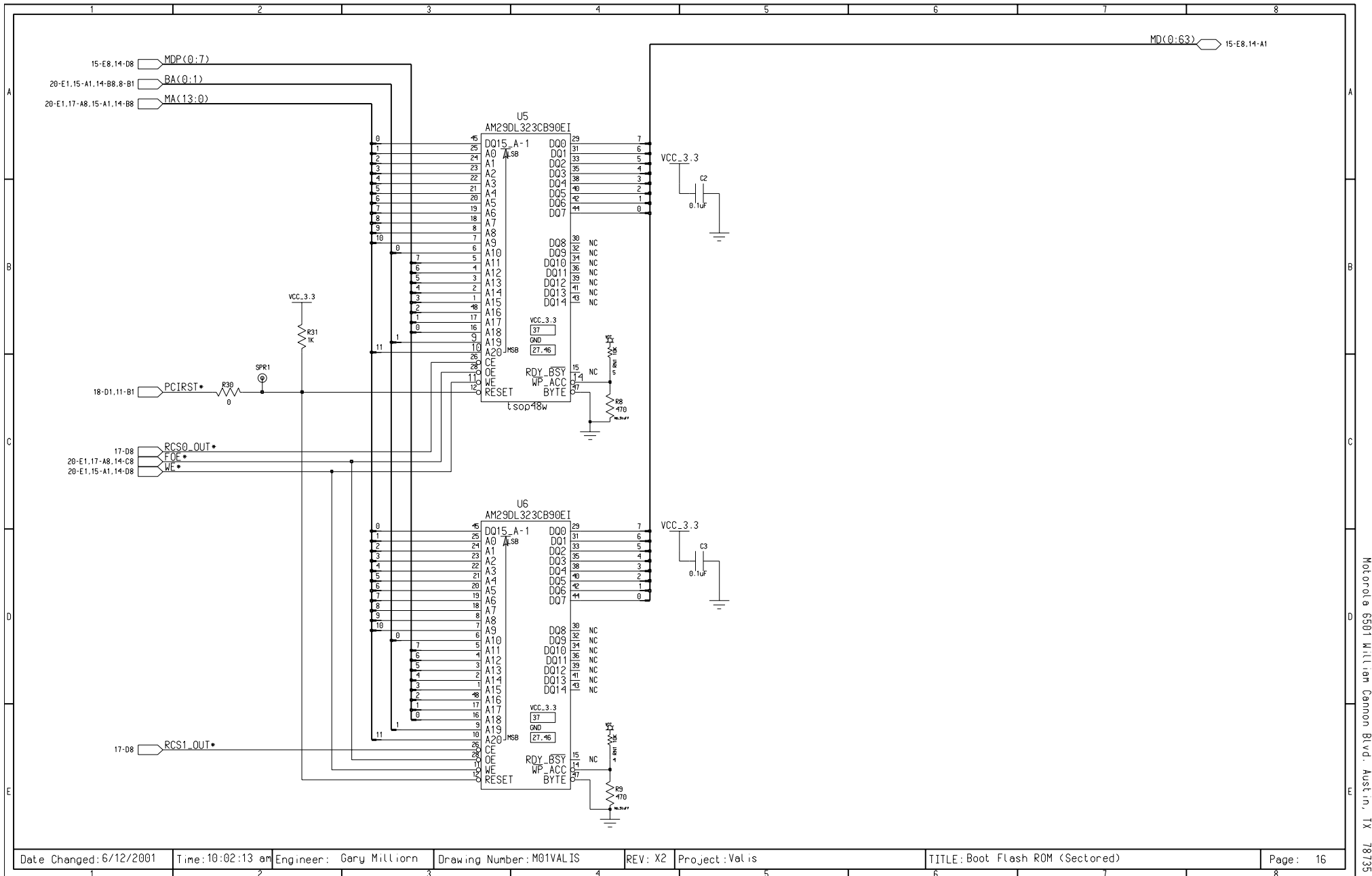
Trace Length = 2.5"

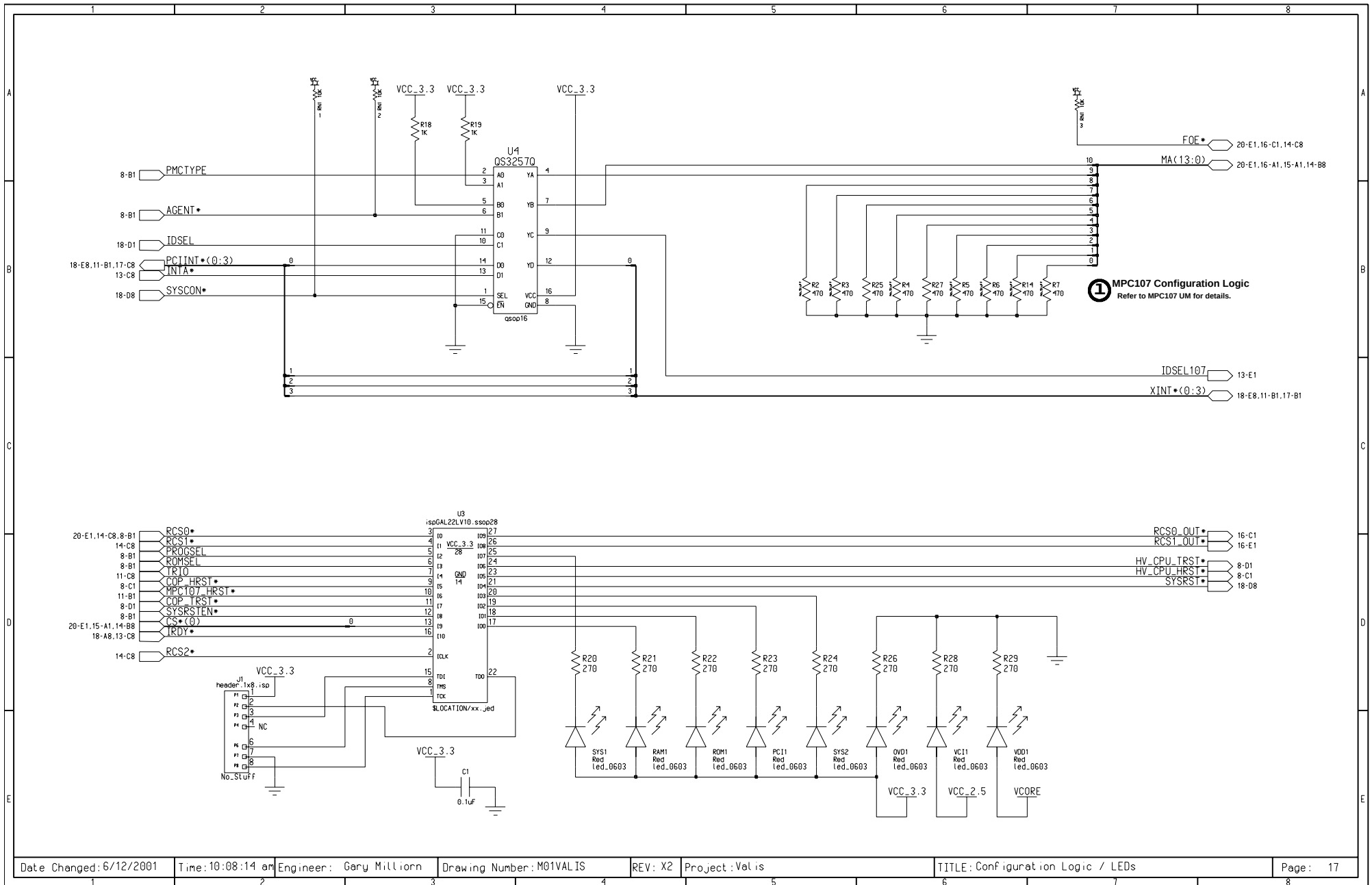


① SDRAM CLOCK ROUTING

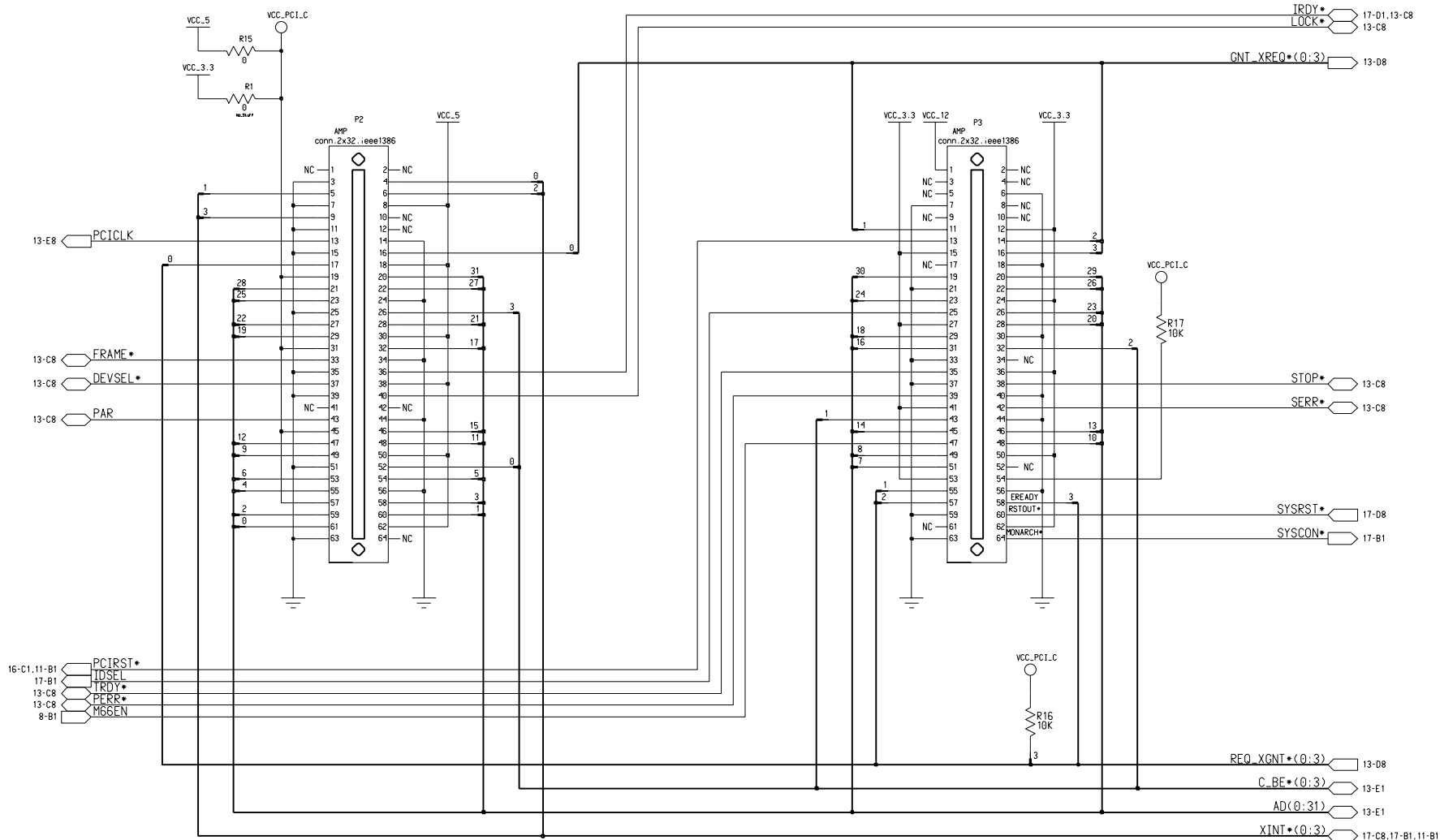
1. Keep MPC107 STERM trace length < 2cm.
2. Route SDCLK1:4 plus SDFEED to equal lengths.
3. Add 15cm (~1ns) ADDITIONAL delay to SDFEED.







1 PCI VIO SELECTION
Select 3.3V or 5V V(I/O) option.
Must match Sandpoint selection.



① 64-bit PMC Header
Used for additional power and ground only.

