
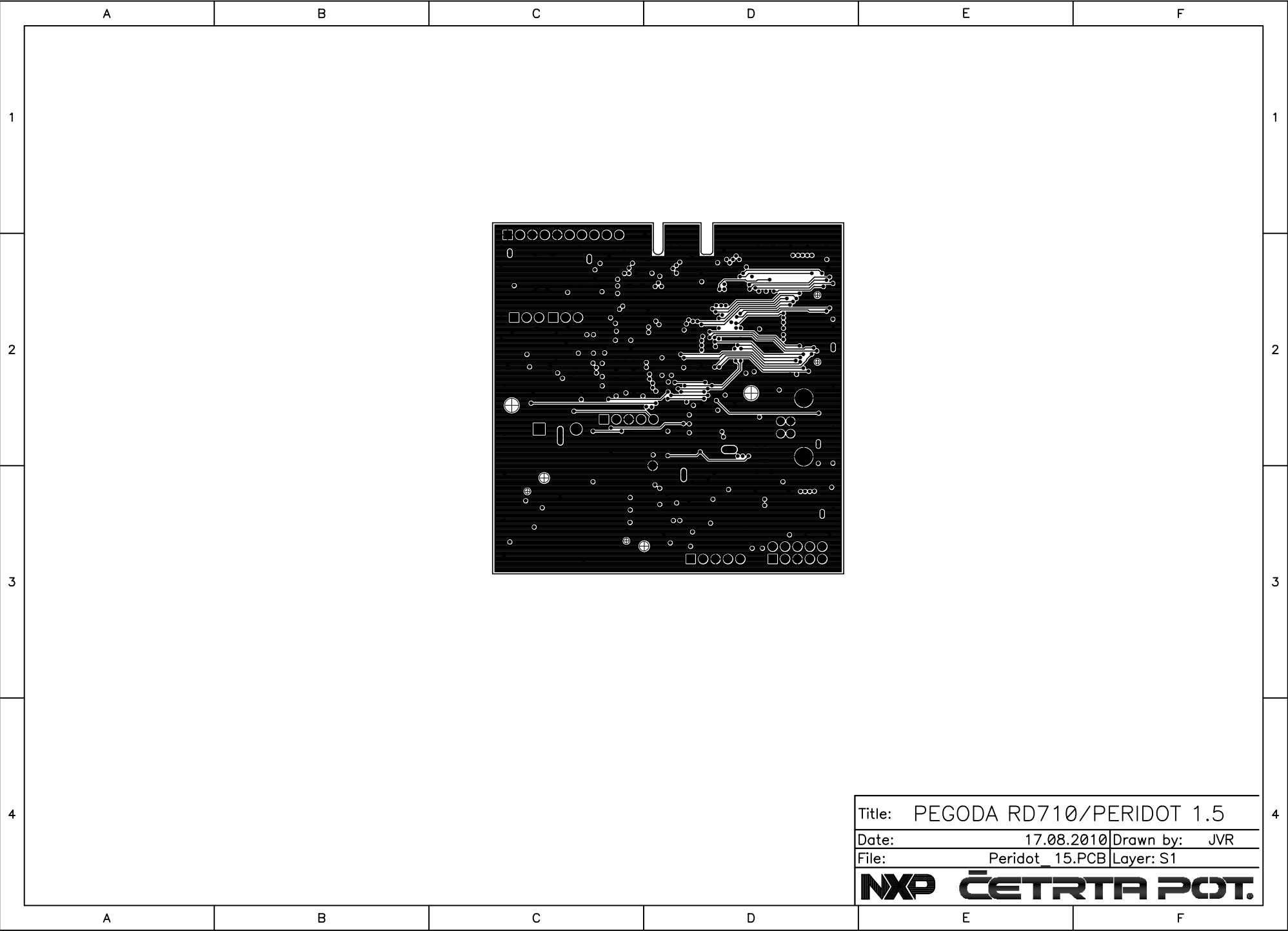
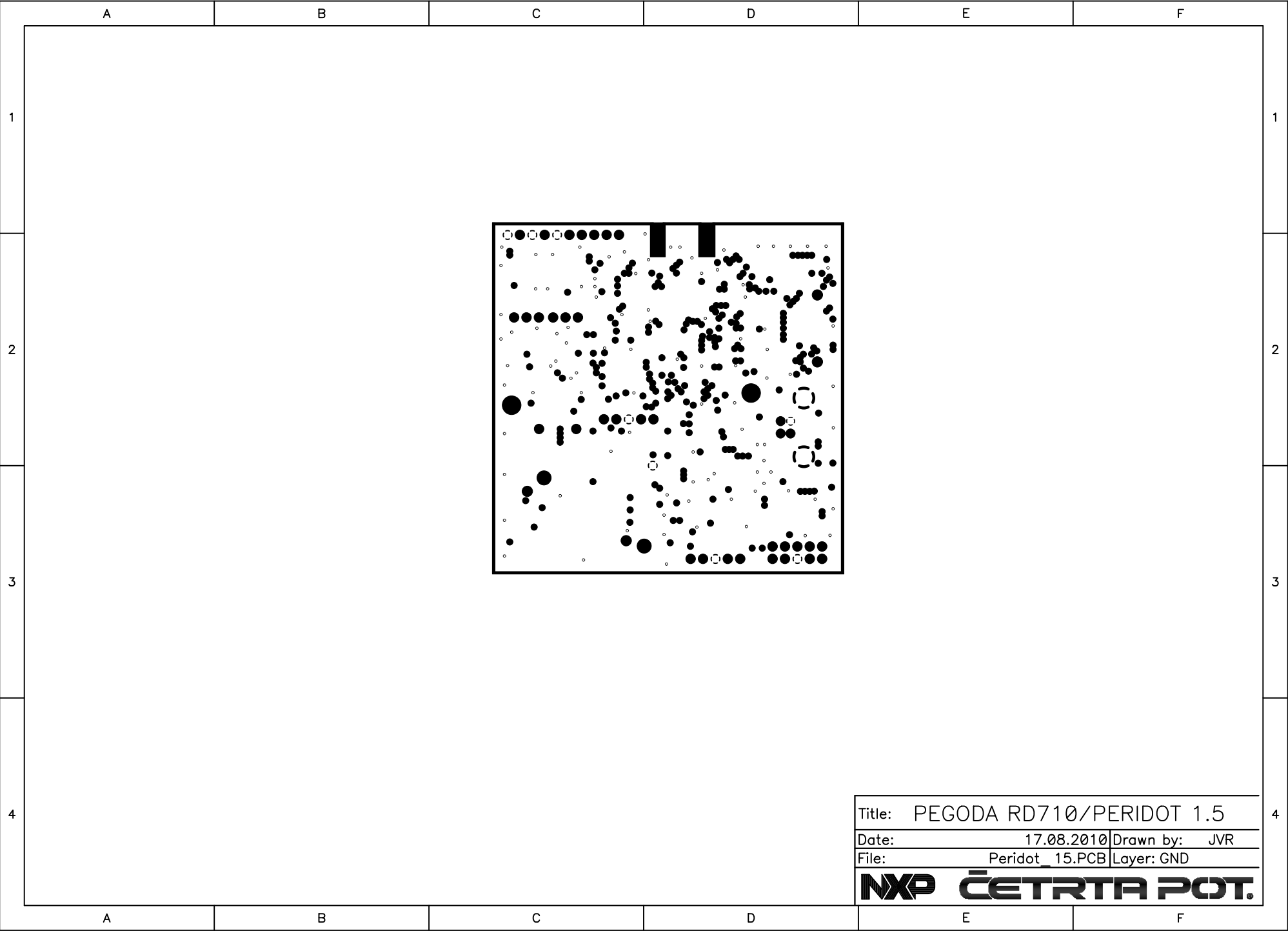
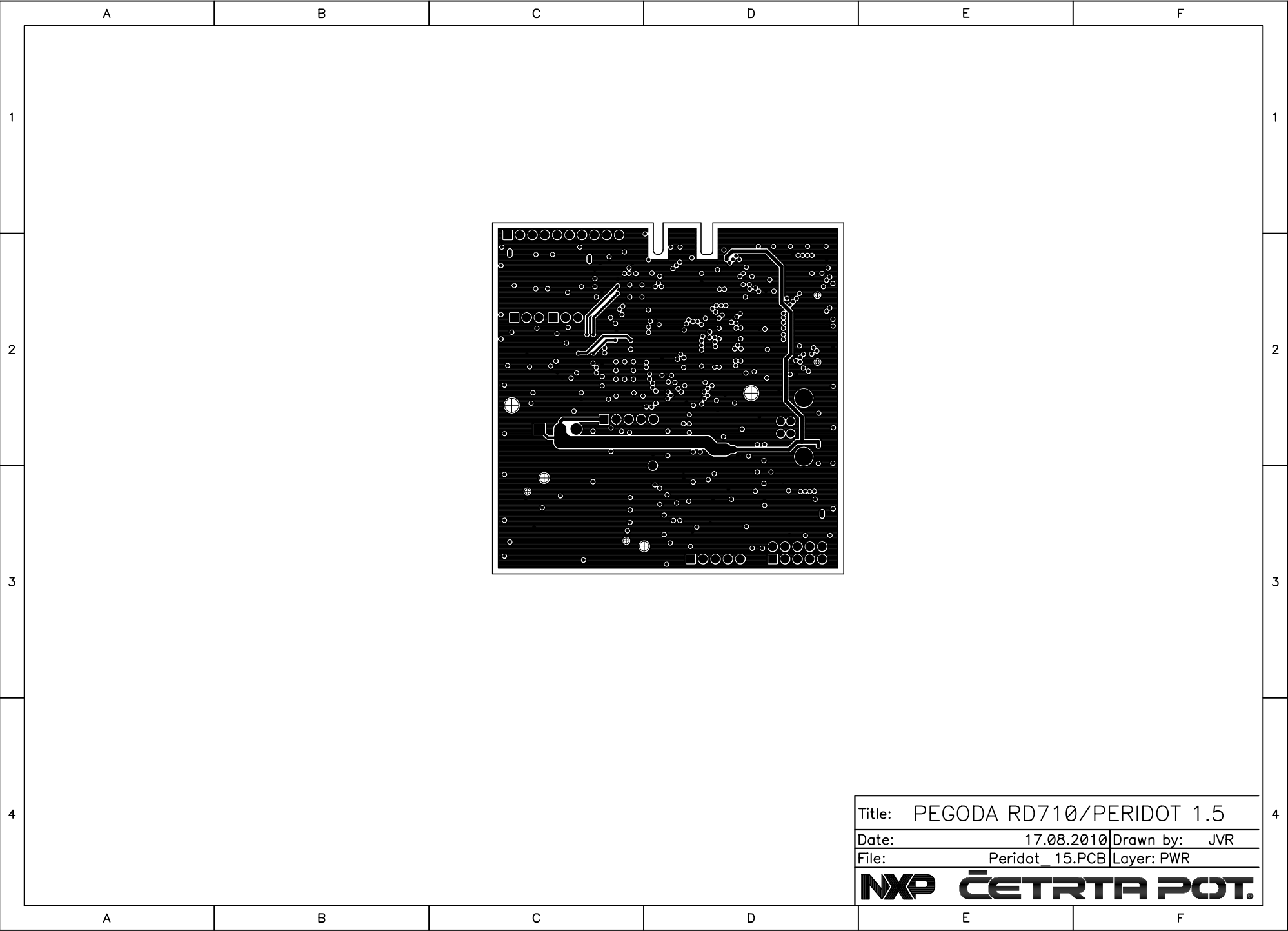


Title: PEGODA RD710/PERIDOT 1.5	
Date: 17.08.2010	Drawn by: JVR
File: Peridot_15.PCB	Layer: Top
	

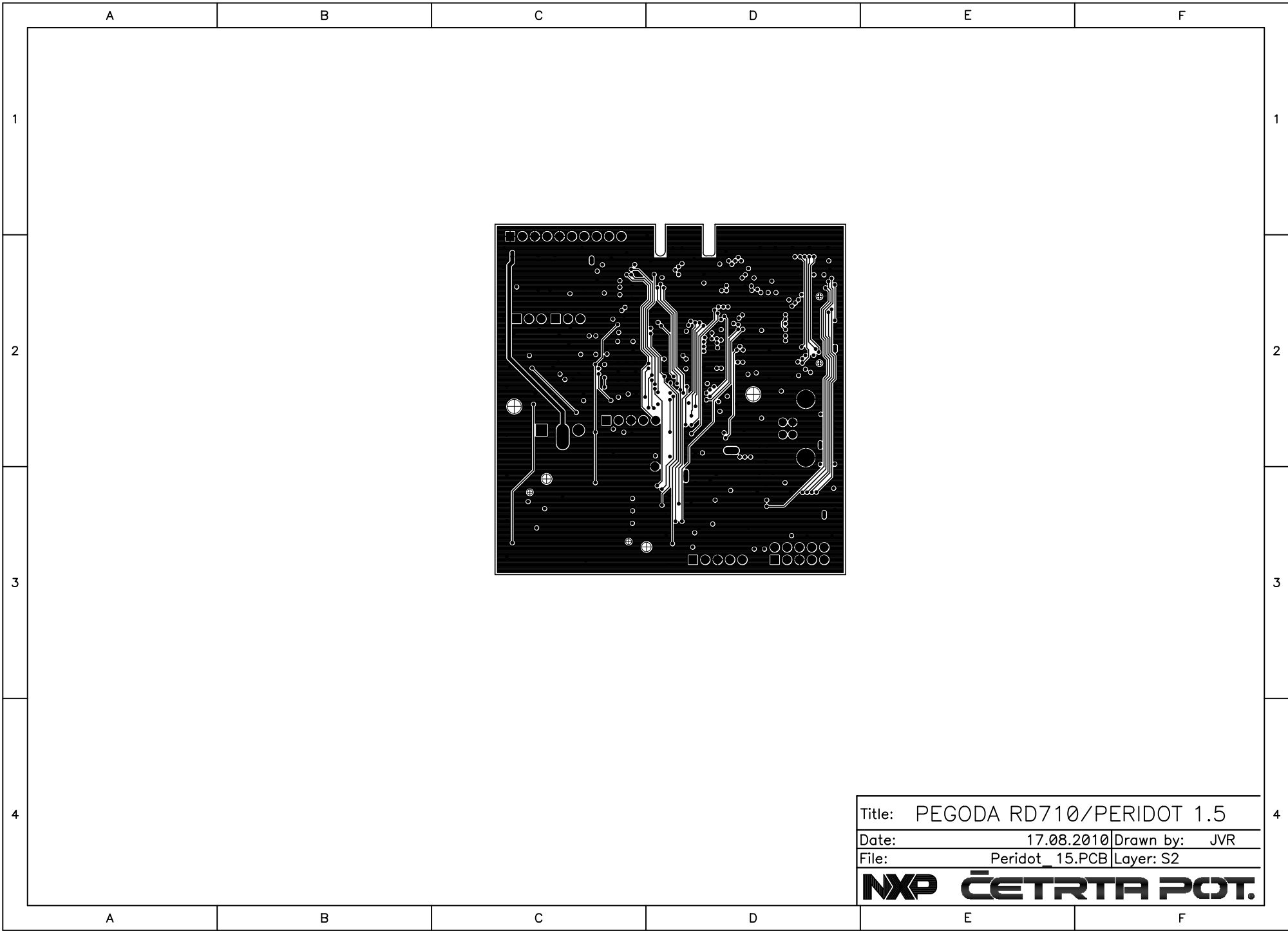




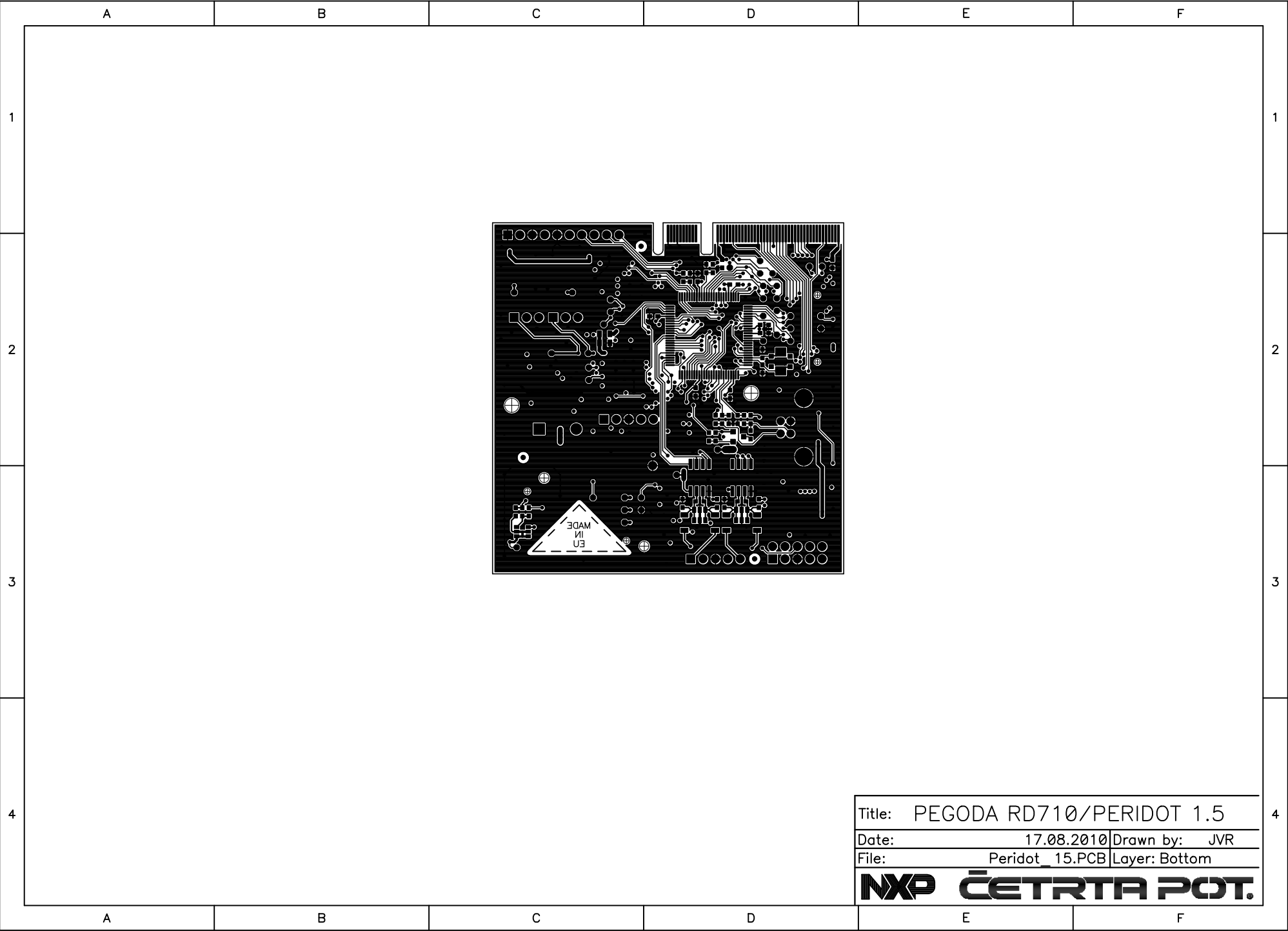
Title: PEGODA RD710/PERIDOT 1.5	
Date: 17.08.2010	Drawn by: JVR
File: Peridot_15.PCB	Layer: GND
NXP ČETRTRA POT.	



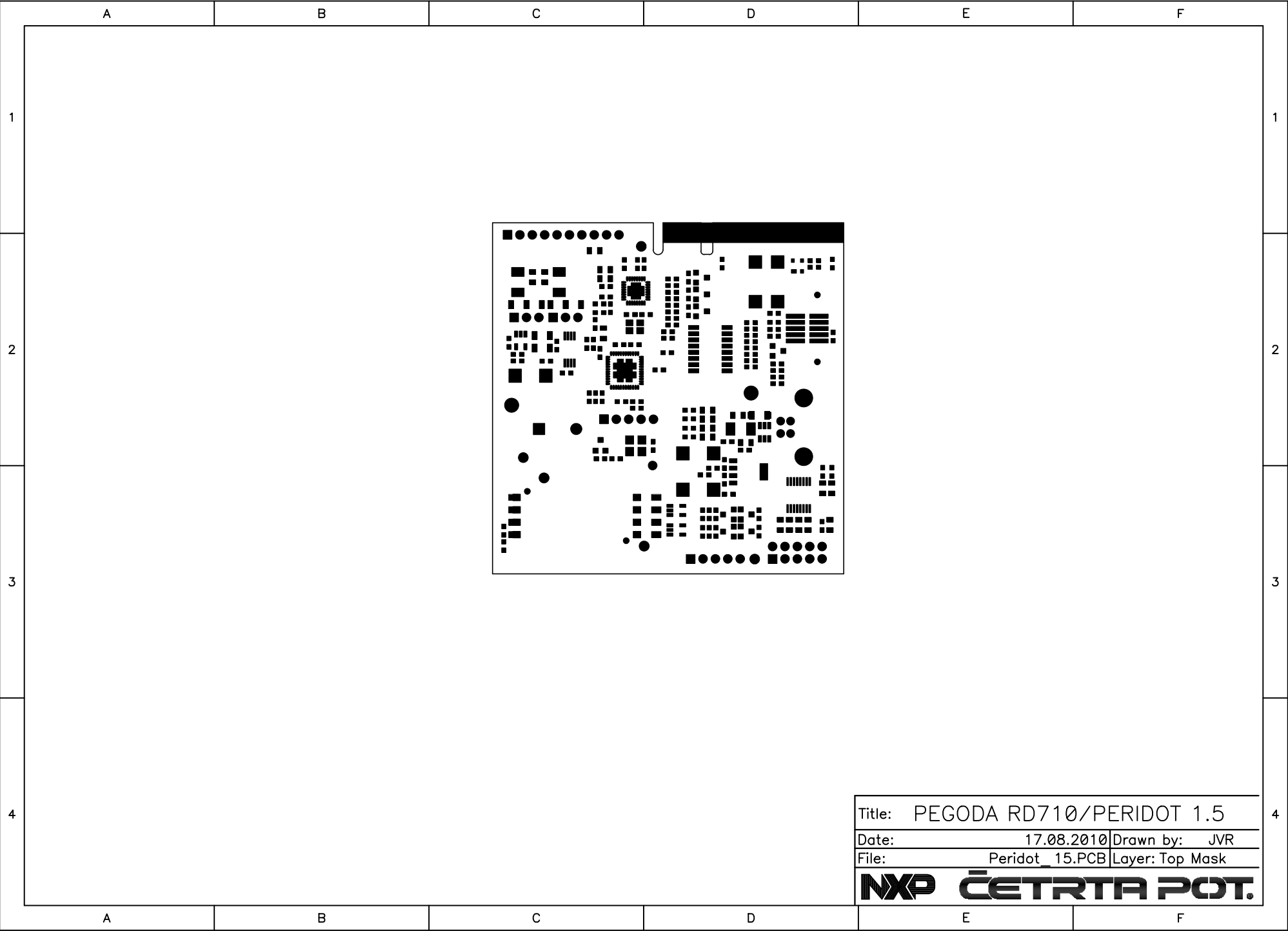
Title: PEGODA RD710/PERIDOT 1.5	
Date: 17.08.2010	Drawn by: JVR
File: Peridot_15.PCB	Layer: PWR
NXP ČETRTRA POT.	

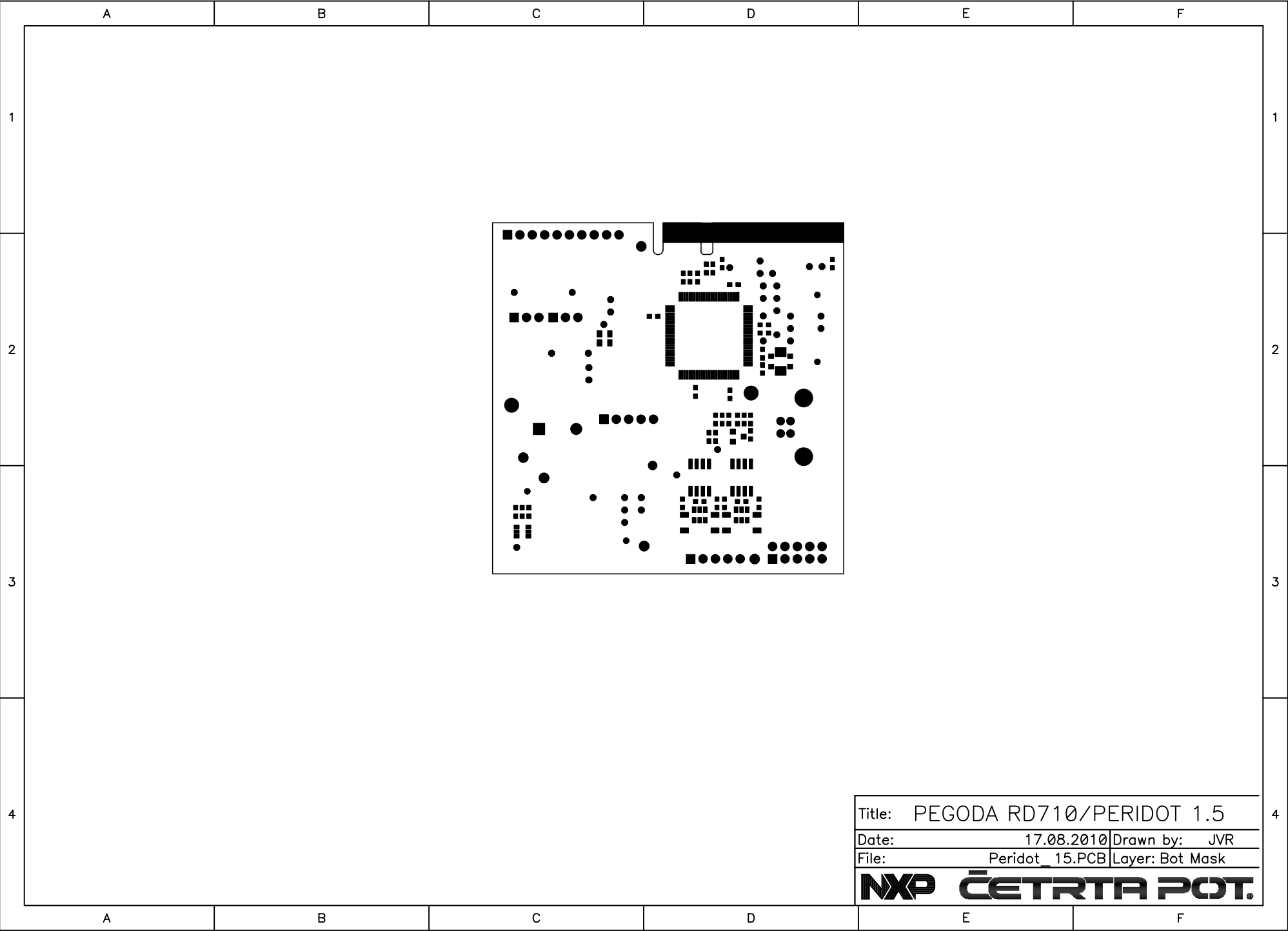


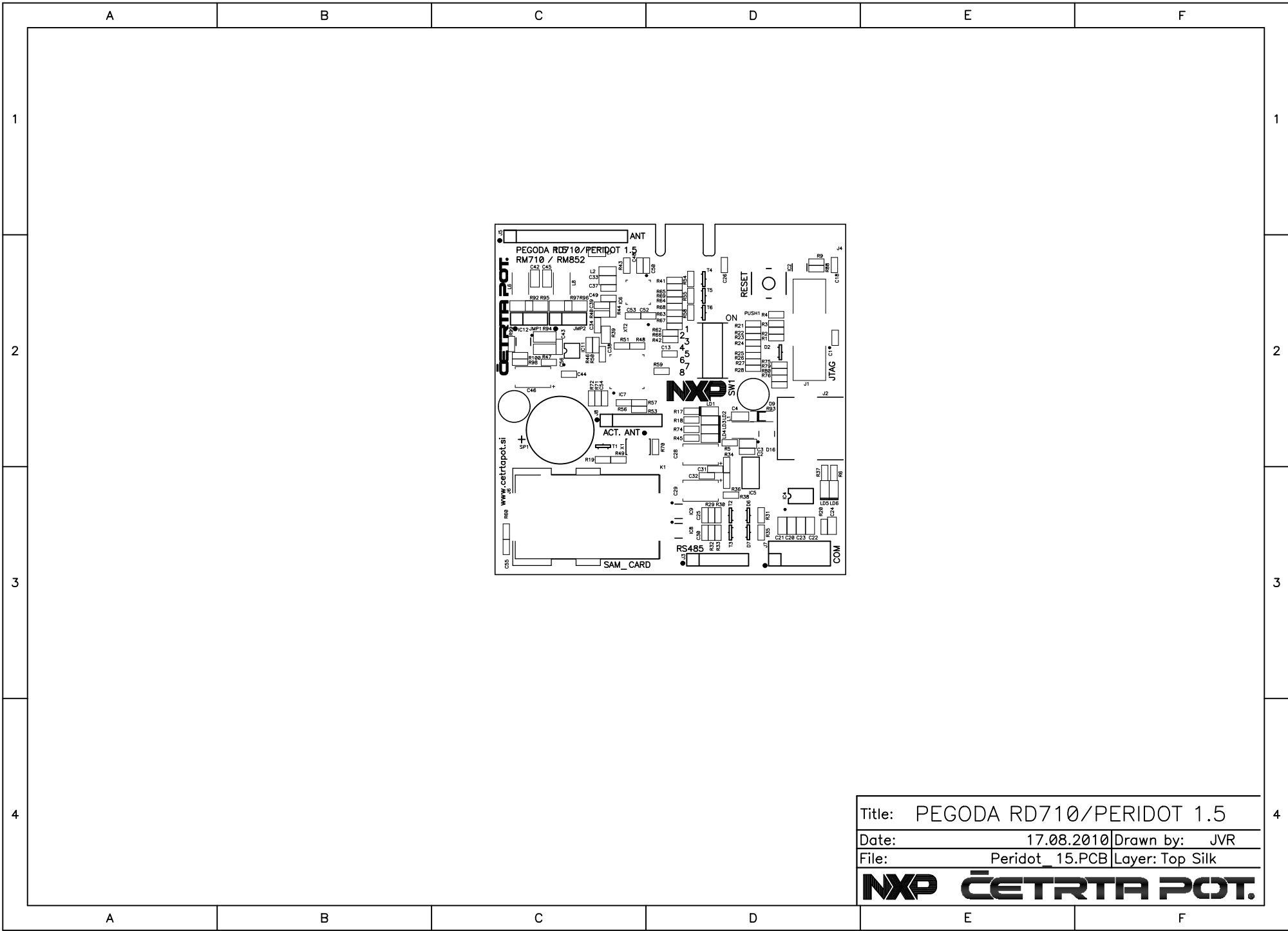
Title: PEGODA RD710/PERIDOT 1.5		
Date:	17.08.2010	Drawn by: JVR
File:	Peridot_15.PCB	Layer: S2
NXP ČETRTRA POT.		



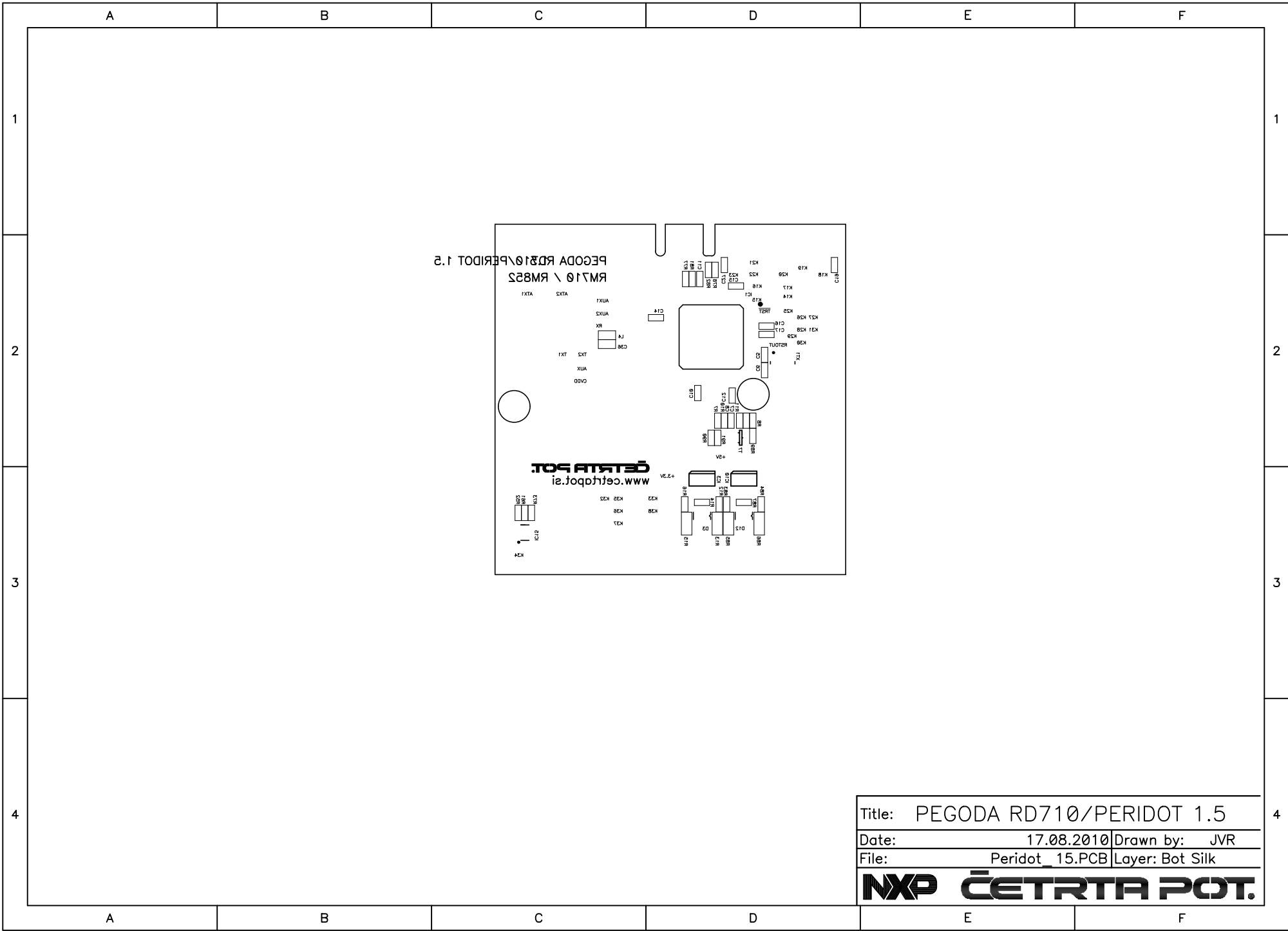
Title: PEGODA RD710/PERIDOT 1.5	
Date: 17.08.2010	Drawn by: JVR
File: Peridot_15.PCB	Layer: Bottom
NXP ČETRTRA POT.	

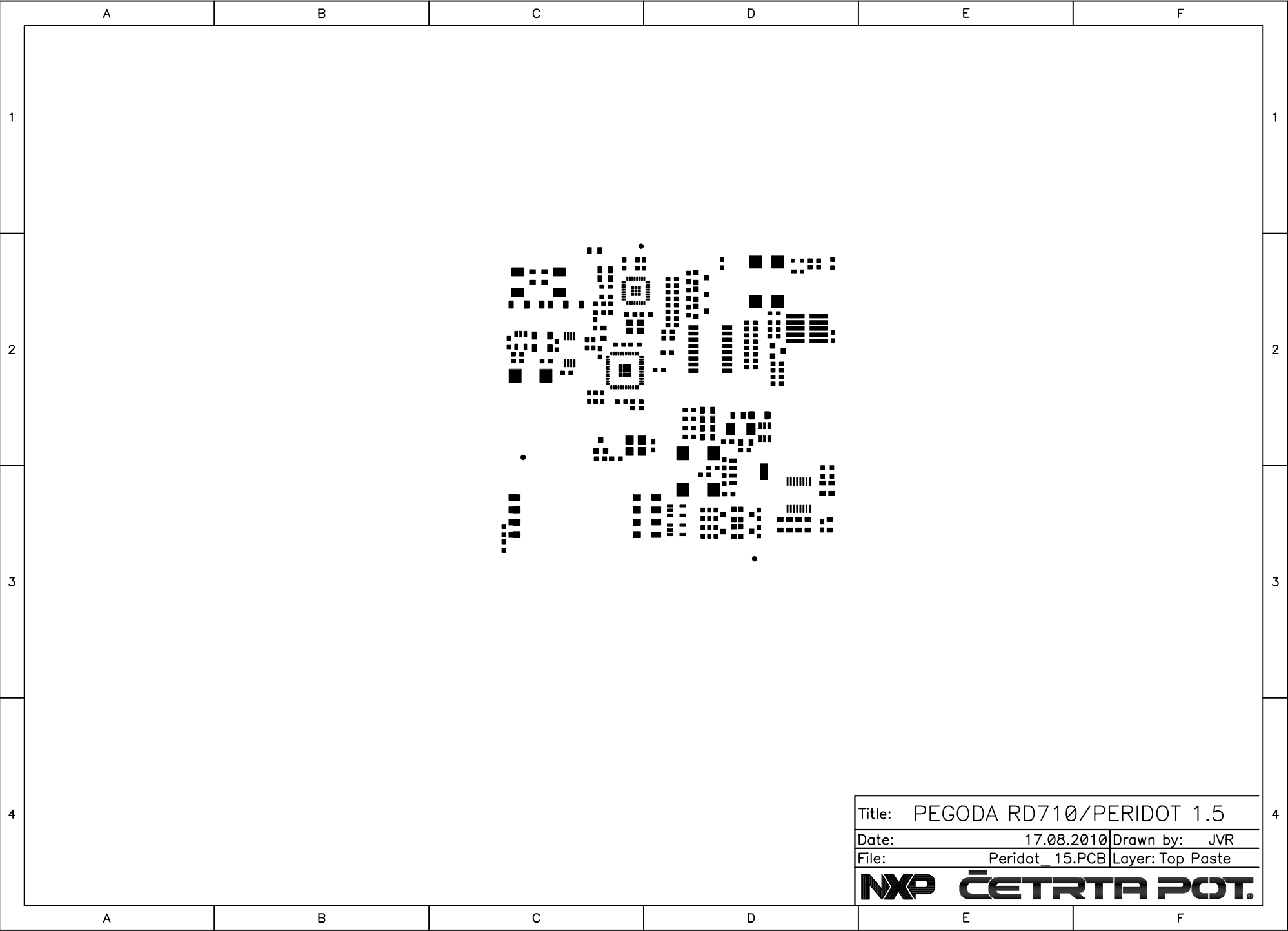


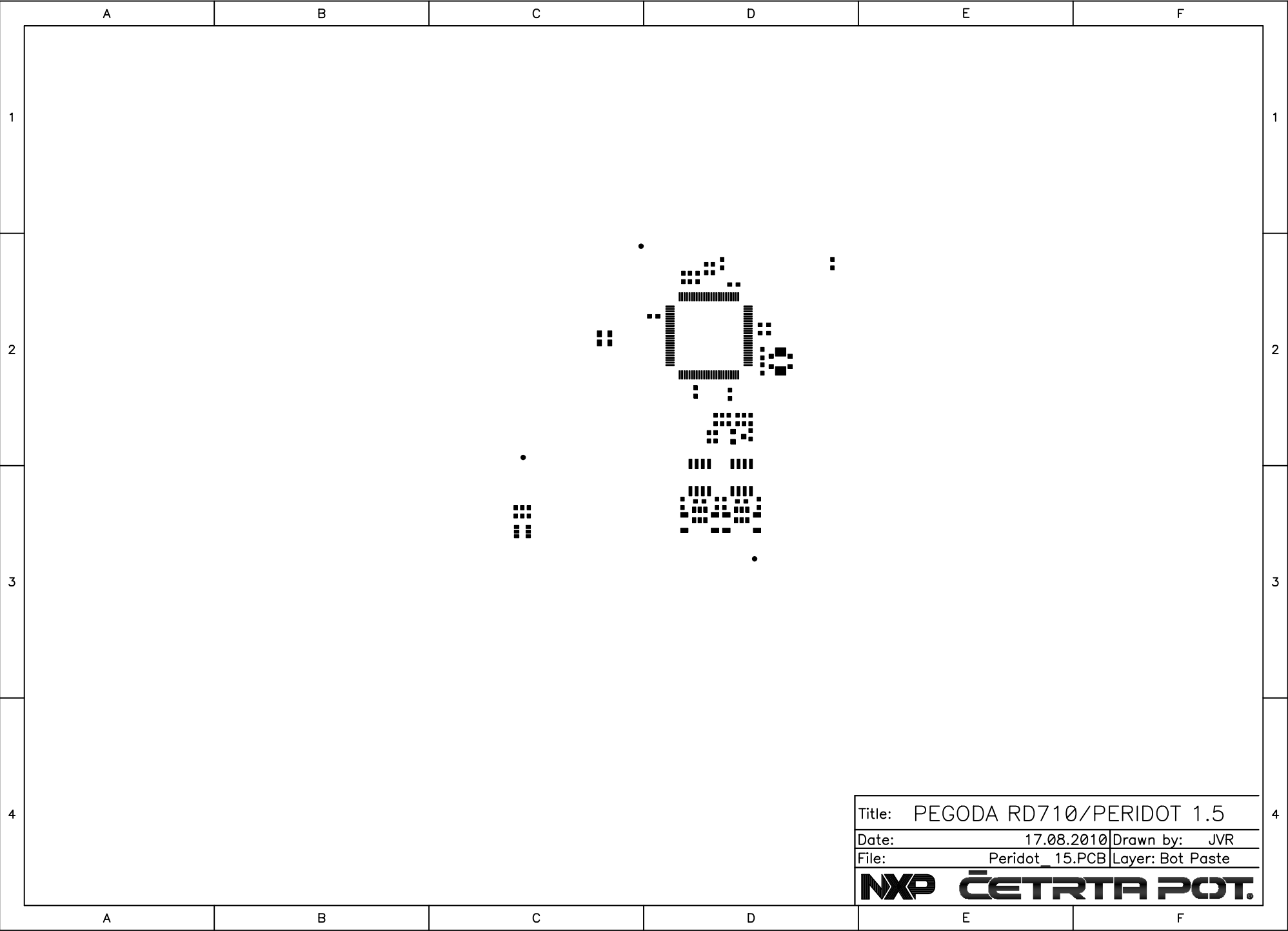




Title: PEGODA RD710/PERIDOT 1.5		
Date:	17.08.2010	Drawn by: JVR
File:	Peridot_15.PCB	Layer: Top Silk
NXP CETRITA POT.		





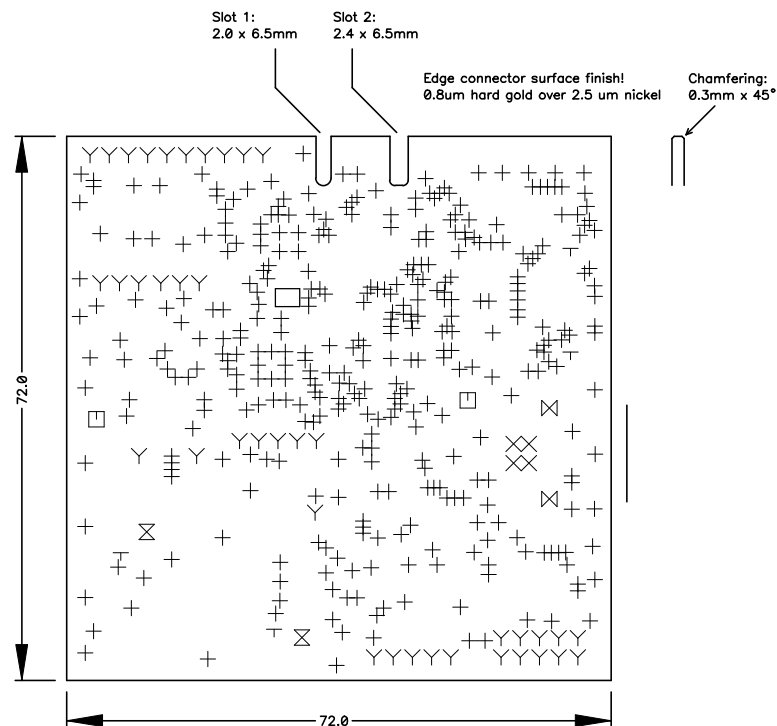


Master drawings: Peridot

- material: FR4
- thickness: 1.55mm
- layer stackup:
 - TOP: cu-foil: 17um
 - prepreg 2125: 100um
 - prepreg 2125: 100um
 - S1: cu-foil: 35um
 - core: 400um
 - GND: cu-foil: 35um
 - prepreg 2125: 100um
 - prepreg 2125: 100um
 - PWR: cu-foil: 35um
 - core: 400um
 - S2: cu-foil: 35um
 - prepreg 2125: 100um
 - prepreg 2125: 100um
 - BOT: cu-foil: 17um
- min. hole metalization: 20um
- surface finishing: HASL (Lead-free)
- solder mask:
 - in accordance with IPC-SM-840
 - Liquid Photo Imageable (LPI)
 - color: green
 - unless otherwise defined (in gerber), solder mask overlap on SMT pads is not allowed
- silk screen:
 - White
 - shall not extend on any pad, land area or plated through hole
- bow and twist:
 - max. 0.75% SMT boards
 - max. 1.5% THT boards
- point of origin (0,0): bottom left corner
- board is designed on 0.050 mm grid
- primary side: TOP layer

Drill Table

Hole Dia (mm)	Symbol	Quantity	Plated
0.300	+	370	Yes
0.920	X	4	Yes
1.016	Y	39	Yes
1.200	T	4	No
2.000	⊗	2	No
2.300	⊠	2	Yes
2.900	□	2	No



Title: PEGODA RD710/PERIDOT 1.5

Date: 17.08.2010 Drawn by: JVR

File: Peridot_15.PCB Layer: MasterDW

NXP **ČETRTRA POT.**