Table of Contents	
01.	TITLE & NOTES
02.	BATUR (P3B1602DP)

Revisions			
Rev	Description	Date	Approved
A	Final release of schematic	04-16-2026	Demetrio Cardenas

BATUR
P3B1602DP-EVB

Do Not Populate

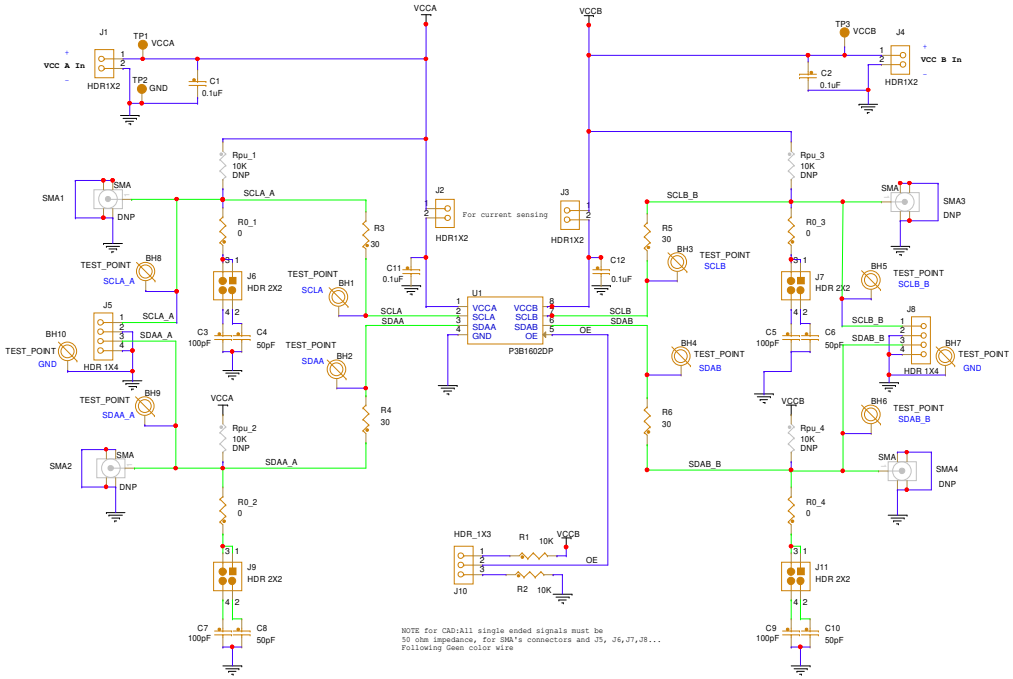
REF DES	*ASSY_OPT*	*PAGE NAME*
Rpu_1,Rpu_2,Rpu_3,Rpu_4,SMA1, SMA2,SMA3,SMA4	DNP	02. BATUR (P3B1602DP)

FUNCTION SPECIFIC ANALOG (FSA)
6501 William Cannon Drive West
Austin, TX 78735-8598

Designer: Demetrio Cardenas	Drawing Title: P3B1602DP-EVB	
Drawn by: Daniel Uribe	Page Title: 01. TITLE & NOTES	
Approved: Demetrio Cardenas	Size C	Document Number SCH-96736 PDF: SPF-96736 Rev A
	Date: Thursday, April 16, 2026	Sheet 1 of 2

BATUR (P3B1602DP)

tespoint de gancho para vcca y vccb y gnd de entraday tp pad para sda scl de los 2 lados.|



Note for CAD: Please put on top layer as custom silkscreen all the nets names that you see on schematic in each pin header or SMA.

NXP	FUNCTION SPECIFIC ANALOG (FSA) 6501 William Cannon Drive West Austin, TX 78735-8598	
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.		
© NXP SEMICONDUCTORS	Classification: Company Internal/Proprietary	
Designer: Demetrio Cardenas	Drawing Title: P3B1602DP-EVB	
Drawn by: Daniel Uribe	Page Title: 02. BATUR (P3B1602DP)	
Approved: Demetrio Cardenas	Size C / Document Number SCH-96736 PDF: SPF-96736	Rev A
	Date: Friday, April 17, 2026	Sheet 2 of 2