MCIMX8QM-CPU MEK Platform

Schematic capture done with Allegro Design Entry CIS 17.2. Schematic also available in 16.2.

ICAP Classification: CP: ___ IUO: ___ PUBI: _X_

Drawing Title: **i.MX 8QM CPU CARD**

Page Title: **FRONT PAGE**

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30	BOARD TO BOARD CONNECTORS
31	LEVEL TRANSLATORS & DRIVERS
32	MISCELLANEOUS

i.MX 8QM CPU Card

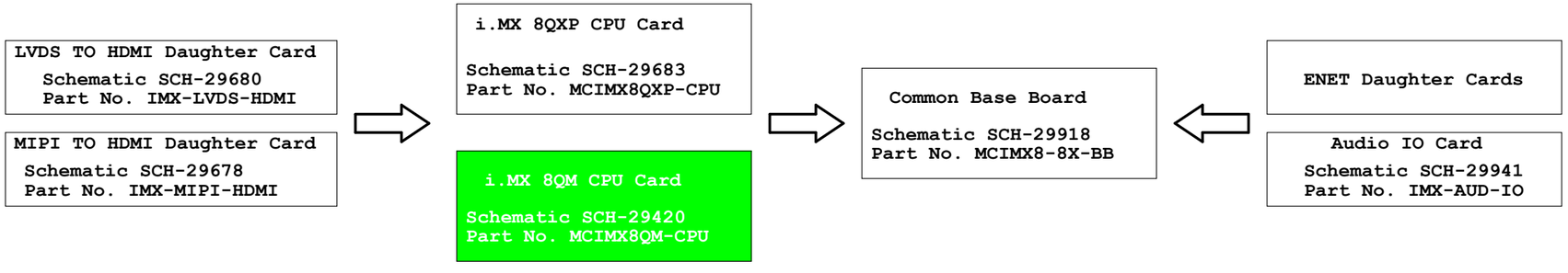
Part Number: MCIMX8QM-CPU

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass production design. For an added resource, refer to Hardware Development Guide document.

Consumer devices were utilized in this design when lead time for equivalent automotive-grade devices conflicted with production schedules. NXP suggests consulting component suppliers for equivalent automotive-grade device information.

DNP appearing near a component signifies "do not populate."
These parts are not installed

REV	Revision Notes	Date
C1	1. Sheet No. 8 : Pull-Up Resistors removed from PMIC pin 1. Pin 44 tied to Pin 41, to minimize quiscent current 2. Sheet No. 17 : SATA Boot Option removed from the boot mode list 3. Sheet No. 22 :1uF Capacitor is added in series with HDMI_RX0_ARC_P (For fixing HDMI RX side issues) 4. Sheet Nos. 9 & 16: Changed R383 from 1K to 100E, SD Card Power Changed from VCC_PER_3V3 to VCC_EXT_3V3 and Discharge Circuit for EXT_1V8 Added (For fixing power discharge issues while Processor reset) 5. Sheet No. 24 : Changed Headphone Jack Pinout to AHJ (Pins 1 & 4 Swapped) and added AHJ Graphic (Headphone JacK reconfiguration) 6. Sheet No. 19 : FTDI Chip updated to FT4232H 7. Sheet No. 30 : Connector J20 symbol updated 8. Sheet Nos.12 & 19 : Option provided for connecting SCU UART signals to FTDI Chip for debug 9. Sheet No . 21 : PCIe clock selection (internal / external) option provided 10. Sheet No 9 : PMIC2 WDI disconnected as per PMIC errata ER023 (R113 Unmounted) 11. Sheet Nos 14 & 15 : DDR_CH0_RST_B & DDR_CH1_RST_B Pulldown to Ground with 10K (Added R1481 & R1482) 12. Sheet Nos 12: Added R1483 & R1484 for ANA_TEST_OUT 0 and 1	08-08-2018
C2	1. Processor part number updated to "PIMX8QM6AVUFFAB"	17-09-2018
C3	C3 is internal release, not used for layout update. 1. PMIC_1 (U10) P/N updated to MC33PF8100EPES PMIC_2 (U23) P/N updated to MC33PF8100EQES 2. Following obsolete P/N updated: DA1,DA2 - BAV99LT1G (ON SEMICONDUCTOR) J1,J6 - 47659-1100 (MOLEX) U17,U18 - MT53E768M32D4DT-053 AIT:E (MICRON)	22-Nov-2019
C4	No electrical changes. 1. Classification changed to Public Information. 2. Note updates. 3. U15 Processor and U10/U23 PMICs updated to production part numbers. 4. Following P/N updated back to: DA1,DA2 - BAV99 (FAIRCHILD) J1,J6 - 47659-1000 (MOLEX)	24-Jan-2020
C5	Following Parts Updated:- 1. HDMI Connector J1 and J6 updated to 476591100. Footprint number differs from layout rev C1, but is compatible per CM. 2. U37 updated to PTN5110NTHQZ 3. DA1 and DA2 updated to BAV99LT1G. Footprint number differs from layout rev C1, but is compatible per CM. 4. C531 made as DNP 5. R369 value changed to 23.2K for increasing Current limit of load switch to 3A	09-Jun-2020
C6	No electrical changes. 1. Processor does not support MLB; removed MLB from diagrams on sheets 3 & 4. Added notations on sheets 6, 10, 13, 16, 30. 2. Added USB VBUS disable pull-down note & VBUS circuit (as a note) to sheet 20. 3. Added UART3 & UART4 net name error notes to sheets 13 & 30.	13-Jan-2021
C7	No electrical changes. 1. Fixed BOM notation error on C547. The assembly option was "NM" and now changed to a blank field. This capacitor has always been installed. See sheet 20.	18-Jan-2021



Additional information on compatible daughter cards, cameras, etc. is provided on the nxp.com website.

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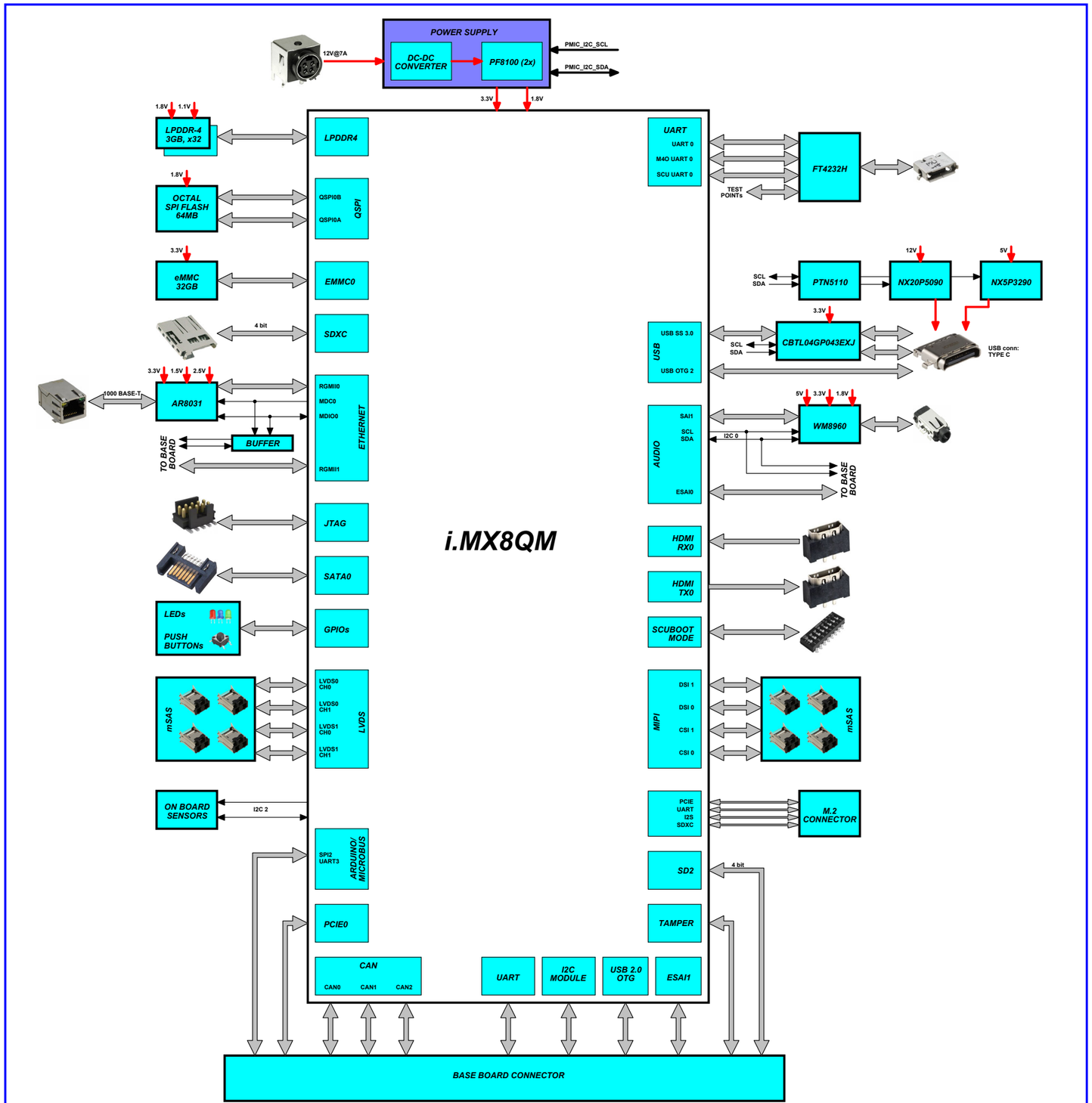
i.MX 8QM CPU BOARD BLOCK_DIAGRAM



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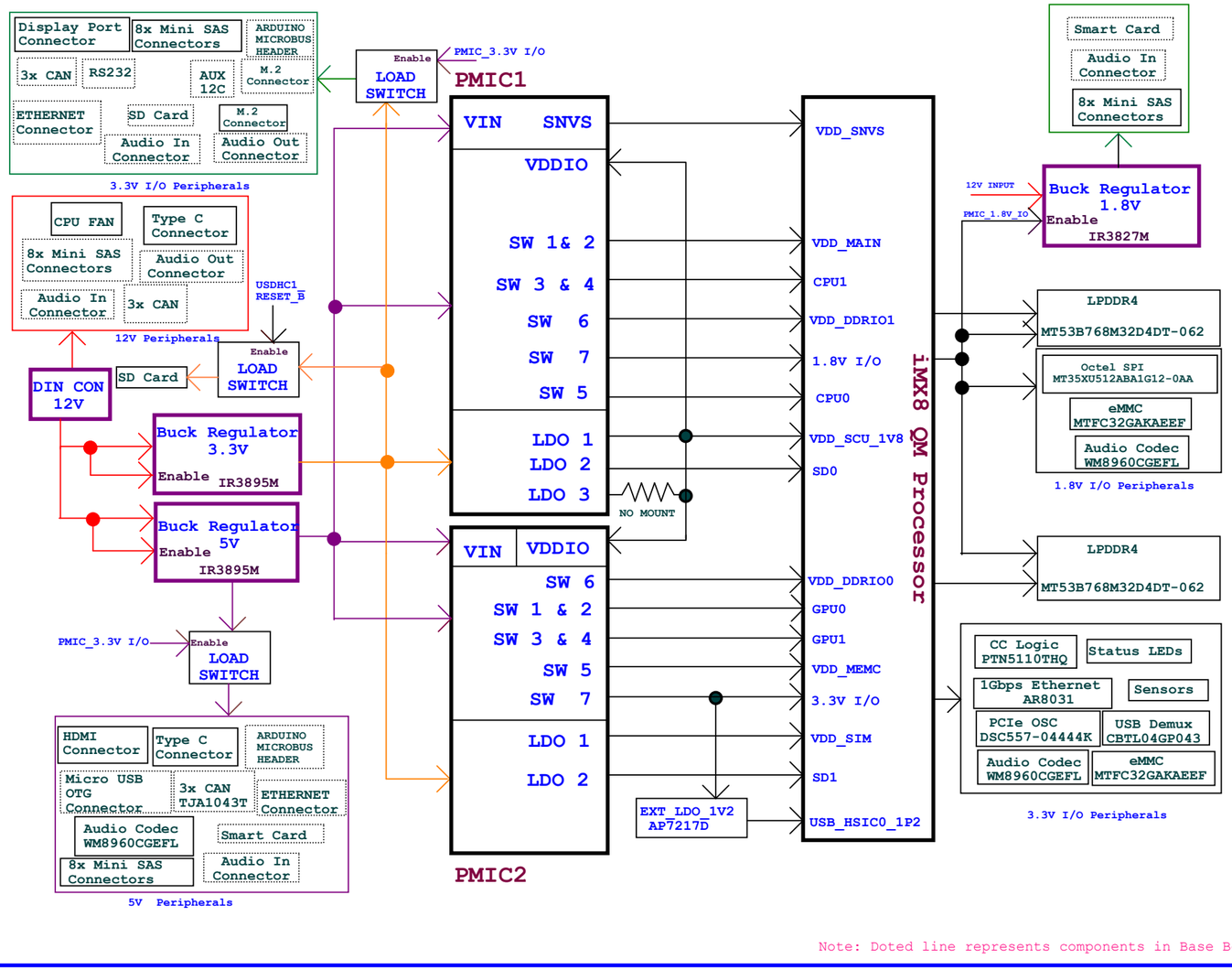
Power Flow Diagram



Note: Doted line represents components in Base Boad.

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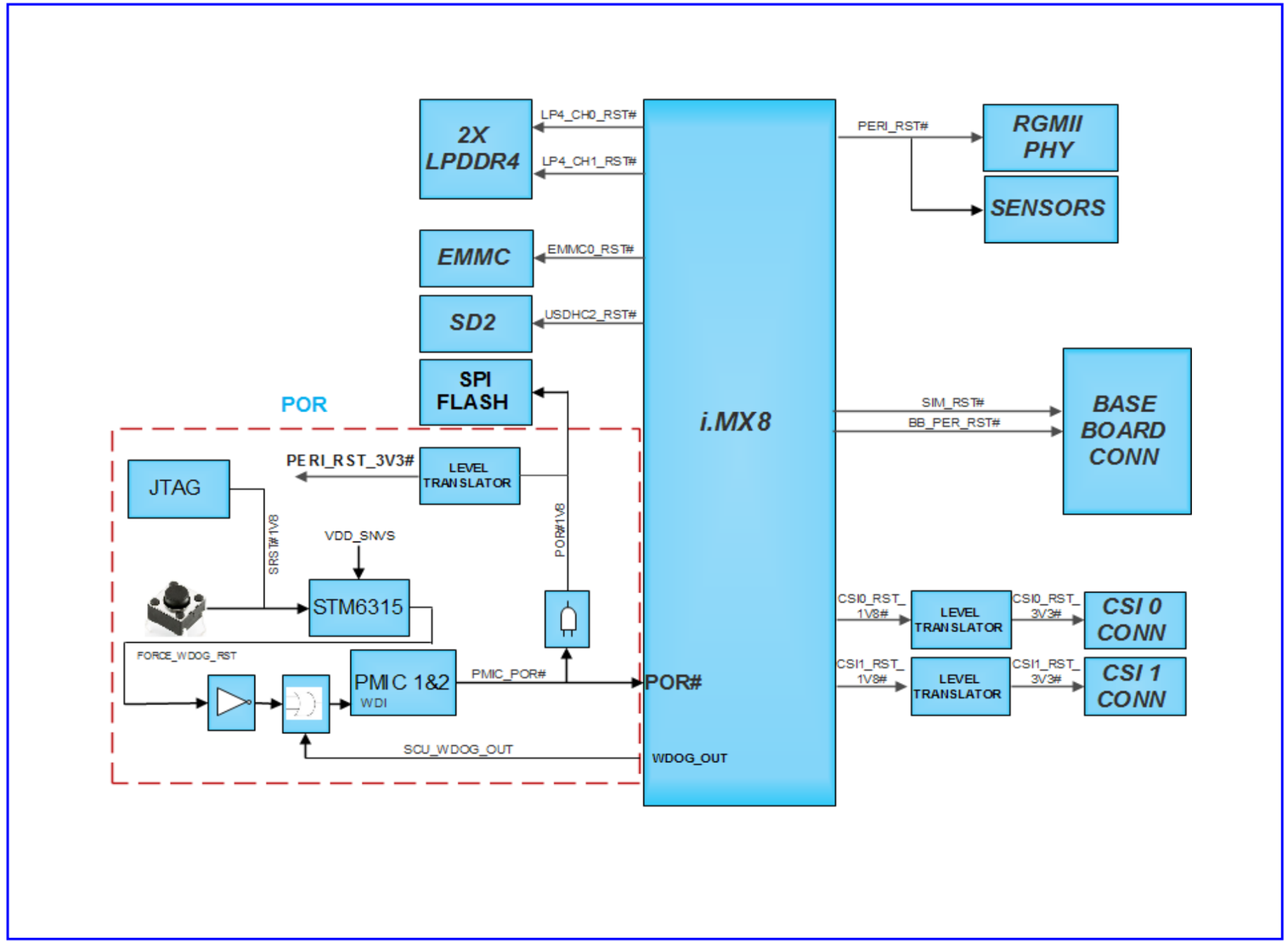
BLOCK DIAGRAM - RESET



ICAP Classification: CP: ___ IUO: ___ PUBI: _X_

Drawing Title: i.MX 8QM CPU CARD

Page Title: BLOCK DIAGRAM - RESET

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i.MX 8QM CPU CARD I2C TABLE

DEVICE	Location	Speed(kbps)	8-bit write addresses	DEVICE ADDRESS	I2C	IO LEVEL
PMIC1	CPU	3400		0x08	PMIC I2C	1.8V
PMIC2	CPU	3400		0x09	PMIC I2C	1.8V
FXOS8700CQ	CPU	400	0x1E	0x1E	I2C0	3.3V
MPL3115A2	CPU	400	0xC0	0x60	I2C0	3.3V
FXAS21002CQR1	CPU	400	0x40	0x20	I2C0	3.3V
PTN5110	CPU	400	0xA2	0x51	I2C0	3.3V
ARDUINO/MIKROBUS	BASE				I2C0	3.3V
ENET CONN	BASE				I2C0	3.3V
MLB*	BASE			0x40	I2C0	3.3V
AUDIO IN/OUT	BASE			0x90	M41.I2C	1.8V
WM8960	CPU			0x34	I2C1	1.8V
AUX I2C	BASE			0x20	I2C4	3.3V

* MLB is not supported by the processor.

ICAP Classification: CP: ___ IUO: ___ PUBI: X

Drawing Title: i.MX 8QM CPU CARD

Page Title: I2C TABLE

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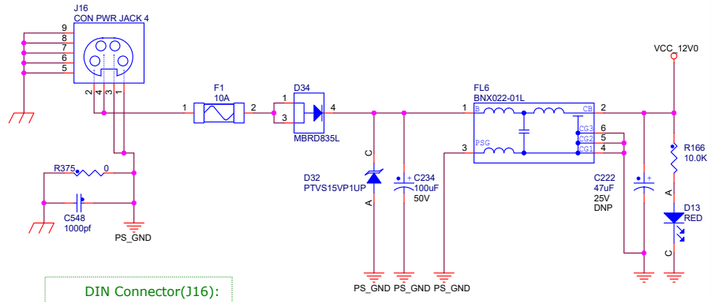
POWER SUPPLY

12V DC INPUT DIN CONNECTOR

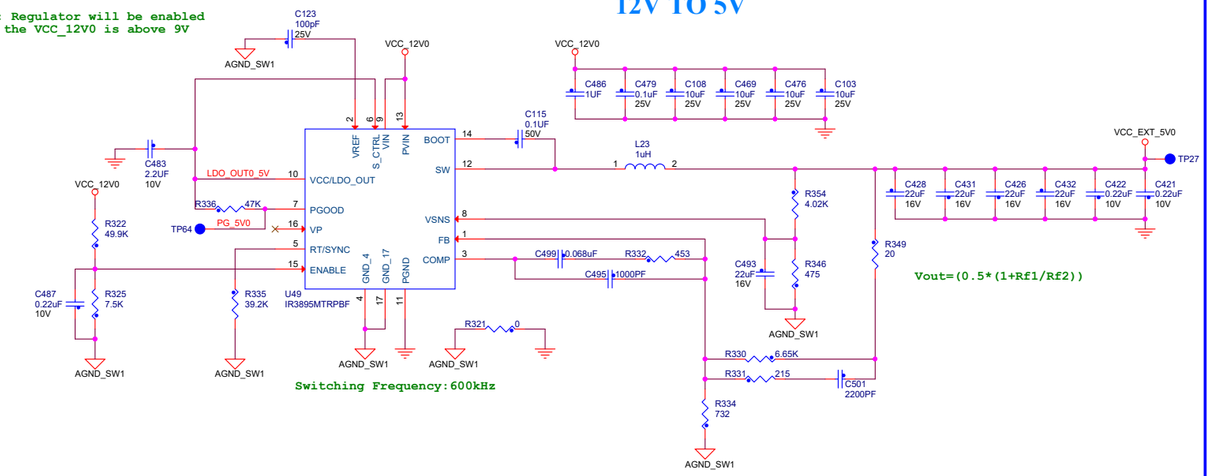


DIN Connector(J16):

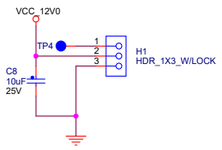
Part number: KPJX-4S-S
Vendor : Kycon

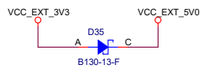
12V TO 5V

Note: Regulator will be enabled once the VCC_12V0 is above 9V

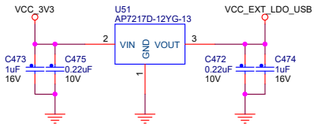


FAN CONNECTOR



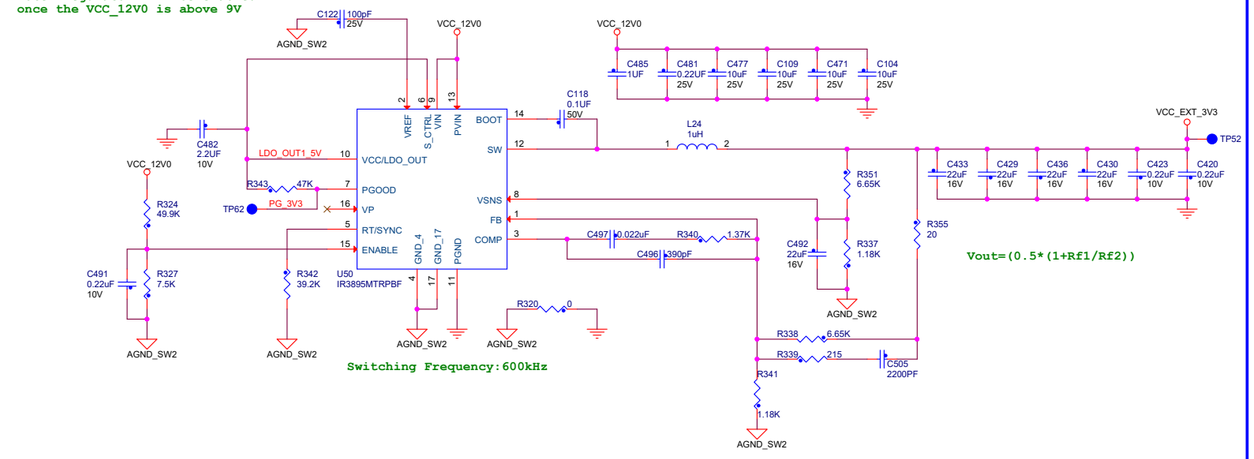


LDO FOR 1V2:VDD_USB_HSIC0_1P2

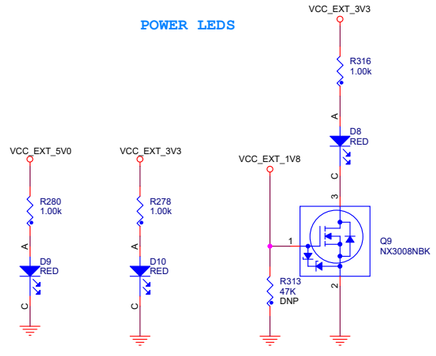


12V TO 3.3V

Note: Regulator will be enabled once the VCC_12V0 is above 9V

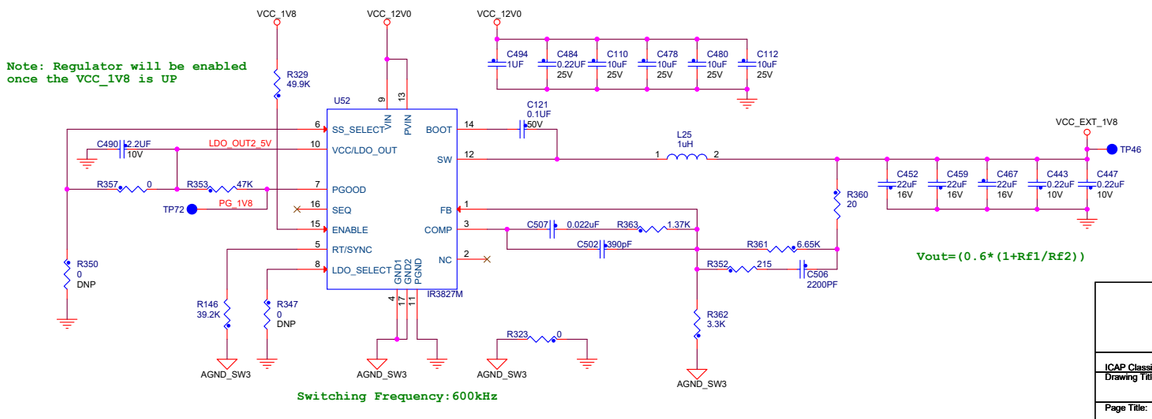


POWER LEDS



12V TO 1.8V

Note: Regulator will be enabled once the VCC_1V8 is UP



Switching Frequency:600kHz

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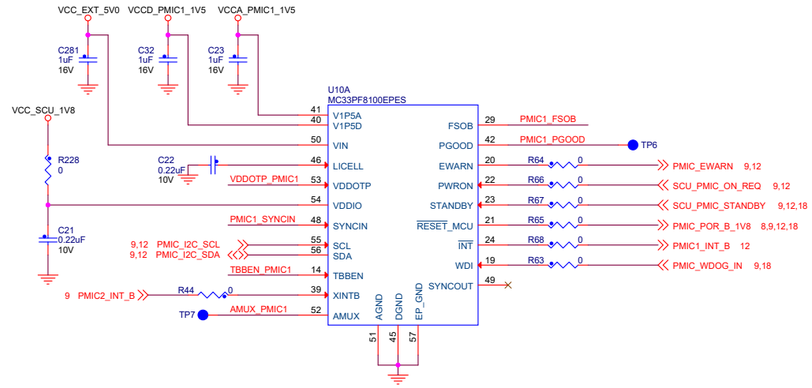
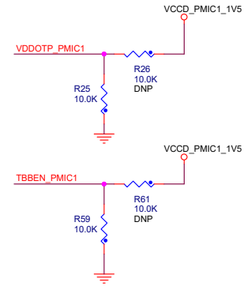
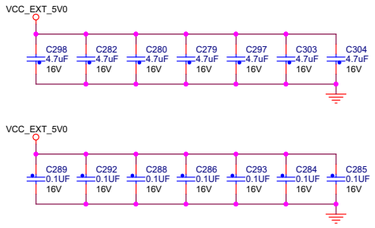
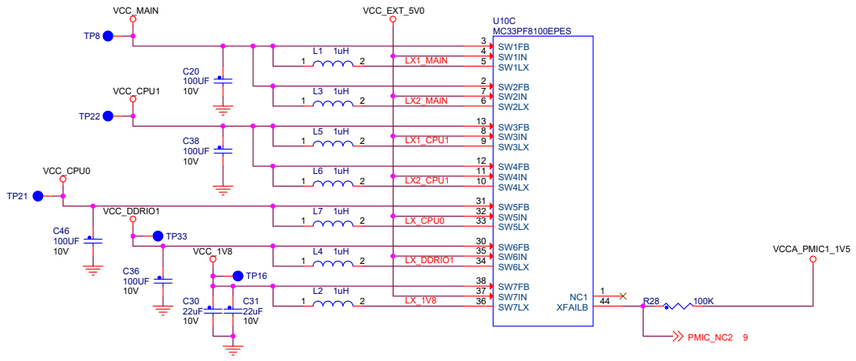
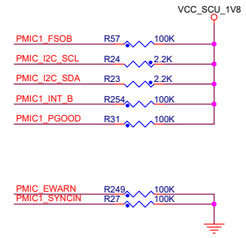
POWER SUPPLY - PMIC 1

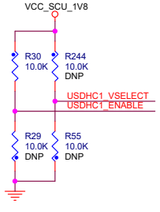


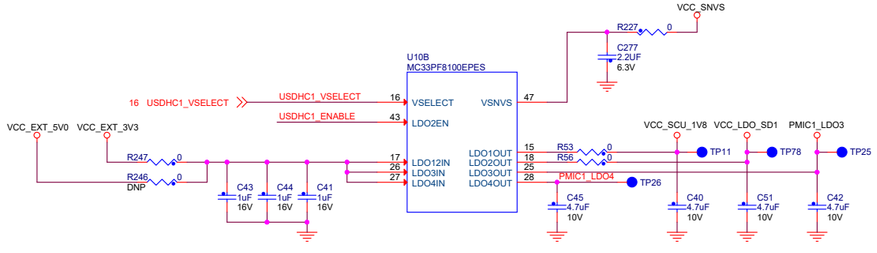


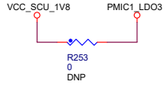




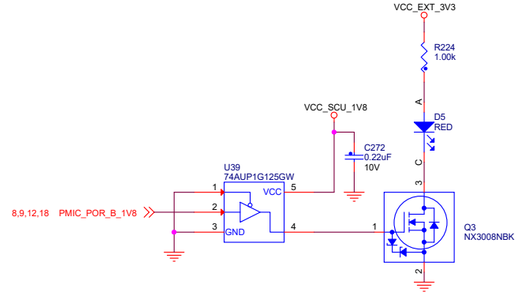








IMX8 RESET INDICATION



LED WILL BE ON WHEN IMX8 IS IN ACTIVE STATE

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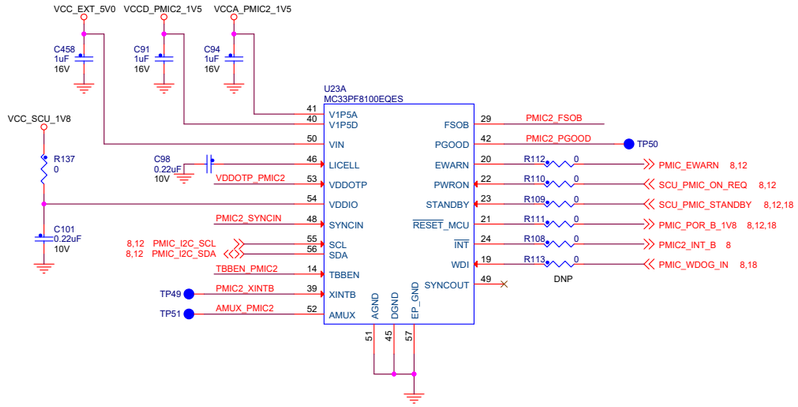
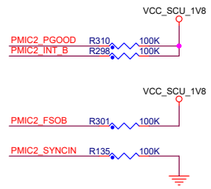
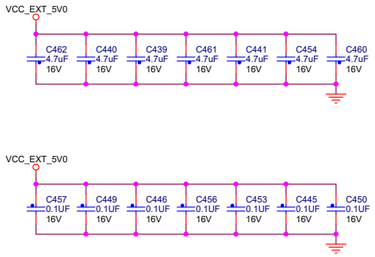
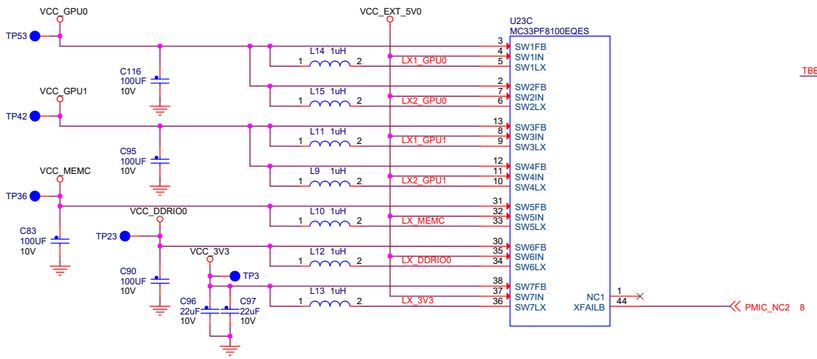
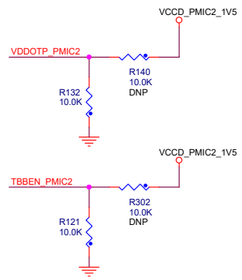
POWER SUPPLY - PMIC 2

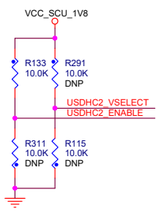


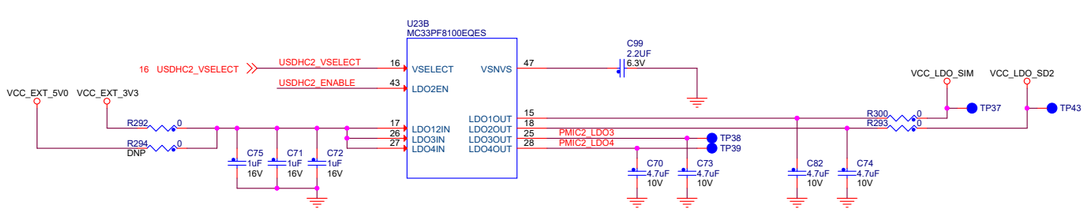




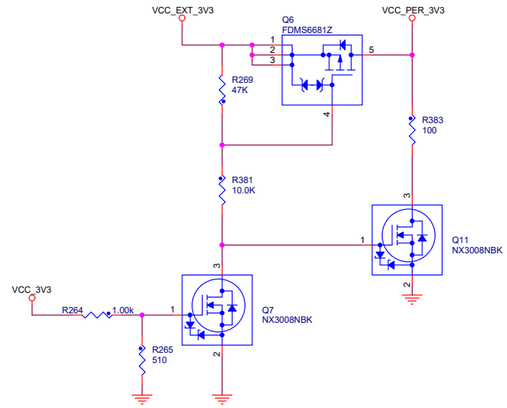




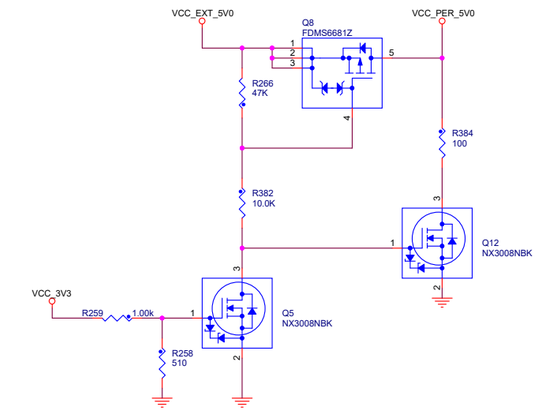




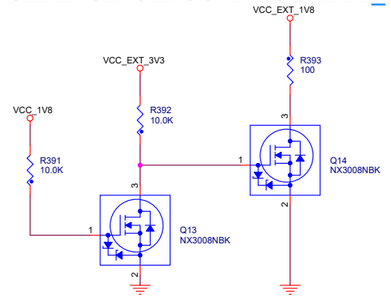
LOAD SWITCH FOR 3V3 PERIPHERALS



LOAD SWITCH FOR 5V0 PERIPHERALS



DISCHARGE CIRCUIT FOR EXT_1V8



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Mount devices between dashed green lines and U15 symbol under BGA.

IMX8QM POWER

U15Q
MIMX8QM6AVUFFAB

VCC_DDRIO1: C283 22uF 16V, C389 22uF 16V, C398 2.2uF 10V, C391 2.2uF 10V, C362 2.2uF 10V, C382 2.2uF 10V, C370 2.2uF 10V, C404 2.2uF 10V

AD16 VDD_DDR_CH1_VDDQ_CKE_3
AC15 VDD_DDR_CH1_VDDQ_CKE_2
AB16 VDD_DDR_CH1_VDDQ_CKE_1
Y16 VDD_DDR_CH1_VDDQ_10
W15 VDD_DDR_CH1_VDDQ_9
V16 VDD_DDR_CH1_VDDQ_8
U15 VDD_DDR_CH1_VDDQ_7
AJ15 VDD_DDR_CH1_VDDQ_6
AH16 VDD_DDR_CH1_VDDQ_5
AG15 VDD_DDR_CH1_VDDQ_4
AF16 VDD_DDR_CH1_VDDQ_3
AE15 VDD_DDR_CH1_VDDQ_2
AA15 VDD_DDR_CH1_VDDQ_1

VCC_DDRIO0: C85 22uF 16V, C100 22uF 16V, C401 2.2uF 10V, C365 2.2uF 10V, C374 2.2uF 10V, C387 2.2uF 10V, C395 2.2uF 10V, C359 2.2uF 10V

AD38 VDD_DDR_CH0_VDDQ_CKE_3
AC39 VDD_DDR_CH0_VDDQ_CKE_2
AB38 VDD_DDR_CH0_VDDQ_CKE_1
Y38 VDD_DDR_CH0_VDDQ_10
W39 VDD_DDR_CH0_VDDQ_9
V38 VDD_DDR_CH0_VDDQ_8
U39 VDD_DDR_CH0_VDDQ_7
AJ39 VDD_DDR_CH0_VDDQ_6
AH38 VDD_DDR_CH0_VDDQ_5
AG39 VDD_DDR_CH0_VDDQ_4
AF38 VDD_DDR_CH0_VDDQ_3
AE39 VDD_DDR_CH0_VDDQ_2
AA39 VDD_DDR_CH0_VDDQ_1

VCC_CPU0: C336 100UF 10V, C335 100UF 10V, C342 2.2uF 10V, C340 2.2uF 10V, C332 2.2uF 10V, C326 2.2uF 10V, C351 2.2uF 10V

AT22 VDD_A53_7
AR25 VDD_A53_6
AR21 VDD_A53_5
AP24 VDD_A53_4
AN23 VDD_A53_3
AM26 VDD_A53_2
AM22 VDD_A53_1

VCC_CPU1: C290 100UF 10V, C295 100UF 10V, C294 100UF 10V, C324 2.2uF 10V, C341 2.2uF 10V, C347 2.2uF 10V, C339 2.2uF 10V, C353 2.2uF 10V

AT34 VDD_A72_12
AR33 VDD_A72_11
AR29 VDD_A72_10
AP32 VDD_A72_9
AP28 VDD_A72_8
AN35 VDD_A72_7
AN31 VDD_A72_6
AN27 VDD_A72_5
AM34 VDD_A72_4
AM30 VDD_A72_3
AL33 VDD_A72_2
AL29 VDD_A72_1

VCC_GPU0: C117 100UF 10V, C106 100UF 10V, C111 100UF 10V, C368 2.2uF 10V, C381 2.2uF 10V, C364 2.2uF 10V, C400 2.2uF 10V, C388 2.2uF 10V, C376 2.2uF 10V

Y22 VDD_GPU0_10
Y18 VDD_GPU0_9
W21 VDD_GPU0_8
V20 VDD_GPU0_7
AE19 VDD_GPU0_6
AD22 VDD_GPU0_5
AD18 VDD_GPU0_4
AC21 VDD_GPU0_3
AB20 VDD_GPU0_2
AA19 VDD_GPU0_1

VCC_GPU1: C464 100UF 10V, C466 100UF 10V, C442 100UF 10V, C394 2.2uF 10V, C377 2.2uF 10V, C360 2.2uF 10V, C386 2.2uF 10V, C375 2.2uF 10V, C366 2.2uF 10V

Y34 VDD_GPU1_10
W33 VDD_GPU1_9
V36 VDD_GPU1_8
U35 VDD_GPU1_7
AE35 VDD_GPU1_6
AD34 VDD_GPU1_5
AC33 VDD_GPU1_4
AB36 VDD_GPU1_3
AB32 VDD_GPU1_2
AA35 VDD_GPU1_1

VCC_MEMC: C434 100UF 10V, C427 100UF 10V, C438 100UF 10V, C385 2.2uF 10V, C357 2.2uF 10V, C363 2.2uF 10V, C392 2.2uF 10V, C361 2.2uF 10V, C358 2.2uF 10V

W37 VDD_MEMC_15
W17 VDD_MEMC_14
AK28 VDD_MEMC_13
AK24 VDD_MEMC_12
AJ27 VDD_MEMC_11
AJ23 VDD_MEMC_10
AH30 VDD_MEMC_9
AH26 VDD_MEMC_8
AH22 VDD_MEMC_7
AG37 VDD_MEMC_6
AG29 VDD_MEMC_5
AG25 VDD_MEMC_4
AG17 VDD_MEMC_3
AC37 VDD_MEMC_2
AC17 VDD_MEMC_1

VCC_MAIN: C278 100UF 10V, C273 100UF 10V, C349 2.2uF 10V, C380 2.2uF 10V, C369 2.2uF 10V, C383 2.2uF 10V, C338 2.2uF 10V, C396 2.2uF 10V, C367 2.2uF 10V, C390 2.2uF 10V, C403 2.2uF 10V, C328 2.2uF 10V, C325 2.2uF 10V, C554 2.2uF 10V, C555 2.2uF 10V

Y30 VDD_MAIN_48
Y26 VDD_MAIN_47
W29 VDD_MAIN_46
W25 VDD_MAIN_45
V32 VDD_MAIN_44
V24 VDD_MAIN_43
U23 VDD_MAIN_42
U19 VDD_MAIN_41
T34 VDD_MAIN_40
AU35 VDD_MAIN_39
AT30 VDD_MAIN_38
AT26 VDD_MAIN_37
AT18 VDD_MAIN_36
AR37 VDD_MAIN_35
AR17 VDD_MAIN_34
AP36 VDD_MAIN_33
AP20 VDD_MAIN_32
AN19 VDD_MAIN_31
AM18 VDD_MAIN_30
AL37 VDD_MAIN_29
AL25 VDD_MAIN_28
AL21 VDD_MAIN_27
AL17 VDD_MAIN_26
AK36 VDD_MAIN_25
AK32 VDD_MAIN_24
AJ31 VDD_MAIN_23
AJ19 VDD_MAIN_22
AH34 VDD_MAIN_21
AH18 VDD_MAIN_20
AG33 VDD_MAIN_19
AG21 VDD_MAIN_18
AF36 VDD_MAIN_17
AF32 VDD_MAIN_16
AF28 VDD_MAIN_15
AF24 VDD_MAIN_14
AF20 VDD_MAIN_13
AE31 VDD_MAIN_12
AE27 VDD_MAIN_11
AE23 VDD_MAIN_10
AD30 VDD_MAIN_9
AD26 VDD_MAIN_8
AC29 VDD_MAIN_7
AC25 VDD_MAIN_6
AB28 VDD_MAIN_5
AB24 VDD_MAIN_4
AA31 VDD_MAIN_3
AA27 VDD_MAIN_2
AA23 VDD_MAIN_1

VCC_MAIN: C16 22uF 16V, C321 2.2uF 10V, C316 2.2uF 10V, C317 2.2uF 10V, C315 2.2uF 10V, C320 2.2uF 10V

AV36 VDD_LVDS0_1P0
AW35 VDD_LVDS1_1P0
AV26 VDD_MIPI_CSI0_1P0
AW25 VDD_MIPI_CSI1_1P0
AU29 VDD_MIPI_DSI0_1P0
AV28 VDD_MIPI_DSI1_1P0
AW29 VDD_MIPI_DSI0_PLL_1P0
AW27 VDD_MIPI_DSI1_PLL_1P0

Processor does not support MLB.

VDD_MLB_1P8 may be tied to the power supply voltage shown or may be terminated, per the Hardware Developer's Guide power supplies of unused functions.

VDD_MLB_DIG_1P8_3P3 may be tied to the power supply voltage shown if other I/O functions are used, as determined by IOMUX selection. Alternately, terminate the MLB supply per the Hardware Developer's Guide power supplies of unused functions.

VDD_SCU_XTAL_1P8 (AU39): C323 0.22uF 10V — Tie this cap to GND. Place under IC

VDD_ANA1_1P8 (U25), VDD_ANA2_1P8 (AJ35), VDD_ANA3_1P8 (AK20), VDD_SCU_1P8_1 (AN39), VDD_SCU_1P8_2 (AP38), VDD_SCU_ANA_1P8 (AR39), VDD_CP_1P8 (AN37) — tie these 7 together to separate 1.8V supply: C346 2.2uF 10V, C343 2.2uF 10V, C345 2.2uF 10V, C350 2.2uF 10V, C309 2.2uF 6.3V, C302 2.2uF 6.3V

VCC_SCU_1V8: L17 600OHM; C300 2.2uF 6.3V; R237 2 OHM — Tie this R+C to VSS_SCU_XTAL.

VSS_SCU_XTAL

Charge-Pump → VDD_M1P8_CAP (AP42): VDD_M1P8_CAP; VCC_DDR0_PLL_1V8; VCC_DDR1_PLL_1V8; C333 2.2uF 6.3V

VDD_DDR_CH0_VDDA_PLL_1P8 (AE43)

VDD_DDR_CH1_VDDA_PLL_1P8 (AE11)

tie these 19 together to separate 1.8V supply: VREFH_ADC (AL11), VDD_ANA0_1P8_1 (U29), VDD_ANA0_1P8_2 (U31), VDD_ADC_1P8 (AL15), VDD_MIPI_CSI0_1P8 (AV24), VDD_MIPI_CSI1_1P8 (AU23), VDD_MIPI_DSI0_1P8 (AW31), VDD_MIPI_DSI1_1P8 (AV30), VDD_LVDS0_1P8 (AV34), VDD_LVDS1_1P8 (AW33), VDD_MLB_1P8 (T30), VDD_PCIE0_PLL_1P8 (N27), VDD_PCIE1_PLL_1P8 (M22), VDD_PCIE_SATA0_PLL_1P8 (N21), VDD_PCIE_IOB_1P8 (T26), VDD_PCIE_LDO_1P8 (U27), VDD_USB_HSIC0_1P8 (V28), VDD_HDMI_RX0_1P8 (AV18), VDD_HDMI_TX0_1P8 (AW17)

VCC_PCIE_1V8: C405 2.2uF 10V, C322 2.2uF 10V, C344 2.2uF 10V, C419 2.2uF 10V, C393 2.2uF 10V, C399 2.2uF 10V, C318 2.2uF 10V, C319 2.2uF 10V

See MLB note.

L20 120OHM; L21 120OHM; C424 100UF 10V; C425 100UF 10V; VCC_1V8

LDO → VDD_HDMI_TX0_LDO_1P0_CAP (AW15), VDD_HDMI_TX0_1P0 (AV16): VDD_HDMI_TX0_LDO_1P0_CAP; C307 2.2uF 10V; C306 2.2uF 6.3V

LDO → VDD_HDMI_RX0_LDO0_1P0_CAP (AU19): VDD_HDMI_RX0_LDO0_1P0_CAP; C312 2.2uF 10V; C308 2.2uF 6.3V

LDO → VDD_HDMI_RX0_LDO1_1P0_CAP (AU21): VDD_HDMI_RX0_LDO1_1P0_CAP; C313 2.2uF 10V; C310 2.2uF 6.3V

LDO → VDD_PCIE_LDO_1P0_CAP (N29), VDD_PCIE0_1P0 (M26), VDD_PCIE1_1P0 (N25), VDD_PCIE_SATA0_1P0 (M24): VDD_PCIE_LDO_1P0_CAP; C407 2.2uF 10V; C417 2.2uF 6.3V

LDO → VDD_USB_SS3_LDO_1P0_CAP (M30), VDD_USB_OTG1_1P0 (M32), VDD_USB_OTG2_1P0 (N31): VDD_USB_SS3_LDO_1P0_CAP; C414 2.2uF 10V; C408 2.2uF 10V; C411 2.2uF 6.3V

3.0V - 4.2V input → LDO → VDD_SNVS_LDO_1P8_CAP (AW39): VDD_SNVS_4P2 (AT38); VCC_SNVS; VCC_SNVS_LDO_1V8; C330 0.22uF 10V; C311 2.2uF 6.3V

VDD_USB_HSIC0_1P2 (V26): VCC_EXT_LDO_USB; C397 2.2uF 10V

VCC_DDR1_PLL_1V8: L19 120OHM; C371 2.2uF 10V; C384 2.2uF 6.3V

VCC_DDR0_PLL_1V8: L18 120OHM; C372 2.2uF 10V; C378 2.2uF 6.3V

tie these two to common digital 1.8V only: VDD_ADC_DIG_1P8 (AK16), VDD_MIPI_CSI_DIG_1P8 (AV22)

VCC_1V8: C354 2.2uF 10V, C314 2.2uF 10V, C331 2.2uF 10V

VDD_PCIE_DIG_1P8_3P3 (T22), VDD_EMMC0_1P8_3P3 (N35), VDD_LVDS_DIG_1P8_3P3 (AV32), VDD_MIPI_DSI_DIG_1P8_3P3 (AU27), VDD_QSPI0_1P8_3P3 (N19), VDD_QSPI1A_1P8_3P3 (M18), VDD_MLB_DIG_1P8_3P3 (M14): VCC_3V3

VCC_3V3: C410 1uF 10V, C327 1uF 10V

See MLB note.

VDD_M4_GPT_UART_1P8_3P3_1 (AL39), VDD_M4_GPT_UART_1P8_3P3_2 (AM38); VDD_SPI_SAI_1P8_3P3_1 (AM16), VDD_SPI_SAI_1P8_3P3_2 (AN15); VDD_SIM0_1P8_3P3 (AK42): VCC_1V8; VCC_LDO_SIM; C352 1uF 10V

for each block, choose appropriate voltage per application 1.8V or 3.3V

VDD_ESAI0_MCLK_1P8_3P3_1 (AP16), VDD_ESAI0_MCLK_1P8_3P3_2 (AR15); VDD_ESAI1_SPDIF_SPI_1P8_3P3 (AU15); VDD_FLEXCAN_1P8_3P3 (N15); VDD_USDHC_VSELECT_1P8_3P3 (T18): VCC_1V8; VCC_3V3; VCC_LDO_SD1; C337 2.2uF 10V; C416 1uF 10V

Sourced by CPU Card (bias only) when unused

Sourced by ENET Card when ENET daughter card plugged in BB Pwr net = VCC_BB_ENT1IO

VCC_3V3; VCC_1V8; VCC_BB_ENT1IO; U12 NX3L1G53GT; BB_ENET_DETECT_B 30; L8 120OHM; VCC_ENET1; C57 4.7uF 10V

0 = Y0 closed
1 = Y1 closed

VDD_USDHC1_1P8_3P3_1 (M36), VDD_USDHC1_1P8_3P3_2 (N37); VDD_USDHC2_1P8_3P3_1 (M38): VCC_LDO_SD2; VCC_ENET0_1V8; C413 1uF 10V

VDD_ENET0_1P8_3P3_1 (M40), VDD_ENET0_1P8_3P3_2 (N39): VCC_ENET0_1V8; C412 2.2uF 10V

1.8V, 2.5V or 3.3V for these two blocks (noted in ball name): VDD_ENET_MDIO_1P8_2P5_3P3 (N17), VDD_ENET1_1P8_2P5_3P3 (T38): VCC_3V3; VCC_ENET1; C402 1uF 10V

Sourced by PHY. Software must program PHY reg to output 1.8 V.

tie these two to common digital 3.3V only: VDD_HDMI_TX0_DIG_3P3 (AW21), VDD_USB_SS3_TC_3P3 (M16): VCC_3V3

VDD_HDMI_RX0_VH_RX_3P3 (AV20), VDD_USB_OTG1_3P3 (N33), VDD_USB_OTG2_3P3 (M34): L22 120OHM; VCC_3V3; C415 1uF 10V; C329 1uF 10V; C435 2.2uF 6.3V

tie these together share with VDD_MAIN supply filter as documented

tie to 3.3V filter as documented

ICAP Classification:	CP: ___ IUO: ___ PUBI: X_
Drawing Title:	i.MX 8QM CPU CARD
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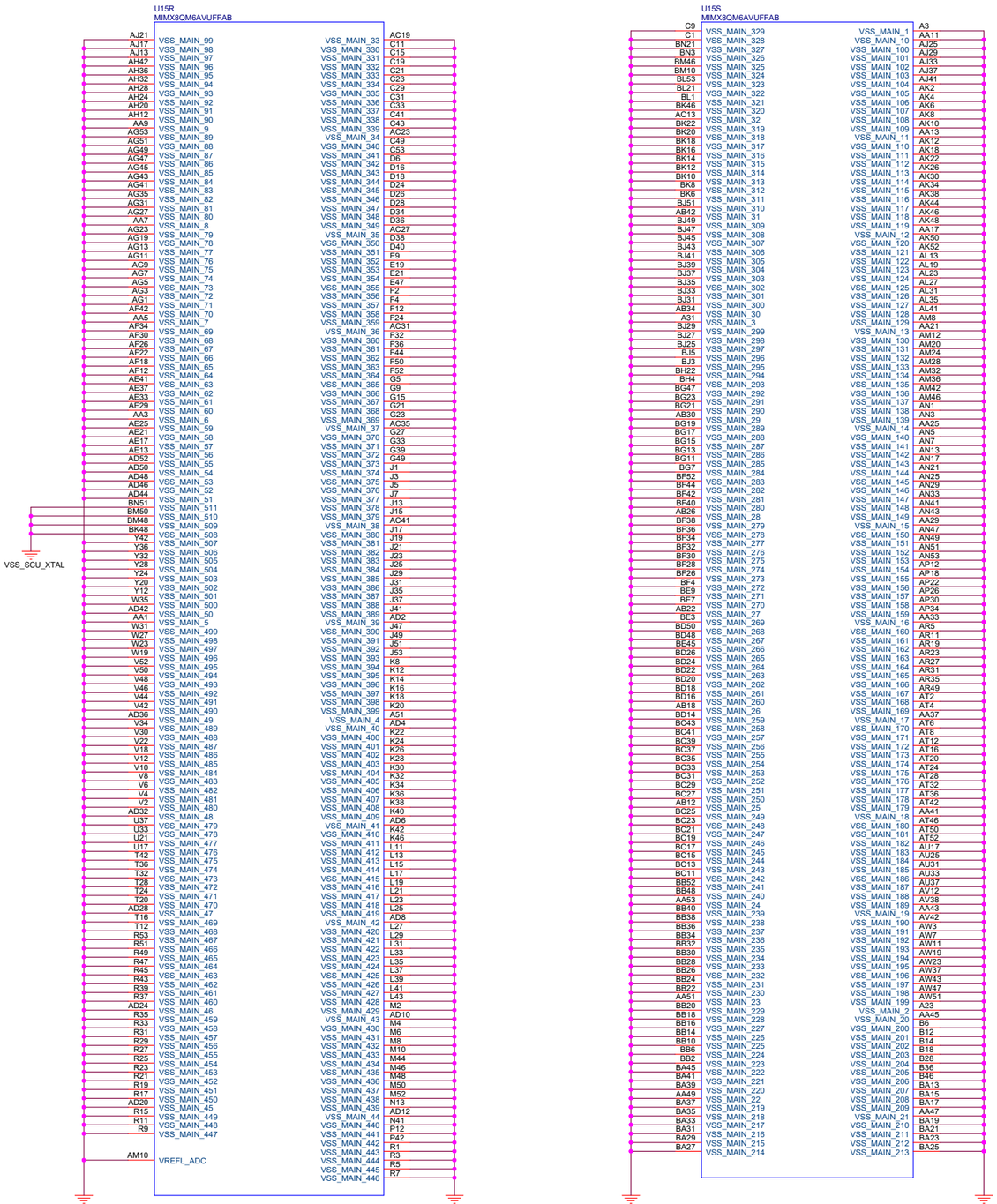
IMX8QM GND SECTIONS



ICAP Classification: CP: ___ IUO: ___ PUBI: X_

Drawing Title: **i.MX 8QM CPU CARD**

Page Title: **IMX8QM GND**

Size	Document Number	Rev
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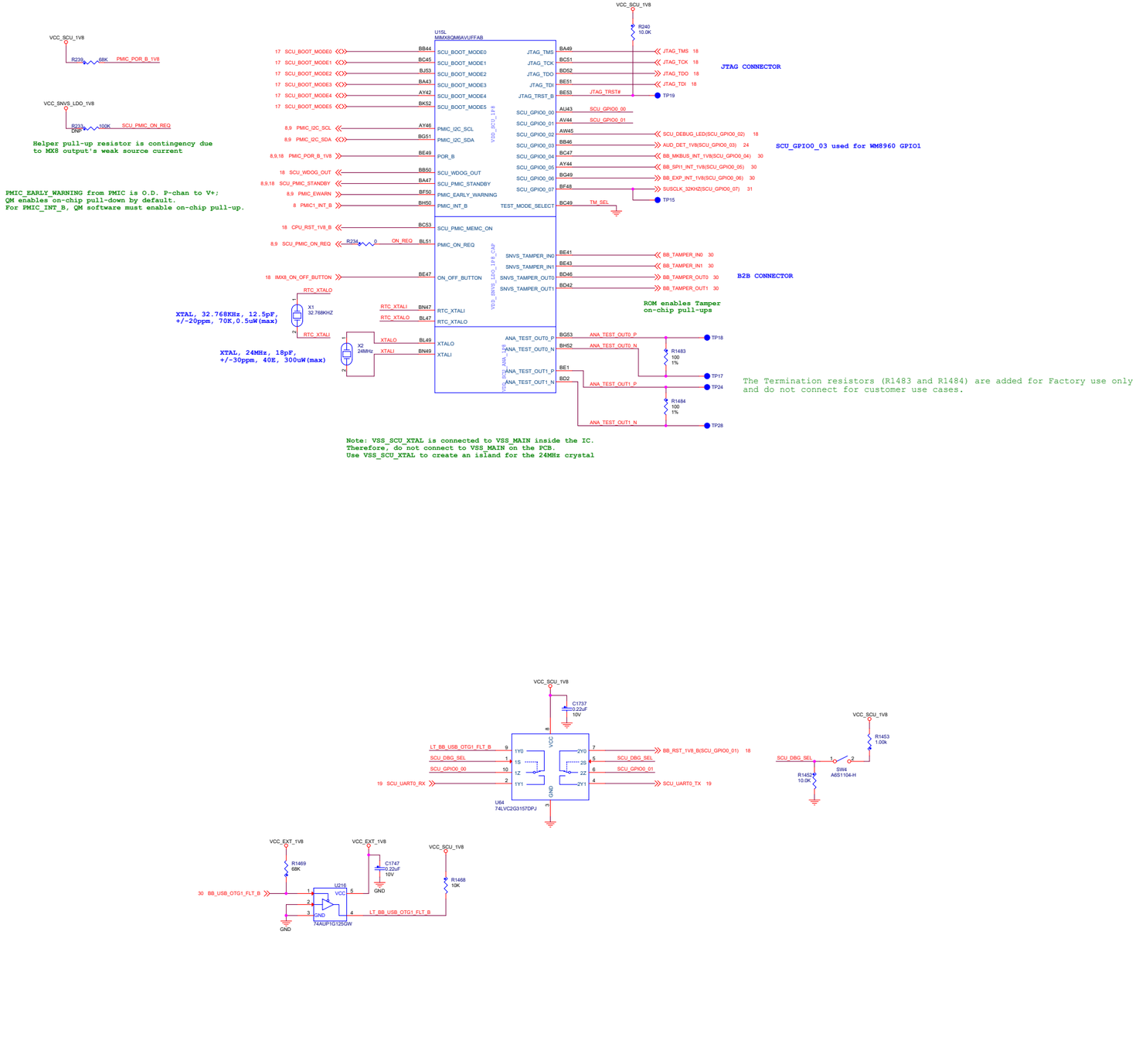
IMX8 SECTIONS_1



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Drawing Title:	i.MX 8QM CPU CARD
Page Title:	IMX8 SECTIONS 1
Size: A1	Document Number: SOURCE: SCH-29420, PDF: SPF-29420
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IMX8 SECTIONS_2

I/O VOLTAGE :3.3V

U15O
MIMX8QM6AVUFFAB

VDD_MLB_DIG_1P8_3P3

MLB_CLK	D2	BB_MLB_CLK 30
MLB_DATA	E3	BB_MLB_DATA 30
MLB_SIG	E1	BB_MLB_SIG 30
MLB_CLK_P	D32	BB_MLB_CLK_P 30
MLB_CLK_N	E33	BB_MLB_CLK_N 30
MLB_DATA_P	F34	BB_MLB_DATA_P 30
MLB_DATA_N	E35	BB_MLB_DATA_N 30
MLB_SIG_P	D30	BB_MLB_SIG_P 30
MLB_SIG_N	E31	BB_MLB_SIG_N 30

3-Wire Single-Ended MLB not supported by the processor.
Other functions are supported as determined by IOMUX selection.
If unused, adopters must follow the Hardware Developer's
Guide Unused input/output terminations section.

MLB(B2B CONNECTOR)

6-Wire Differential MLB not supported by the processor.
Adopters must follow the Hardware Developer's Guide
Unused input/output terminations section.

I/O VOLTAGE :1.8V

U15P
MIMX8QM6AVUFFAB

1.8V only

ADC_IN0	AP10	BB_GPIO_1V8(ADC_IN0) 30
ADC_IN1	AN11	BB_SPI3_INT_1V8(ADC_IN1) 30
ADC_IN2	AP8	WIFI_WAKE_B(ADC_IN2) 25
ADC_IN3	AR9	BB_SPI1_CLK(ADC_IN3) 30
ADC_IN4	AN9	BB_SPI1_SDO(ADC_IN4) 30
ADC_IN5	AR7	BB_SPI1_SDI(ADC_IN5) 30
ADC_IN6	AL9	BB_SPI1_CS0(ADC_IN6) 30
ADC_IN7	AP6	BB_SPI1_CS1(ADC_IN7) 30

ENET CARD SPI(IN BB)

U15N
MIMX8QM6AVUFFAB

VDD_SIM0_1P8_3P3

SIM0_CLK	AL45	BB_SIM_CLK 30
SIM0_IO	AN45	BB_SIM_IO 30
SIM0_RST	AP48	BB_SIM_RST 30
SIM0_POWER_EN	AT48	BB_SIM_POWER_EN 30
SIM0_PD	AL43	BB_SIM_PD 30
SIM0_GPIO0_00	AP46	BB_SIM_INT_B 30

SIM(B2B CONNECTOR)

I/O VOLTAGE :3.3V

U15T
MIMX8QM6AVUFFAB

VDD_FLEXCAN_1P8_3P3

FLEXCAN0_TX	H6	BB_CAN0_TX 30
FLEXCAN0_RX	C5	BB_CAN0_RX 30
FLEXCAN1_TX	G7	BB_CAN1_TX 30
FLEXCAN1_RX	E5	BB_CAN1_RX 30
FLEXCAN2_TX	E7	BB_CAN2_TX 30
FLEXCAN2_RX	C3	BB_CAN2_RX 30

CAN 0,1,2(B2B CONNECTOR)

NXP is aware that the UART net names are inaccurate. There is no plan
to change the net names.

Adopters please note:
UART3 net name on contact AR47/AU53 should be UART4.
UART4 net name on contact AP44/AU47 should be UART3.
2-Wire AUDIN function not available on Base Board.

I/O VOLTAGE :1.8V

U15U
MIMX8QM6AVUFFAB

VDD_M4_GPT_UART_1P8_3P3

M40_GPIO0_00	AR47	BB_ARD_MIK_UART3_RX 30
M40_GPIO0_01	AU53	BB_ARD_MIK_UART3_TX 30
M40_I2C0_SCL	AM44	FTDI_M40_UART0_RX 19
M40_I2C0_SDA	AU51	FTDI_M40_UART0_TX 19
M41_GPIO0_00	AP44	BB_UART4_RX_AUDIN 30
M41_GPIO0_01	AU47	BB_UART4_TX_AUDIN 30
M41_I2C0_SCL	AR45	BB_M41_I2C0_1V8_SCL 30
M41_I2C0_SDA	AU49	BB_M41_I2C0_1V8_SDA 30
GPT0_CLK	AY52	I2C1_1V8_SCL 24,25
GPT0_CAPTURE	AV52	I2C1_1V8_SDA 24,25
GPT0_COMPARE	AW53	ENET0_INT_B 23
GPT1_CLK	BA53	BB_IOEXP_CAN_INT_B(GPT1_CLK) 30
GPT1_CAPTURE	AY50	BB_IOEXP_INT_B(GPT1_CAPTURE) 30
GPT1_COMPARE	BA51	BB_AUD_PWR_PWM(GPT1_COMPARE) 30
UART0_TX	AV48	FTDI_UART0_TX 19
UART0_RX	AV50	FTDI_UART0_RX 19
UART0_RTS_B	AU45	BB_UART2_RX 30
UART0_CTS_B	AW49	BB_UART2_TX 30
UART1_TX	AY48	BT_UART1_TX 25
UART1_RX	AT44	BT_UART1_RX 25
UART1_RTS_B	AR43	BT_UART1_RTS 25
UART1_CTS_B	AV46	BT_UART1_CTS 25

ARDUINO & MIKROBUS(IN BB)

FTDI DEBUG

VCC_1V8
BB_M41_I2C0_1V8_SCL R380 4.7K
BB_M41_I2C0_1V8_SDA R379 4.7K

AUDIO CONNECTOR,(IN BB)
I2C ALSO USED FOR CAN GPIO EXPANDER (IN BB)

M.2,WM8960

VCC_1V8
I2C1_1V8_SCL R60 4.7K
I2C1_1V8_SDA R62 4.7K

Three interrupts are connected to
M4_GPT1 configured as LSIO GPIO.
These are pulled to 1.8 V on Sheet 30 to avoid false
triggering when the Base Board is not installed.
The Base Board has voltage translation as needed.

CAN signals ERR, WAKE, and INT are combined together on
the Base Board to provide the CAN_INT_B signal.

FTDI DEBUG

DBG CONNECTOR(IN BB)

M.2 CONNECTOR

M.2 CONNECTOR

ICAP Classification: CP: ___ IUO: ___ PUBI: X

Drawing Title: **i.MX 8QM CPU CARD**

Page Title: **IMX8 SECTIONS 2**

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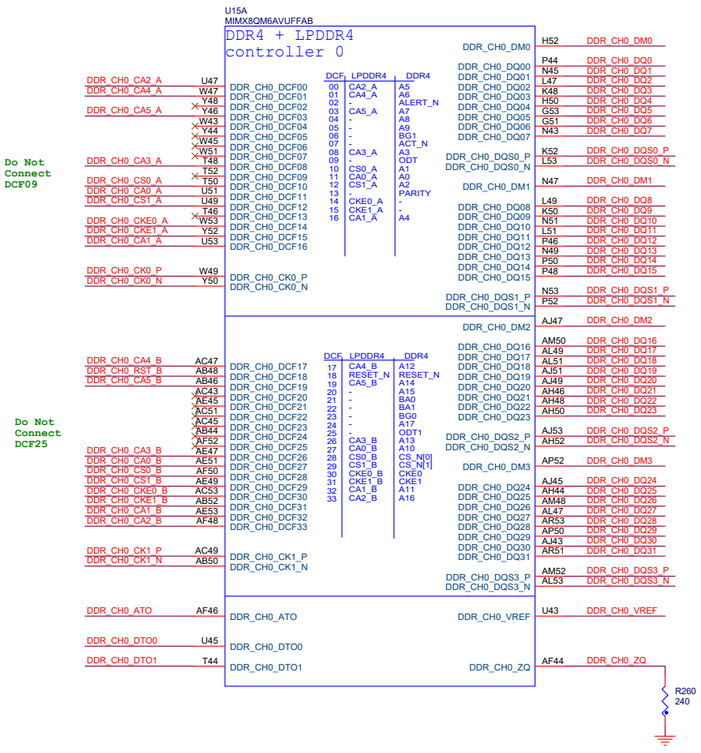
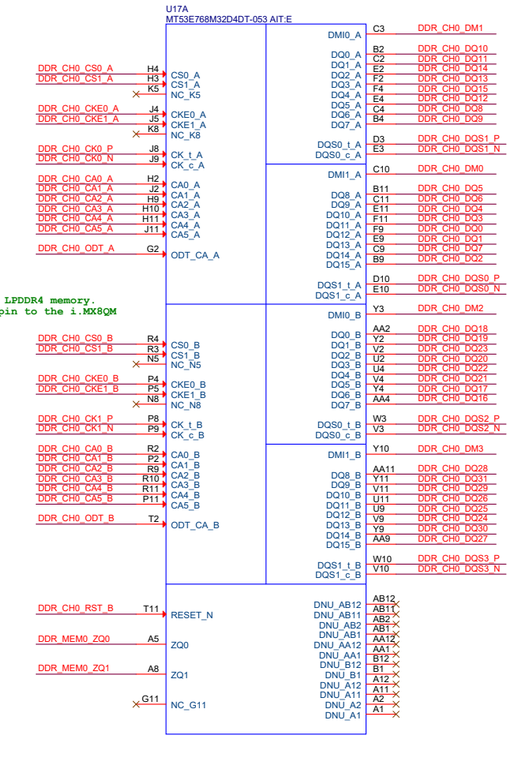
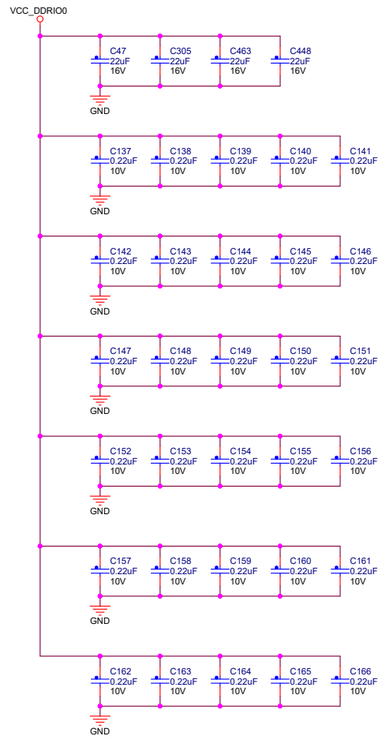
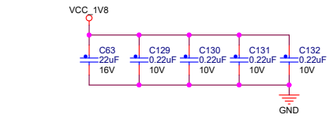
LPDDR4 DRAM 1 OF 2

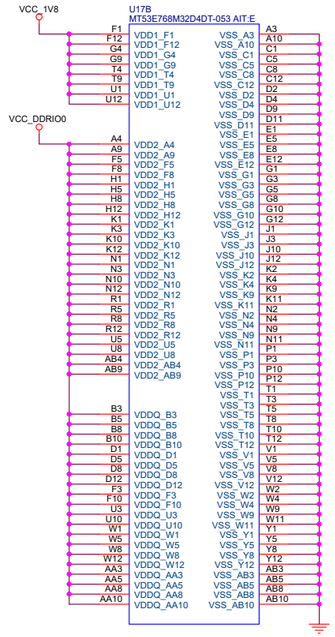
Total System DRAM = 6 Gbyte



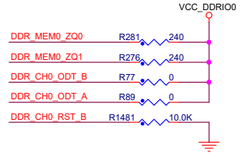








The processor requires x16 for each chip inside the DRAM package.
The x8 configuration is not compatible.



ICAP Classification:	CP: ___	IUO: ___	PUBI: X
Drawing Title:	i.MX 8QM CPU CARD		
Page Title:	LPDDR4 DRAM 1 OF 2		
Size A2	Document Number: SOURCE: SCH-29420, PDF: SPF-29420		Rev C7
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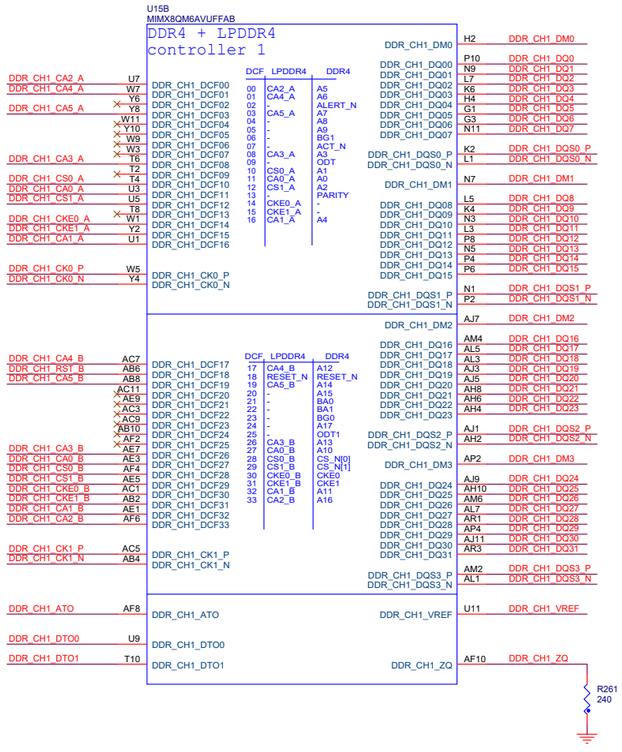
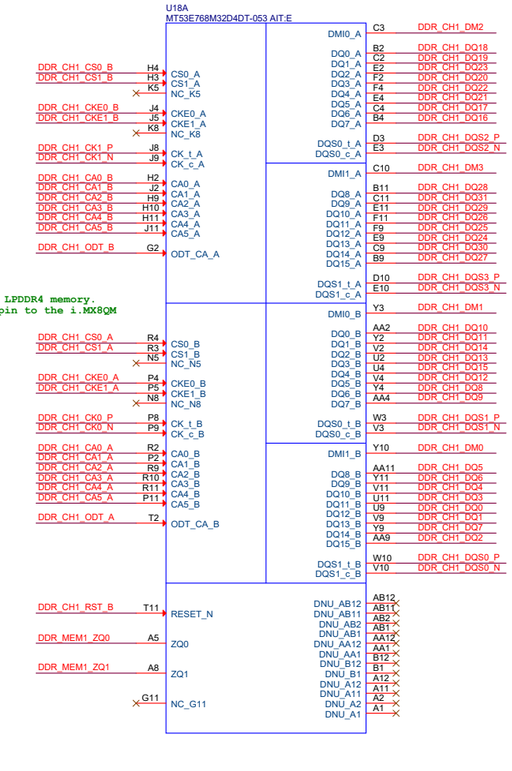
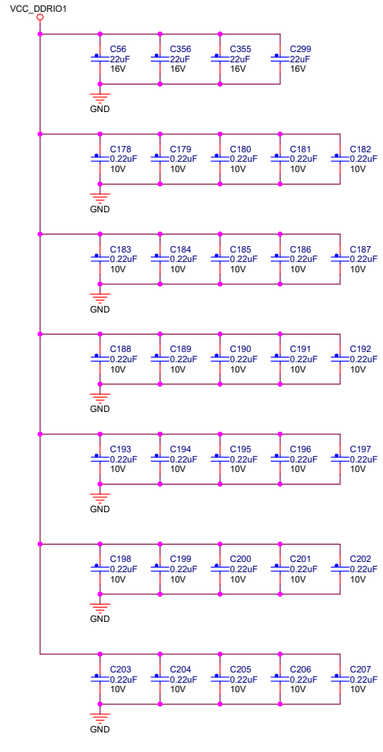
LPDDR4 DRAM 2 OF 2

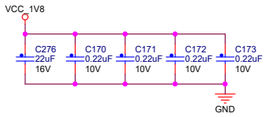
Total System DRAM = 6 Gbyte

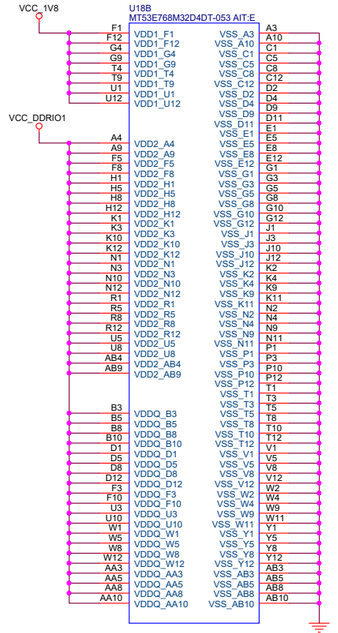




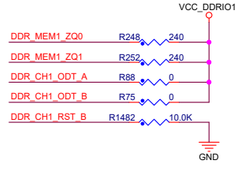
Pullup ODT_CA_A/B on LPDDR4 memory.
Do not connect this pin to the i.MX8QM







The processor requires x16 for each chip inside the DRAM package.
The x8 configuration is not compatible.



ICAP Classification:	CP: ___	IUO: ___	PUBI: X
Drawing Title:	i.MX 8QM CPU CARD		
Page Title:	LPDDR4 DRAM 2 OF 2		
Size A2	Document Number: SOURCE: SCH-29420, PDF: SPF-29420		Rev C7
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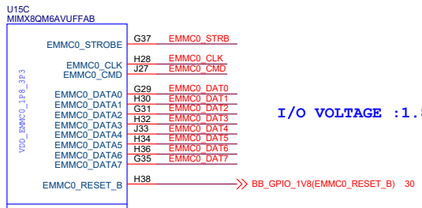
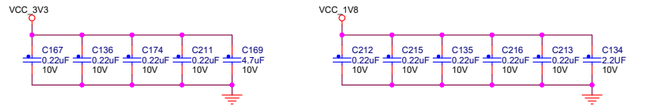
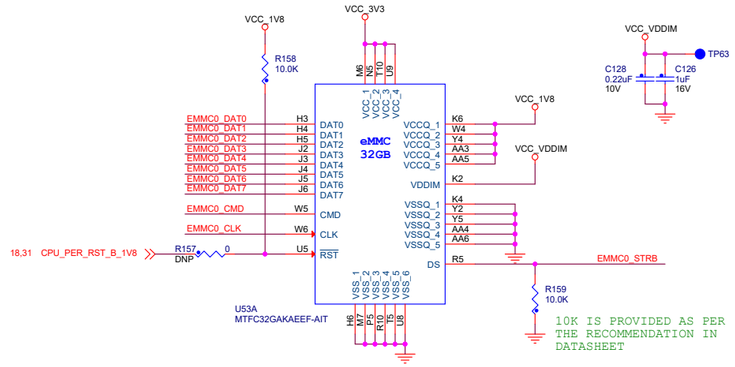
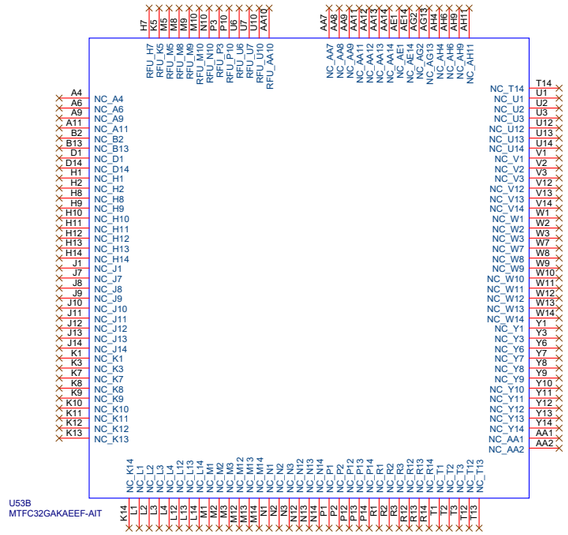
eMMC

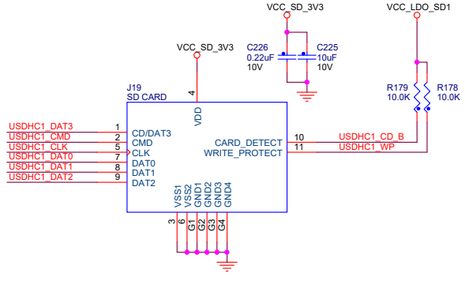


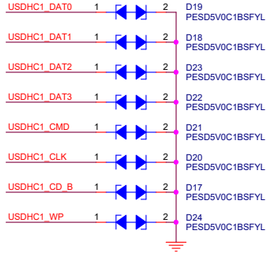




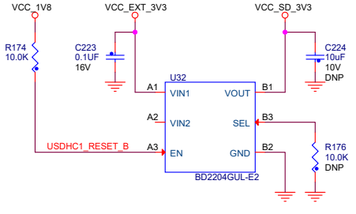


SD CARD INTERFACE





SDXC Power Control



Bulk capacitance already present in this rail (C225)

SEL Input has Internal Pulldown(700k)

ICAP Classification: CP: ___ IUO: ___ PUBI: X_			
Drawing Title: i.MX 8QM CPU CARD			
Page Title: eMMC & SD CARD			
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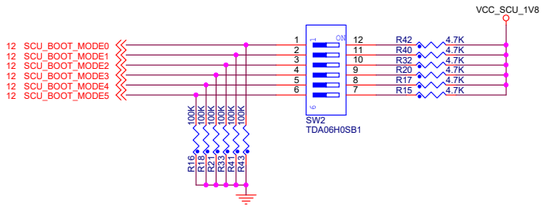
BOOT CONFIGURATIONS

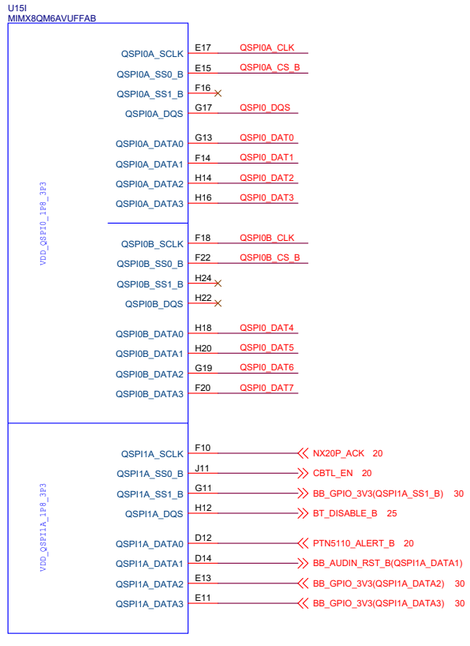


BOOT MODE

MODE	5	4	3	2	1	0
FUSE	0	0	0	0	0	0
SERIAL BOOT	0	0	0	1	0	0
eMMC0	0	0	1	0	0	0
SD1	0	0	1	1	0	0
Octal SPI	0	1	1	0	0	0

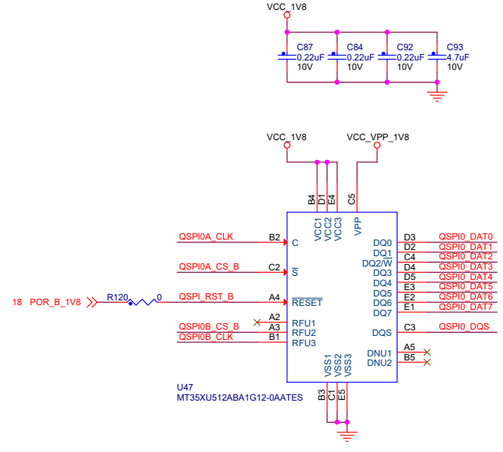
OCTAL/XSPI/QSPI FLASH

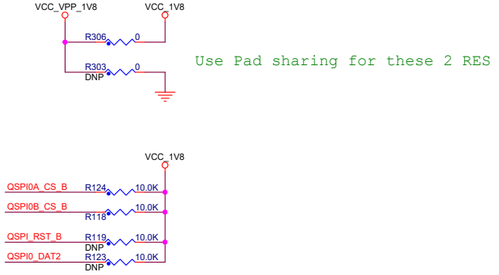
I/O VOLTAGE :1.8V



I/O VOLTAGE :3.3V

B2B CONNECTOR





ICAP Classification: CP: ___ IUO: ___ PUBI: X_

Drawing Title: **i.MX 8QM CPU CARD**

Page Title: **BOOT CONFIGURATION & SPI FLASH**

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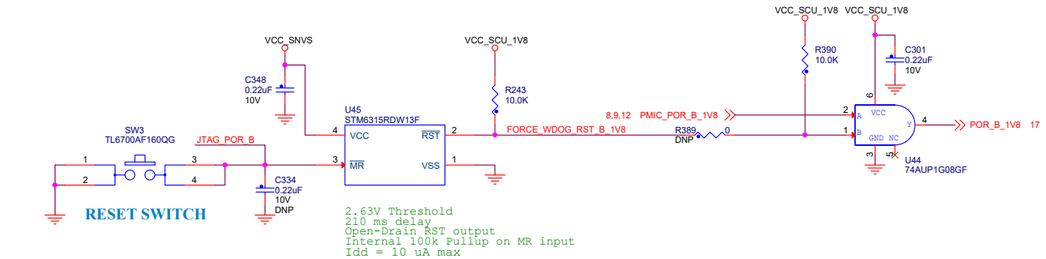
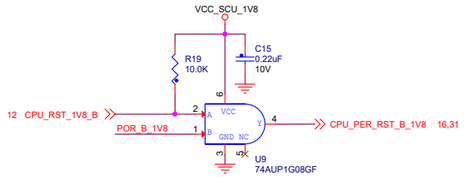
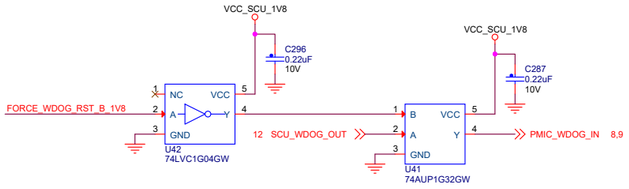
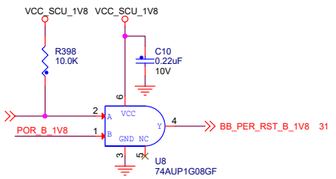
RESET GENERATION

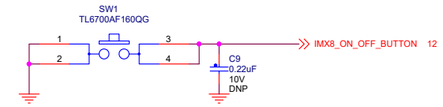








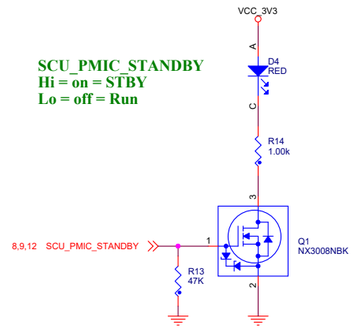
SYSTEM ON/OFF



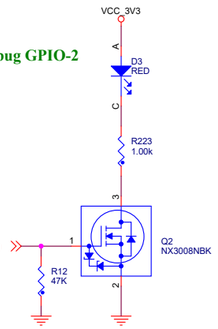
* Hold SW1 for 5 sec for force OFF
* Hold SW1 for 0.5 sec to turn ON

LED INDICATIONS

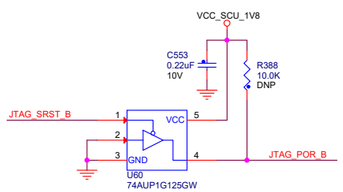
SCU_PMIC_STANDBY
Hi = on = STBY
Lo = off = Run

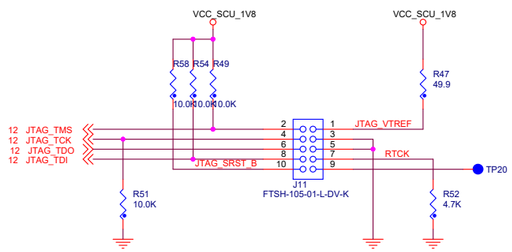


SCU Debug GPIO-2
Hi = on
Lo = off



JTAG





MX8QM On-Chip 50 kohm Pulls

JTAG_TMS = PU
JTAG_TCK = PD
JTAG_TDI = PU
JTAG_TRST_B = PU
TEST_MODE_SELECT = PD

ICAP Classification: CP: ___ IUO: ___ PUBI: X_

Drawing Title: **i.MX 8QM CPU CARD**

Page Title: **RESET LOGIC & JTAG**

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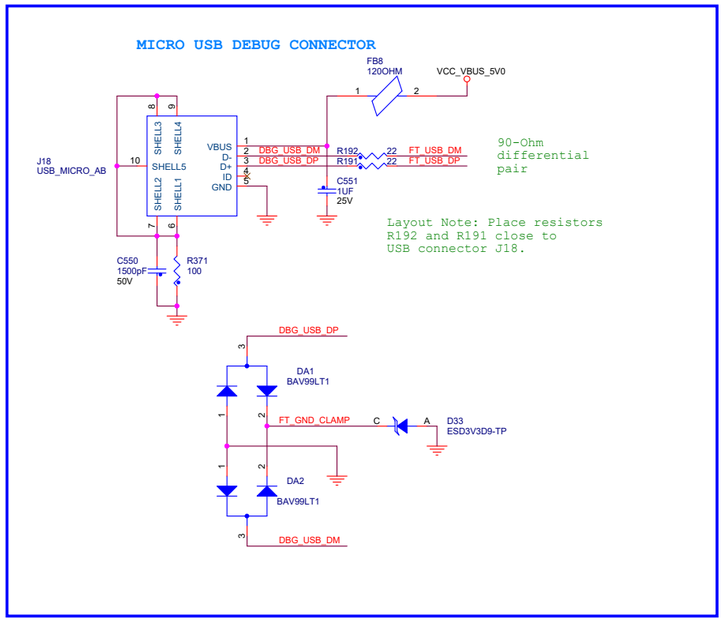
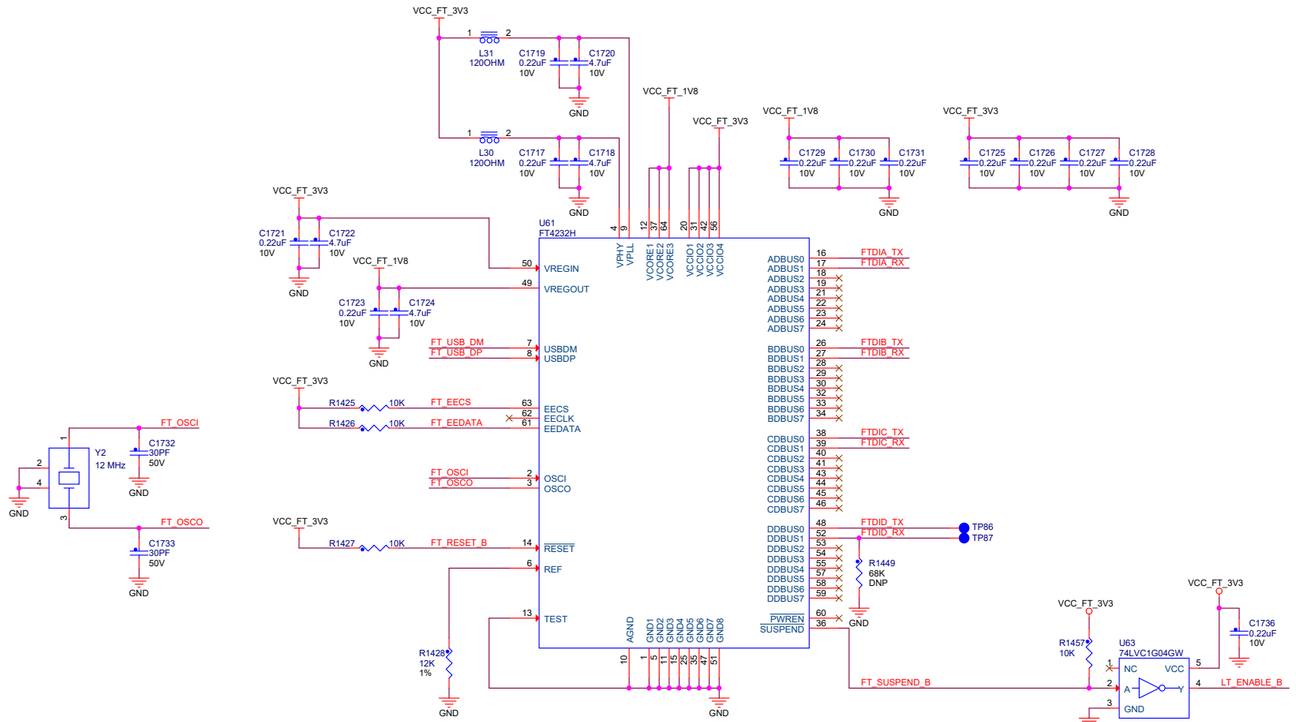
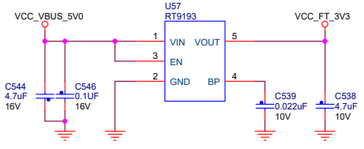
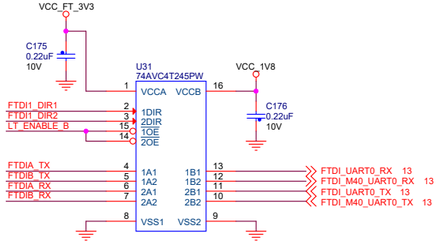
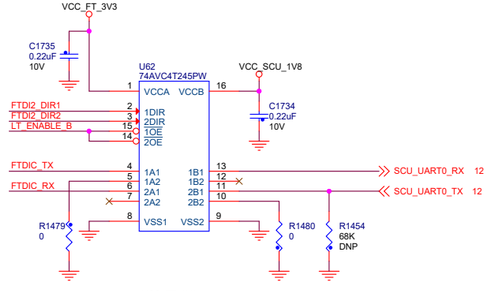
DEBUG UART-USB

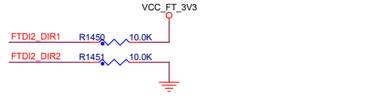












ICAP Classification:	CP: ___ IUO: ___ PUBI: _X_	
Drawing Title:	i.MX 8QM CPU CARD	
Page Title:	DEBUG UART_USB	
Size A2	Document Number SOURCE: SCH-29420, PDF: SPF-29420	Rev C7
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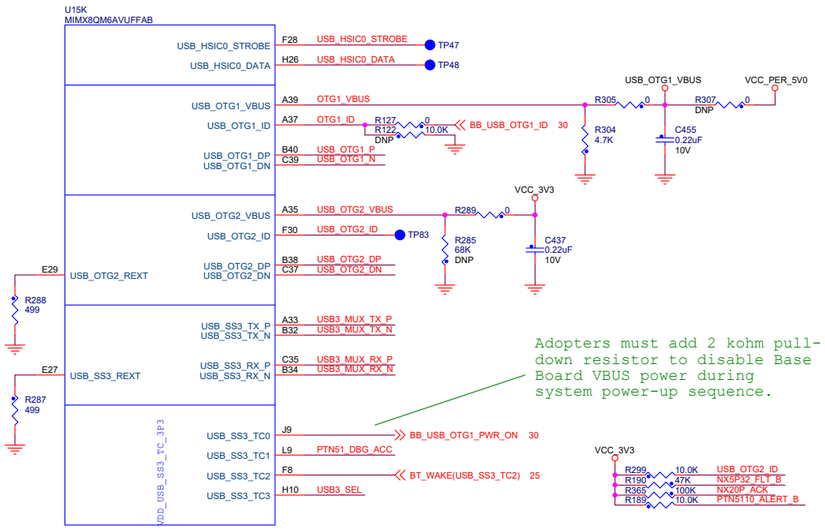
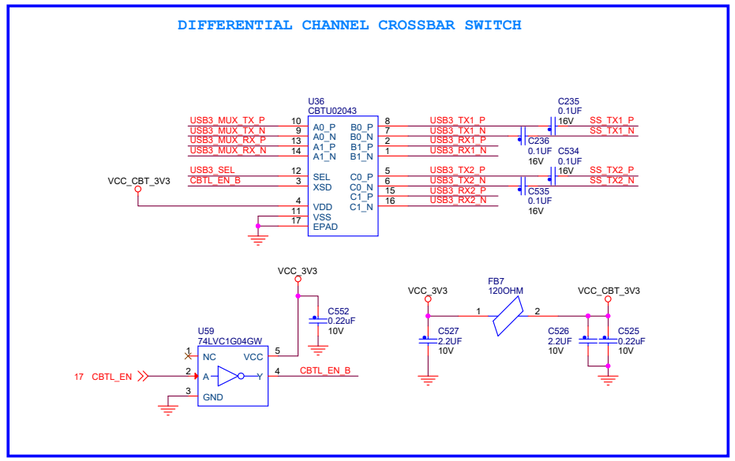
USB 3.x Type C

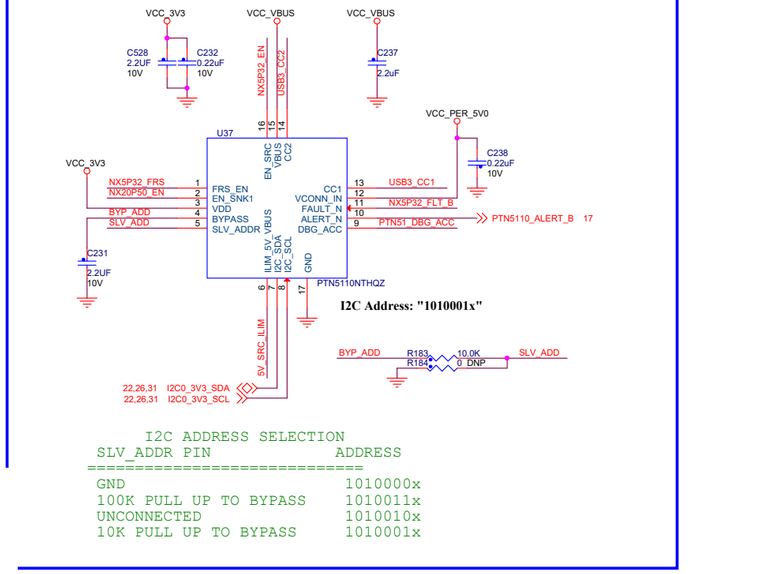
I/O VOLTAGE :3.3V



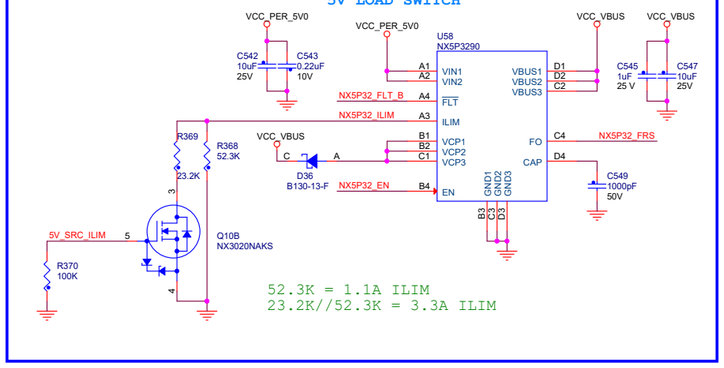
DIFFERENTIAL CHANNEL CROSSBAR SWITCH



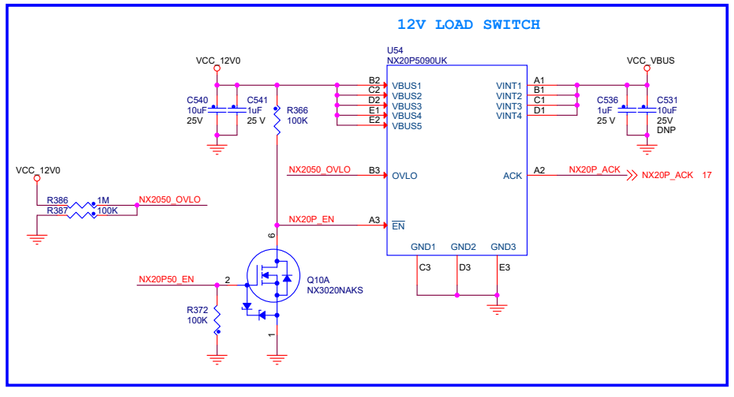
CC LOGIC DETECTION



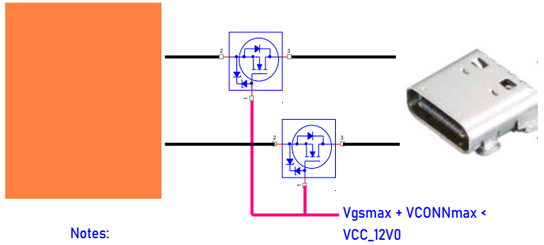
5V LOAD SWITCH



12V LOAD SWITCH



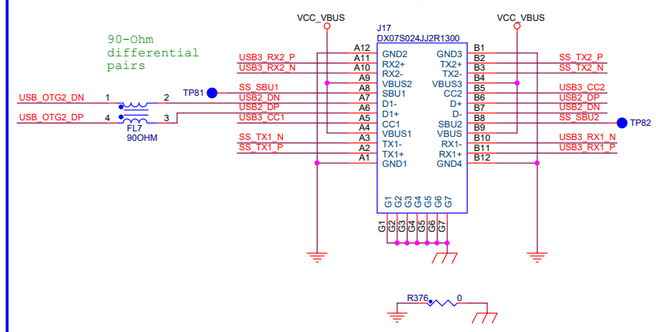
Isolation Circuit Required to Pass CC Unpowered Voltage Test



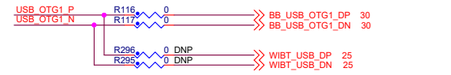
Notes:

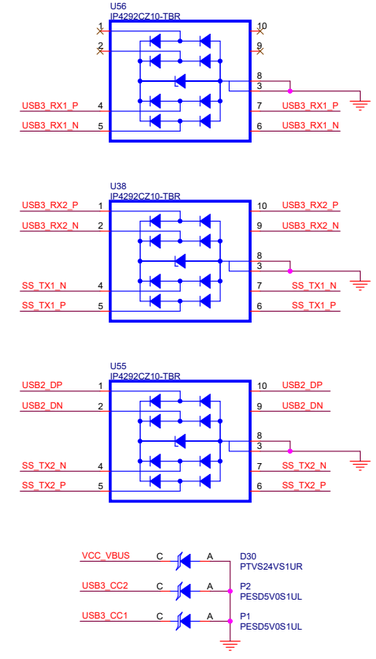
1. NMOS FETs should be *off* when the board is not powered and switch to *on* when the board is powered.
2. Refer to PTN5110 errata ES_PTN5110NTHQ.

USB3.0 TYPE C CONNECTOR



OTG1 Can be connected to M.2 Connector or Baseboard USB2.0 port using these resistor options.





ICAP Classification:	CP: ___ IUO: ___ PUBI: _X_
Drawing Title:	i.MX 8QM CPU CARD
Page Title:	USB 3.x Type C
Size A2	Document Number SOURCE: SCH-29420, PDF: SPF-29420 Rev C7
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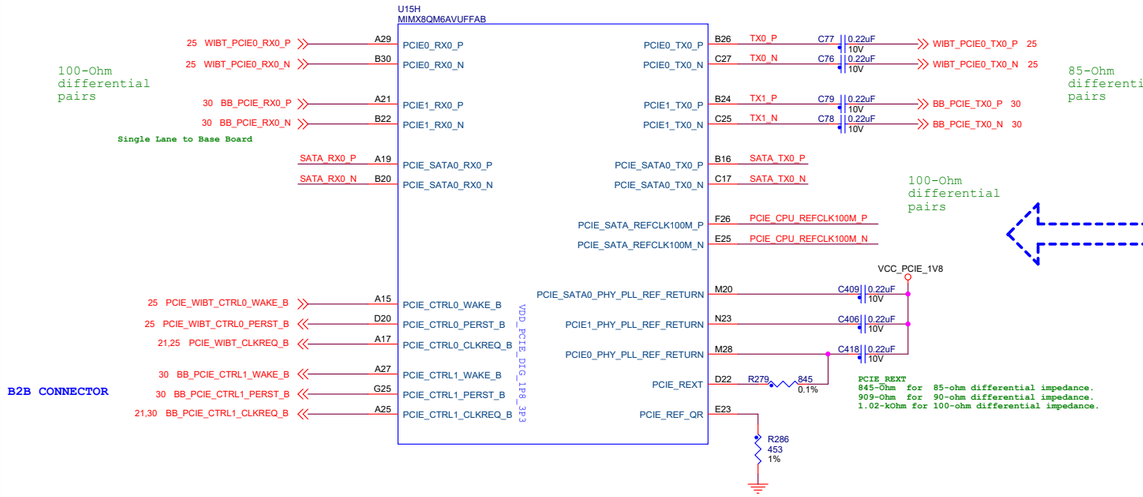
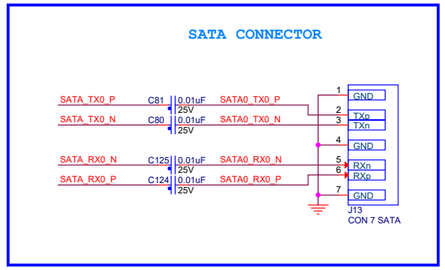
PCIe & SATA

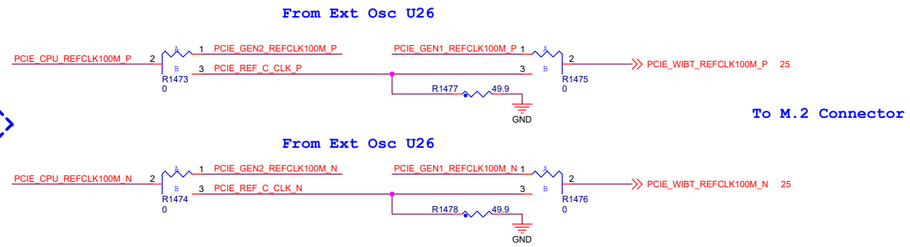
I/O VOLTAGE :3.3V



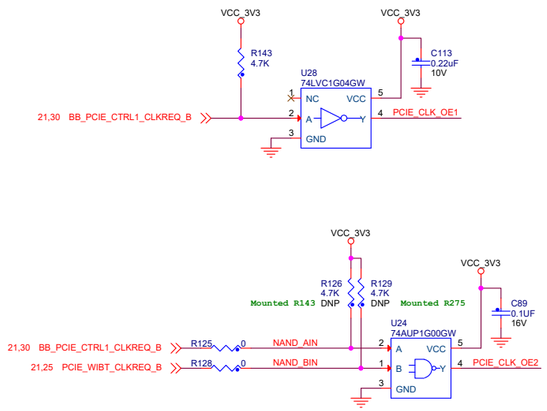


M.2 Connector on CPU Card has two PCIe Clock options:
(Set resistor strapping as per table)
1. Processor (NXP experimental use only; not recommended for customer use)
2. External Clock generator (By default)

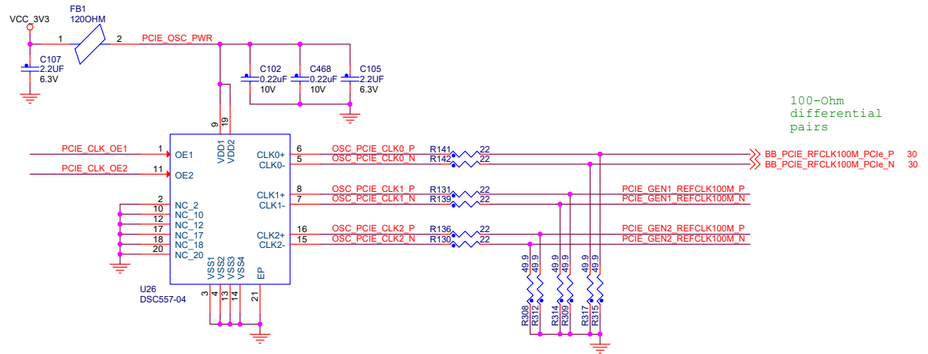
M.2 Connector on Base Card has PCIe Clock
Option only from External clock generator.
(Set resistor strapping as per table)



PCIe CLOCK ENABLE LOGIC



PCIe 100MHz OSCILLATOR



DSC557 has internal 40kOhm pullup on OE1 and OE2.
Default always ON for DSC557 Osc.

CLOCK CONFIG

OE1	OE2	CLK0	CLK1	CLK2
0	0	Hi-Z	Hi-Z	Hi-Z
0	1	Hi-Z	EN	EN
1	0	EN	Hi-Z	Hi-Z
1	1	EN	EN	EN

	Option Resistors	Clock Source	
		Processor	Clock Generator
M.2 Connector on CPU Card	R1473	POS B	POS A
	R1474	POS B	POS A
	R1475	POS B	POS A
	R1476	POS B	POS A
	R128	DNP	MOUNT
	R129	MOUNT	DNP
	R130	DNP	MOUNT
	R131	DNP	MOUNT
	R136	DNP	MOUNT
	R139	DNP	MOUNT
M.2 Connector on Base Card	R1473	NA	POS A
	R1474	NA	POS A
	R1475	NA	POS A
	R1476	NA	POS A
	R128	NA	MOUNT
	R129	NA	DNP
	R130	NA	MOUNT
	R131	NA	MOUNT
	R136	NA	MOUNT
	R139	NA	MOUNT

ICAP Classification: CP: ___ IUO: ___ PUBI: X_
Drawing Title: i.MX 8QM CPU CARD
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Size A2 | Document Number SOURCE: SCH-29420, PDF: SPF-29420 | Rev C7
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HDMI TX & RX

U15D
MIMX8QM6AVUFFAB

HDMI - RX

HDMI_RX0_DATA2_P / HDMI_RX0_DATA2_N — BM20 HDMI_RX0_DAT2_P, BL19 HDMI_RX0_DAT2_N
HDMI_RX0_DATA1_P / HDMI_RX0_DATA1_N — BM18 HDMI_RX0_DAT1_P, BL17 HDMI_RX0_DAT1_N
HDMI_RX0_DATA0_P / HDMI_RX0_DATA0_N — BM16 HDMI_RX0_DAT0_P, BL15 HDMI_RX0_DAT0_N
HDMI_RX0_CLK_P / HDMI_RX0_CLK_N — BM12 HDMI_RX0_CLK_P, BL11 HDMI_RX0_CLK_N
HDMI_RX0_ARC_P / HDMI_RX0_ARC_N — BM14 HDMI_RX0_ARC_P, C556 1uF 16V, HDMI_RX0_ARC_P_CON; BL13 (X)
HDMI_RX0_CEC — BJ9 HDMI_RX0_CEC
HDMI_RX0_DDC_SCL — BH10 HDMI_DDC_SCL
HDMI_RX0_DDC_SDA — BE13 HDMI_DDC_SDA
HDMI_RX0_MON_5V — BN11
HDMI_RX0_HPD — BF14 HDMI_RX0_HPD, R241 1M DNP
HDMI_RX0_REXT — BJ11, R235 499

ARC_N not used on i.MX8QM

HDMI_TX0_DAT2_EDP0_P — C28 0.1UF 16V — HDMI_TX_DAT2_P
HDMI_TX0_DAT2_EDP0_N — C29 0.1UF 16V — HDMI_TX_DAT2_N
HDMI_TX0_DAT1_EDP1_P — C26 0.1UF 16V — HDMI_TX_DAT1_P
HDMI_TX0_DAT1_EDP1_N — C27 0.1UF 16V — HDMI_TX_DAT1_N
HDMI_TX0_DAT0_EDP2_P — C24 0.1UF 16V — HDMI_TX_DAT0_P
HDMI_TX0_DAT0_EDP2_N — C25 0.1UF 16V — HDMI_TX_DAT0_N
HDMI_TX0_CLK_EDP3_P — C33 0.1UF 16V — HDMI_TX_CLK_P
HDMI_TX0_CLK_EDP3_N — C35 0.1UF 16V — HDMI_TX_CLK_N
HDMI_TX0_AUX_ARC_P — C37 1uF 16V — HDMI_TX0_ARC_P

DP & HDMI - TX

HDMI_TX0_DATA2_EDP0_P / HDMI_TX0_DATA2_EDP0_N — BL9 HDMI_TX0_DAT2_EDP0_P, BM8 HDMI_TX0_DAT2_EDP0_N
HDMI_TX0_DATA1_EDP1_P / HDMI_TX0_DATA1_EDP1_N — BL7 HDMI_TX0_DAT1_EDP1_P, BM6 HDMI_TX0_DAT1_EDP1_N
HDMI_TX0_DATA0_EDP2_P / HDMI_TX0_DATA0_EDP2_N — BL5 HDMI_TX0_DAT0_EDP2_P, BM4 HDMI_TX0_DAT0_EDP2_N
HDMI_TX0_CLK_EDP3_P / HDMI_TX0_CLK_EDP3_N — BL3 HDMI_TX0_CLK_EDP3_P, BK2 HDMI_TX0_CLK_EDP3_N
HDMI_TX0_AUX_P / HDMI_TX0_AUX_N — BH2 HDMI_TX0_AUX_ARC_P, BG3 (X)
HDMI_TX0_CEC — BJ1 HDMI_TX0_CEC
HDMI_TX0_DDC_SCL — BG1 HDMI_TX0_DDC_SCL
HDMI_TX0_DDC_SDA — BN5 HDMI_TX0_DDC_SDA
HDMI_TX0_HPD — BH8 HDMI_TX0_HPD
HDMI_TX0_TS_SCL — BN9
HDMI_TX0_TS_SDA — BN7
HDMI_TX0_REXT — BJ7, R236 499

20,26,31 I2C0_3V3_SCL — R232 4.7K — VCC_3V3
20,26,31 I2C0_3V3_SDA — R231 4.7K — VCC_3V3
VCC_3V3 — R233 4.7K — HDMI_TX0_TS_SCL / HDMI_TX0_TS_SDA

VCC_3V3 — R50 27K — D2 BAT54-E3-08 — HDMI_TX0_CEC

DP: Pulldown unused DDC and CEC pins
HDMI: DDC requires 2K pullup to 5V
HDMI: CEC requires 27K pullup to 3V3 with blocking diode

AUX_N not used on i.MX8QM

HPD Pulldown:
DP 100K
HDMI 1M

I/O VOLTAGE :3.3V

R45 604 HDMI_TX_CLK_P
R48 604 HDMI_TX_CLK_N
R36 604 HDMI_TX_DAT1_P
R37 604 HDMI_TX_DAT1_N
R34 604 HDMI_TX_DAT0_P
R35 604 HDMI_TX_DAT0_N
R38 604 HDMI_TX_DAT2_P
R39 604 HDMI_TX_DAT2_N

VCC_PCIE_1V8 — Q4 NX3008NBK

U1 IP4292CZ10-TBR
HDMI_RX0_DAT2_P 1 — 10 HDMI_RX0_DAT2_P
HDMI_RX0_DAT2_N 2 — 9 HDMI_RX0_DAT2_N
8, 3
HDMI_RX0_DAT1_P 4 — 7 HDMI_RX0_DAT1_P
HDMI_RX0_DAT1_N 5 — 6 HDMI_RX0_DAT1_N

U2 IP4292CZ10-TBR
HDMI_RX0_DAT0_P 1 — 10 HDMI_RX0_DAT0_P
HDMI_RX0_DAT0_N 2 — 9 HDMI_RX0_DAT0_N
8, 3
HDMI_RX0_CLK_P 4 — 7 HDMI_RX0_CLK_P
HDMI_RX0_CLK_N 5 — 6 HDMI_RX0_CLK_N

U3 IP4292CZ10-TBR
HDMI_RX0_CEC 1 — 10 HDMI_RX0_CEC
HDMI_RX0_ARC_P_CON 2 — 9 HDMI_RX0_ARC_P_CON
8, 3
HDMI_TX0_HPD 4 — 7 HDMI_TX0_HPD
HDMI_RX0_HPD 5 — 6 HDMI_RX0_HPD

R196 27K — 3 — 1 — VCC_3V3
NC — 2 — D1 BAT54-E3-08

U4 IP4292CZ10-TBR
HDMI_TX0_DAT2_P 1 — 10 HDMI_TX0_DAT2_P
HDMI_TX0_DAT2_N 2 — 9 HDMI_TX0_DAT2_N
8, 3
HDMI_TX0_DAT1_P 4 — 7 HDMI_TX0_DAT1_P
HDMI_TX0_DAT1_N 5 — 6 HDMI_TX0_DAT1_N

U5 IP4292CZ10-TBR
HDMI_TX0_DAT0_P 1 — 10 HDMI_TX0_DAT0_P
HDMI_TX0_DAT0_N 2 — 9 HDMI_TX0_DAT0_N
8, 3
HDMI_TX0_CLK_P 4 — 7 HDMI_TX0_CLK_P
HDMI_TX0_CLK_N 5 — 6 HDMI_TX0_CLK_N

U6 IP4292CZ10-TBR
HDMI_TX0_CEC 1 — 10 HDMI_TX0_CEC
HDMI_TX0_ARC_P 2 — 9 HDMI_TX0_ARC_P
8, 3
HDMI_TX0_DDC_SCL 4 — 7 HDMI_TX0_DDC_SCL
HDMI_TX0_DDC_SDA 5 — 6 HDMI_TX0_DDC_SDA

J1
HDMI_RX0_DAT2_P 1
HDMI_RX0_DAT2_N 3
HDMI_RX0_DAT1_P 4
HDMI_RX0_DAT1_N 6
HDMI_RX0_DAT0_P 7
HDMI_RX0_DAT0_N 9
HDMI_RX0_CLK_P 10
HDMI_RX0_CLK_N 12
HDMI_RX0_CEC 13
HDMI_RX0_ARC_P_CON 14
HDMI_DDC_SCL 15
HDMI_DDC_SDA 16
HDMI_RX0_HPD 19
11, 17, 18, 20, 21, 22
HDMI TYPE A 19

VCC_HDMI_5V0 — R199 0 — HDMI_RX0_HPD
VCC_HDMI_5V0 — C4 0.22uF 10V
R8 0 — C5 1000pf 2KV

VCC_HDMI_5V0
HDMI_DDC_SCL — R210 47K
HDMI_RX0_HPD — R229 1.00k
HDMI_DDC_SDA — R220 2.00k DNP

VCC_PER_5V0 — C2 0.22uF 10V
U7 AP2331SA-7 (3 IN, GND 1, OUT 2)
VCC_TX_5V0 — C3 0.22uF 10V

HDMI_TX_DAT2_N 1 — 2 HDMI_TX0_DAT2_N
HDMI_TX_DAT2_P 4 — 3 HDMI_TX0_DAT2_P — FL1 120 Ohm
HDMI_TX_DAT1_N 1 — 2 HDMI_TX0_DAT1_N
HDMI_TX_DAT1_P 4 — 3 HDMI_TX0_DAT1_P — FL2 120 Ohm
HDMI_TX_DAT0_N 1 — 2 HDMI_TX0_DAT0_N
HDMI_TX_DAT0_P 4 — 3 HDMI_TX0_DAT0_P — FL3 120 Ohm
HDMI_TX_CLK_N 1 — 2 HDMI_TX0_CLK_N
HDMI_TX_CLK_P 4 — 3 HDMI_TX0_CLK_P — FL4 120 Ohm

100-Ohm differential pairs

J6
HDMI_TX0_DAT2_P 1
HDMI_TX0_DAT2_N 3
HDMI_TX0_DAT1_P 4
HDMI_TX0_DAT1_N 6
HDMI_TX0_DAT0_P 7
HDMI_TX0_DAT0_N 9
HDMI_TX0_CLK_P 10
HDMI_TX0_CLK_N 12
HDMI_TX0_CEC 13
HDMI_TX0_ARC_P 14
HDMI_TX0_DDC_SCL 15
HDMI_TX0_DDC_SDA 16
HDMI_TX0_HPD 19
2, 5, 8, 11, 17, 18, 20, 21, 22
HDMI TYPE A 19

VCC_TX_5V0 — R217 0 — HDMI_TX0_HPD
VCC_TX_5V0 — C6 0.22uF 10V
R9 0 — C7 1000pf

VCC_TX_5V0
HDMI_TX0_DDC_SCL — R10 2.00k
HDMI_TX0_DDC_SDA — R11 2.00k

ICAP Classification:	CP: ___ IUO: ___ PUBI: X_
Drawing Title:	i.MX 8QM CPU CARD
Page Title:	HDMI TX & RX
Size: A2	Document Number: SOURCE: SCH-29420, PDF: SPF-29420 — Rev: C7
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1 Gbps ETHERNET PHY

U15M
MIMX8QM6AVUFFAB

VDD_ENET_MDIO_1P8_2P5_3P3

ENET0_MDC	A9	ENET0_MDC
ENET0_MDIO	D10	ENET0_MDIO
ENET0_REFCLK_125M_25M	B10	BB_ARD_MIK_RST_B 30
ENET1_MDC	A13	I2C4_3V3_SCL 31
ENET1_MDIO	C13	I2C4_3V3_SDA 31
ENET1_REFCLK_125M_25M	A11	ENET1_REFCLK 30

VDD_ENET0_1P8_3P3

ENET0_RGMII_TXC	A41	ETH0_RGMII_TXC
ENET0_RGMII_TX_CTL	E41	ETH0_RGMII_TX_CTL
ENET0_RGMII_TXD0	A43	ETH0_RGMII_TXD0
ENET0_RGMII_TXD1	B42	ETH0_RGMII_TXD1
ENET0_RGMII_TXD2	A45	ETH0_RGMII_TXD2
ENET0_RGMII_TXD3	D42	ETH0_RGMII_TXD3
ENET0_RGMII_RXC	B44	ETH0_RGMII_RXC
ENET0_RGMII_RX_CTL	E43	ETH0_RGMII_RX_CTL
ENET0_RGMII_RXD0	A47	ETH0_RGMII_RXD0
ENET0_RGMII_RXD1	D44	ETH0_RGMII_RXD1
ENET0_RGMII_RXD2	C45	ETH0_RGMII_RXD2
ENET0_RGMII_RXD3	E45	ETH0_RGMII_RXD3

VDD_ENET1_1P8_2P5_3P3

ENET1_RGMII_TXC	D46	ENET1_RGMII_TXC 31
ENET1_RGMII_TX_CTL	B48	ENET1_RGMII_TX_CTL 31
ENET1_RGMII_TXD0	A49	ENET1_RGMII_TXD0 31
ENET1_RGMII_TXD1	C47	ENET1_RGMII_TXD1 31
ENET1_RGMII_TXD2	G47	ENET1_RGMII_TXD2 31
ENET1_RGMII_TXD3	D48	ENET1_RGMII_TXD3 31
ENET1_RGMII_RXC	B50	BB_ENET1_RGMII_RXC 30
ENET1_RGMII_RX_CTL	E49	BB_ENET1_RGMII_RX_CTL 30
ENET1_RGMII_RXD0	E51	BB_ENET1_RGMII_RXD0 30
ENET1_RGMII_RXD1	C51	BB_ENET1_RGMII_RXD1 30
ENET1_RGMII_RXD2	D52	BB_ENET1_RGMII_RXD2 30
ENET1_RGMII_RXD3	E53	BB_ENET1_RGMII_RXD3 30

VCC_3V3
R290 4.7K
R297 4.7K

NOTE:
Pull up resistor required to support open drain PHY MDIO pin, when PHY is outputting data. Pull up not required on MDC since line is only driven by i.MX8QM.

VCC_3V3 — FB6 120OHM — ATH_AVDD33
C517 1uF 10V
C516 0.22uF 10V
ATH_VDD33
C518 10uF 25V
C509 0.22uF 10V

VCC_ENET0_1V8
ATH_VDDIO_REG
C512 0.22uF 10V
C510 1uF 16V

VDDH_ETH_2V5
ATH_VDDH_REG
C513 1uF 16V

ATH_LX — L16 4.7uH — VCC_ETH_1V1
C119 10uF 25V
C114 0.22uF 10V

U30
AR8031

VDD33	4	
AVDD33	16	
VDDIO_REG	29	
VDDH_REG	10	
LX	3	
DVDDL	47	ATH_DVDDL
AVDDL1	8	ATH_AVDDL
AVDDL2	44	
AVDDL3	13	
AVDDL4	19	

VCC_ETH_1V1
C133 0.22uF 10V
FB2 120OHM — VCC_ETH_1V1
C503 0.22uF 10V
C514 0.22uF 10V
C511 0.22uF 10V
C515 0.22uF 10V

ETH0_RGMII_TXC	35	GTX_CLK
ETH0_RGMII_TXD0	36	TXD0
ETH0_RGMII_TXD1	37	TXD1
ETH0_RGMII_TXD2	38	TXD2
ETH0_RGMII_TXD3	39	TXD3
ETH0_RGMII_TX_CTL	34	TX_EN
ETH0_RGMII_RXC	33	RX_CLK
ETH0_RGMII_RXD0	31	RXD0
ETH0_RGMII_RXD1	30	RXD1
ETH0_RGMII_RXD2	28	RXD2
ETH0_RGMII_RXD3	27	RXD3
ETH0_RGMII_RX_CTL	32	RX_DV
	46	SIP
	45	SIN
	43	SOP
	42	SON
	41	SD
ENET_PHY_RST_B	2	RST
ETH_WOL	40	WOL_INT
ETH_INT	5	INT
ETH_PPS	22	PPS
ETH_CLKOUT	25	CLK_25M
ENET0_MDC	1	MDC
ENET0_MDIO	48	MDIO
XTLO	6	XTLO
XTLI	7	XTLI
RBIAS	9	RBIAS

TRXP0	11	ETH_TRX0_P
TRXN0	12	ETH_TRX0_N
TRXP1	14	ETH_TRX1_P
TRXN1	15	ETH_TRX1_N
TRXP2	17	ETH_TRX2_P
TRXN2	18	ETH_TRX2_N
TRXP3	20	ETH_TRX3_P
TRXN3	21	ETH_TRX3_N

100-Ohm differential pairs

LED_LINK10_100	26	ETH_LED_10/100_B
LED_LINK1000	24	ETH_LED_1G_B
LED_ACT	23	ETH_LED_ACT_B

R173 1.00k — D16 RED — 1 Gbps

C218 470pF DNP
C217 470pF DNP
C219 470pF DNP

EMI Filter Reserved
470pF for LED

VCC_ETH_1V1
R147 2.37K
R145 10.0K DNP

B2B CONNECTOR

X3 25MHz
C210 22pF 50V
C177 22pF 50V

R168 2.37K

VCC_1V8
ETH_WOL R144 10.0K
ETH_INT R359 10.0K

VCC_3V3
R148 68K
D12 MBR140SFT
ENET_PHY_RST_B
D11 MBR140SFT
CPU_PER_RST_3V3 26,31
C504 1uF 16V

ETH_CT
J14 RJ-45

CT	1	ETH_CT
TRD1+	2	ETH_TRX0_P
TRD1-	3	ETH_TRX0_N
TRD2+	4	ETH_TRX1_P
TRD2-	5	ETH_TRX1_N
TRD3+	6	ETH_TRX2_P
TRD3-	7	ETH_TRX2_N
TRD4+	8	ETH_TRX3_P
TRD4-	9	ETH_TRX3_N
GND	10	
SH1	11	R374 270 ETH_LED_ACT_B
SH2	12	
	13	
	14	R373 270 ETH_LED_10/100_B

ETH_CT
C522 0.22uF 10V
C520 0.22uF 10V
R367 0
C537 1000pf 2KV

VCC_ENET0_1V8 / VDDH_ETH_2V5

R152 10.0K DNP		ETH_LED_ACT_B
R149 10.0K DNP	R175 10.0K	ETH0_RGMII_RXD0
R169 10.0K DNP	R156 10.0K	ETH0_RGMII_RXD1
R163 10.0K DNP	R161 10.0K	ETH0_RGMII_RXD2
R160 10.0K DNP	R164 10.0K	ETH0_RGMII_RXD3
R156 10.0K DNP	R170 10.0K	ETH0_RGMII_RXC
R177 10.0K DNP	R150 10.0K	ETH0_RGMII_RX_CTL
	R153 10.0K	ETH_LED_1G_B
	R172 10.0K	

ANA_MOD
Select the core voltage level:
0:1.1V, 1:1.2V

PHYADDRESS2
PHYADDRESS0
PHYADDRESS1
MODE[3]
MODE[2]
MODE[1]
MODE[0]
SEL_GPIO_INT
Pin 5 mode:
0: INT ; 1:GPIO

MODE[3:0]
(Default assemble: 0000)

0000 1000 BaseT, RGMII;
0001 1000 BaseT, SGMII;
0010 1000X, RGMII, 500HMS;
0011 1000X, RGMII, 750HMS;
0100 1000X, TRANS, 500HMS;
0101 1000X, TRANS, 750HMS;
0110 100X, RGMII, 500HMS;
0111 100X, TRANS, 500HMS;
1100 BaseT, RMII1;
1101 BaseT, RMII2;
1110 100X, RGMII, 750HMS;
1111 100X, TRANS, 750HMS;
Others Reserved

B2B CONNECTOR

VCC_3V3 — R319 1.5K — C489 0.22uF 10V
VCC_3V3 — C488 0.22uF 10V — R318 1.5K

30 BB_ENET1_MDC	2	A1	B1 13 ENET0_MDC
30 BB_ENET1_MDIO	3	A2	B2 12 ENET0_MDIO
		A3	B3 11
		A4	B4 10
	8	OE	NC1 9
			NC2 6
		VCCA 14	VCCB 1
		GND 7	

U48 NTS0104PW

Isolation required due to MDIO interaction between certain PHYs & Switches per prior system bring-up. Users should evaluate their systems & eliminate if possible.

U34 IP4292CZ10-TBR

ETH_TRX0_P	1	10	ETH_TRX0_P
ETH_TRX0_N	2	9	ETH_TRX0_N
		8	
		3	
ETH_TRX1_P	4	7	ETH_TRX1_P
ETH_TRX1_N	5	6	ETH_TRX1_N

U33 IP4292CZ10-TBR

ETH_TRX2_P	1	10	ETH_TRX2_P
ETH_TRX2_N	2	9	ETH_TRX2_N
		8	
		3	
ETH_TRX3_P	4	7	ETH_TRX3_P
ETH_TRX3_N	5	6	ETH_TRX3_N

ICAP Classification: CP: ___ IUO: ___ PUBI: _X_

Drawing Title: **i.MX 8QM CPU CARD**

Page Title: **ETHERNET PHY**

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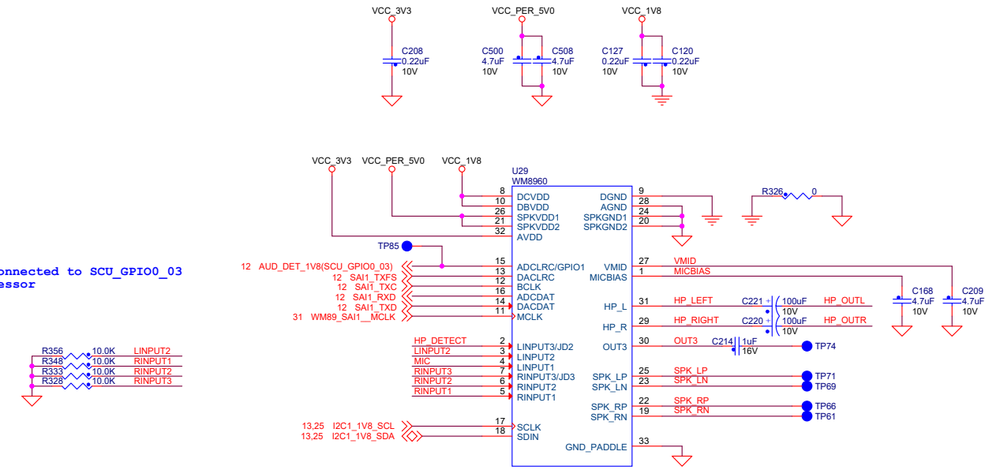
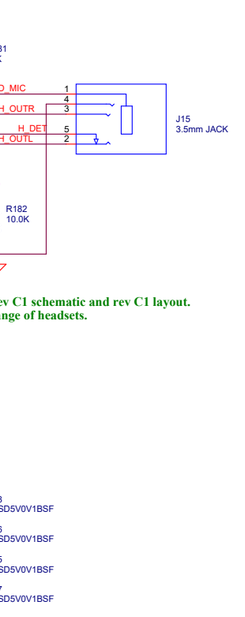
AUDIO CODEC WM8960

GPIO1 connected to SCU_GPIO0_03 of processor

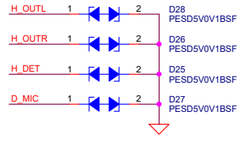


7-bit I2C Address: "0011010"

AHJ 'AV' Connector Interface	
PIN	**Description**
1	Microphone
4	Ground
3	Right Side Earpiece
2	Left Side Earpiece



Headphone Jack pinout changed from OMTP to AHJ on rev C1 schematic and rev C1 layout.
GND and MIC changed locations to accomodate a wider range of headsets.



ICAP Classification: CP: ___ IUO: ___ PUBI: X_

Drawing Title: **i.MX 8QM CPU CARD**

Page Title: **AUDIO CODEC WM8960**

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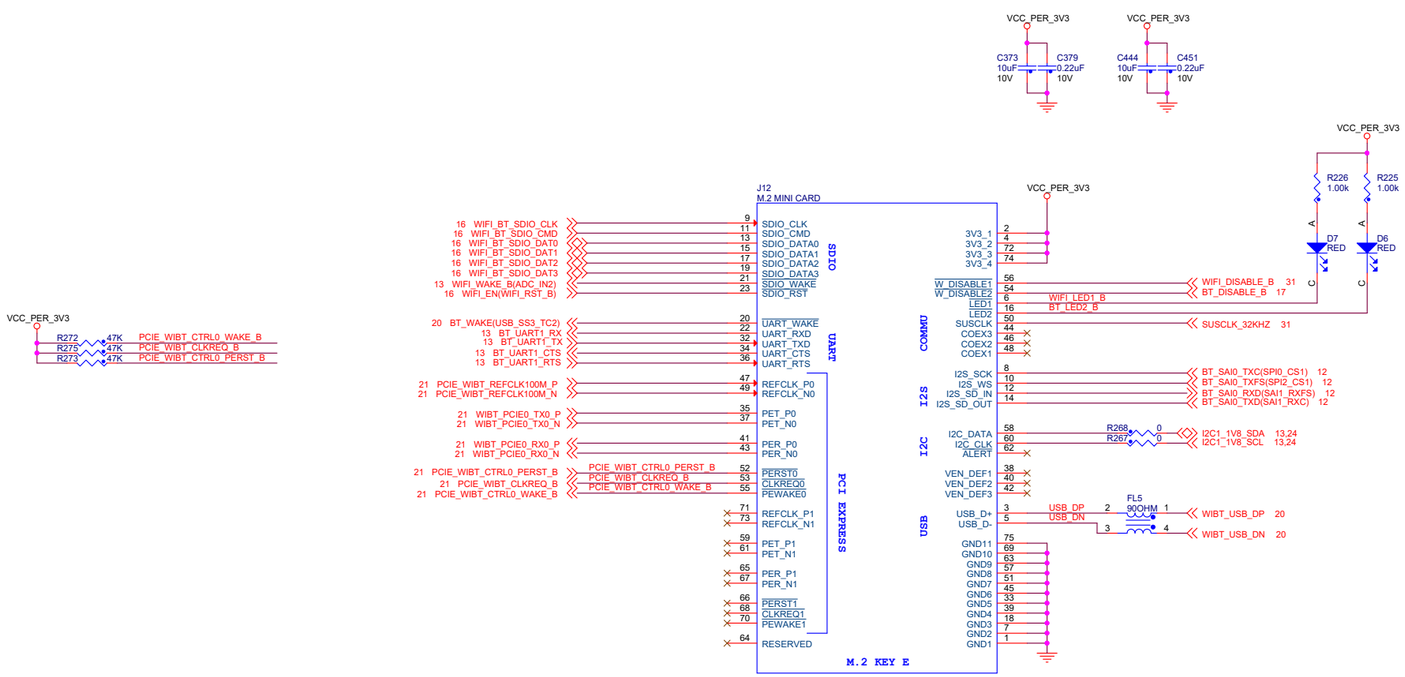
WIFI_BLUETOOTH -M.2 CONNECTOR E-KEY



Add On Card used will be M.2 with E-Key Type 30x30 Dimension.

Information on compatible cards is provided on the nxp.com website.

ICAP Classification: CP: ___ IUO: ___ PUBI: X_			
Drawing Title: i.MX 8QM CPU CARD			
Page Title: WIFI_BLUETOOTH -M.2 CONNECTOR E-KEY			
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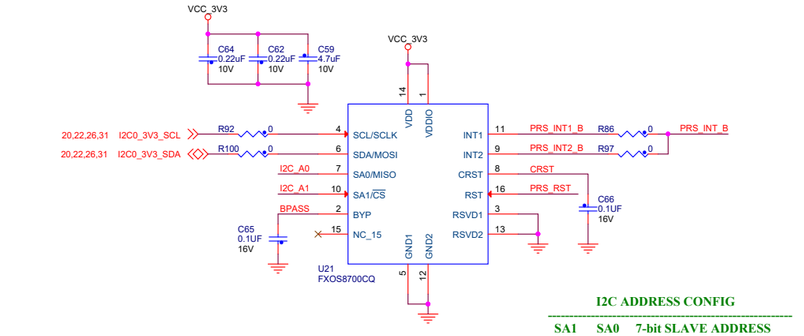
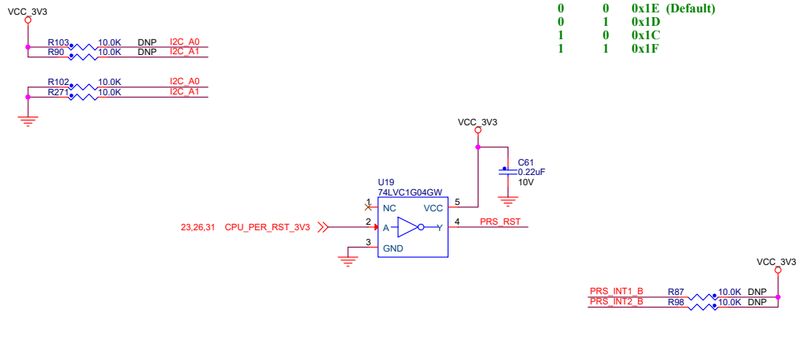
SENSORS

ACCELEROMETER

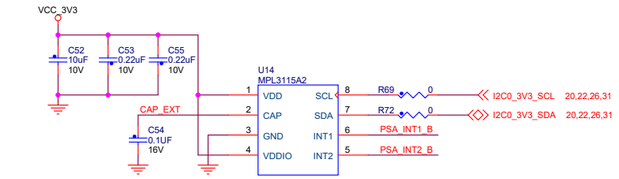


I2C ADDRESS CONFIG

SA1	SA0	7-bit SLAVE ADDRESS
0	0	0x1E (Default)
0	1	0x1D
1	0	0x1C
1	1	0x1F

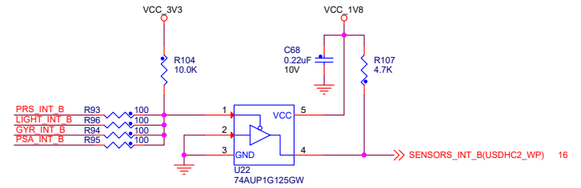


PRESSURE SENSOR WITH ALTIMETRY



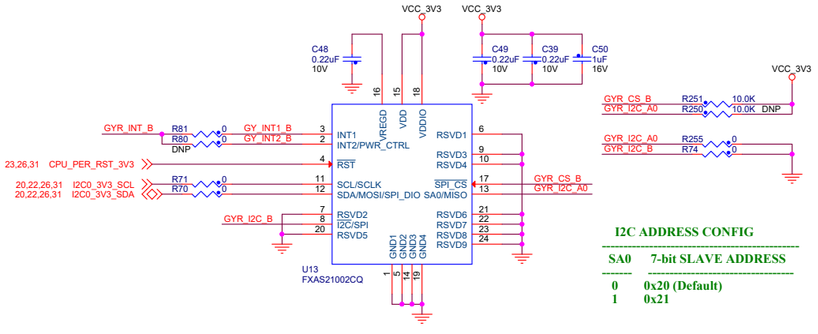
7-bit I2C Address: 0x60

SENSOR INTERRUPT



CONFIGURE ACCELEROMETER,GYROSCOPE,PRESSURE SENSOR INTERRUPTS AS OPEN DRAIN,ACTIVE LOW IN RESPECTIVE REGISTERS

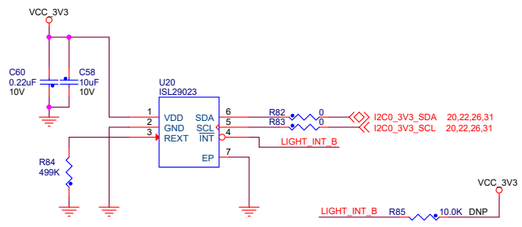
GYROSCOPE



I2C ADDRESS CONFIG

SA0	7-bit SLAVE ADDRESS
0	0x20 (Default)
1	0x21

AMBIENT LIGHT SENSOR



7-bit I2C Address: 0x44

ICAP Classification:	CP: ___	IUO: ___	PUBI: X
Drawing Title:	i.MX 8QM CPU CARD		
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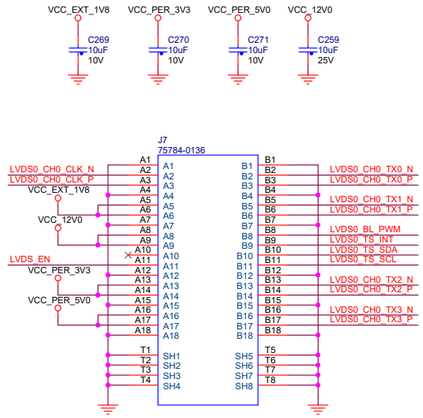
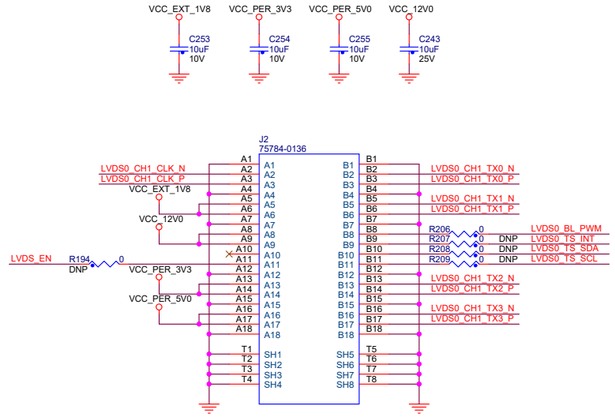
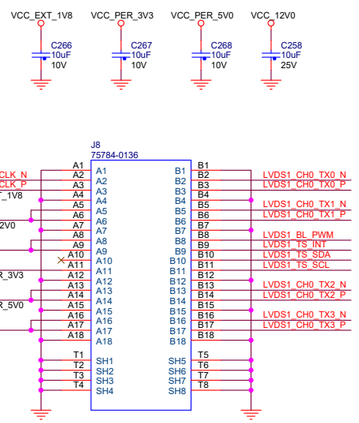
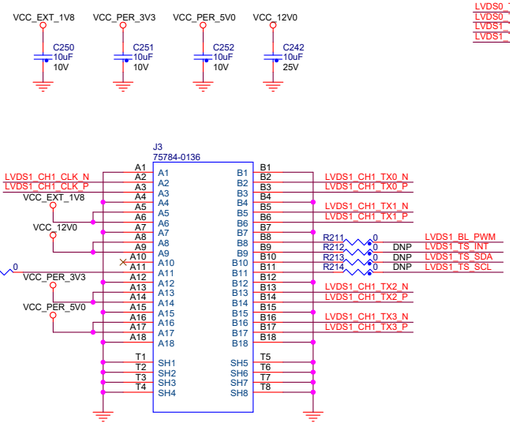
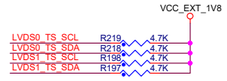
LVDS0 CH0 & CH1 CONNECTORS











ICAP Classification: CP: ___ IUO: ___ PUBI: X

Drawing Title: **i.MX 8QM CPU CARD**

Page Title: **LVDS0 CONNECTORS**

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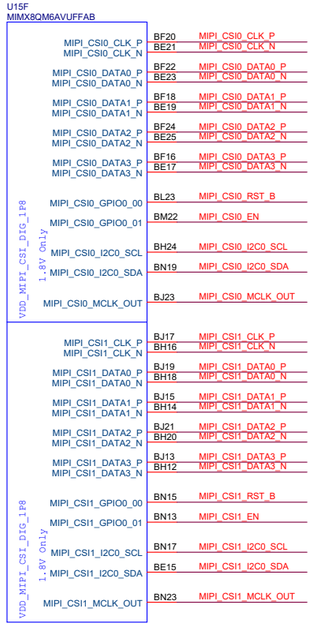
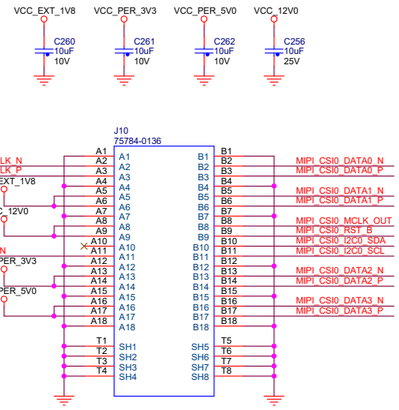
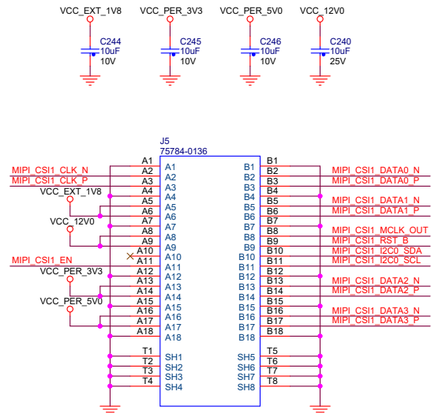
MIPI CSI CONNECTORS

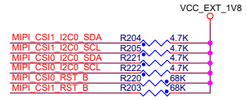


100-Ohm differential pairs

100-Ohm differential pairs







ICAP Classification:	CP: ___ IUO: ___ PUBI: X_	
Drawing Title:	i.MX 8QM CPU CARD	
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MIPI DSI CONNECTORS

U15G
MIMX8QM6AVUFFAB

VDD_MIPI_DSI_DIG_1P8_3P3

MIPI_DSI0_CLK_P	BL27	MIPI_DSI0_CLK_P
MIPI_DSI0_CLK_N	BN27	MIPI_DSI0_CLK_N
MIPI_DSI0_DATA0_P	BK28	MIPI_DSI0_DATA0_P
MIPI_DSI0_DATA0_N	BM28	MIPI_DSI0_DATA0_N
MIPI_DSI0_DATA1_P	BK26	MIPI_DSI0_DATA1_P
MIPI_DSI0_DATA1_N	BM26	MIPI_DSI0_DATA1_N
MIPI_DSI0_DATA2_P	BL29	MIPI_DSI0_DATA2_P
MIPI_DSI0_DATA2_N	BN29	MIPI_DSI0_DATA2_N
MIPI_DSI0_DATA3_P	BL25	MIPI_DSI0_DATA3_P
MIPI_DSI0_DATA3_N	BN25	MIPI_DSI0_DATA3_N
MIPI_DSI0_GPIO0_00	BD30	MIPI_DSI0_BL_PWM
MIPI_DSI0_GPIO0_01	BD28	MIPI_DSI0_TS_INT_B
MIPI_DSI0_I2C0_SCL	BE29	MIPI_DSI0_TS_SCL
MIPI_DSI0_I2C0_SDA	BE31	MIPI_DSI0_TS_SDA

100-Ohm differential pairs

MIPI_DSI1_CLK_P	BG31	MIPI_DSI1_CLK_P
MIPI_DSI1_CLK_N	BH30	MIPI_DSI1_CLK_N
MIPI_DSI1_DATA0_P	BG33	MIPI_DSI1_DATA0_P
MIPI_DSI1_DATA0_N	BH32	MIPI_DSI1_DATA0_N
MIPI_DSI1_DATA1_P	BG29	MIPI_DSI1_DATA1_P
MIPI_DSI1_DATA1_N	BH28	MIPI_DSI1_DATA1_N
MIPI_DSI1_DATA2_P	BG35	MIPI_DSI1_DATA2_P
MIPI_DSI1_DATA2_N	BH34	MIPI_DSI1_DATA2_N
MIPI_DSI1_DATA3_P	BG27	MIPI_DSI1_DATA3_P
MIPI_DSI1_DATA3_N	BH26	MIPI_DSI1_DATA3_N
MIPI_DSI1_GPIO0_00	BM24	MIPI_DSI1_BL_PWM
MIPI_DSI1_GPIO0_01	BK24	MIPI_DSI1_TS_INT_B
MIPI_DSI1_I2C0_SCL	BE27	MIPI_DSI1_TS_SCL
MIPI_DSI1_I2C0_SDA	BG25	MIPI_DSI1_TS_SDA

100-Ohm differential pairs

VCC_EXT_1V8 — C263 10uF 10V
VCC_PER_3V3 — C264 10uF 10V
VCC_PER_5V0 — C265 10uF 10V
VCC_12V0 — C257 10uF 25V

J9
75784-0136

MIPI_DSI0_CLK_N	A2	B2 MIPI_DSI0_DATA0_N
MIPI_DSI0_CLK_P	A3	B3 MIPI_DSI0_DATA0_P
VCC_EXT_1V8	A4	B4
	A5	B5 MIPI_DSI0_DATA1_N
VCC_12V0	A6	B6 MIPI_DSI0_DATA1_P
	A7	B7
	A8	B8 MIPI_DSI0_BL_PWM
	A9	B9 MIPI_DSI0_TS_INT_B
	A10	B10 MIPI_DSI0_TS_SDA
27,29 MIPI_DSI0_1_EN	A11	B11 MIPI_DSI0_TS_SCL
VCC_PER_3V3	A12	B12
	A13	B13 MIPI_DSI0_DATA2_N
	A14	B14 MIPI_DSI0_DATA2_P
VCC_PER_5V0	A15	B15
	A16	B16 MIPI_DSI0_DATA3_N
	A17	B17 MIPI_DSI0_DATA3_P
	A18	B18
	T1	T5
	T2 SH1	SH5 T6
	T3 SH2	SH6 T7
	T4 SH3	SH7 T8
	SH4	SH8

VCC_EXT_1V8 — C247 10uF 10V
VCC_PER_3V3 — C248 10uF 10V
VCC_PER_5V0 — C249 10uF 10V
VCC_12V0 — C241 10uF 25V

J4
75784-0136

MIPI_DSI1_CLK_N	A2	B2 MIPI_DSI1_DATA0_N
MIPI_DSI1_CLK_P	A3	B3 MIPI_DSI1_DATA0_P
VCC_EXT_1V8	A4	B4
	A5	B5 MIPI_DSI1_DATA1_N
VCC_12V0	A6	B6 MIPI_DSI1_DATA1_P
	A7	B7
	A8	B8 MIPI_DSI1_BL_PWM
	A9	B9 MIPI_DSI1_TS_INT_B
	A10	B10 MIPI_DSI1_TS_SDA
27,29 MIPI_DSI0_1_EN	A11	B11 MIPI_DSI1_TS_SCL
VCC_PER_3V3	A12	B12
	A13	B13 MIPI_DSI1_DATA2_N
	A14	B14 MIPI_DSI1_DATA2_P
VCC_PER_5V0	A15	B15
	A16	B16 MIPI_DSI1_DATA3_N
	A17	B17 MIPI_DSI1_DATA3_P
	A18	B18
	T1	T5
	T2 SH1	SH5 T6
	T3 SH2	SH6 T7
	T4 SH3	SH7 T8
	SH4	SH8

VCC_EXT_1V8

MIPI_DSI0_TS_SDA	R215	4.7K
MIPI_DSI0_TS_SCL	R216	4.7K
MIPI_DSI1_TS_SDA	R200	4.7K
MIPI_DSI1_TS_SCL	R201	4.7K

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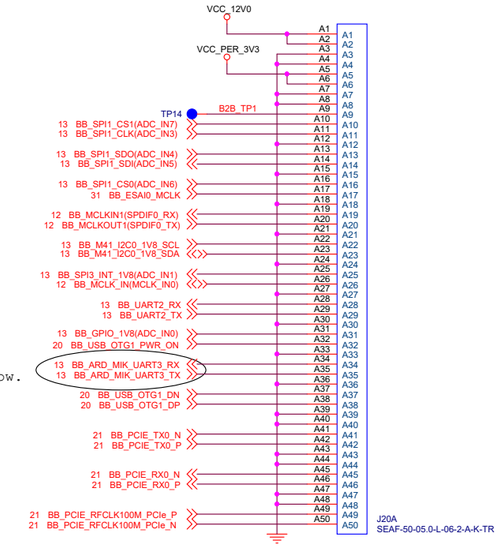
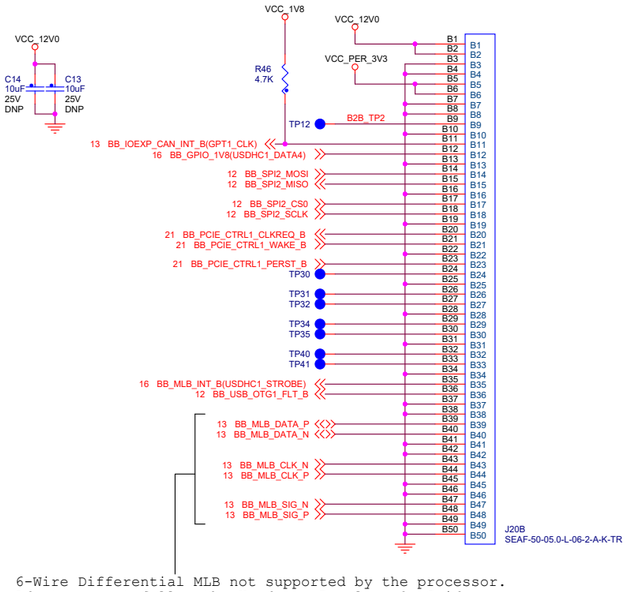
B2B CONNECTOR

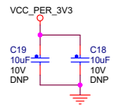
EACH CONNECTOR PIN
CAPABLE OF 1.2 A

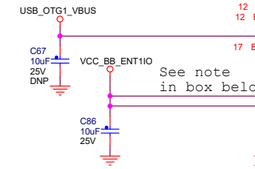


See note
in box below.

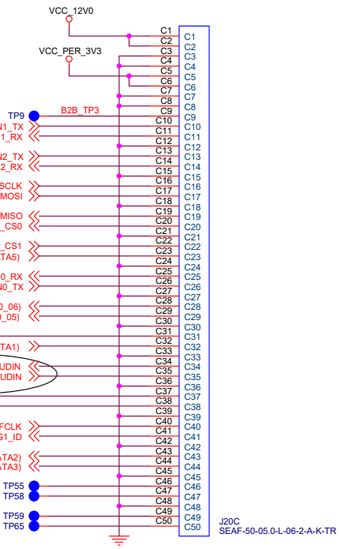


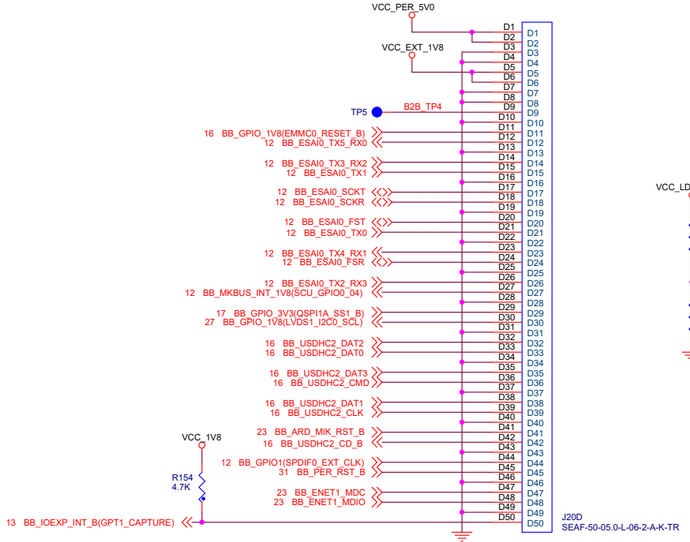
6-Wire Differential MLB not supported by the processor.
Adopters must follow the Hardware Developer's Guide
Unused input/output terminations section.

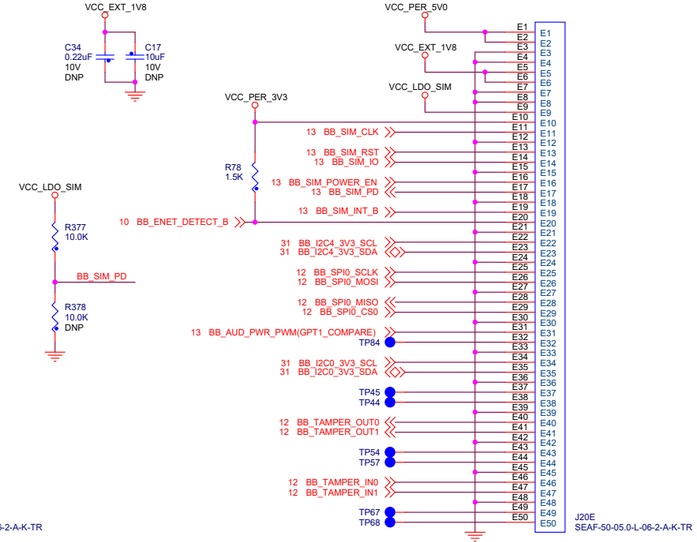


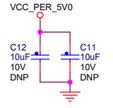


See note
in box below.

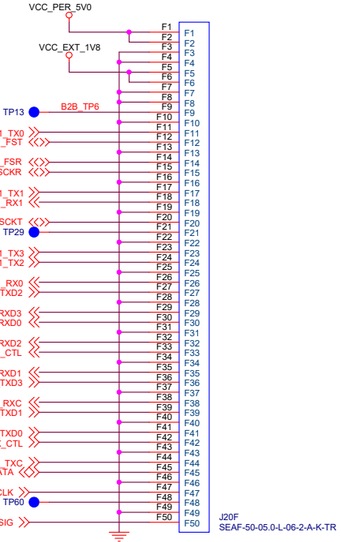








Users can install both ENET and
AUD cards simultaneously in BB



SOME PINS ARE RESERVED TO FACILITATE A COMMON BASE BOARD FOR QM AND QXP.

3-Wire Single-Ended MLB not supported by the processor.
Other functions are supported as determined by IOMUX selection.
If unused, adopters must follow the Hardware Developer's
Guide Unused input/output terminations section.

NXP is aware that the UART net names circled are inaccurate. There is no plan to change the net names.

Adopters please note:
UART3 net name on pins A34 & A35 should be UART4.
UART4 net name on pins C34 & C35 should be UART3.
2-Wire AUDIN function not available on Base Board.

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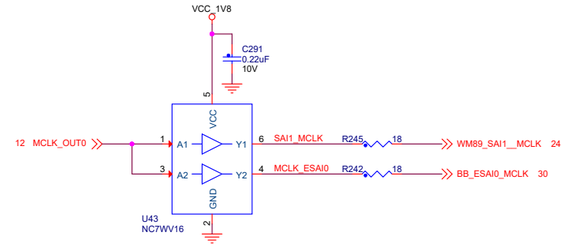
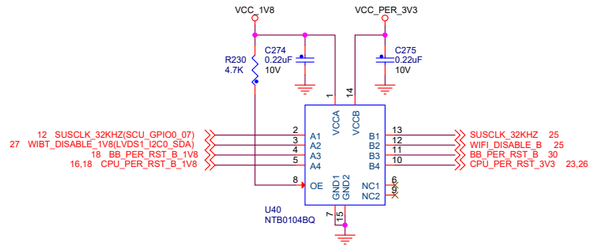
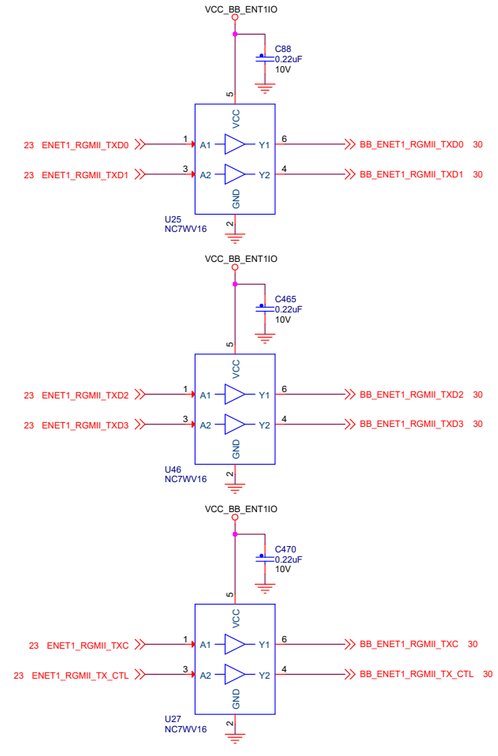
MCLK CLOCK DRIVERS FOR BASE BOARD FAN OUT



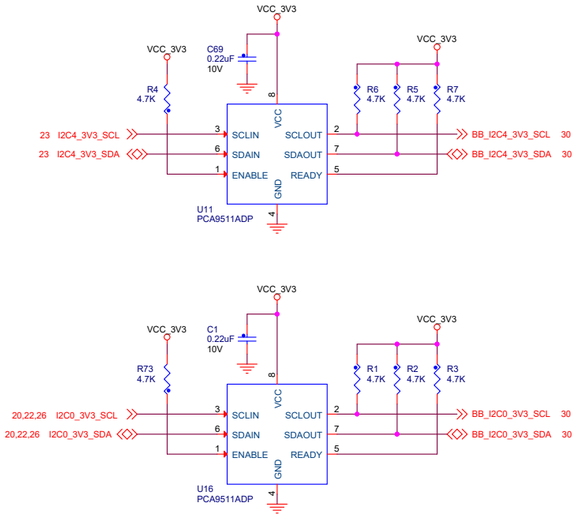
LEVEL TRANSLATOR



ETHERNET TX BUFFERS FOR BASEBOARD



I2C BUFFERS FOR BASE BOARD



ICAP Classification: CP: ___ IUO: ___ PUBI: X_

Drawing Title:

i.MX 8QM CPU CARD

Page Title:

LEVEL TRANSLATORS & DRIVERS

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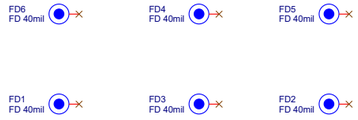
MISCELLANEOUS

GLOBAL FIDUCIALS

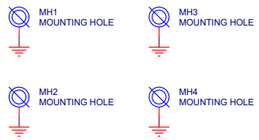


HEATSINK WITH FAN

Part number: 30-1944-01
Vendor : Cofan USA

TEST POINTS

MOUNTING HOLES



MOUNTING HOLE FOR M.2 CARD

ICAP Classification: CP: ___ IUO: ___ PUBI: X_

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