PTN3460I Eval. Board with AUO 7" Panel Rev.1.0

REVISION HISTORY :

1.0 Aug. 19, 2014
- Base on PTN3460 E-Tool design
- Chang eCFG3, CFG4 definition
- Rework R60. Add 10K from U4-1 to U4-2
- Rework 3-pin headers. Add JP23, 24, 25.

NXP Semiconductors

1251 McKay Dr. M/S-60SJ, San Jose, CA 95131-1706

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Document Name: **(e)DP-LVDS (PTN3460I) to LCD PANEL**

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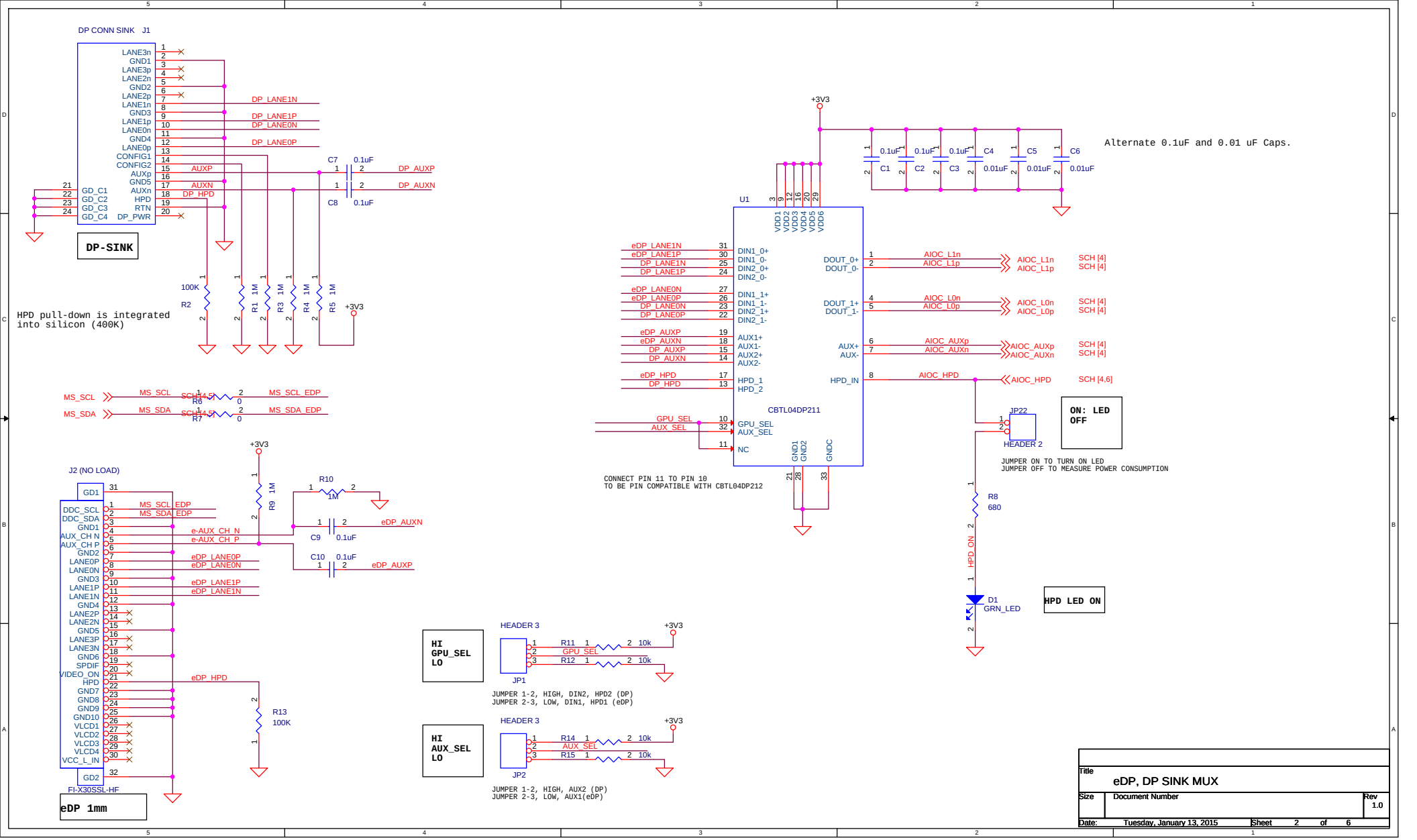
DP CONN SINK J1
DP-SINK
HPD pull-down is integrated into silicon (400K)
MS_SCL
MS_SDA
J2 (NO LOAD)
eDP 1mm
FI-X30SSL-HF
HI GPU_SEL LO
HI AUX_SEL LO
JUMPER 1-2, HIGH, DIN2, HPD2 (DP)
JUMPER 2-3, LOW, DIN1, HPD1 (eDP)
JUMPER 1-2, HIGH, AUX2 (DP)
JUMPER 2-3, LOW, AUX1(eDP)
U1
CBTL04DP211
CONNECT PIN 11 TO PIN 10
TO BE PIN COMPATIBLE WITH CBTL04DP212
Alternate 0.1uF and 0.01 uF Caps.
JP22
HEADER 2
ON: LED OFF
JUMPER ON TO TURN ON LED
JUMPER OFF TO MEASURE POWER CONSUMPTION
D1
GRN_LED
HPD LED ON
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eDP, DP SINK MUX
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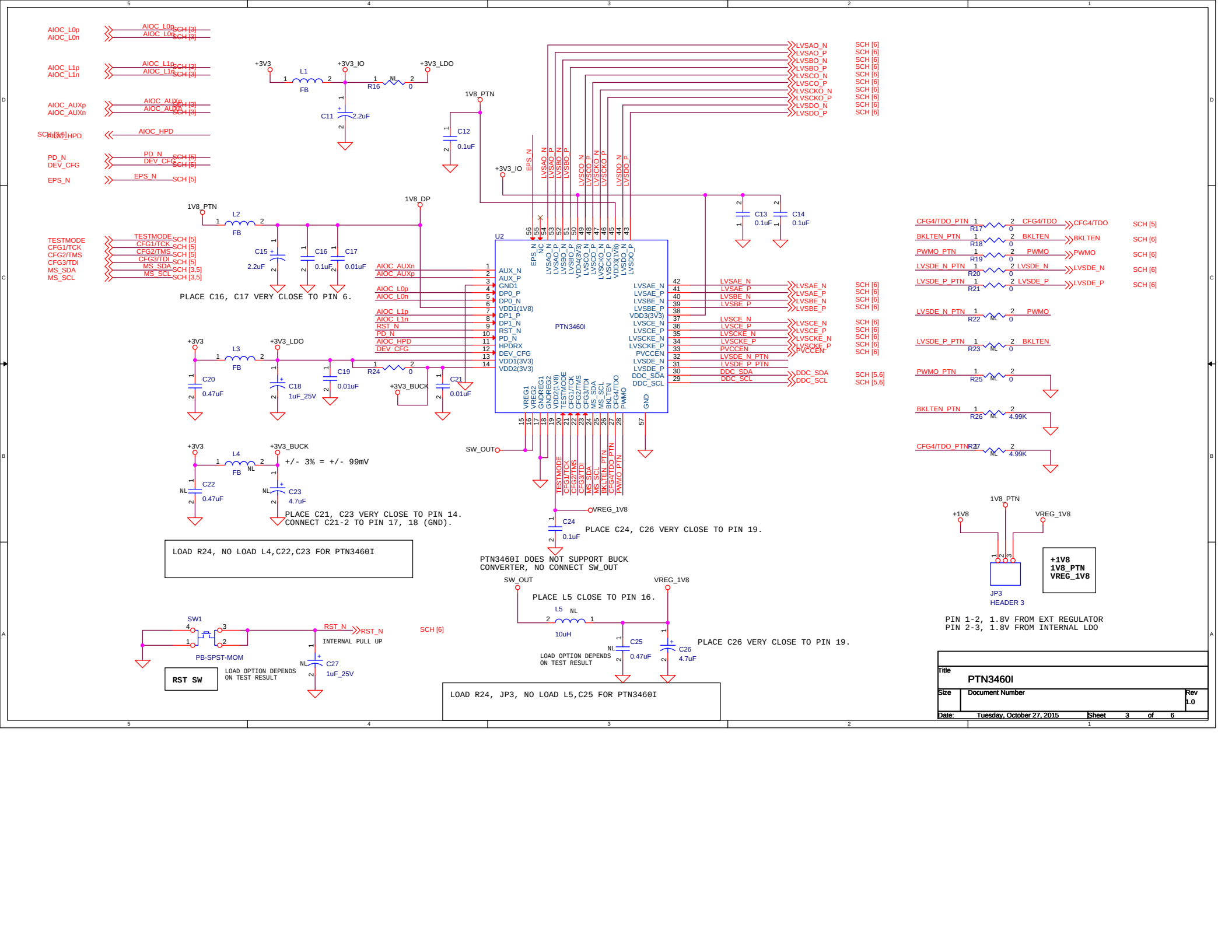
AIOC_L0p
AIOC_L0n
AIOC_L1p
AIOC_L1n
AIOC_AUXp
AIOC_AUXn
AIOC_HPD
PD_N
DEV_CFG
EPS_N
SCH [3]
SCH [5]
+3V3
+3V3_IO
+3V3_LDO
L1
FB
R16
NL
0
C11
2.2uF
C12
0.1uF
1V8_PTN
1V8_DP
L2
C15
2.2uF
C16
0.1uF
C17
0.01uF
TESTMODE
CFG1/TCK
CFG2/TMS
CFG3/TDI
MS_SDA
MS_SCL
PLACE C16, C17 VERY CLOSE TO PIN 6.
U2
PTN3460I
AUX_N
AUX_P
GND1
DP0_P
DP0_N
VDD1(1V8)
DP1_P
DP1_N
RST_N
PD_N
HPDRX
DEV_CFG
VDD1(3V3)
VDD2(3V3)
VREG1
VREG2
GNDREG1
GNDREG2
VDD2(1V8)
TESTMODE
CFG1/TCK
CFG2/TMS
CFG3/TDI
MS_SDA
MS_SCL
BKLTEN
CFG4/TDO
PWMO
GND
LVSAE_N
LVSAE_P
LVSBE_N
LVSBE_P
VDD3(3V3)
LVSCE_N
LVSCE_P
LVSCKE_N
LVSCKE_P
PVCCEN
LVSDE_N
LVSDE_P
DDC_SDA
DDC_SCL
LVSAO_N
LVSAO_P
LVSBO_N
LVSBO_P
LVSCO_N
LVSCO_P
LVSCKO_N
LVSCKO_P
VDD4(3V3)
LVSDO_N
LVSDO_P
LVSDE_N_PTN
LVSDE_P_PTN
PWMO_PTN
BKLTEN_PTN
CFG4/TDO_PTN
C13
0.1uF
C14
0.1uF
L3
C20
0.47uF
C18
1uF_25V
C19
0.01uF
R24
0
+3V3_BUCK
C21
0.01uF
PLACE C21, C23 VERY CLOSE TO PIN 14.
CONNECT C21-2 TO PIN 17, 18 (GND).
L4
+/- 3% = +/- 99mV
C22
0.47uF
C23
4.7uF
LOAD R24, NO LOAD L4,C22,C23 FOR PTN3460I
SW_OUT
VREG_1V8
C24
0.1uF
PLACE C24, C26 VERY CLOSE TO PIN 19.
PTN3460I DOES NOT SUPPORT BUCK
CONVERTER, NO CONNECT SW_OUT
PLACE L5 CLOSE TO PIN 16.
L5
10uH
C25
0.47uF
C26
4.7uF
LOAD OPTION DEPENDS
ON TEST RESULT
PLACE C26 VERY CLOSE TO PIN 19.
LOAD R24, JP3, NO LOAD L5,C25 FOR PTN3460I
SW1
PB-SPST-MOM
RST_N
INTERNAL PULL UP
C27
1uF_25V
RST SW
R17
R18
R19
R20
R21
R22
R23
R25
R26
R27
4.99K
JP3
HEADER 3
+1V8
1V8_PTN
VREG_1V8
PIN 1-2, 1.8V FROM EXT REGULATOR
PIN 2-3, 1.8V FROM INTERNAL LDO
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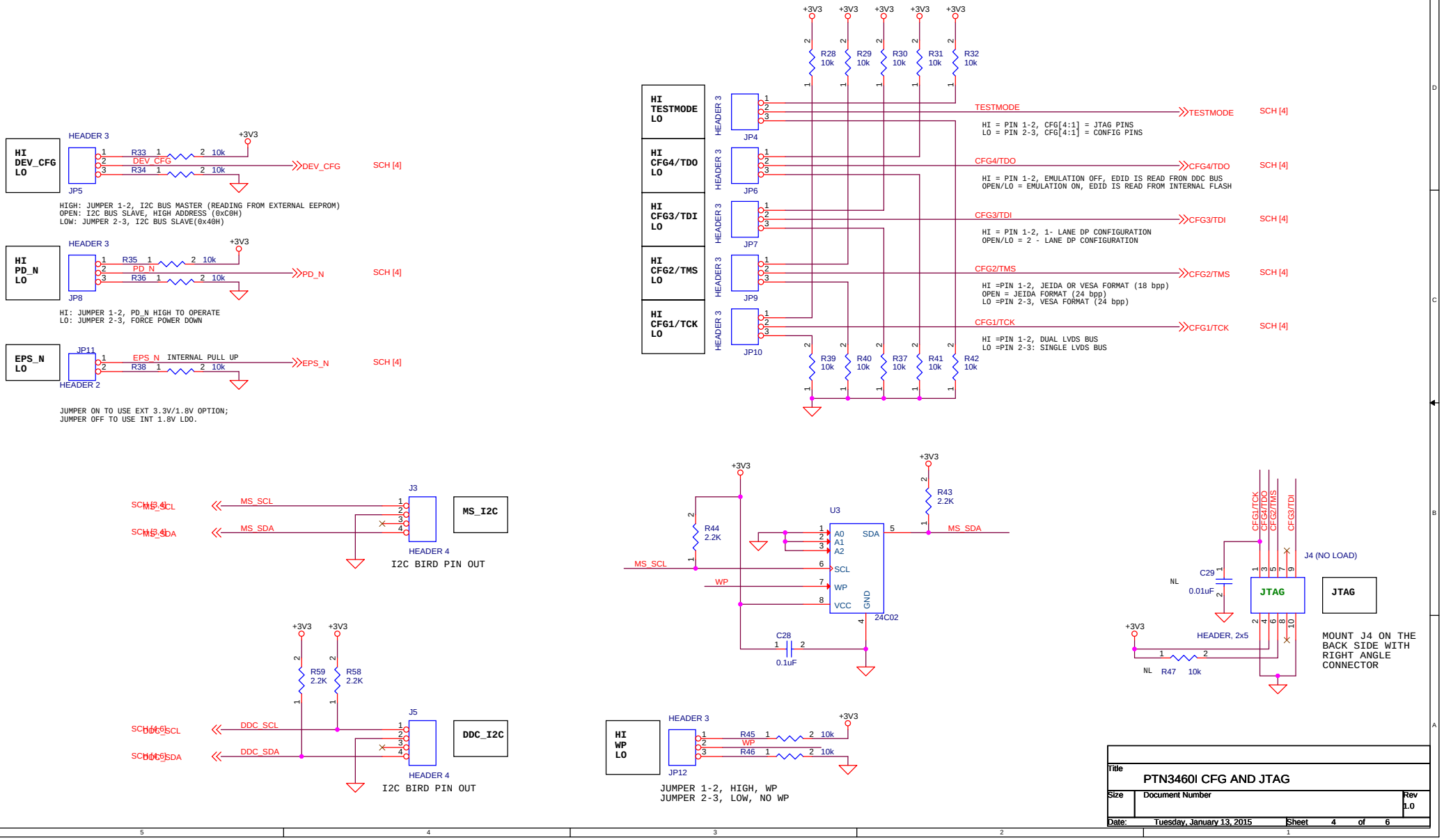
HI DEV_CFG LO
HEADER 3
+3V3
R33 1 2 10k
DEV_CFG
R34 1 2 10k
JP5
DEV_CFG
SCH [4]
HIGH: JUMPER 1-2, I2C BUS MASTER (READING FROM EXTERNAL EEPROM)
OPEN: I2C BUS SLAVE, HIGH ADDRESS (0xC0H)
LOW: JUMPER 2-3, I2C BUS SLAVE(0x40H)
HI PD_N LO
HEADER 3
+3V3
R35 1 2 10k
PD_N
R36 1 2 10k
JP8
PD_N
SCH [4]
HI: JUMPER 1-2, PD_N HIGH TO OPERATE
LO: JUMPER 2-3, FORCE POWER DOWN
EPS_N LO
JP11
EPS_N INTERNAL PULL UP
R38 1 2 10k
HEADER 2
EPS_N
SCH [4]
JUMPER ON TO USE EXT 3.3V/1.8V OPTION;
JUMPER OFF TO USE INT 1.8V LDO.
+3V3
R28 10k
R29 10k
R30 10k
R31 10k
R32 10k
HI TESTMODE LO
HI CFG4/TDO LO
HI CFG3/TDI LO
HI CFG2/TMS LO
HI CFG1/TCK LO
HEADER 3
JP4
JP6
JP7
JP9
JP10
TESTMODE
CFG4/TDO
CFG3/TDI
CFG2/TMS
CFG1/TCK
SCH [4]
HI = PIN 1-2, CFG[4:1] = JTAG PINS
LO = PIN 2-3, CFG[4:1] = CONFIG PINS
HI = PIN 1-2, EMULATION OFF, EDID IS READ FRON DDC BUS
OPEN/LO = EMULATION ON, EDID IS READ FROM INTERNAL FLASH
HI = PIN 1-2, 1- LANE DP CONFIGURATION
OPEN/LO = 2 - LANE DP CONFIGURATION
HI =PIN 1-2, JEIDA OR VESA FORMAT (18 bpp)
OPEN = JEIDA FORMAT (24 bpp)
LO =PIN 2-3, VESA FORMAT (24 bpp)
HI =PIN 1-2, DUAL LVDS BUS
LO =PIN 2-3: SINGLE LVDS BUS
R39 10k
R40 10k
R37 10k
R41 10k
R42 10k
J3
MS_I2C
HEADER 4
MS_SCL
MS_SDA
I2C BIRD PIN OUT
R44 2.2K
R43 2.2K
U3
A0
A1
A2
SDA
SCL
WP
VCC
GND
24C02
C28
0.1uF
J4 (NO LOAD)
JTAG
C29
0.01uF
NL
HEADER, 2x5
R47 10k
MOUNT J4 ON THE BACK SIDE WITH RIGHT ANGLE CONNECTOR
R59 2.2K
R58 2.2K
J5
DDC_I2C
DDC_SCL
DDC_SDA
I2C BIRD PIN OUT
HI WP LO
JP12
R45 1 2 10k
R46 1 2 10k
JUMPER 1-2, HIGH, WP
JUMPER 2-3, LOW, NO WP
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PTN3460I CFG AND JTAG
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TO BE USED WITH 90-PIN DIFFERENTIAL LOGIC PROBE E5387A

RE-WORKS: 3-PIN HEADERS GLUE ON BOARD WITH WIRES FOR SMALL PANEL WITH 20-PIN LVDS INTERFACE (OPTIONAL)

LVDS DUAL BUS 24bpp (8-BITS) PANEL

LVSAO_N / LVSAO_P SCH [4]
LVSBO_N / LVSBO_P SCH [4]
LVSCO_N / LVSCO_P SCH [4]
LVSDO_N / LVSDO_P SCH [4]
LVSCKO_N / LVSCKO_P SCH [4]
LVSAE_N / LVSAE_P SCH [4]
LVSBE_N / LVSBE_P SCH [4]
LVSCE_N / LVSCE_P SCH [4]
LVSDE_N / LVSDE_P SCH [4,6]
LVSCKE_N / LVSCKE_P SCH [4]
LVSDE_N / LVSDE_P SCH [4,6]
DDC_SDA / DDC_SCL SCH [4,5]
PVCCEN / PWMO / BKLTEN SCH [4]
AIOC_HPD / RST_N SCH [3,4] / SCH [4]

J6 — SOFT TOUCH CONN E5387-68701 NL

J8 — SOFT TOUCH CONN E5387-68701 NL

HI UD LO — HEADER 3 — R62 10k (UD) / R61 10k — JP23 (NL)
HIGH: JUMPER 1-2, NORMAL MODE
OPEN: NORMAL MODE
LOW: JUMPER 2-3, VERTICAL REVERSE SCAN

HI LR LO — HEADER 3 — R64 10k (LR) / R63 10k — JP24 (NL)
HIGH: JUMPER 1-2, NORMAL MODE
OPEN: NORMAL MODE
LOW: JUMPER 2-3, HORIZONTAL REVERSE SCAN

HI SEL_68 LO — HEADER 3 — R66 10k (SEL_68) / R65 10k — JP25 (NL)
HIGH: JUMPER 1-2, 8 BIT INPUT MODE
OPEN: 6 BIT INPUT MODE
LOW: JUMPER 2-3, 6 BIT INPUT MODE

J7 — FI-XB30SRL-HF11
LVDS 32 1MM

C30 0.1uF / C31 0.1uF / C32 0.1uF

LVDS VDD SELECT

HEADER 3 — JP13 — +5V / +3V3
+3V3 VDD_VDL +5V
Q1 MOSFET P-CH — VDD_VDL — R48 1M — C38 0.01uF — C37 22uF_16V — C36 0.1uF — +V_RUN
VDD_EN — R49 100K — MOSFET N-CH Q3 — PVCCEN_PTN — R51 100K

HI PVCCEN_PTN PVCCEN — HEADER 3 — JP16 — R54 10k — +3V3 — PVCCEN_PTN / PVCCEN

HI PVCCEN LO — HEADER 3 NL — JP17 — R55 10k (PVCCEN) / R56 10k — +3V3

JUMPER 1-2, HIGH, I2C_ADDR 0xB0h-0xBFh
JUMPER 2-3, LOW, I2C_ADDR 0x10h-0x1Fh

+5V +INV_PWR +12V

INV PWR ENABLE

HEADER 3 — JP14 — +5V / +12V
Q2 MOSFET P-CH — +INV_PWR — R50 100K — C39 1uF_25V — C40 1uF_25V — C41 1uF_25V — +INV_PWR_SRC
INV_PWR_ON — R53 47k — +V_RUN — MOSFET N-CH Q4

HI BKLTEN_CN BKLTEN — HEADER 3 — JP15 — R52 10k — +V_RUN — BKLTEN_CN / BKLTEN

+INV_PWR_SRC
C33 0.1uF / C34 0.1uF / C35 0.1uF
CN1 — S8B-PH-SM4-TB(LF)(SN)
PWMO / BKLTEN_CN
BACKLIGHT CONN

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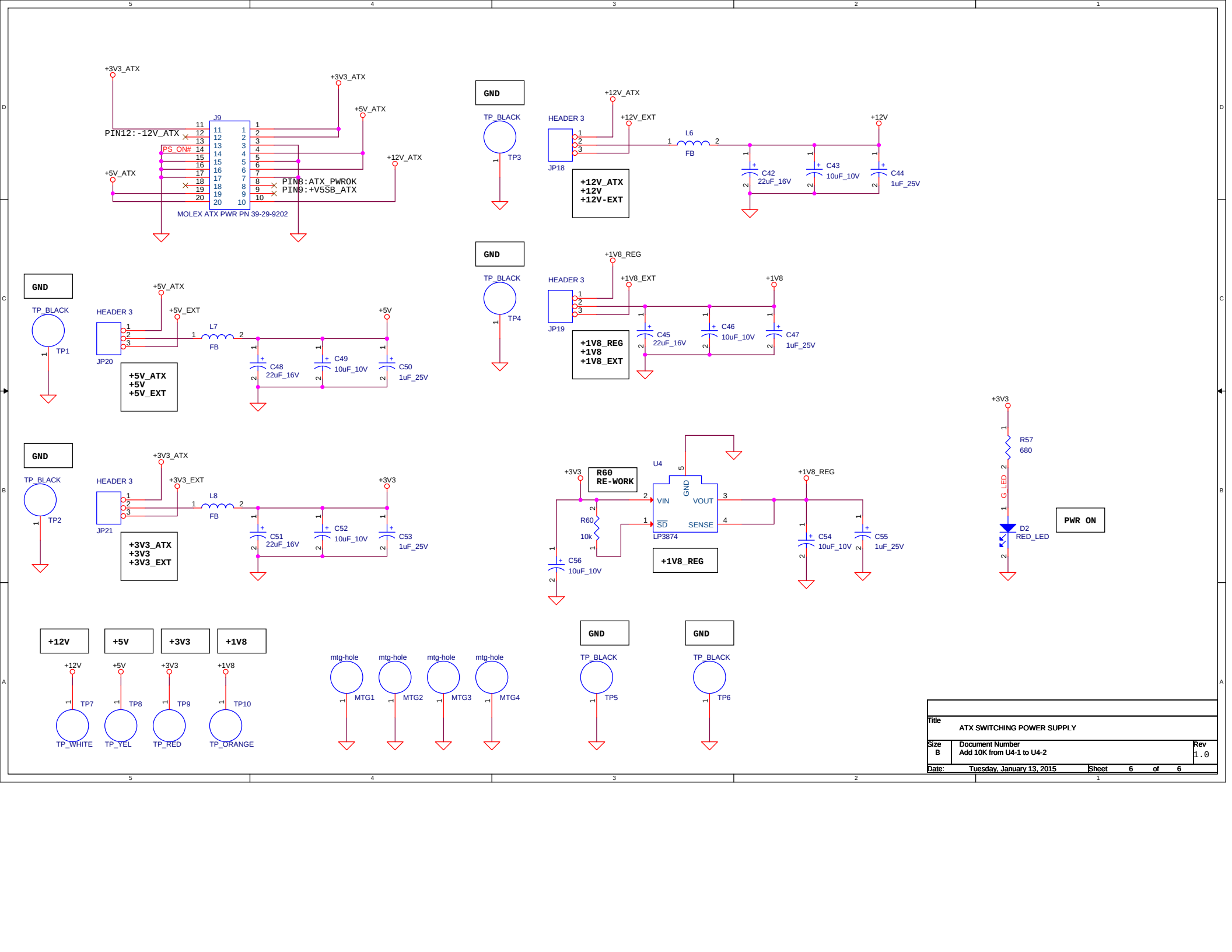
+3V3_ATX
+3V3_ATX
+5V_ATX
+12V_ATX
+5V_ATX
PIN12:-12V_ATX
PS_ON#
PIN8:ATX_PWROK
PIN9:+V5SB_ATX
J9
MOLEX ATX PWR PN 39-29-9202
GND
TP_BLACK
TP3
HEADER 3
+12V_ATX
+12V_EXT
L6
FB
+12V
JP18
+12V_ATX
+12V
+12V-EXT
C42
22uF_16V
C43
10uF_10V
C44
1uF_25V
GND
TP_BLACK
TP4
HEADER 3
+1V8_REG
+1V8_EXT
+1V8
JP19
+1V8_REG
+1V8
+1V8_EXT
C45
22uF_16V
C46
10uF_10V
C47
1uF_25V
GND
TP_BLACK
TP1
HEADER 3
+5V_ATX
+5V_EXT
L7
FB
+5V
JP20
+5V_ATX
+5V
+5V_EXT
C48
22uF_16V
C49
10uF_10V
C50
1uF_25V
GND
TP_BLACK
TP2
HEADER 3
+3V3_ATX
+3V3_EXT
L8
FB
+3V3
JP21
+3V3_ATX
+3V3
+3V3_EXT
C51
22uF_16V
C52
10uF_10V
C53
1uF_25V
+3V3
R60
RE-WORK
U4
VIN
GND
VOUT
SD
SENSE
LP3874
+1V8_REG
R60
10k
C56
10uF_10V
+1V8_REG
C54
10uF_10V
C55
1uF_25V
+3V3
R57
680
G_LED
D2
RED_LED
PWR ON
+12V
+5V
+3V3
+1V8
+12V
+5V
+3V3
+1V8
TP7
TP8
TP9
TP10
TP_WHITE
TP_YEL
TP_RED
TP_ORANGE
mtg-hole
mtg-hole
mtg-hole
mtg-hole
MTG1
MTG2
MTG3
MTG4
GND
TP_BLACK
TP5
GND
TP_BLACK
TP6
Title
ATX SWITCHING POWER SUPPLY
Size
B
Document Number
Add 10K from U4-1 to U4-2
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