



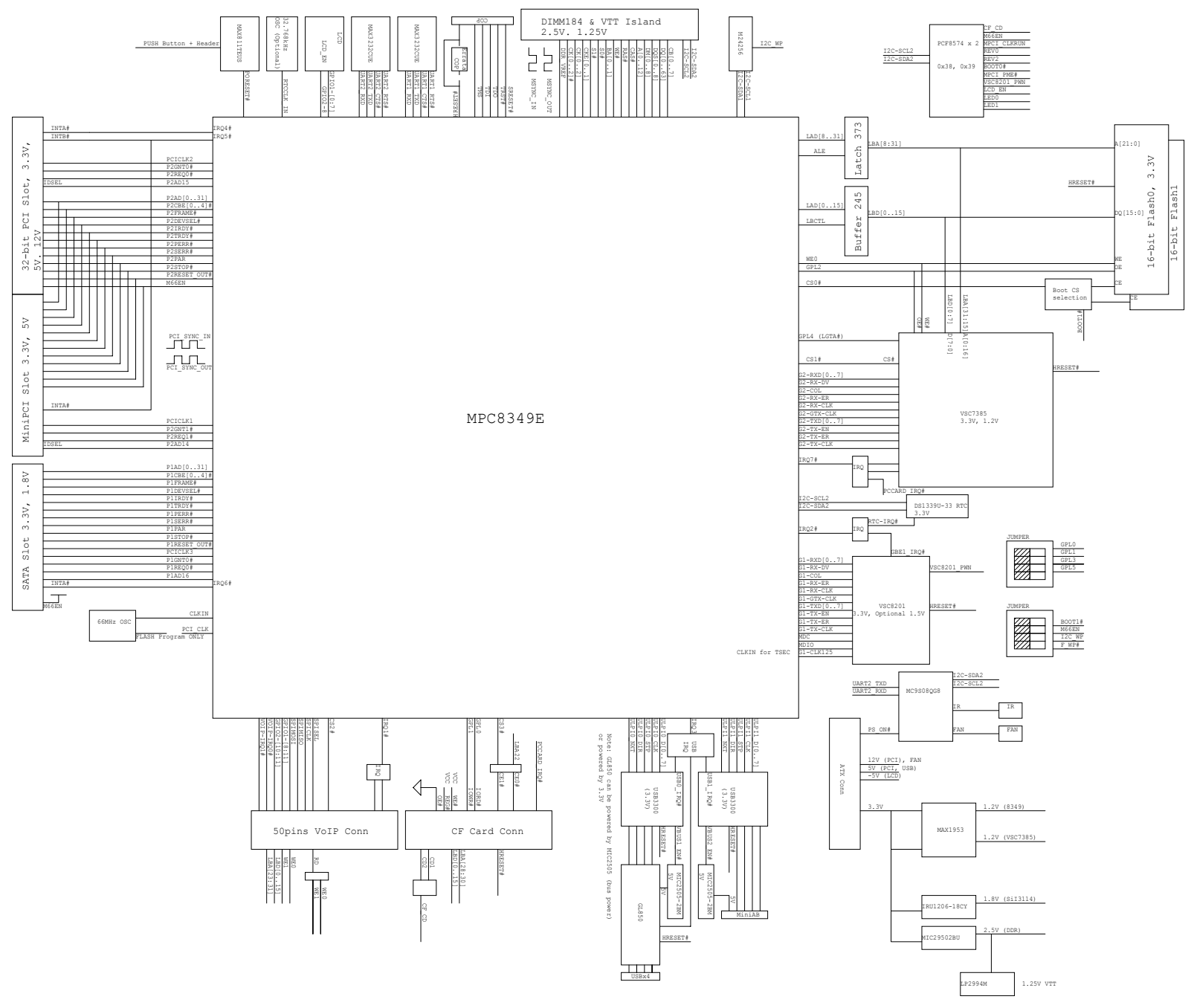
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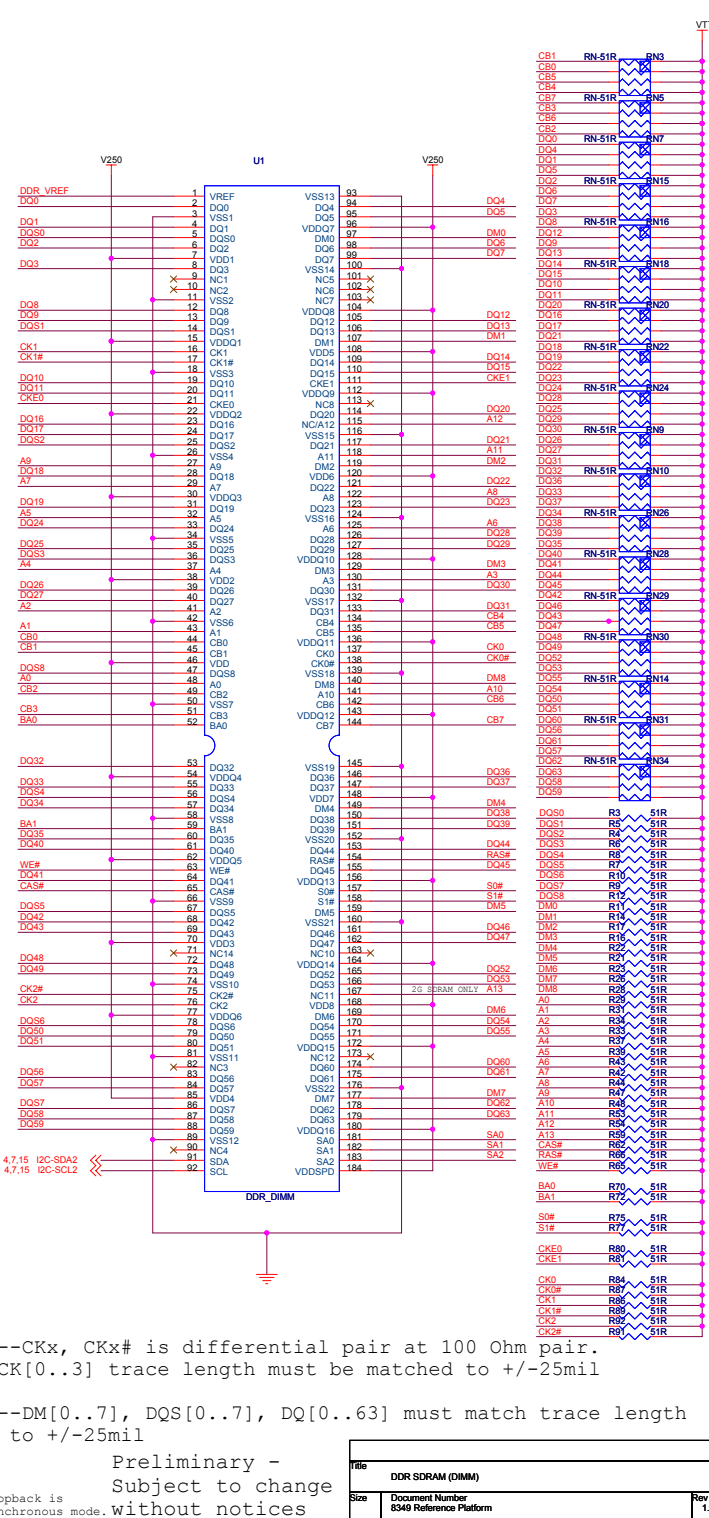
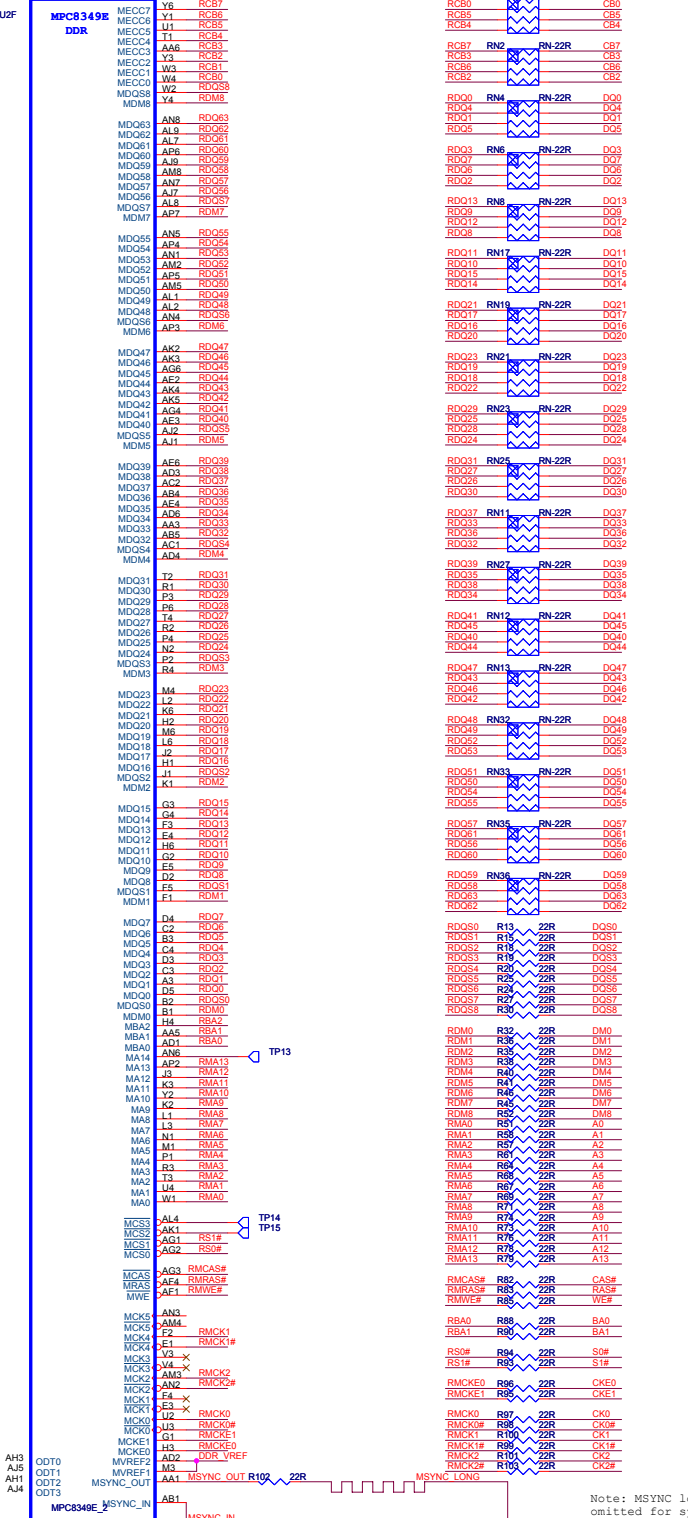
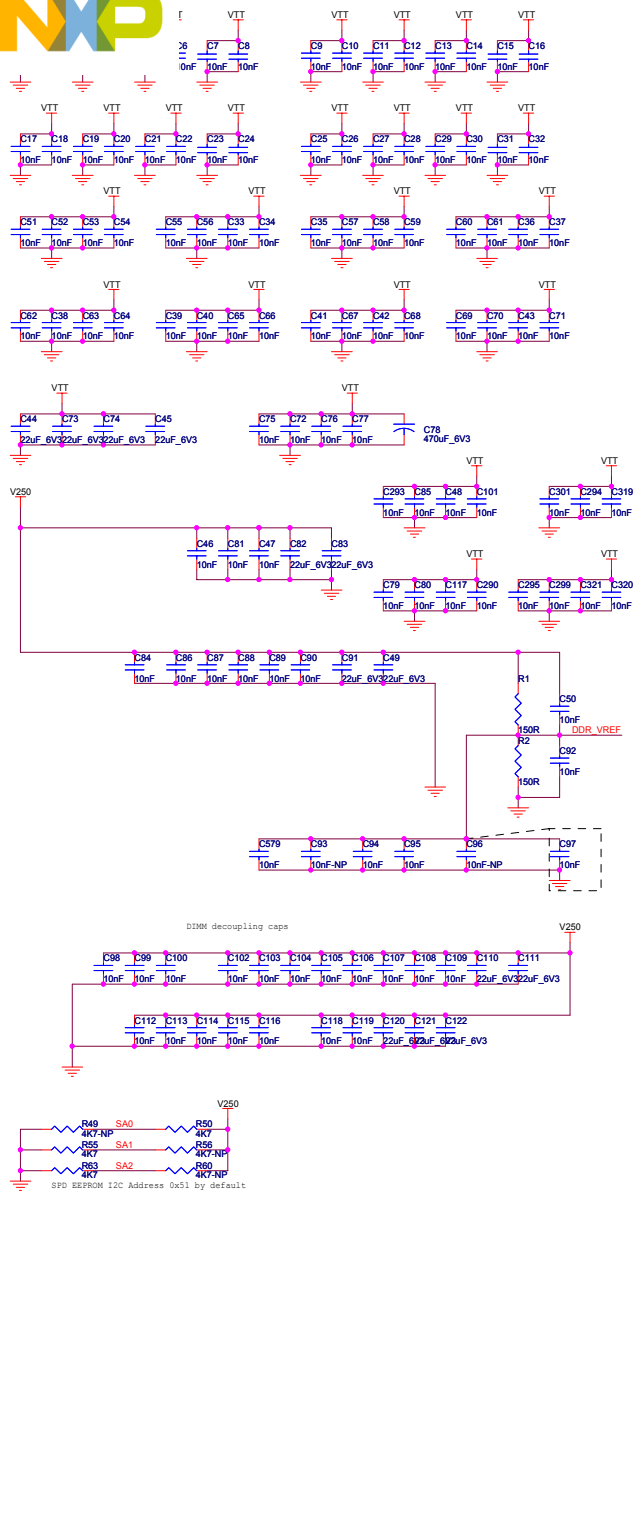
Revision History

Rev 0.0	12Jul05
Rev 0.1	10Nov05
Rev 1.0	03MAR06

Title		
List of Pages		
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Title		Block Diagram	
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--CKx, CKx# is differential pair at 100 Ohm pair.
 CK[0..3] trace length must be matched to +/-25mil

--DM[0..7], DQS[0..7], DQ[0..63] must match trace length to +/-25mil

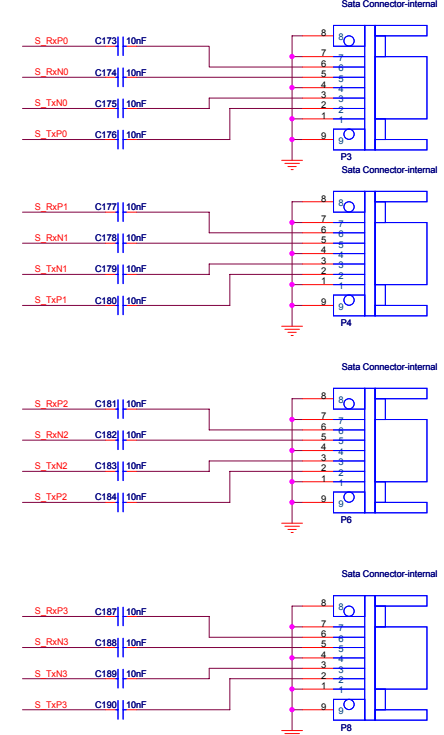
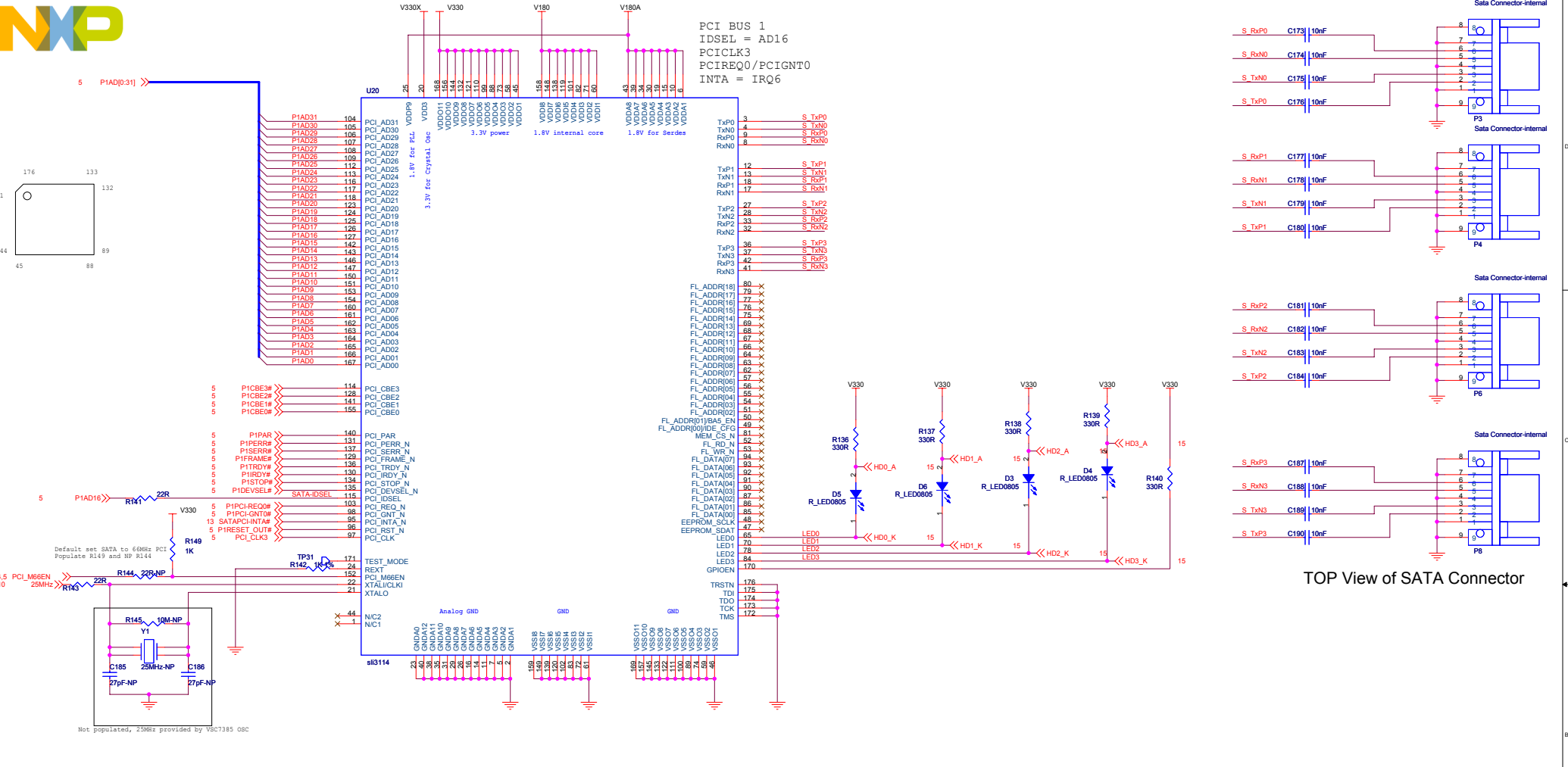
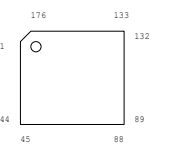
Preliminary -
 Subject to change
 without notices

Title		DDR SDRAM (DIMM)	
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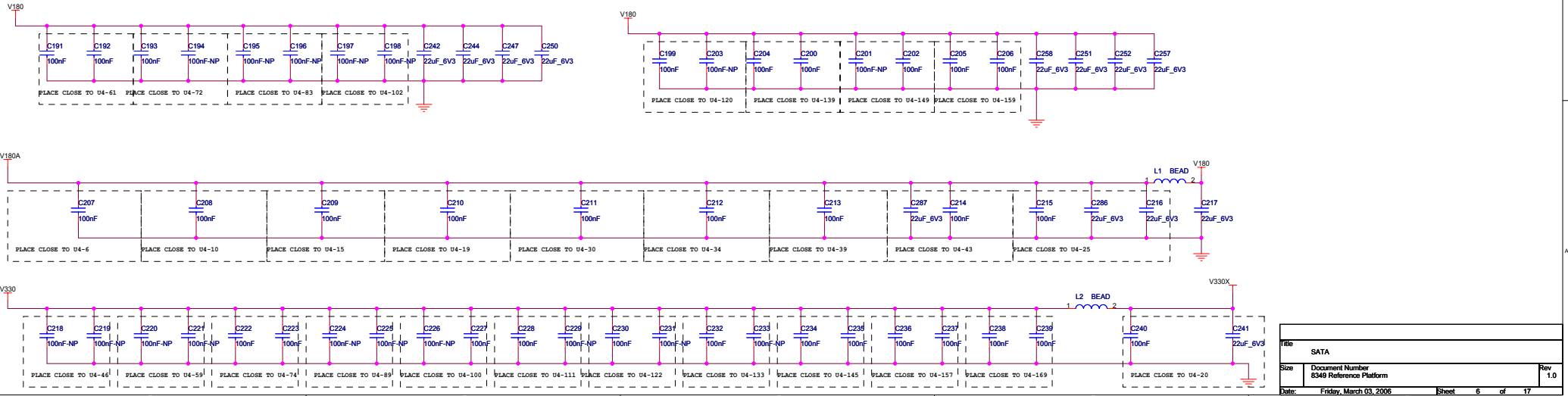
Note: M5SYNC loopback is omitted for synchronous mode.



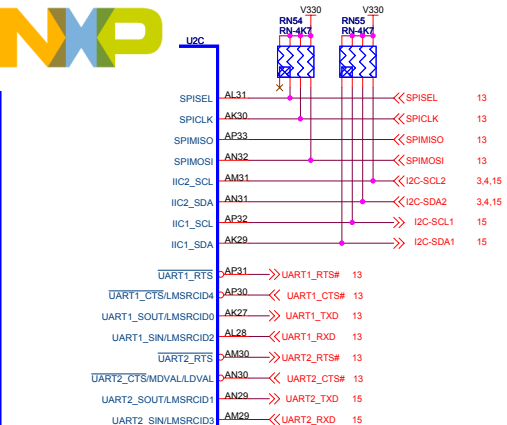
PCI BUS 1
 IDSEL = AD16
 PCICLK3
 PCIREQ0/PCIGNT0
 INTA = IRQ6



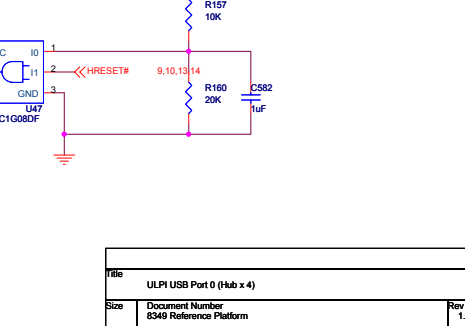
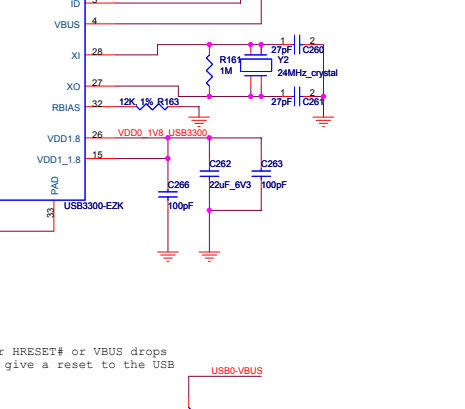
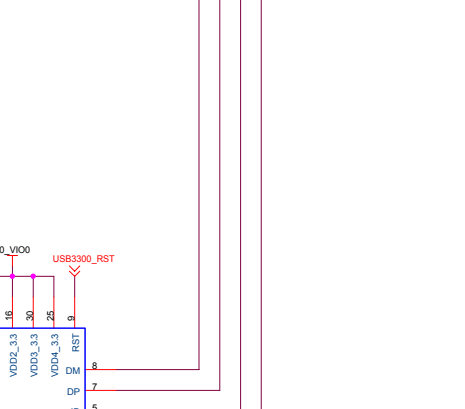
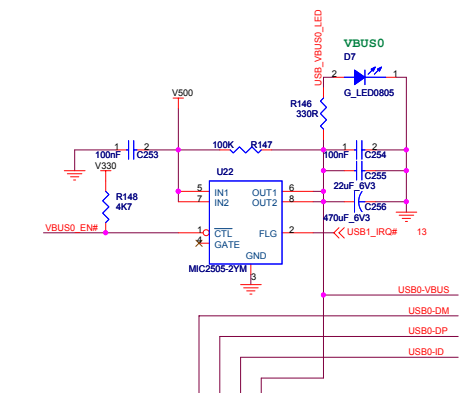
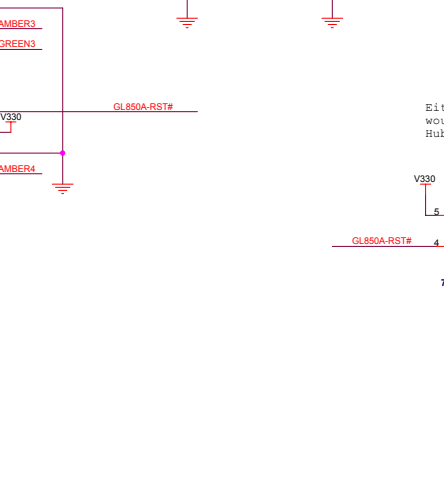
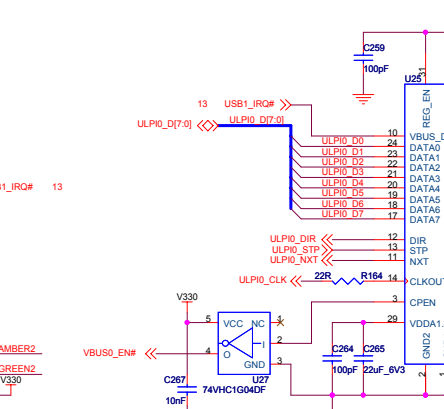
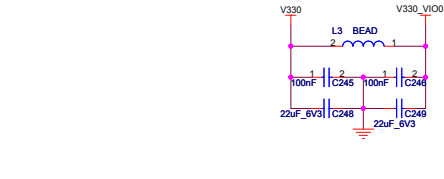
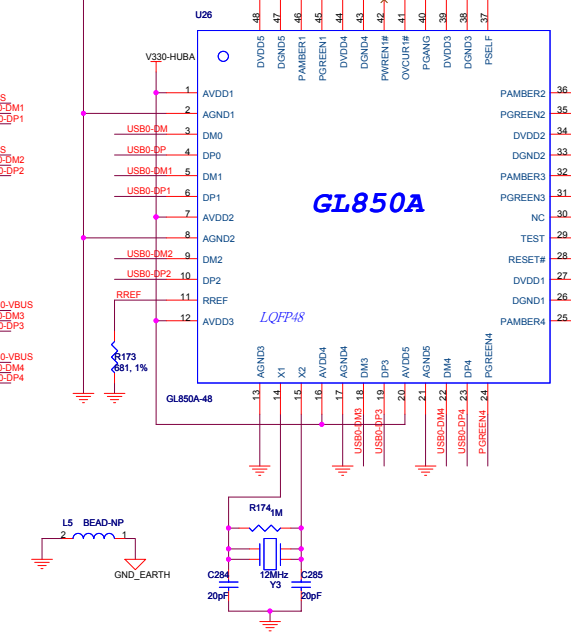
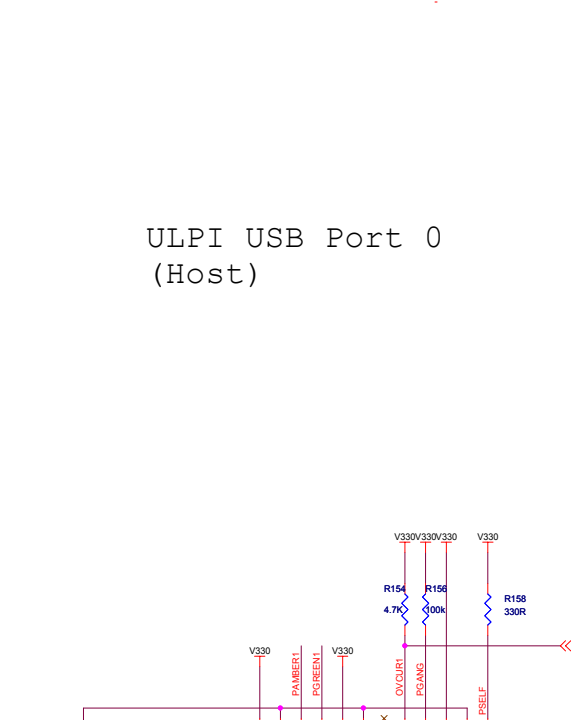
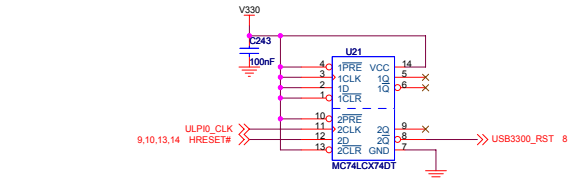
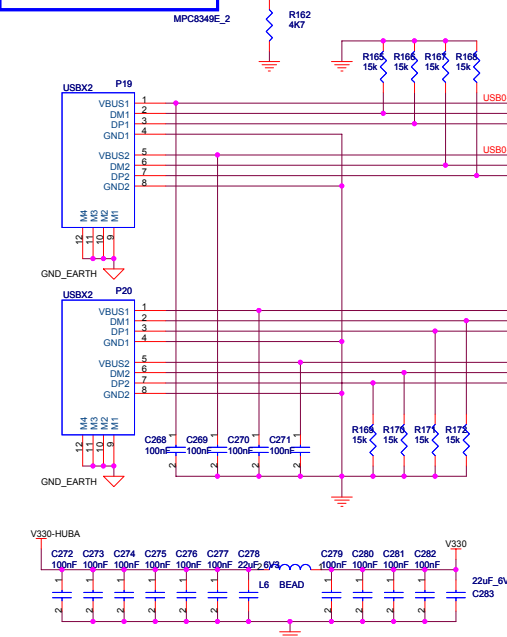
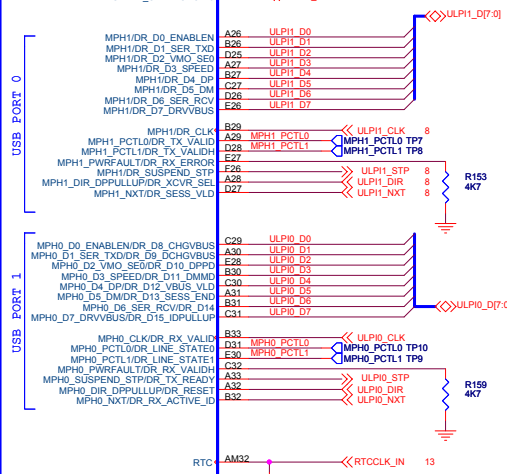
TOP View of SATA Connector



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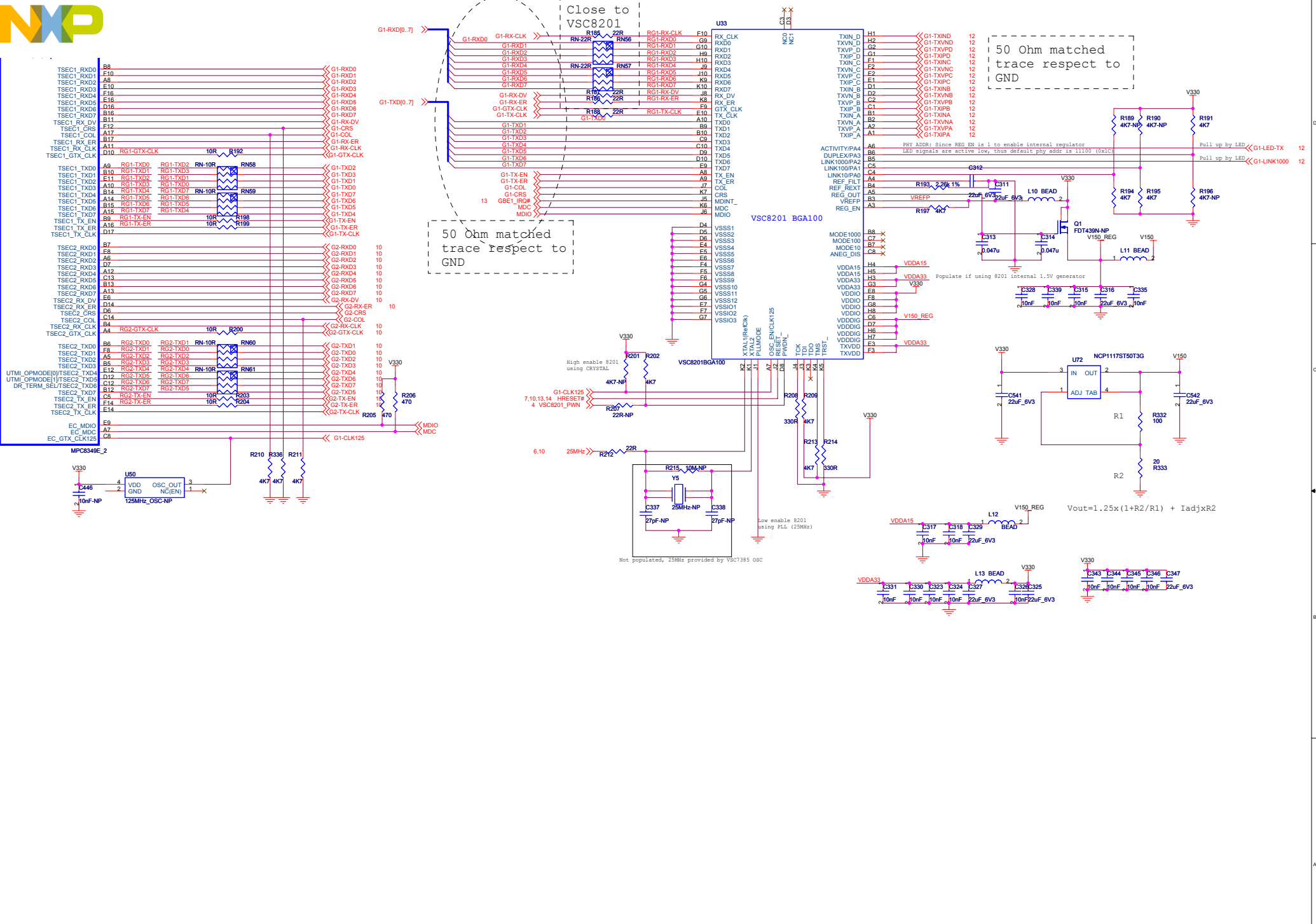


ULPI USB Port 0 (Host)



Either HRESET# or VBUS drops would give a reset to the USB Hub

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ULPI USB Port 0 (Hub x 4)		
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50 Ohm matched trace respect to GND

50 Ohm matched trace respect to GND

Pull up by LED << G1-LED-TX << G1-LINK1000

Populate if using 8201 internal 1.5V generator

$$V_{out} = 1.25x(1 + R2/R1) + I_{adj} \times R2$$

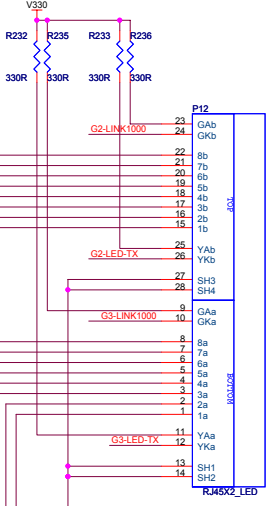
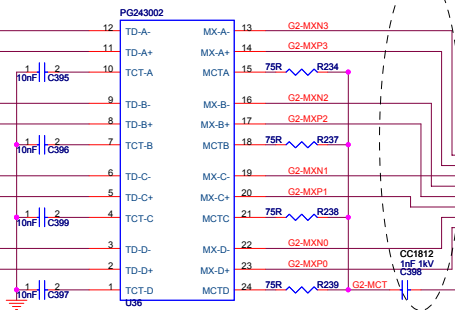
Not populated, 25MHz provided by VSC7385 OSC

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U35E
VSC7385_SparX-G5

P0_D3N	A21	G2-MDI3N
P0_D3P	B21	G2-MDI3P
P0_D2N	A20	G2-MDI2N
P0_D2P	B20	G2-MDI2P
P0_D1N	A19	G2-MDI1N
P0_D1P	B19	G2-MDI1P
P0_D0N	A18	G2-MDI0N
P0_D0P	B18	G2-MDI0P
P1_D3N	A17	G3-MDI3N
P1_D3P	B17	G3-MDI3P
P1_D2N	A16	G3-MDI2N
P1_D2P	B16	G3-MDI2P
P1_D1N	A15	G3-MDI1N
P1_D1P	B15	G3-MDI1P
P1_D0N	A14	G3-MDI0N
P1_D0P	B14	G3-MDI0P

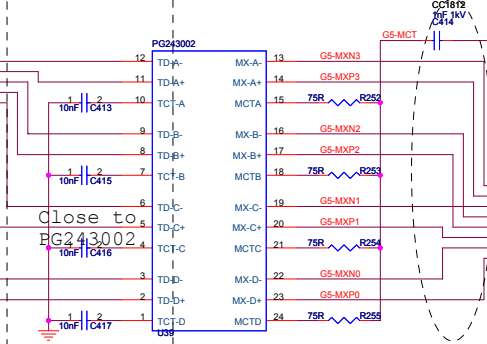
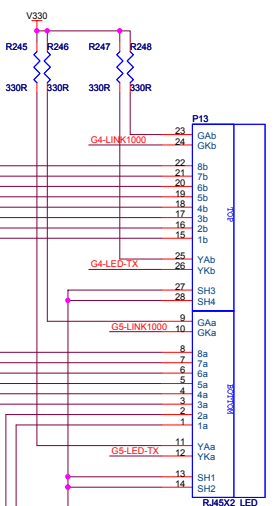
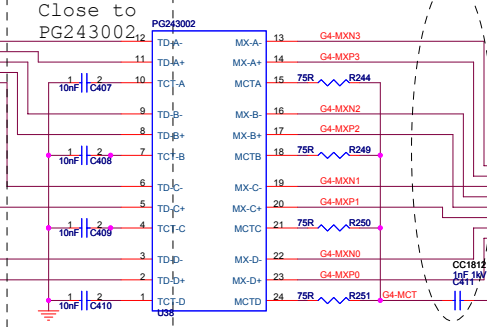


U35L
VSC7385_SparX-G5

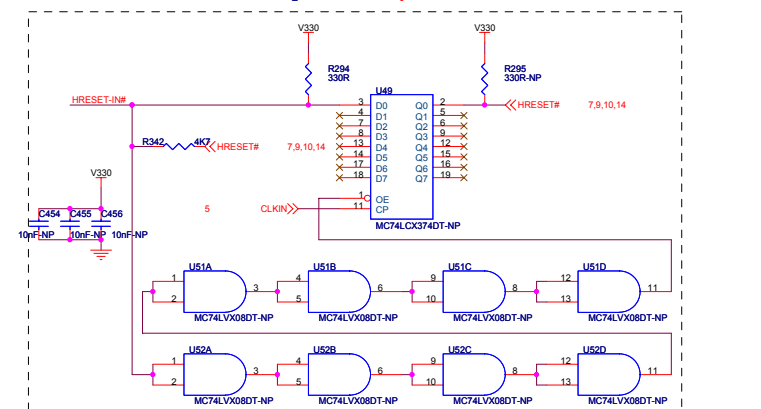
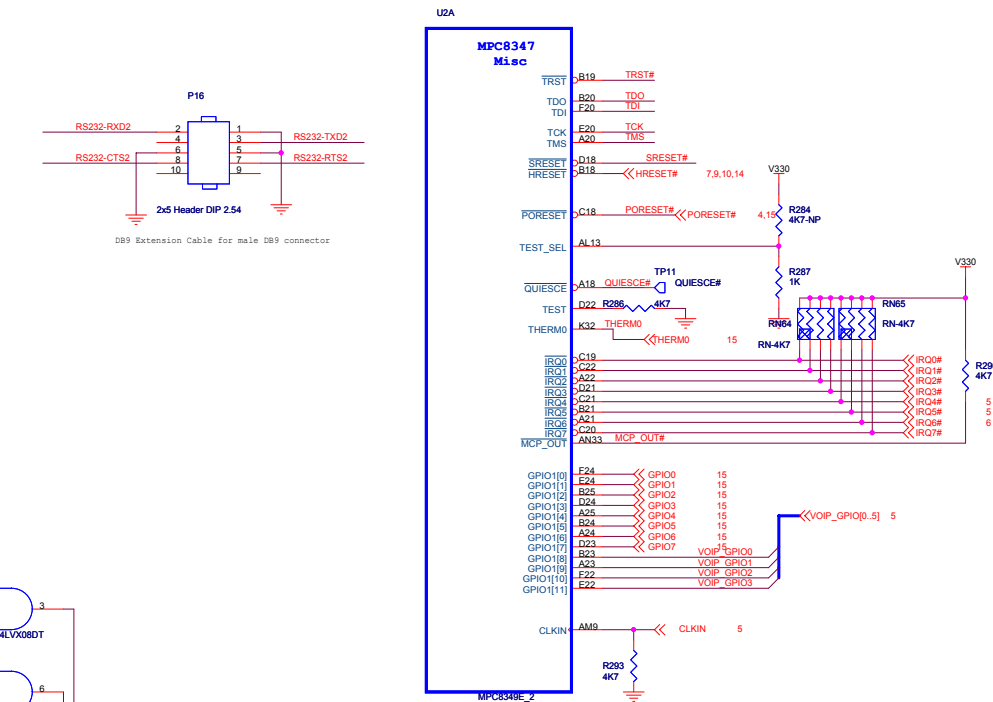
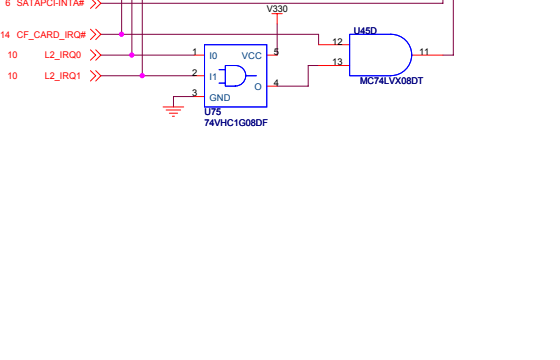
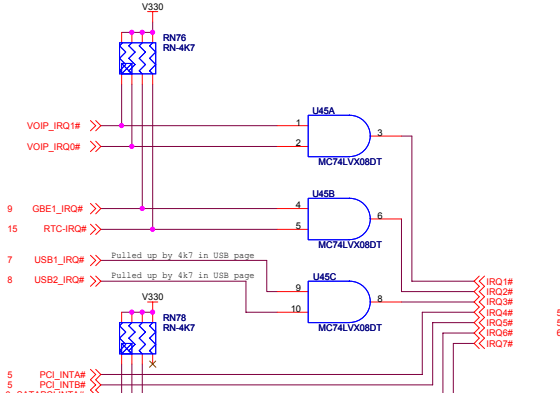
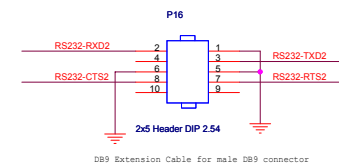
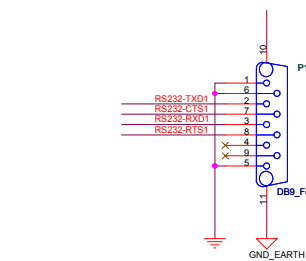
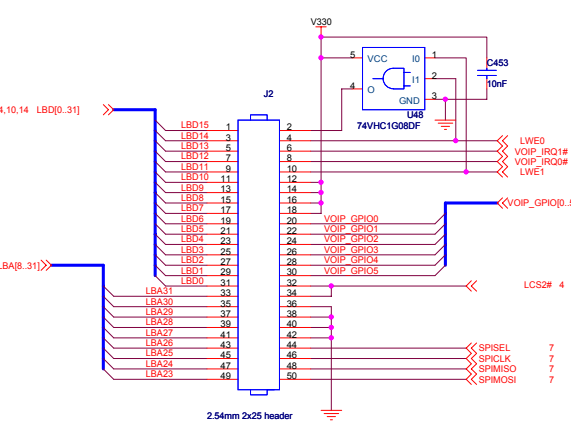
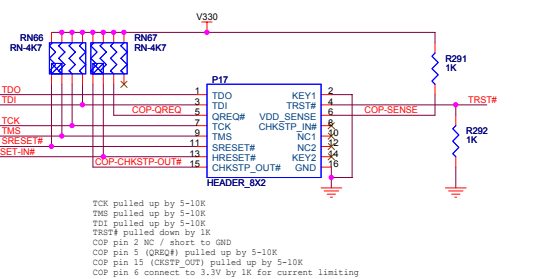
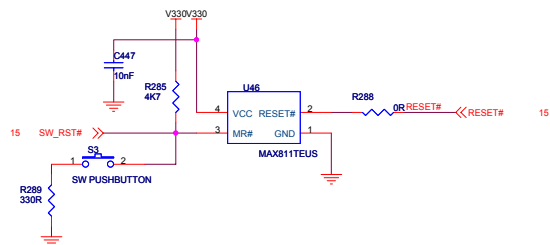
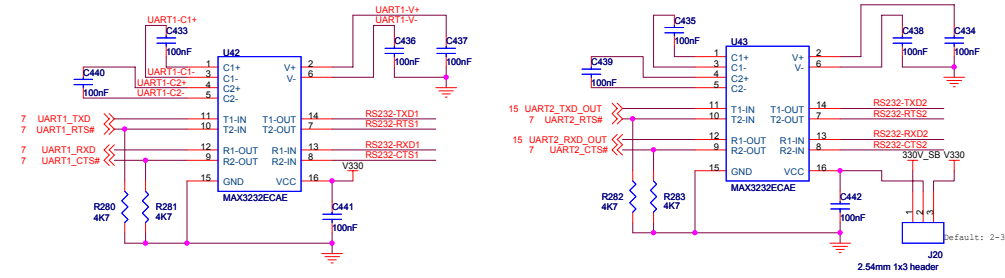
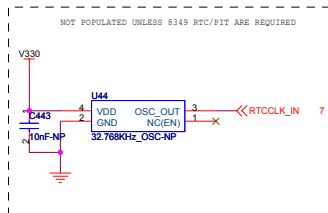
G2-LINK1000 E20	LED0_0SD	LED4_0	J1	G6-LINK1000	12
G2-LED-TX E22	LED0_VSCK	LED4_1	H3	G6-LED-TX	G6-LED-TX
TP53 E21	LED0_2	LED4_2	H2	TP51	
TP54 E20	LED0_3	LED4_3	H1	TP52	
G3-LINK1000 G22	LED1_0	LED3_3	J2	G5-LINK1000	
G3-LED-TX G21	LED1_1	LED3_2	J3	G5-LED-TX	
TP55 E20	LED1_2	LED3_1	K3	TP48	
TP56 E22	LED1_3	LED3_0	K2	TP49	
G4-LINK1000 H21	LED2_0	LED2_0			
G4-LED-TX H20	LED2_1	LED2_1			
TP57 E21	LED2_2	LED2_2			
TP58 E21	LED2_3	LED2_3			

U35F
VSC7385_SparX-G5

P2_D3N	A13	G4-MDI3N
P2_D3P	B13	G4-MDI3P
P2_D2N	A12	G4-MDI2N
P2_D2P	B12	G4-MDI2P
P2_D1N	A11	G4-MDI1N
P2_D1P	B11	G4-MDI1P
P2_D0N	A10	G4-MDI0N
P2_D0P	B10	G4-MDI0P
P3_D3N	A9	G5-MDI3N
P3_D3P	B9	G5-MDI3P
P3_D2N	A8	G5-MDI2N
P3_D2P	B8	G5-MDI2P
P3_D1N	A7	G5-MDI1N
P3_D1P	B7	G5-MDI1P
P3_D0N	A6	G5-MDI0N
P3_D0P	B6	G5-MDI0P

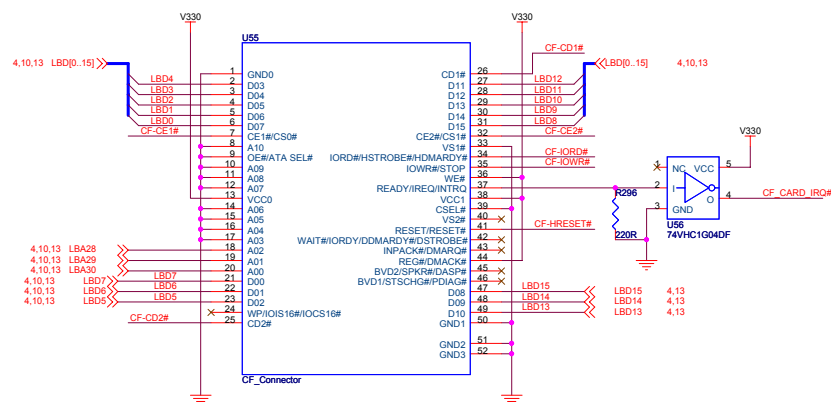


Title			GBE Transformer		
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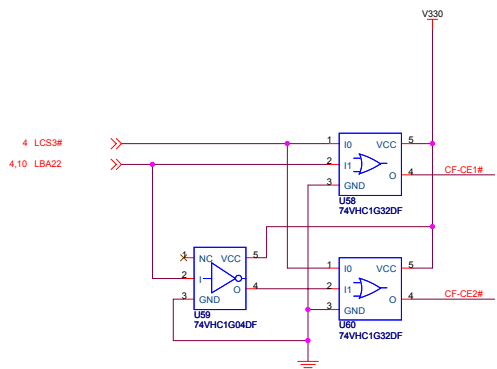
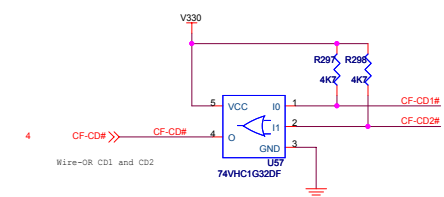
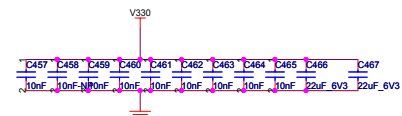
885871 Errata in Rev 1.0 silicon
 Delay >1: PCI CLKIN (chosen >30ns delay (33MHz))
 Remove all parts in this circuit and rename COP_HRESET-IN# to HRESET# after silicon fixed.

Title		
RTC,CLK,RST,RS232,COP		
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7,8,10,13 HRESET# >>> CF-HRESET#
 13 CF_CARD_IRQ# >>> CF_CARD_IRQ#
 4 LGPL0 >>> CF-IORD#
 4 LGPL1 >>> CF-IOWR#

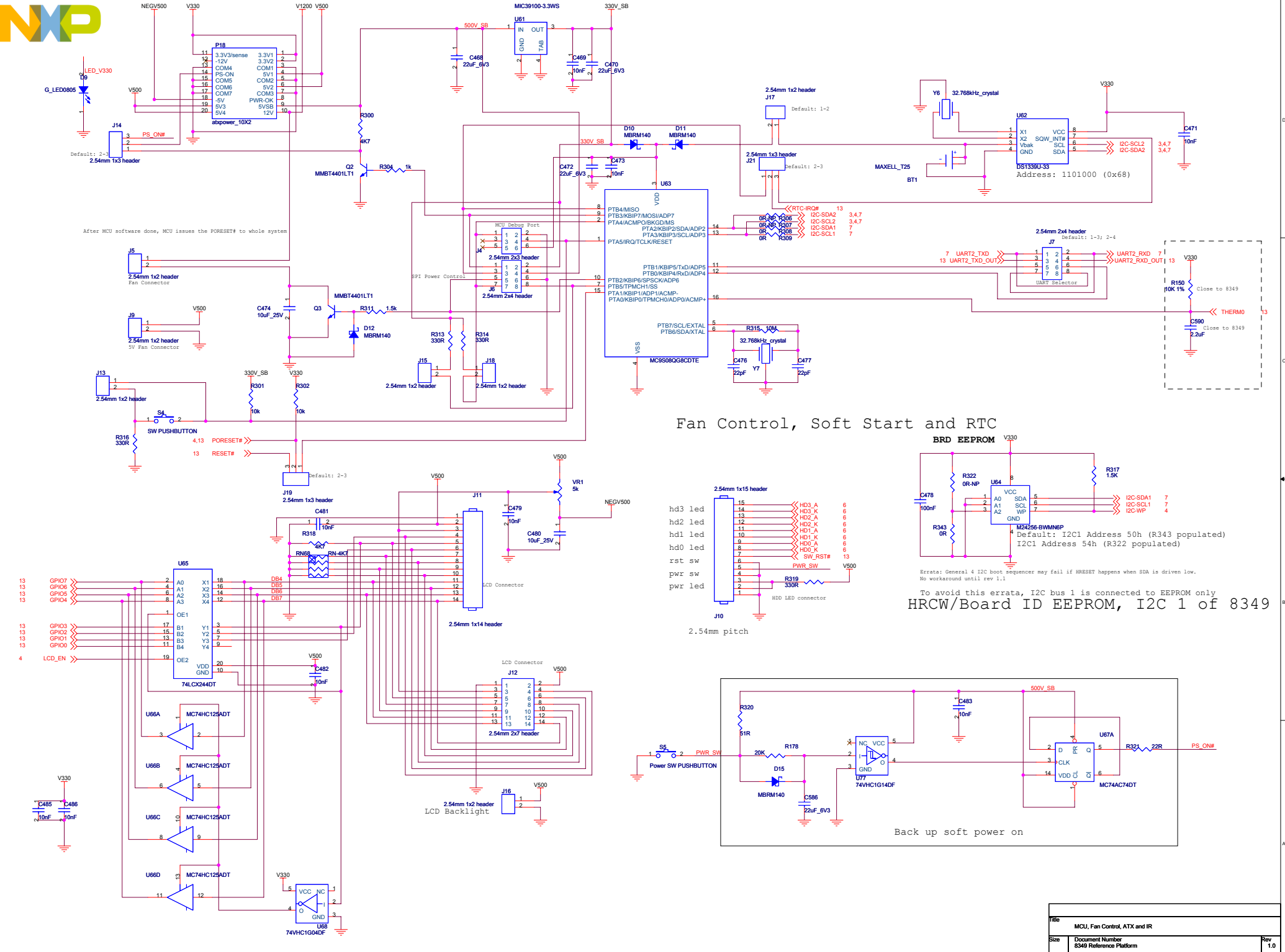
CF in True IDE Mode
 83xx
 =====
 LBCS3# CE1#
 LBD[7:0] D[0:7]
 LBD[15:8] D[8:15]
 LBA[30..28] A[0..2]
 VCC REG#
 GND WE#
 IRQ7# ATA_SEL#/OE#
 LBGPL0 CF_CARD_IRQ#
 LBGPL1 IOWR#



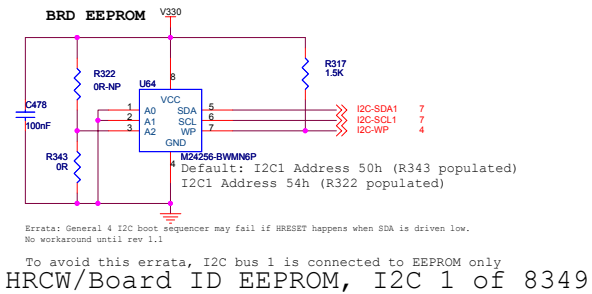
CE2# CE1# Addr. Read (IORD# = L) Write (IOWR# = L)

```

=====
1 0 0xn000 Data Register (16 bit) Data Register (16 bit)
1 0 0xn002 Error Register Feature Register
1 0 0xn004 Sector Count Register Sector Count Register
1 0 0xn006 Sector Number Register Sector Number Register
1 0 0xn008 Cylinder Low Register Cylinder Low Register
1 0 0xn00a Cylinder High Register Cylinder High Register
1 0 0xn00c Drive Head Register Drive Head Register
1 0 0xn00e Status Register Command Register
0 1 0xn020c Alt. Status Register Device Control Register
0 1 0xn020e Drive Address Register Reserved
  
```

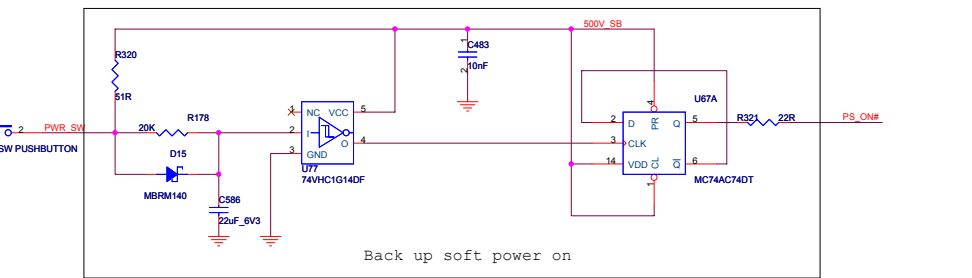
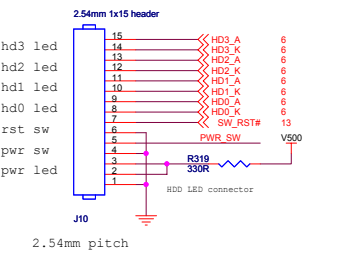


Fan Control, Soft Start and RTC

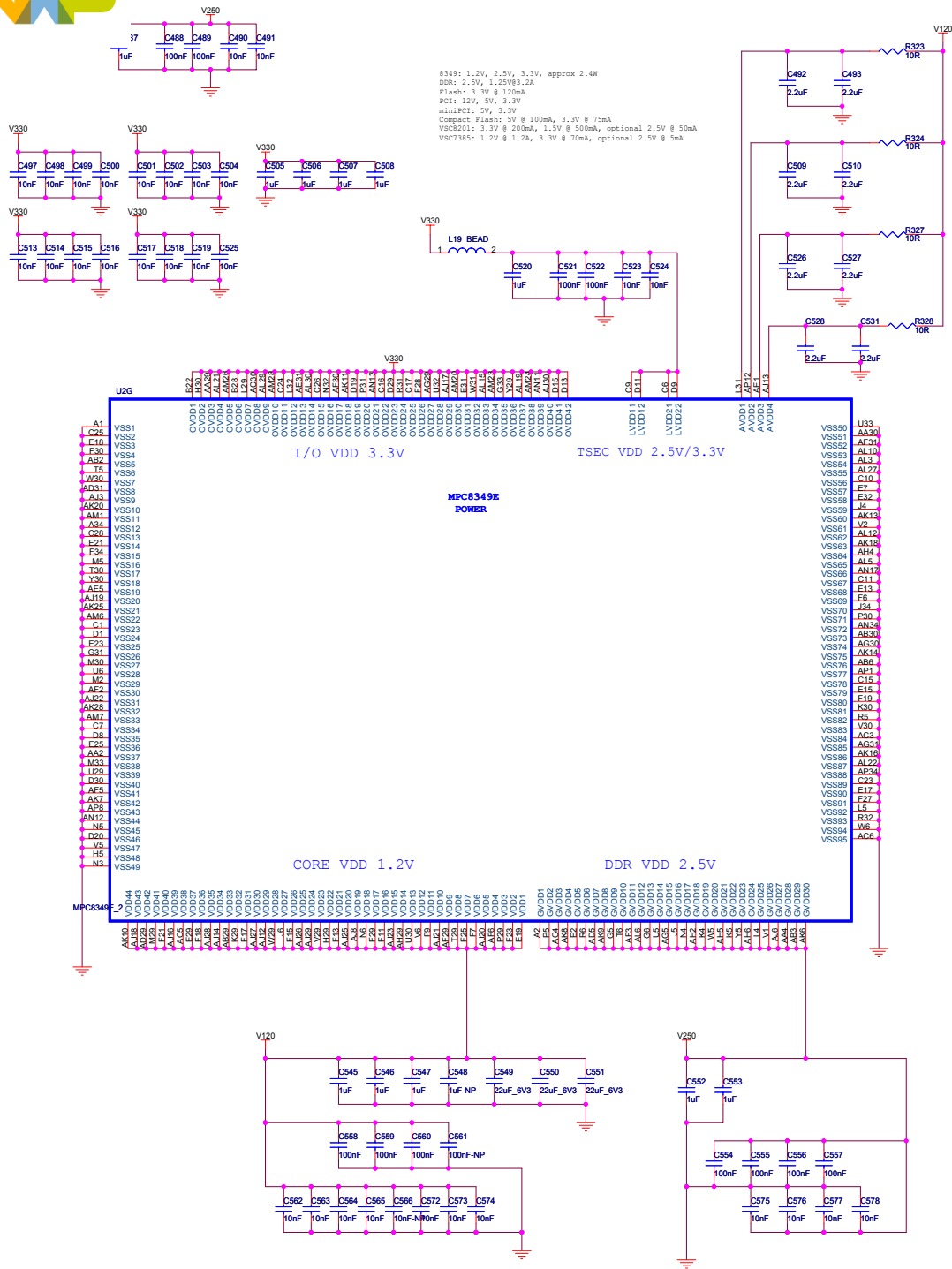


Errata: General 4 I2C boot sequencer may fail if HRESET happens when SDA is driven low. No workaround until rev 1.1.

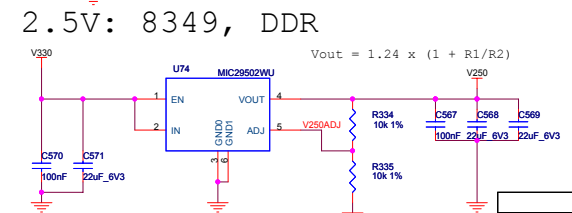
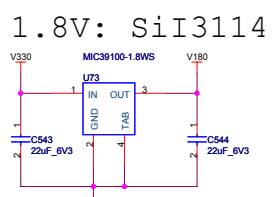
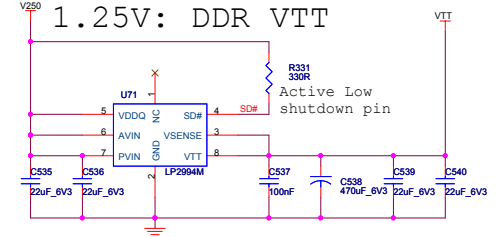
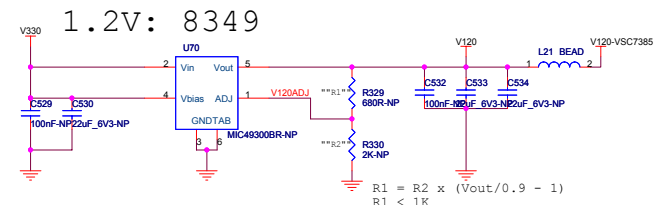
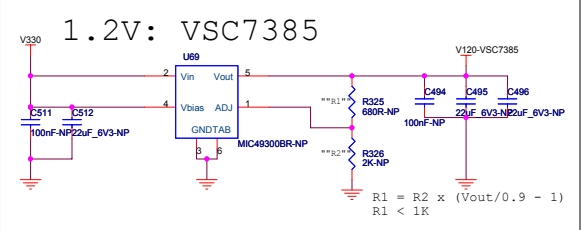
To avoid this errata, I2C bus 1 is connected to EEPROM only HRCW/Board ID EEPROM, I2C 1 of 8349



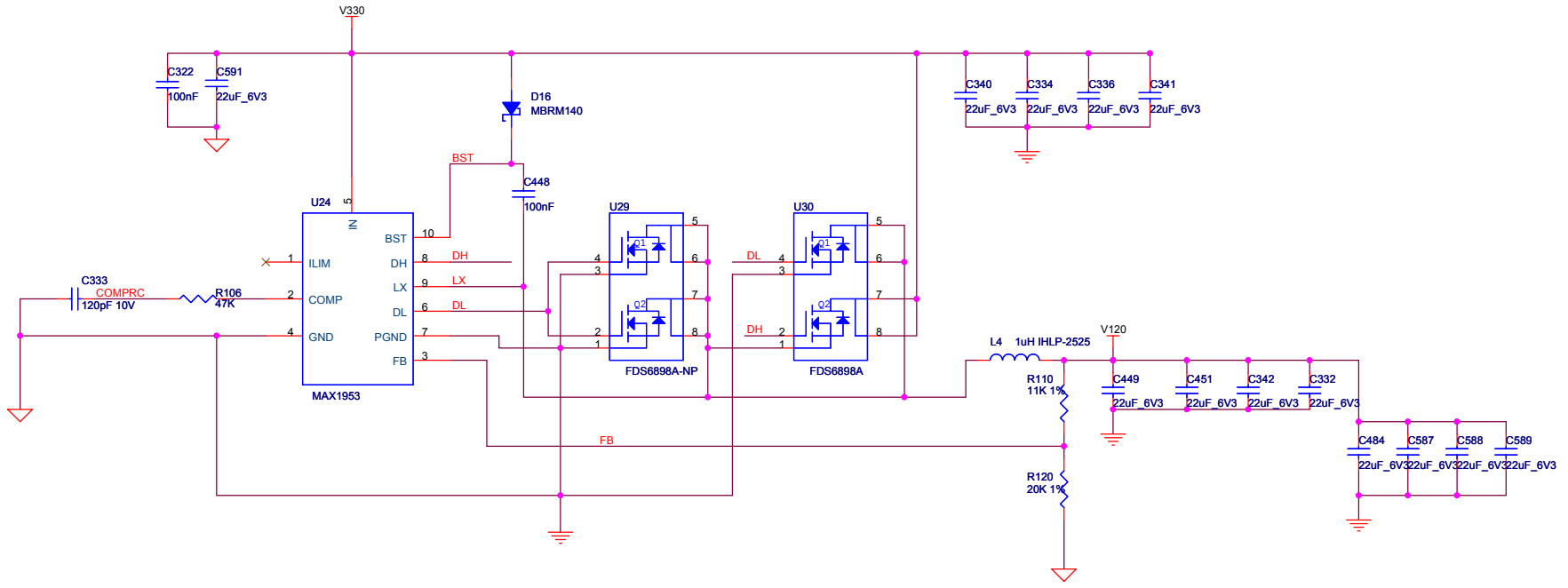
Title		
MCU, Fan Control, ATX and IR		
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Since 8349 1.2V power consumption is not finalized, additional regulator is place on board for VSC7385
 Not populated if 8349+7385 < 3.0A
 VSC7385 1.2V @ 1.2A



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Power		
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$$V_{out} = (R1/R2 + 1) \times 0.8$$

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Power		
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