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Revisions

Rev	Description	Date	Approved
A	Prototype Release	02/21/08	DK
A1	Change power solution, 5V wall input instead MC34717 to generate 3.3V and 1.8V	04/11/08	TQ
	Remove MCU socket (U5), put silicon onboard		
	Remove compression connectors (Previous Page12)		
	Tie J1.56 to AGND (VSSA)		
	Remove oscillator in Y1.		
	DNP SMA conn (J17), battery (BT1)		
	Update MCU pinout, Clkmod0 is pin 143 Clkmod1 is pin 144		
	Disconnect 48MHz crystal to CPLD		
	Add ferrite bead on MCU_VDDPLL		
	Change Y3 due to EOL		
	Remove J27 and connect test pin to GND via 0 ohm resistor		
	Remove J42		
	Remove J2 & J3; short Vdda & VRH, Vssa & VRL		
	Replace J29 to J32 with J51		
	Add USB BDM Block on P13		
	Change F1 from 5A to 2.6A		
	Change R112 & R113 to 33 ohm		
	Add necessary notes in schematics		
	Change R100 to 0 ohm		
	Add more protection diodes on wall power input		
	Update part reference for SW1-SW4		
	Use MCU_DDATA[0..3] for switches and PHY GPIO; Remove J14		
A2	Replace 210-30080 with 210-75439	04/21/08	TQ
	NC R108.1 to aviod dangling line.		
	Swap RN117		
	Change J41.1 to UART1_RTS_B		
A3	Swap MB_AD11 and MB_AD12	04/25/08	TQ
A4	Replace 470-30464 symbol with discrete resistors	04/29/08	TQ
	Replace U5 with new socket		
B	Re-sequence and release	05/06/08	TQ
C	Release for Rev C by A085	07/15/08	TQ
C1	Change 341-75288 to 341-75308	07/29/08	TQ
C2	Add 2 1UF caps on page2 Add 1V8 LED indicator	09/16/08	TQ
D	Add GND loops	09/18/08	TQ
D1	DNP JP1	10/09/08	TQ

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Microcontroller Solutions Group

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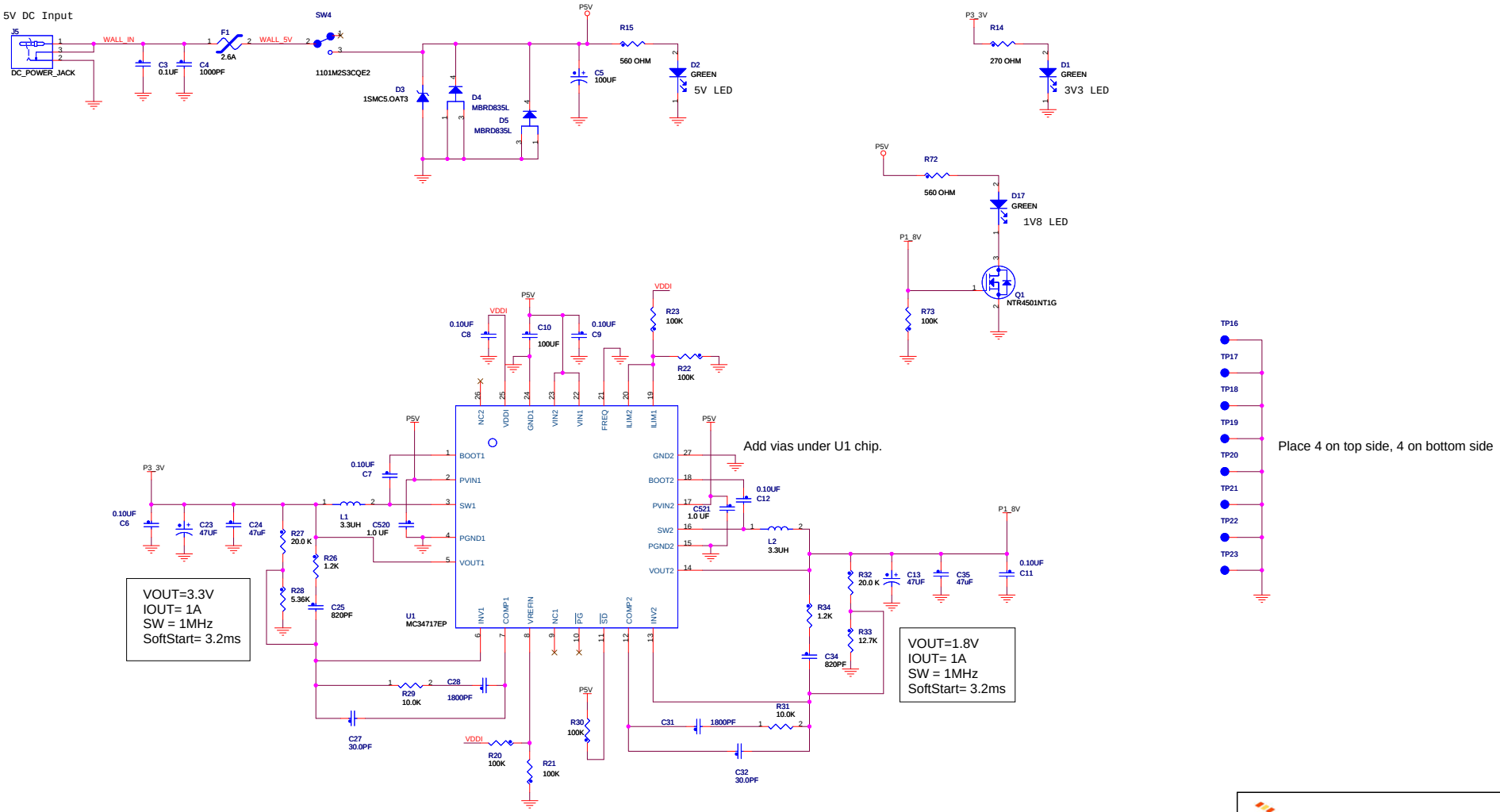
Austin, TX 78735-8598

ICAP Classification: FCP: FIUO: X PUBl:

Designer: Tanis Qiu	Drawing Title: **M52259EVB**	
Drawn by: Tanis Qiu	Page Title: **TITLE PAGE**	
Approved: Daniel Kruczek	Size C	Document Number PDF: SPF-24470 SOURCE: SCH-24470 Rev D1
	Date: Thursday, October 09, 2008	Sheet 1 of 13



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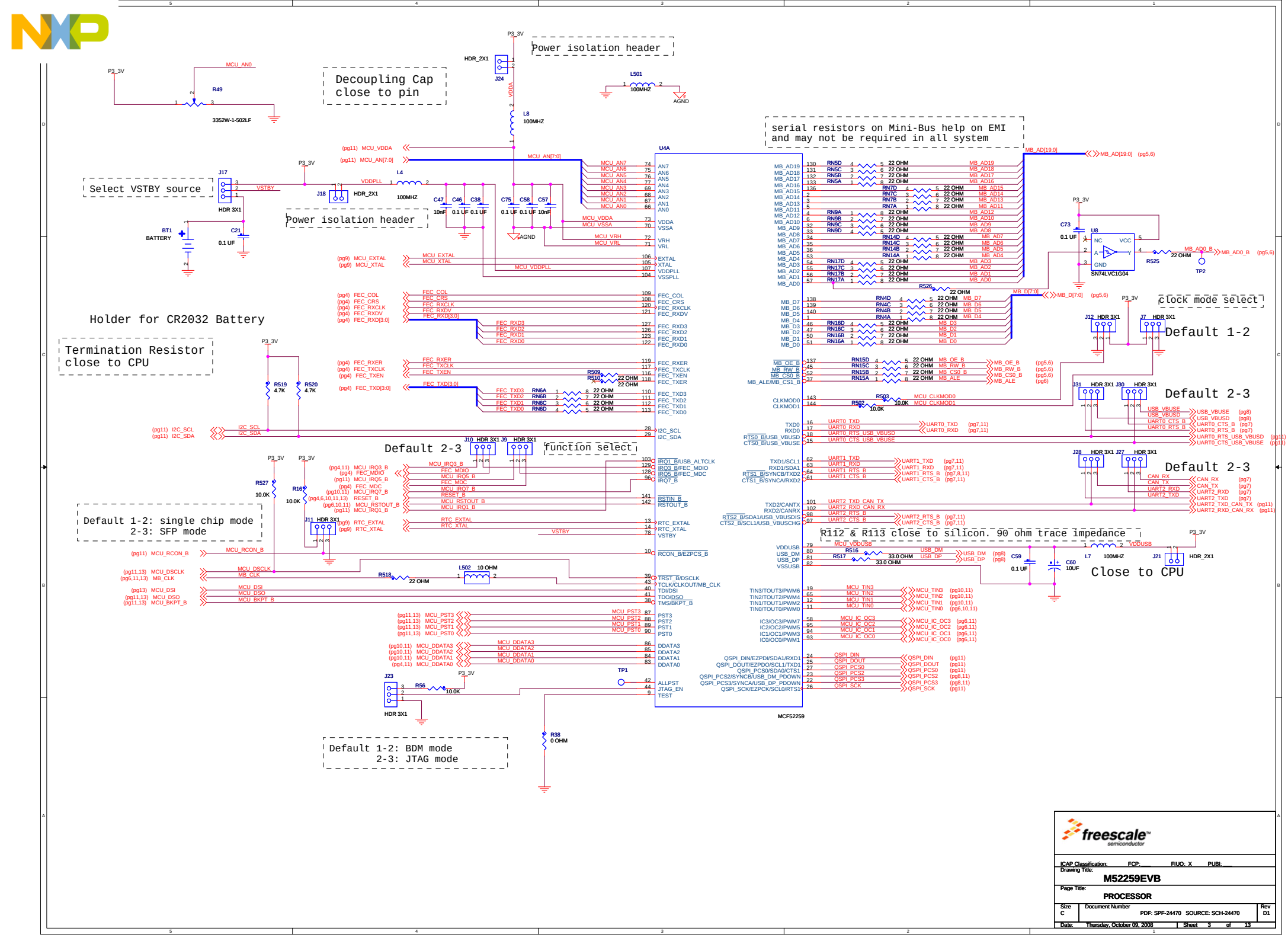
Power isolation header
Decoupling Cap close to pin
serial resistors on Mini-Bus help on EMI and may not be required in all system
Select VSTBY source
Power isolation header
Holder for CR2032 Battery
Termination Resistor close to CPU
clock mode select
Default 1-2
Default 2-3
Default 2-3
Default 2-3
function select
Default 1-2: single chip mode
2-3: SFP mode
R112 & R113 close to silicon. 90 ohm trace impedance
Close to CPU
Default 1-2: BDM mode
2-3: JTAG mode
U4A
MCF52259
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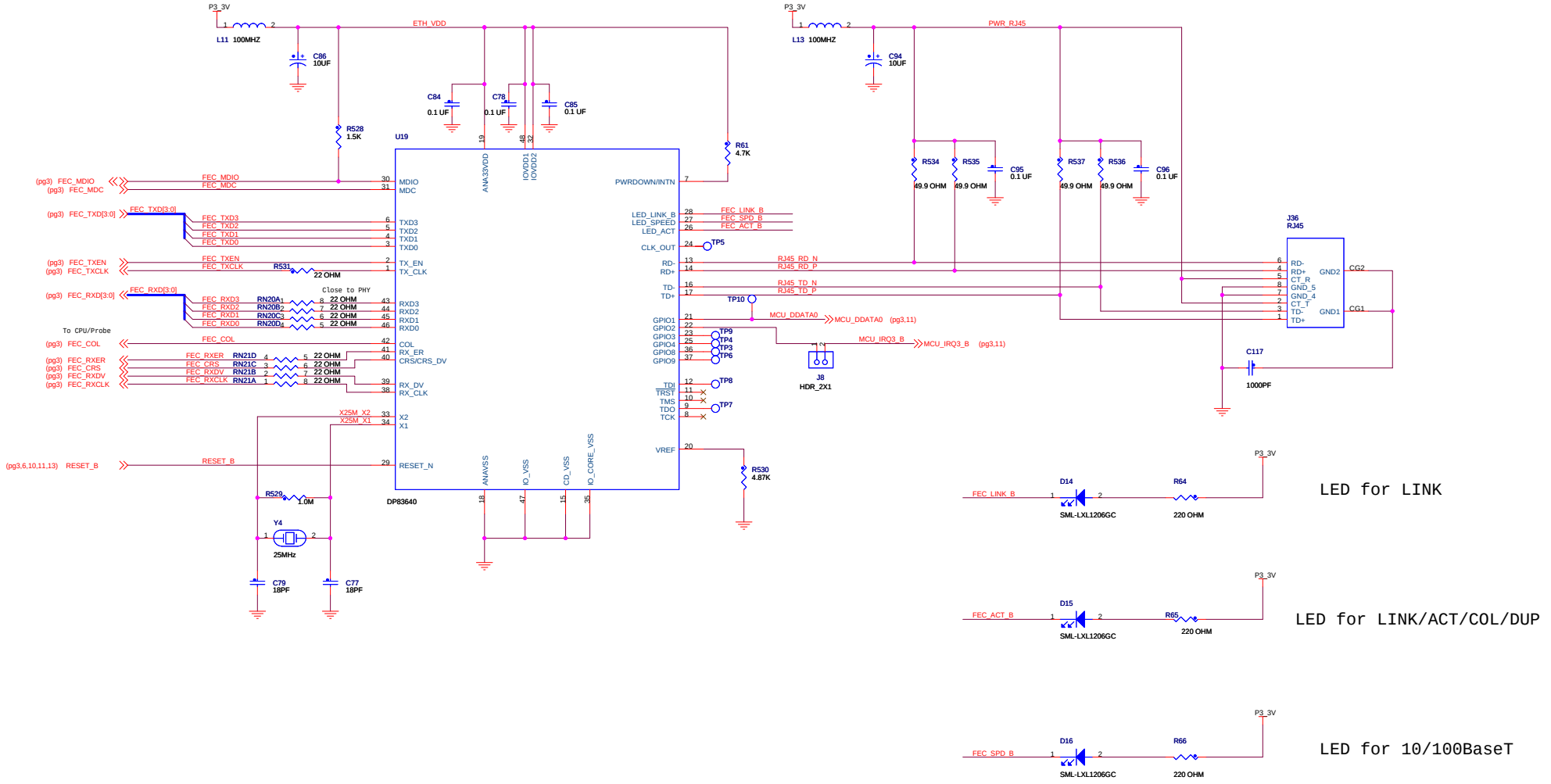

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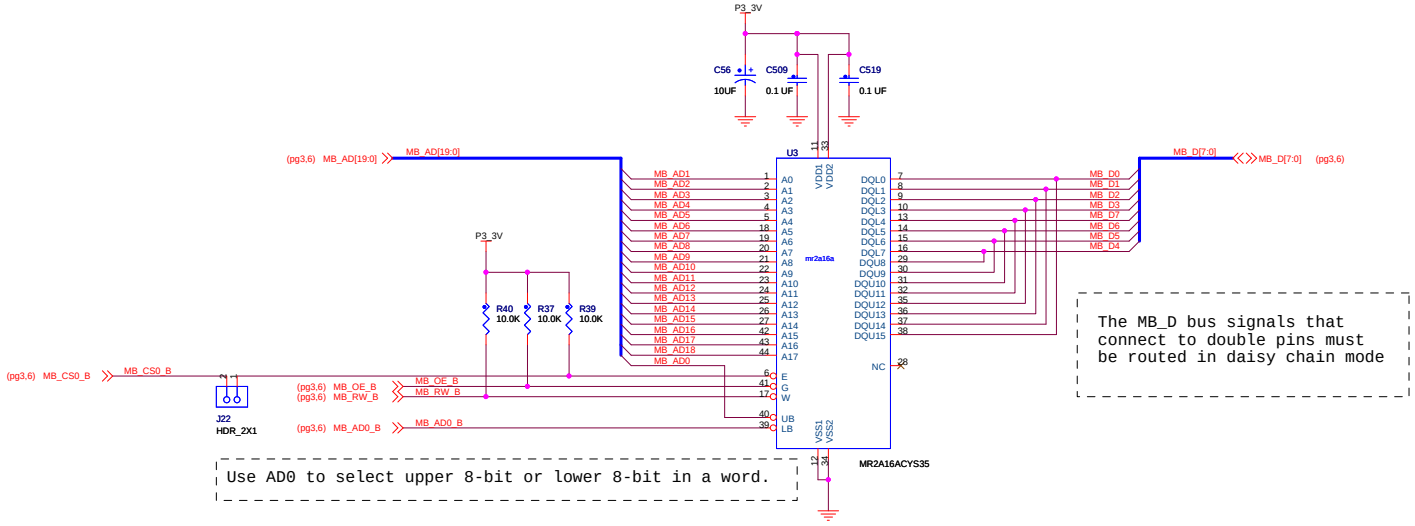

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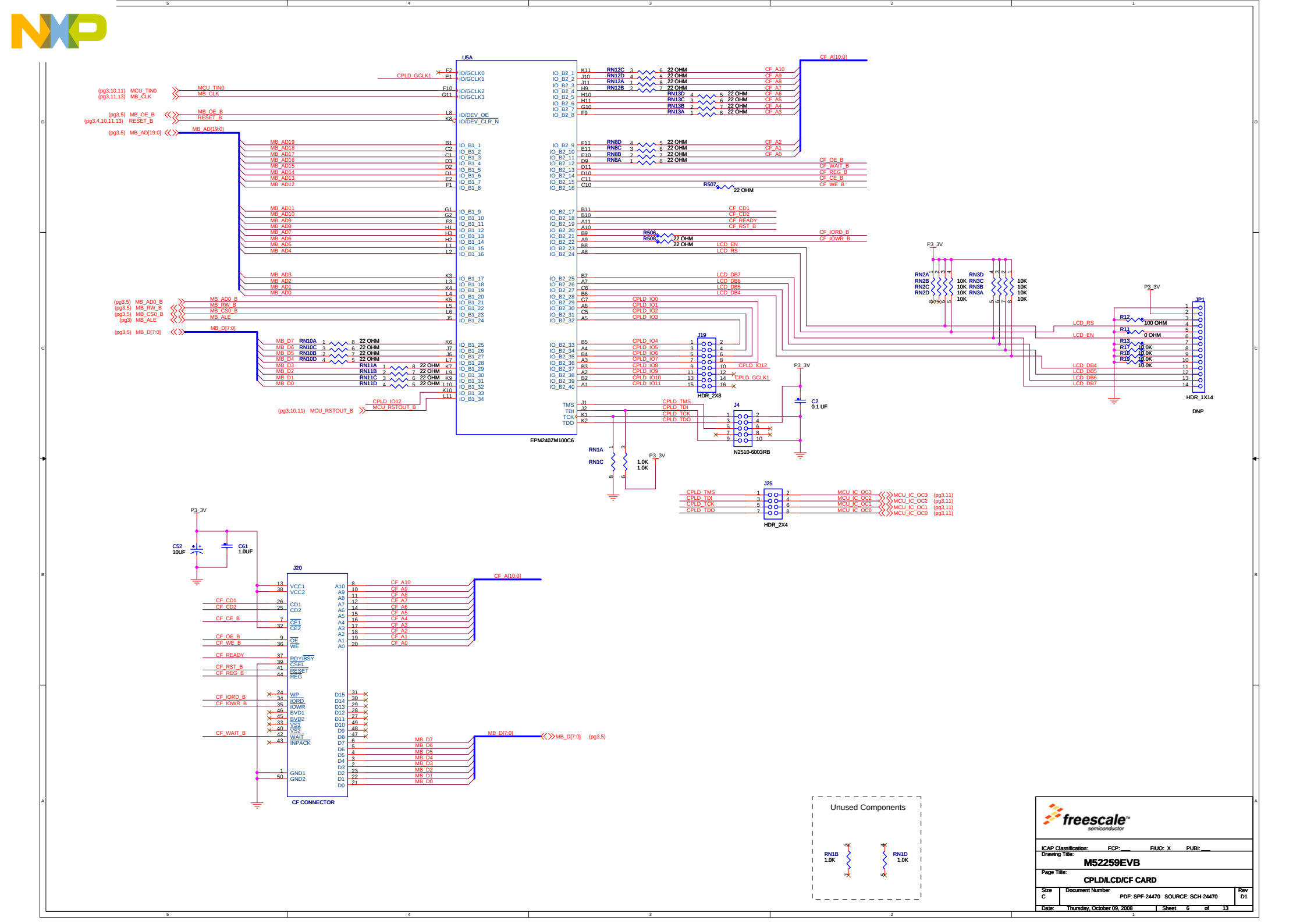

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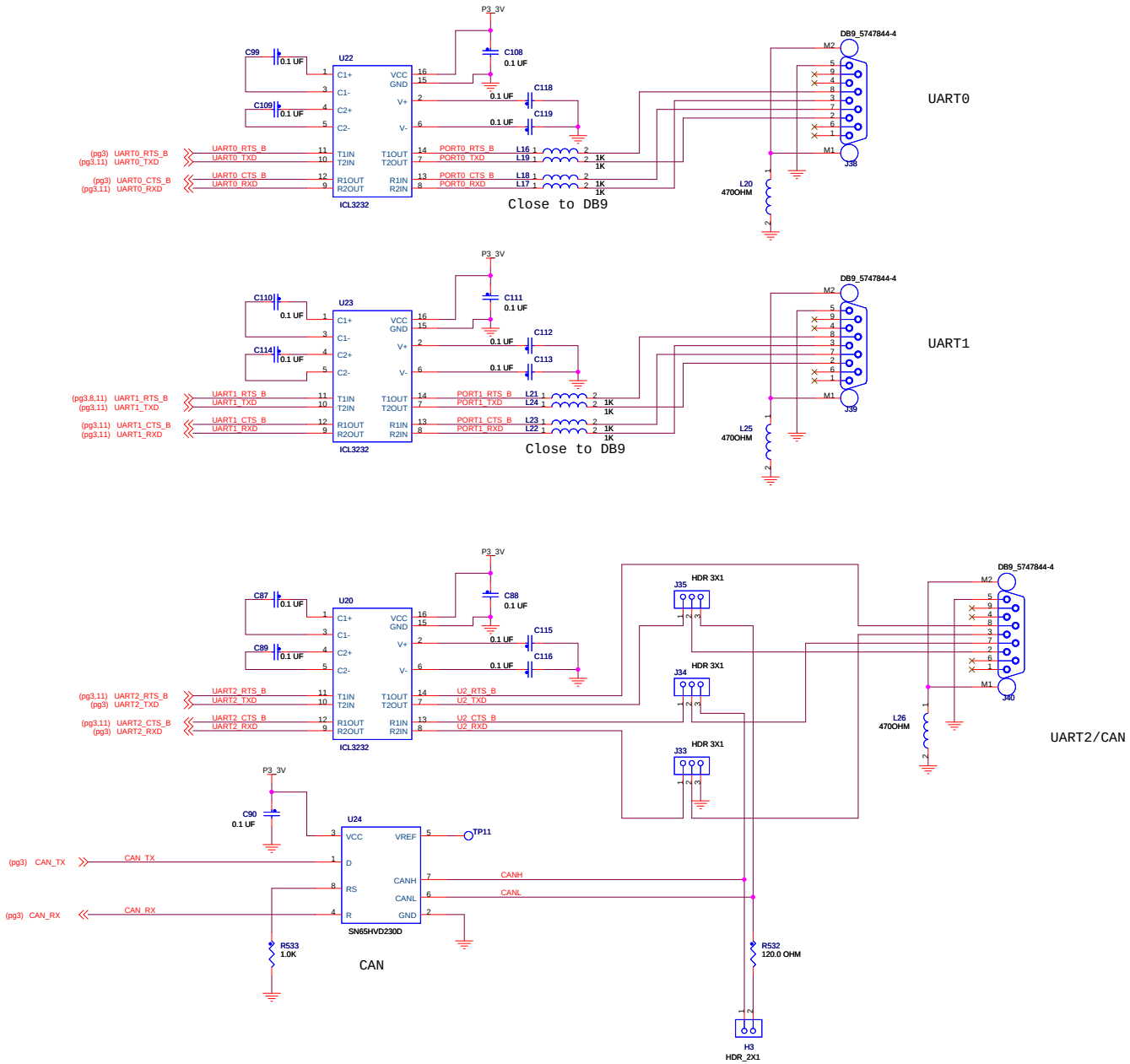

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Drawing Title: **M52259EVB**

Page Title: **SERIAL PORTS**

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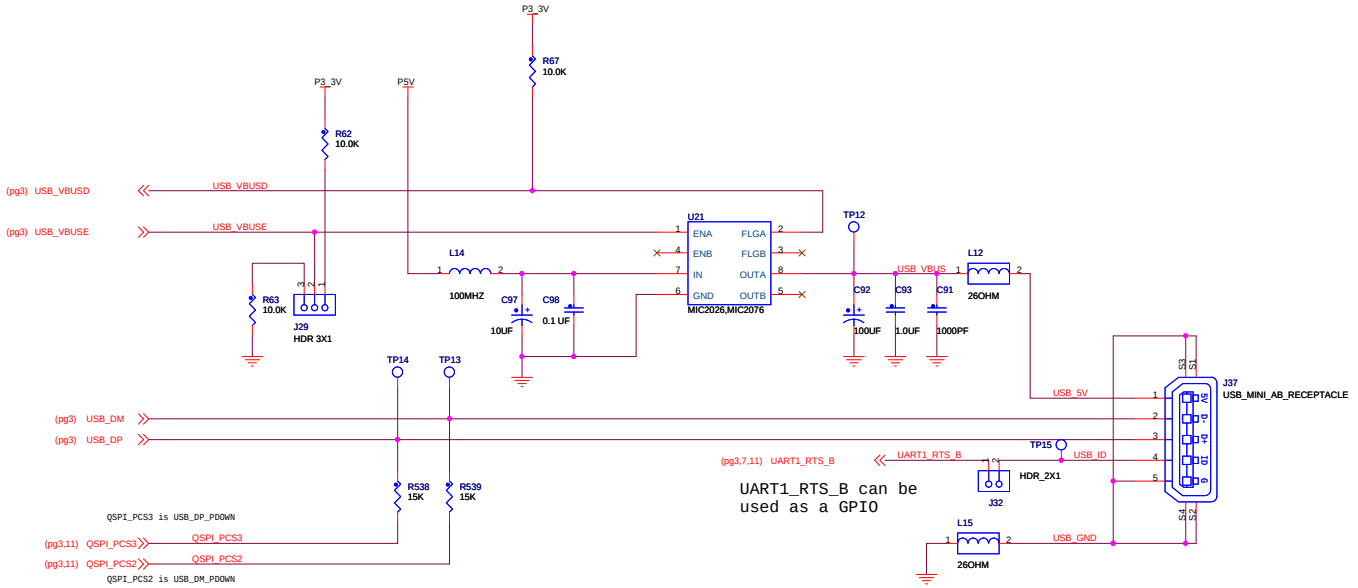

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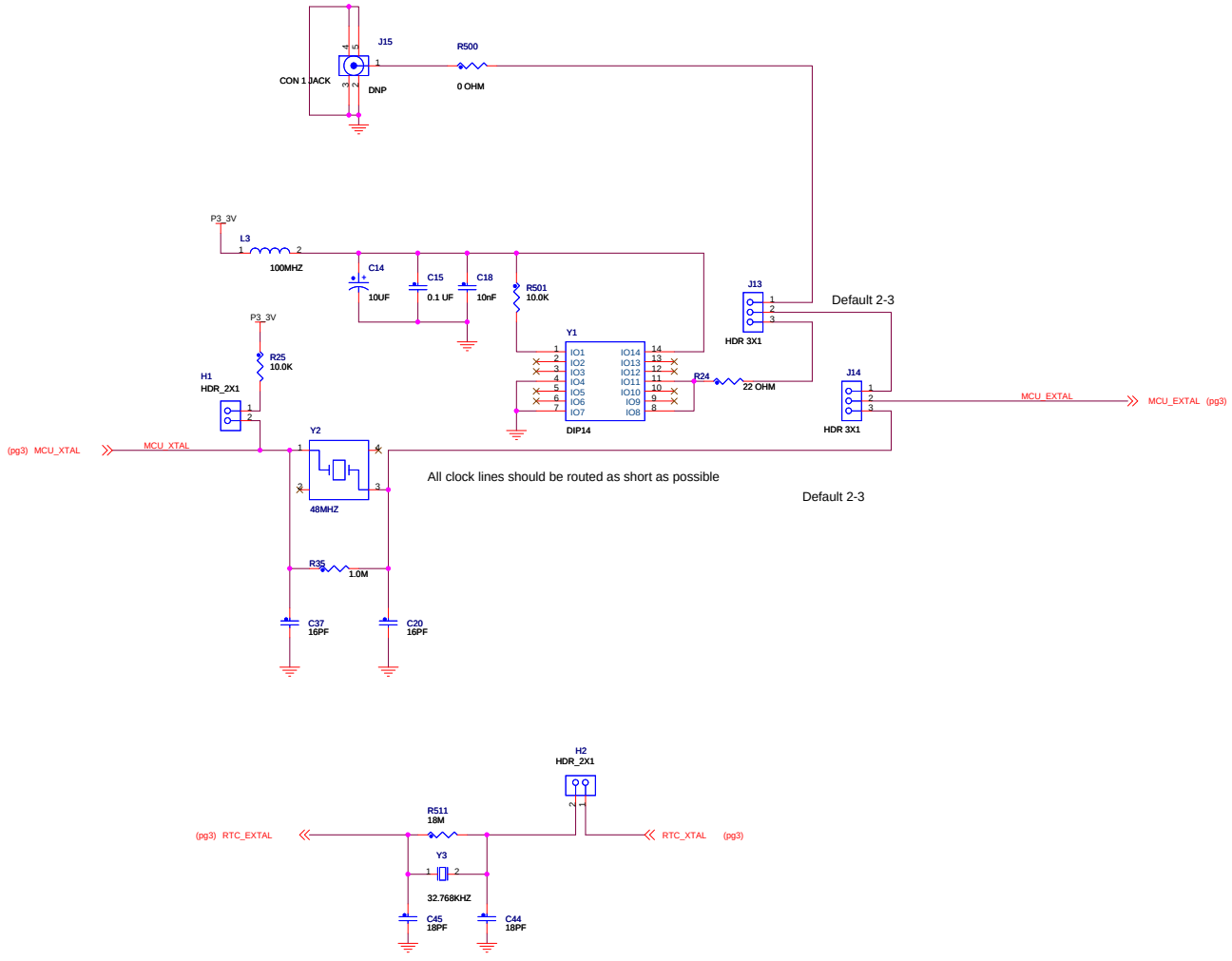

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Page Title:	CLOCKS		
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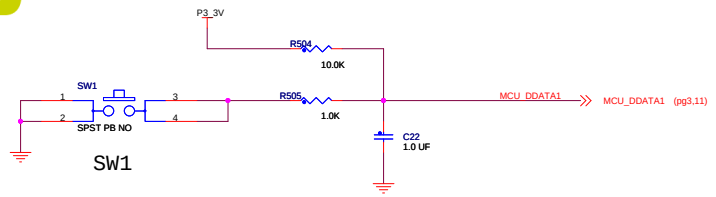

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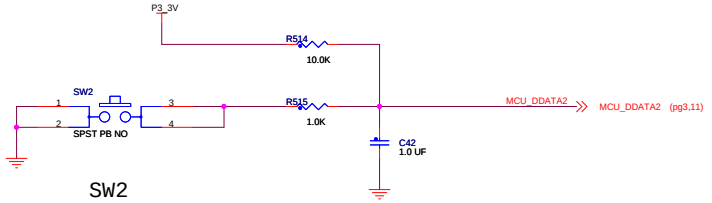

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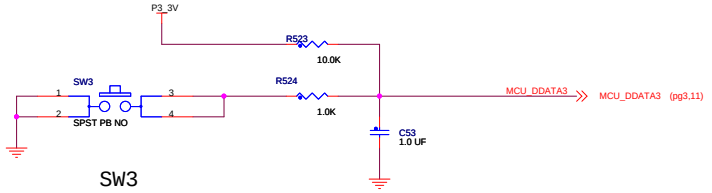

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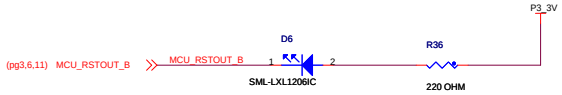

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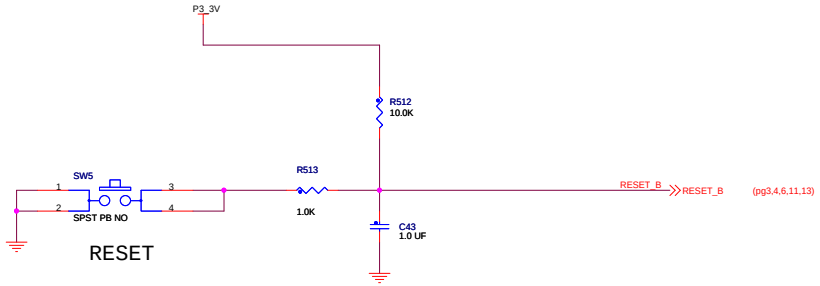

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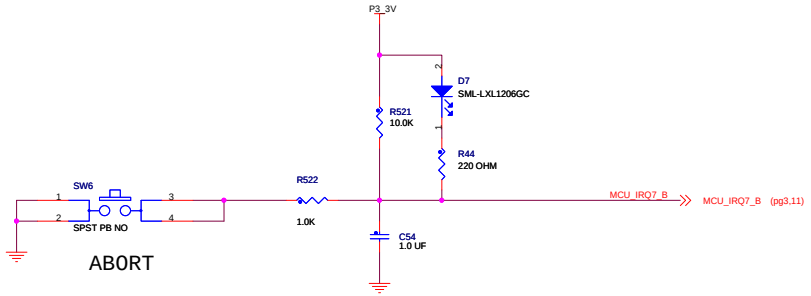

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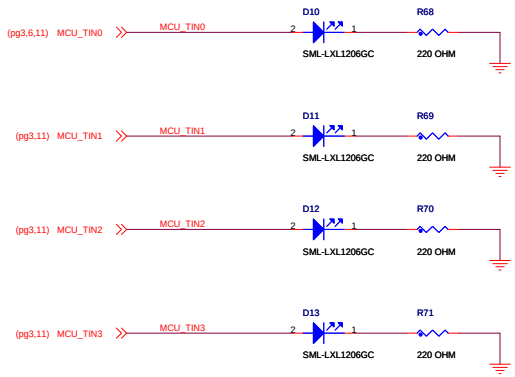

LED for DTIN[3:0]

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Page Title: **LED AND SWITCH**

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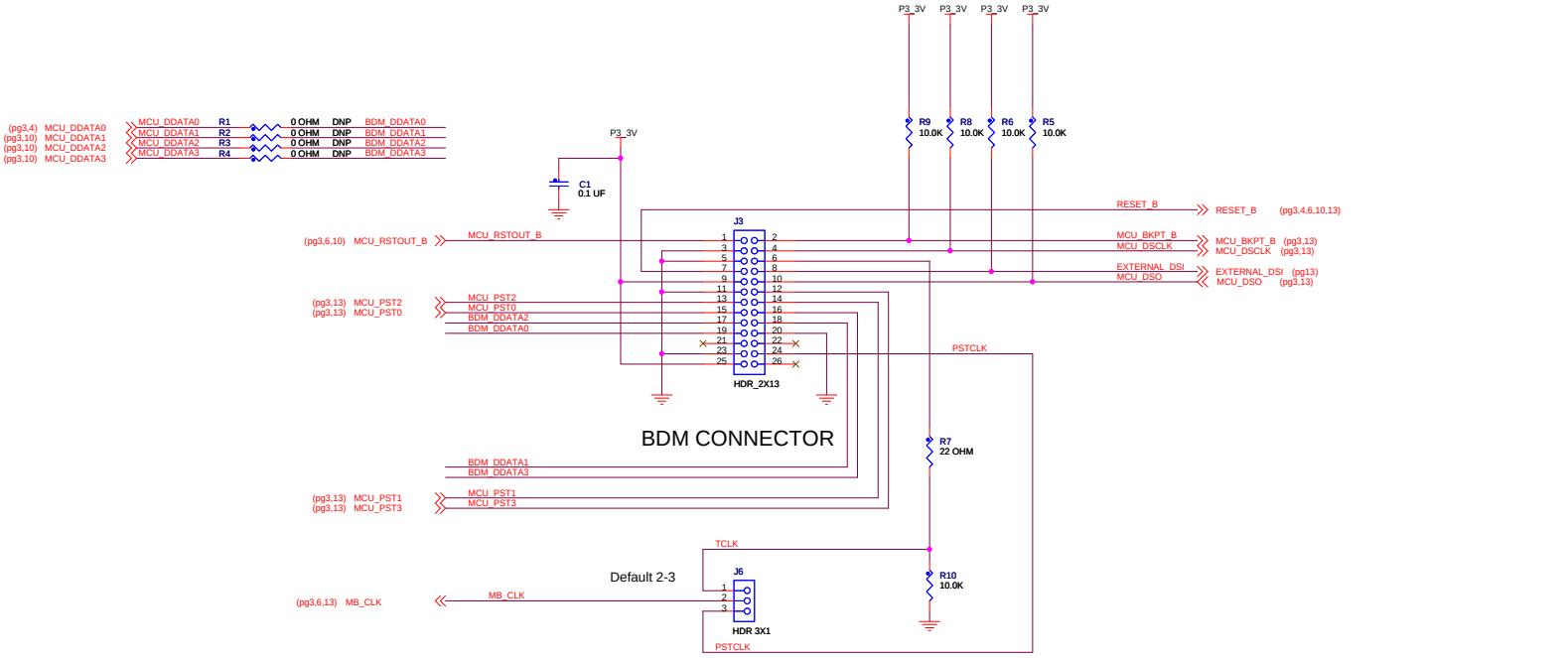

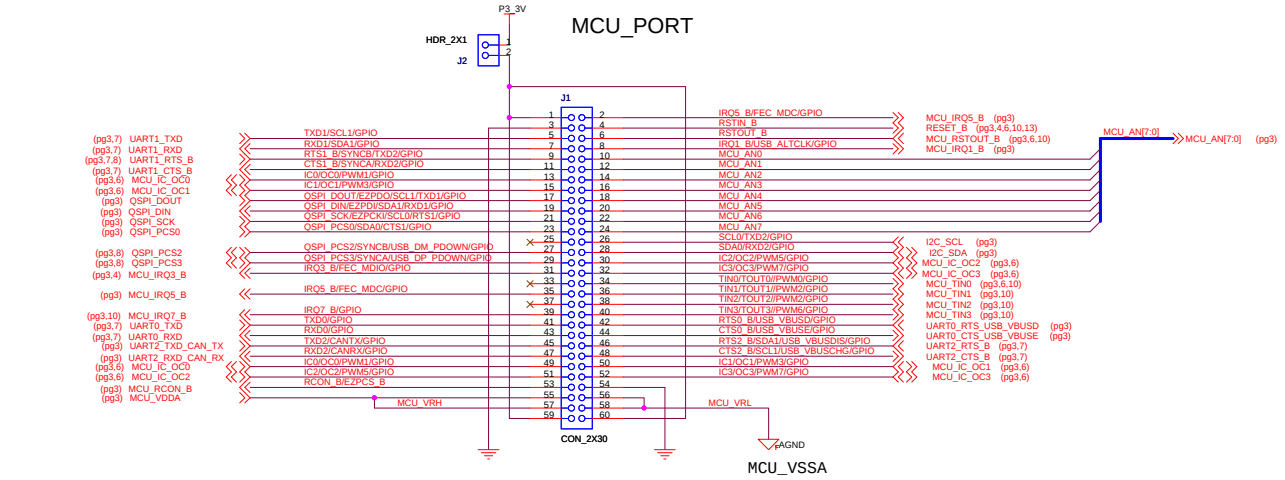

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Page Title: **BDM AND BREAKOUT CONNECTOR**

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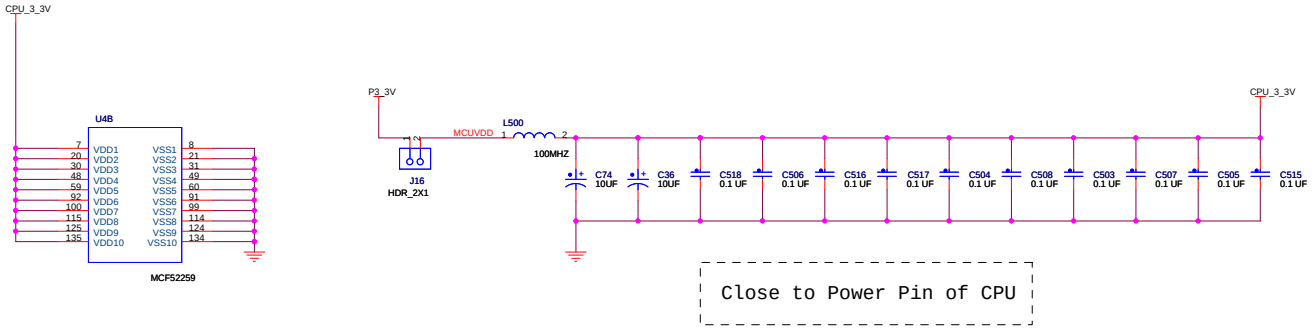

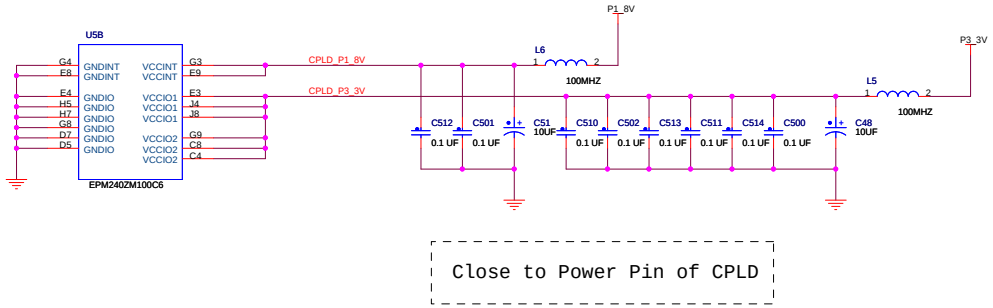

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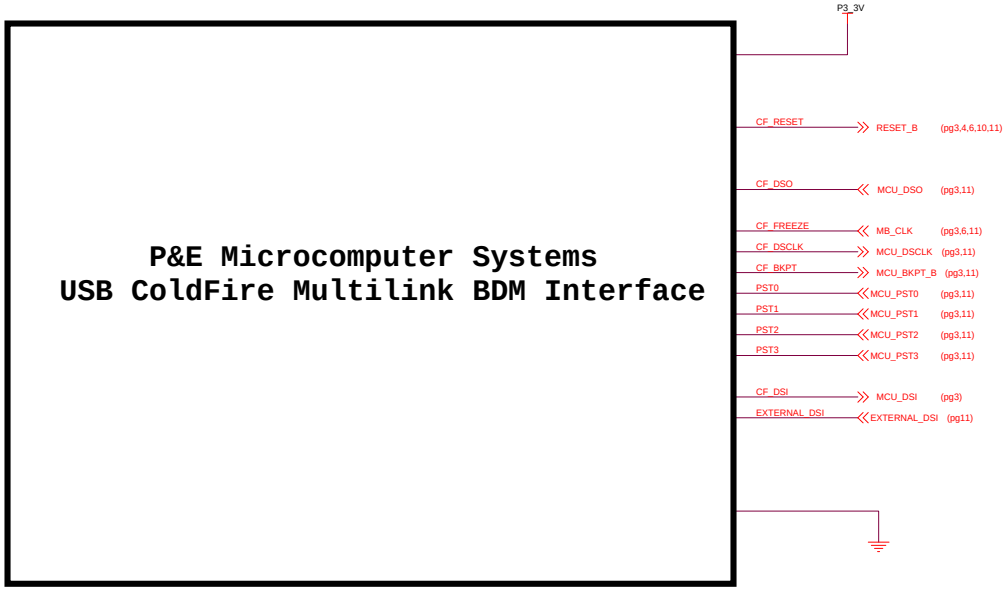

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Page Title: USB TO BDM BLOCK

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