

NOTES (UNLESS OTHERWISE SPECIFIED):

- THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-6012 CLASS 2 (LATEST REVISION).
- THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
- BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101D-26, 83 or 98  
T<sub>g</sub> - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.  
T<sub>d</sub> - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
- COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
- CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B'
- MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .007"/.005"
- PLATING FINISH: A. BOTH SIDES ENIG: TO MEET THE REQUIREMENTS OF IPC-4552 (LATEST REVISION).

8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.

9. SOLDERMASK - TO MEET THE REQUIREMENTS OF IPC-SM-840E (OR LATEST REVISION). GREEN COLOR, BOTH SIDES. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP. TYPE: LPI OR EQUIVALENT.  
A. LOCATION = +/- .002" OF PLATED PADS.  
B. DIAMETER OR SIZE = +/- .002 OF ORIGINAL DATA

10. SILKSCREEN - WHITE EPOXY OR ACRYLIC INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.

11. ELECTRICAL TEST - 100% IPCD356.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DFM CHECK MUST BE RUN ON BOARD DATA BEFORE BUILDING BOARDS. UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.

14. TEARDROPS MAY BE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.

15. TWO SOLDER SAMPLES TO BE PROVIDED.

16. SUPPLIER MARKINGS - ON SECONDARY SIDE ONLY, WHERE SHOWN. - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

17. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (Pb)

18. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

19. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM UNLESS OTHERWISE SPECIFIED.

20. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.

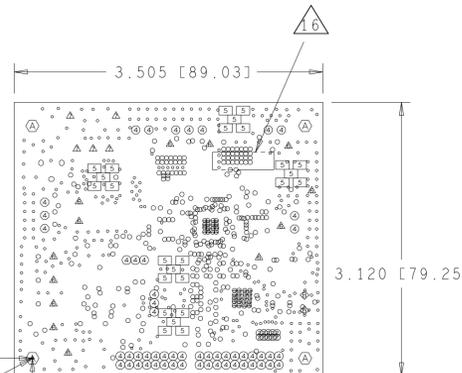
21. THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS. KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES.

22. THIS BOARD USES VIA-IN-PAD: SEE FAB\_VIAFILL.ART  
A. ALL VIAS USING X.1 DRILL SIZES ARE TO BE FILLED WITH NON-CONDUCTIVE VIA FILL. LACKWERKE-PETERS PP2795 OR EQUIVALENT AND MADE PLANAR TO THE PADS.  
B. OVERPLATE THE FILLED VIA AND APPLY FINISH METAL TREATMENT.  
C. DIMPLE OR PROTRUSION ON VIA-IN-PADS MUST BE NO GREATER THAN .001".

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	05-28-20	D.A
	B	ECO123369 Changes	07-17-20	D.A

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
1	10.0	+0.0/-10.0	PLATED	344
2	10.1	+0.0/-10.1	PLATED	36
3	12.0	+0.0/-12.0	PLATED	348
4	16.0	+2.0/-2.0	PLATED	3
5	28.0	+2.0/-2.0	PLATED	10
6	40.0	+3.0/-3.0	PLATED	42
7	48.0	+3.0/-3.0	PLATED	12
8	52.0	+3.0/-3.0	PLATED	25
9	63.0	+3.0/-3.0	PLATED	13
10	73.0	+3.0/-3.0	PLATED	5
11	126.0	+3.0/-3.0	PLATED	4
12	35.0	+2.0/-2.0	NON-PLATED	2
13	63.0x52.0	+3.0/-3.0	PLATED	2
14	63.0x52.0	+3.0/-3.0	PLATED	1

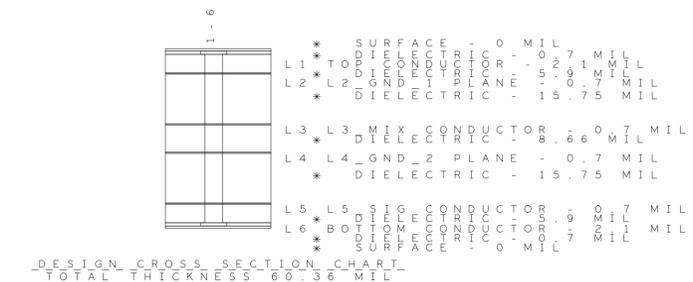
TOTAL HOLES: 847



PRIMARY DATUM GRID ORIGIN

DETAIL B  
IMPEDANCE REQUIREMENTS  
IMPEDANCE TOLERANCE IS 10%

LAYERS	SE		DIFF			REFERENCE LAYER
	TRACE WIDTH	IMPEDANCE	TRACE WIDTH	TRACE SPACING	IMPEDANCE	
L1 PS	9.00	50	7.00	6.00	90	2
L3 MIX	9.5	50				
L5 SIG	7.3	50				
L6 SS	9.00	50	7.00	6.00	90	4



BOARD THICKNESS TOLERANCE +/-10%

DETAIL A  
LAYER STACKUP  
SCALE: NONE

ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL MEET THE ROHS COMPLIANCE DELEGATED DIRECTIVE (EU) 2011/65 OF 21 MARCH 2011 AND THE ANNEX I TO DIRECTIVE 2011/65/EU. A CERTIFICATE OF COMPLIANCE IS REQUIRED UPON REQUEST.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:  
DECIMALS .XX .01 .03  
ANGLES 0-30° .XXX DEGS  
RMS ALL MACHINED SURFACES. BREAK ALL SHARP EDGES AND CORNERS. REMOVE BURRS. UNDERLINED DIM. NOT TO SCALE. THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

PART NO. 170-47345		NXP SEMICONDUCTORS	
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO NXP AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCEDURE OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP.		6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA	
APPROVALS		DATE	
DRAWN Guru {LnT}		07-17-20	
CHECKED Dafne .A		07-17-20	
DESIGN ENGINEER Varodha {LnT}		07-17-20	
SCALE 1/1	DO NOT SCALE DRAWING	SHEET 1 OF 2	

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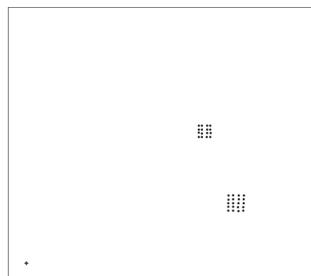
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	A	ORIGINAL RELEASE	05-28-20	D.A
	B	ECO123369 Changes	07-17-20	D.A

THIS FAB\_VIAFILL.ART SHOWS LOCATIONS OF VIA-IN-PAD TO BE FILLED.

FAB SUPPLIER: DISREGARD THIS PAGE IF VIA-IN-PAD DOESN'T APPLY OR NOT REQUIRED ON FAB.ART



- COMPANY PUBLIC
- COMPANY INTERNAL
- COMPANY CONFIDENTIAL

PART NO. 170-47345

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NXP SEMICONDUCTORS

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ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL MEET THE BOSS COMMISSION DELEGATED DIRECTIVE (EU) 2012/18 OF 21 MARCH 2012 AND/OR ANNEX 1 OF DIRECTIVE 2011/65/EU. A CERTIFICATE OF COMPLIANCE IS REQUIRED UPON REQUEST.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS ANGLES .XX .01 0-30° .XXX .005

RMS ALL MACHINED SURFACES. BREAK ALL SHARP EDGES AND CORNERS. REMOVE BURRS. UNDERLINED DIM. NOT TO SCALE. THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

APPROVALS	DATE
DRAWN Guru (LnT)	07-17-20
CHECKED Dafne .A	07-17-20
DESIGN ENGINEER Varadha (LnT)	07-17-20

TITLE: PRINTED WIRING BOARD KITFS84AUTEVM

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-47345	FAB-47345	B

ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL NOT CONTAIN ANY OF THE SUBSTANCES OF VERY HIGH CONCERN (SVHC) ABOVE THE THRESHOLD VALUE PER THE CURRENT TECHNICAL LIST OF SVHC'S AND WITH ANNEX XVII AND ANNEX XVII OF EACH DIRECTIVE. TEST PROPOSED. INVESTIGATE OF COMPLIANCE IS REQUIRED UPON REQUEST.

SCALE 1/1 DO NOT SCALE DRAWING SHEET 2 OF 2

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