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Rev	Revision History
X1	Initail Draft
A	1. Add optional SYSCLK circuit for sysclk input. 2. Add one bit of DIP-Switch to control the Nor Bank Boot Selection; 3. Add Stay-on option, this function is controlled by CPLD and DIP switch; 4. Add sideband connector for SGMII RISER CARD and XAUI RISER CARD. 5. Modify SATA circuit for correcting the mistake of SATA circuit. 6. Change 1588 connector
A1	1. R55, R644, R646 DNP and populate R66, R645, R647 with 1K resistors to change the address of XAUI rise card to 000. 2. DNP C280
B	1. Change CPLD from LCMXO256C to LCMXO1200C 2. Change the package of J14 to SMT based on the PE requirement. 3. Add two power resistors for ATX power supply based on the PE requirement. 4. Connect the unused pins of SW3 to CPLD for debug in the future. 5. Change SW3[5] to control TEST_SEL instead of resistors(Remove r241 and r242)
C	1. Change +CPU_VDD power supply to new part (ZL6100). 2. Change AVDD filter circuit according to spec. 3. Adjust decoupling capacitors according to spec. 4. Change R338,R330,R328,R326 and R323 to 1Kohm. 5. Add NAND flash (U78). Add mux control chip(U65) for flash chip select control. 6. Remove J8, J9 and connect pin AB17, AB19 to GND. 7. Remove TP43, NC pin. 8. Trust Arch: Add U27 for LP_TMP_DETECT_N. Add SW3.6 for TMP_DETECT_N. Add J24 for VDD_LP. 9. J17 remove. 10. Change temp sensor. Replace U24 with U79(ADT7461). And connect the output to IRQ10, remove LOAD_DEFAULT_N signal which is no use. 11. Add TP53 for PORESET. 12. Add U24, U66 for ATX preload. Remove R682 and R683. 13. Remove C259 which is no useful. Connect J5.11pin to +12V.
C1	1. Change R539 from 4.7K to 330ohm. 2. Q5 change to be populated.
D	1. Change U44 to PI6C557-03A to support PCIE Gen2 clock. 2. Change U42 to PI6C557-03A to support PCIE Gen2 clock. 3. Swap the direction of SATA connectors in layout.
D1	1. Update J2,J3 RJ45 part number with yellow and green LEDs. Note: just part number update, no change for parts. 2. Update CPU part number.
D2	1. Update NOR flash and SPI flash P/N. 2. Update CPU P/N to rev2.0.

Revisions			
Rev	Description	Date	Approved
X1	Original Release	Jul 25, 11	SH HW Team
A	1st Formal release	Aug 31, 11	SH HW Team
A1	2nd Formal release	Sep 13, 11	SH HW Team
B	PCB revB formal release	Oct 10, 11	SH HW Team
C	PCB revC formal release	Jan 06, 12	SH HW Team
C1	RevC1 formal release	Feb 28, 12	SH HW Team
D	RevD formal release	Sep 11, 12	SH HW Team
D1	RevD1 formal release	Jan 22, 13	SH HW Team
D2	RevD2 formal release	Jan 29, 13	SH HW Team

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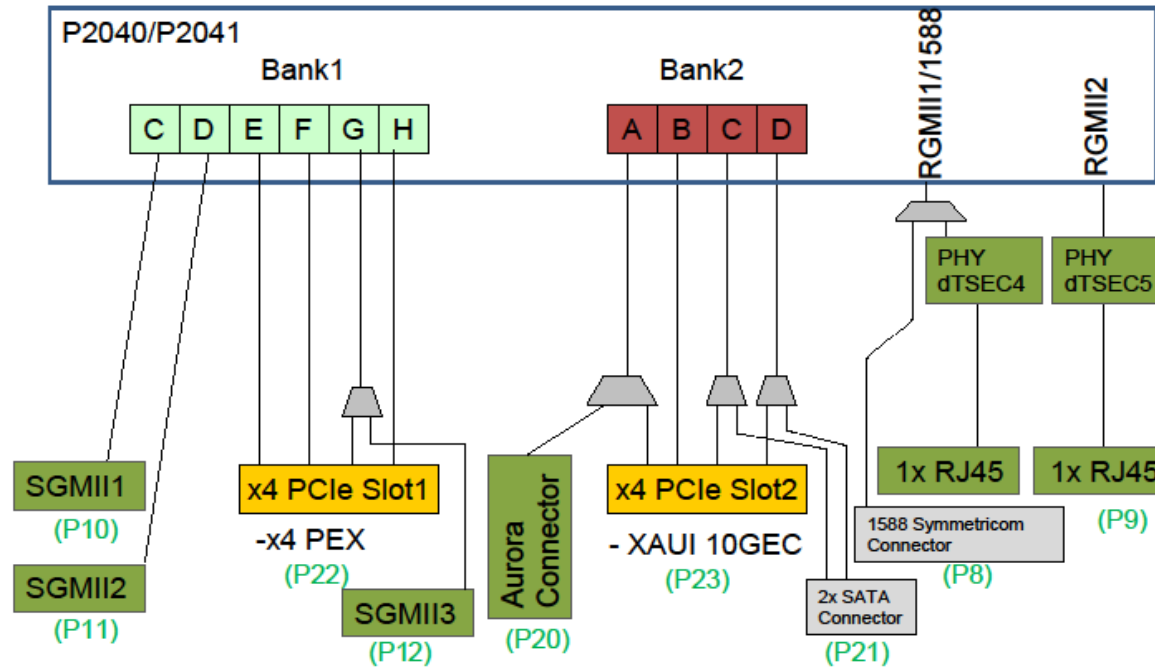
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P2040RDB-PC P2041RDB-PC Schematic

		Networking & Multimedia Group 6501 William Cannon Drive West Austin, TX 78735-8598	
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Designer: SH HW Team	Drawing Title: P2041RDB-PC		
Drawn by: SH HW Team	Page Title: Cover Page		
Approved: SH HW Team	Size C	Document Number SCH-20914 PDF: SPF-20914	Rev D2
Date: Tuesday, March 26, 2013		Sheet 1	of 26

Multiplexing Options



SerDes Connectivity

	BANK1						BANK2			
SRDS_PRTCL(HEX)	C	D	E	F	G	H	A	B	C	D
19	SGMII#1	SGMII#2	-		SGMII#3	-	-	-	SATA#1	SATA#2
09	SGMII#1	SGMII#2	PEX#2				XUAI 10GEC			



ICAP Classification: FCP: FIUO: PUB: x

Drawing Title:

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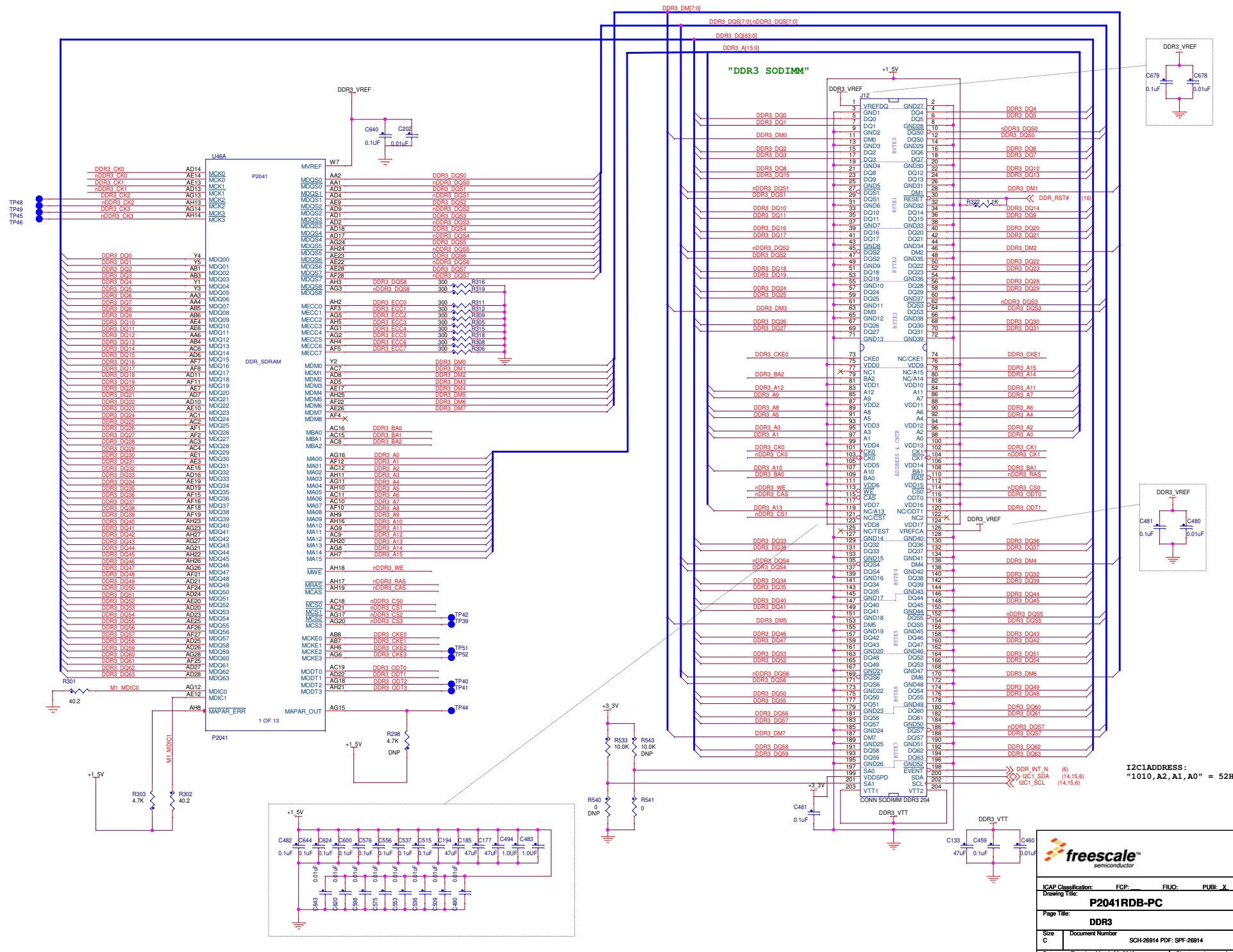
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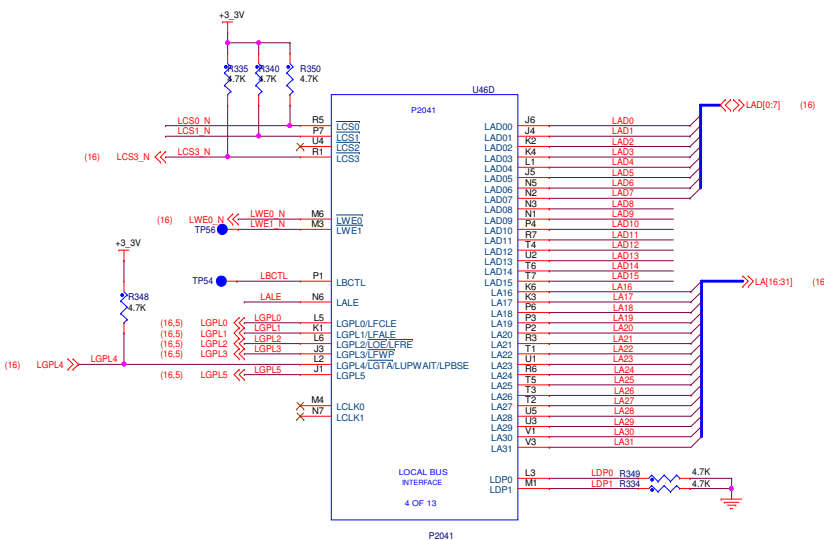
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Size C Document Number SCH-26914 PDF: SPF-26914

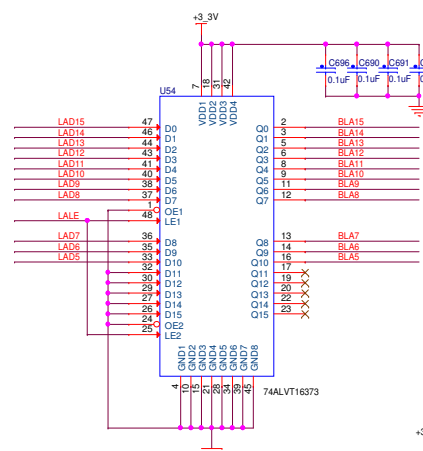
Rev 02

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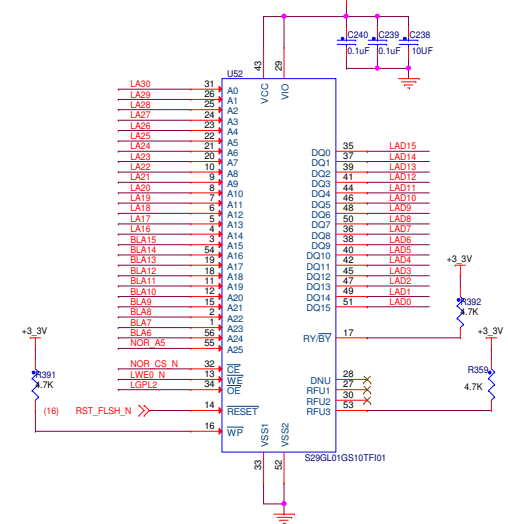




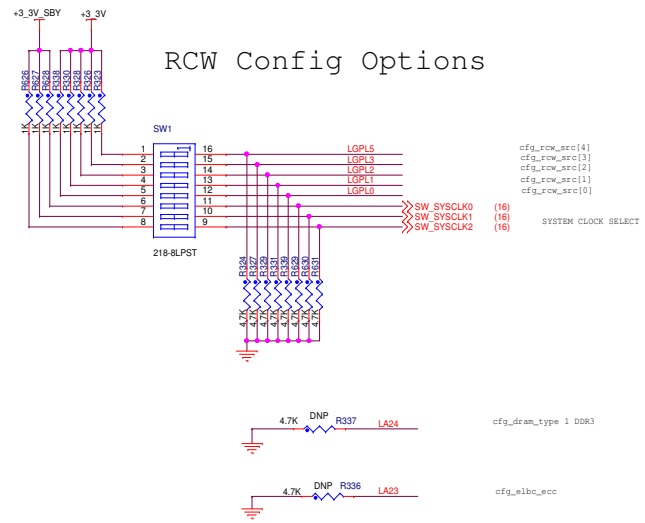
LOCAL BUS INTERFACE ADDRESS - LATCH



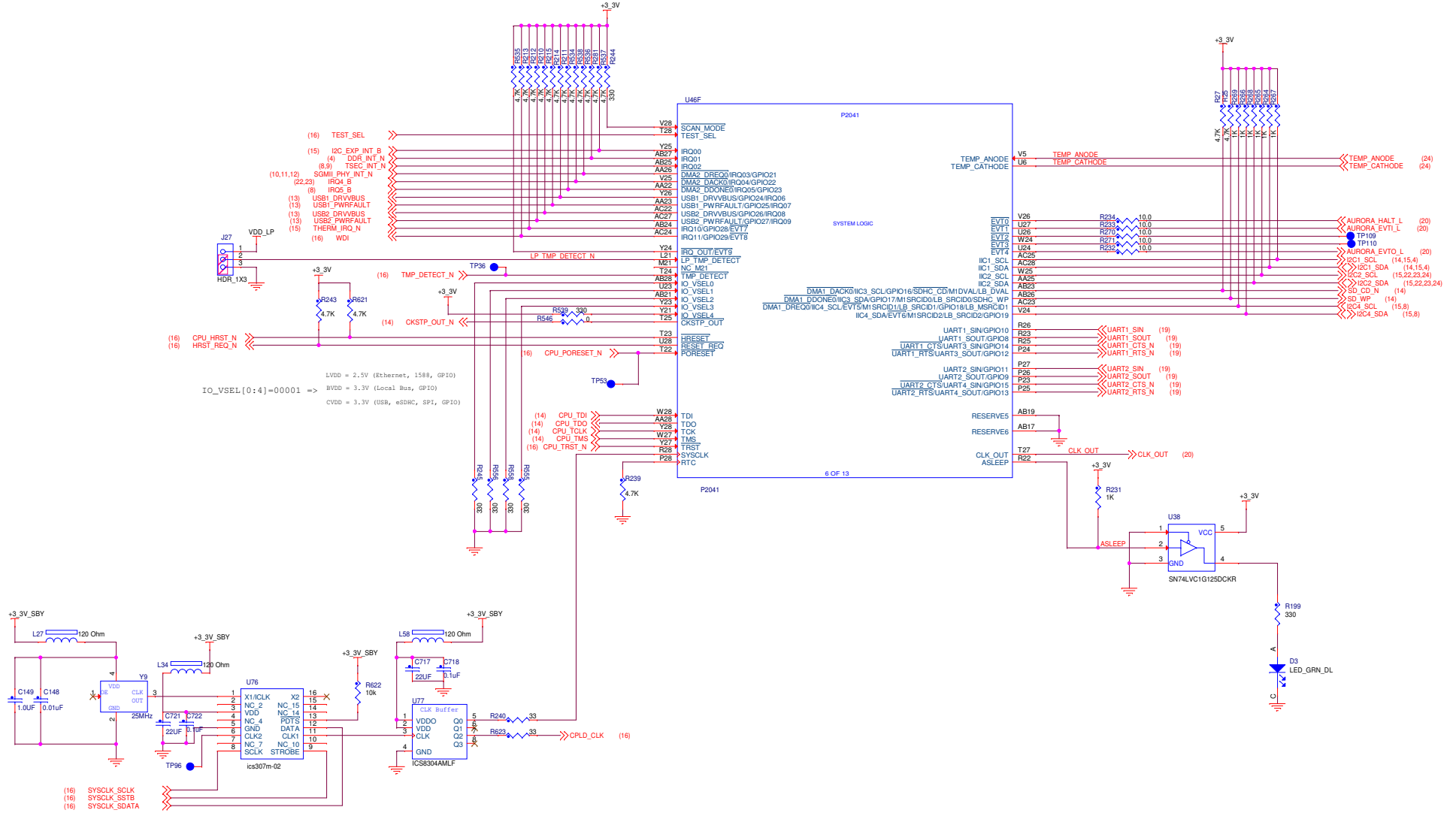
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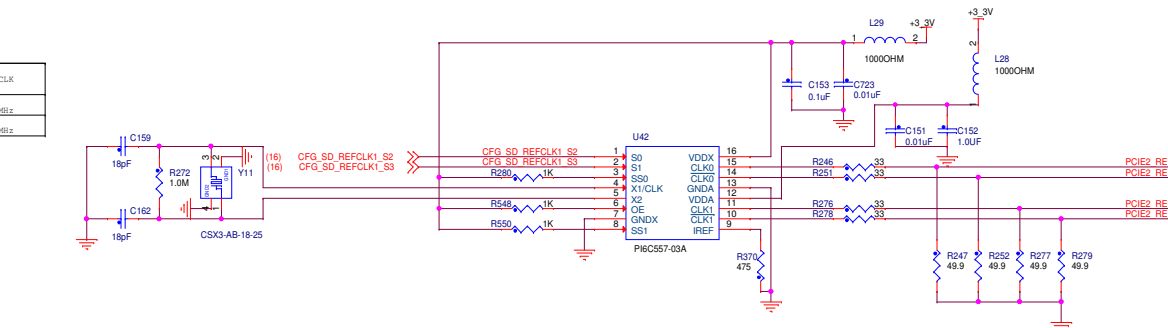


RCW Config Options



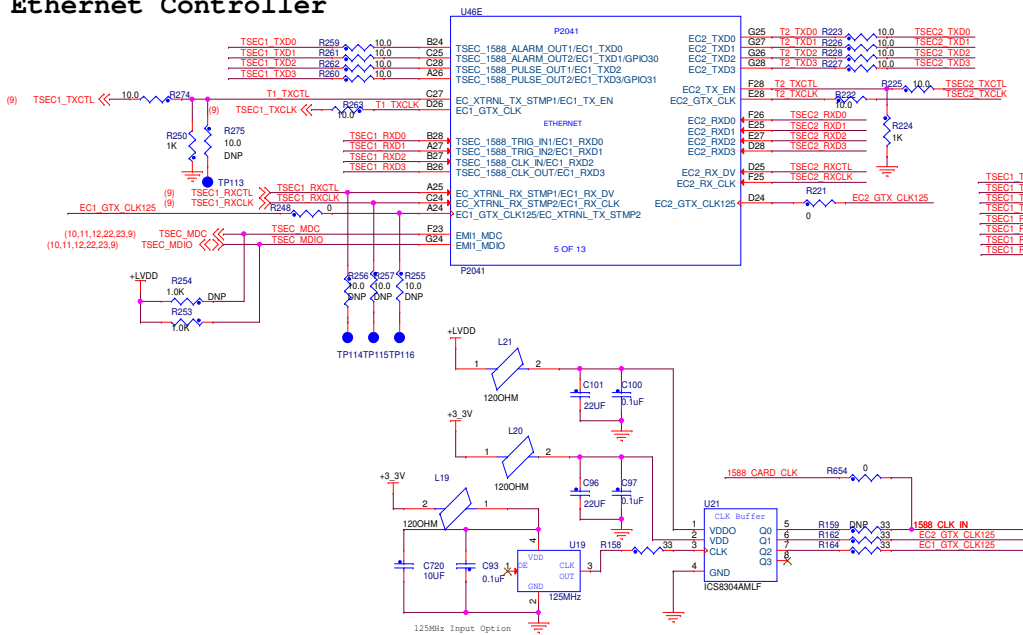
CPU MISC



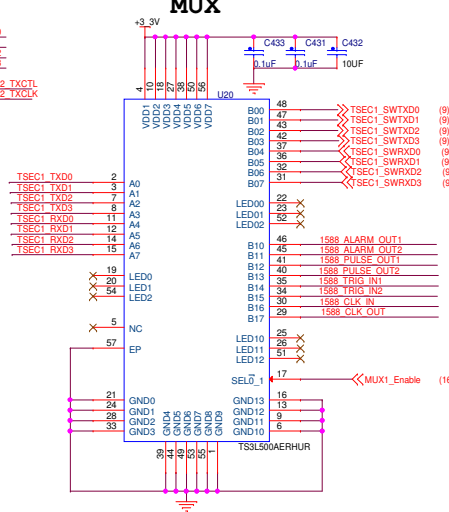


CFG_SD_REFCLK1_S2 SW2[5]	CFG_SD_REFCLK1_S3 SW2[6]	OUTCLK
1	0	100MHz
0	1	125MHz

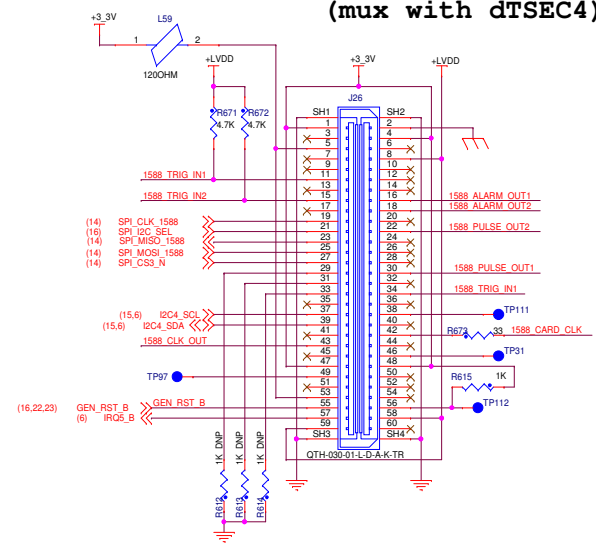
Ethernet Controller



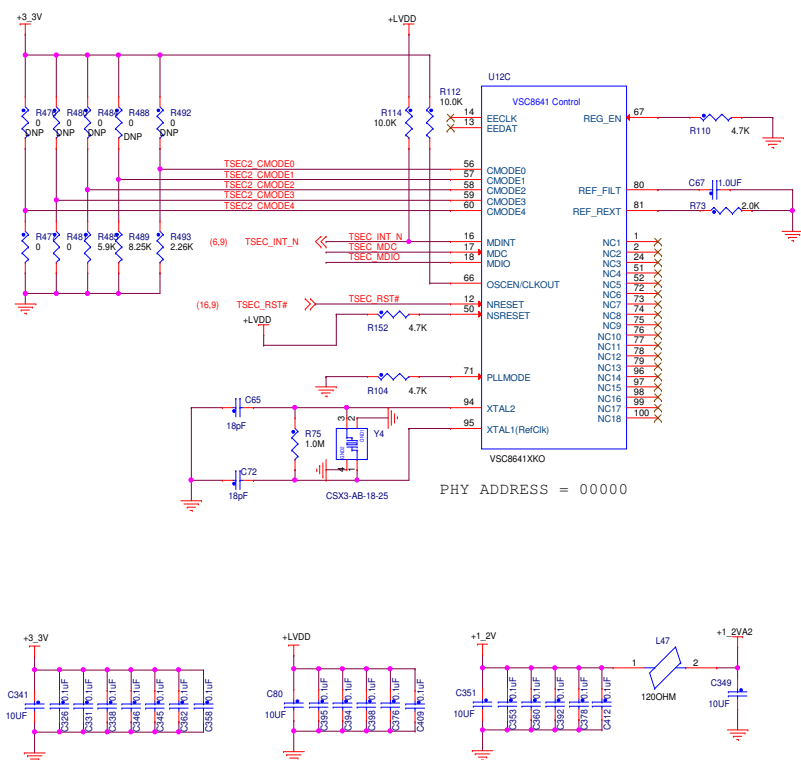
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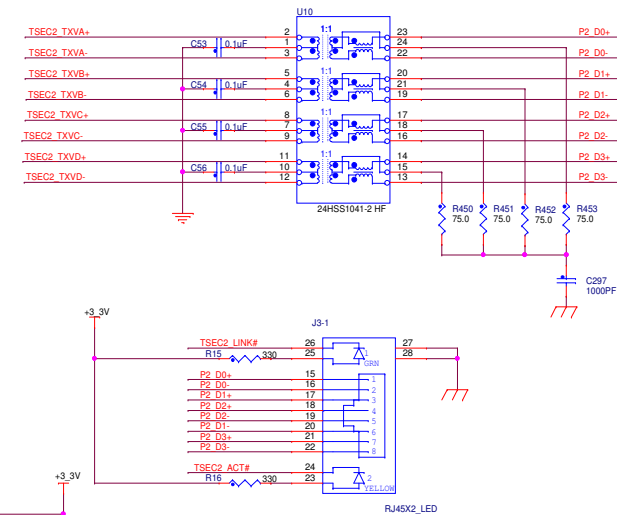
IEEE 1588
(mux with dTSEC4)



.....
dTSEC5-RGMII



Transformer

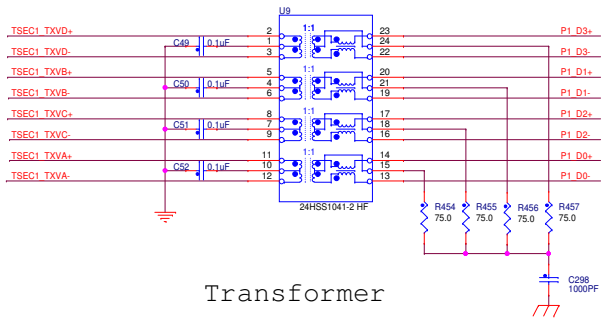
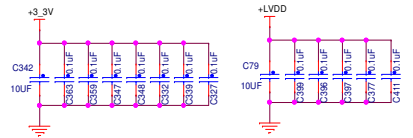
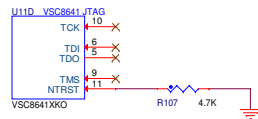
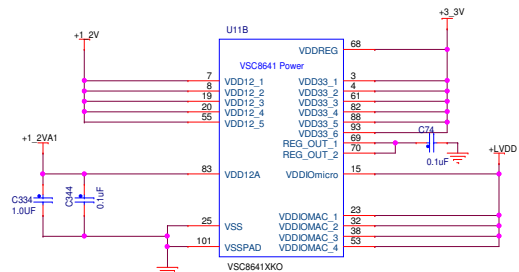
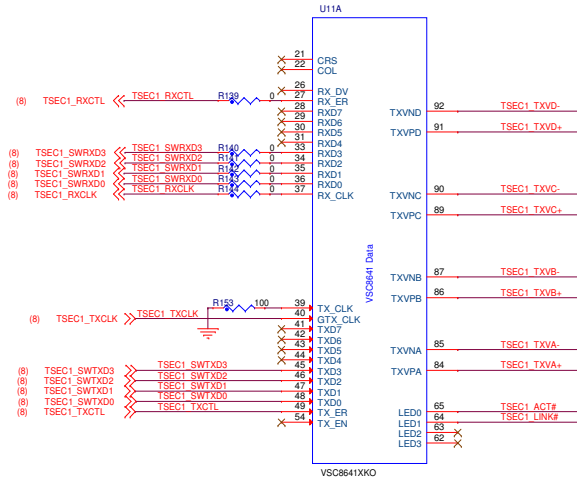
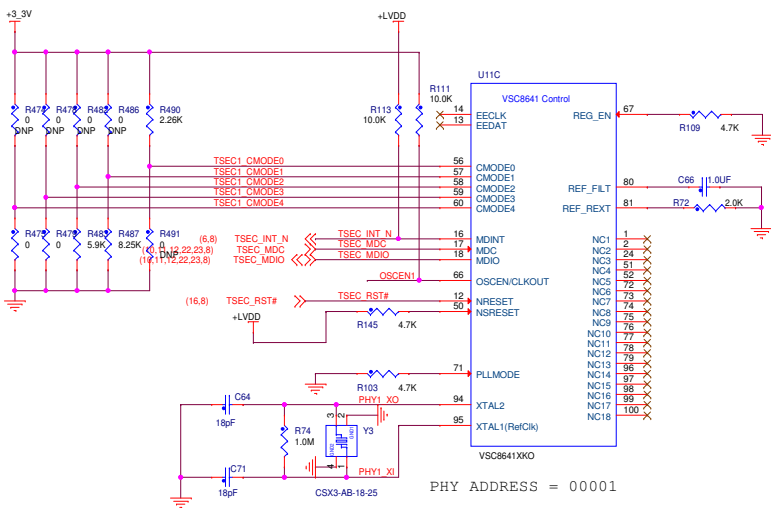


RJ45

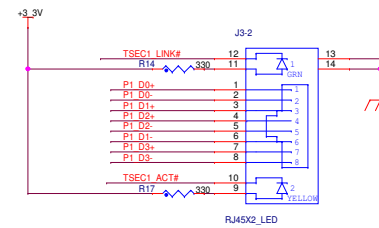


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dTSEC5 RGMII PHY/1588							
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dTSEC4-RGMII

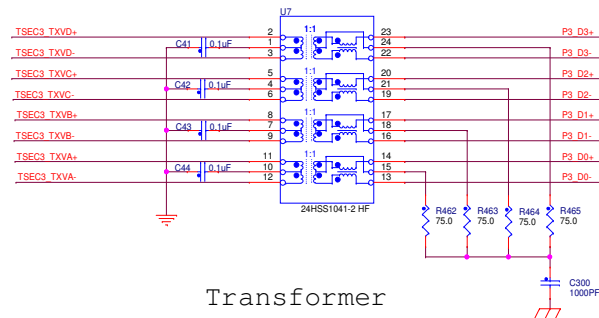
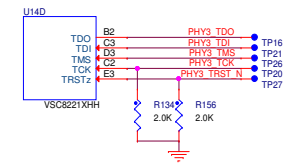
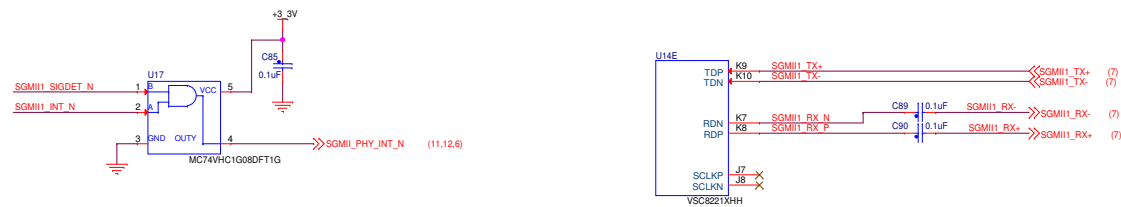
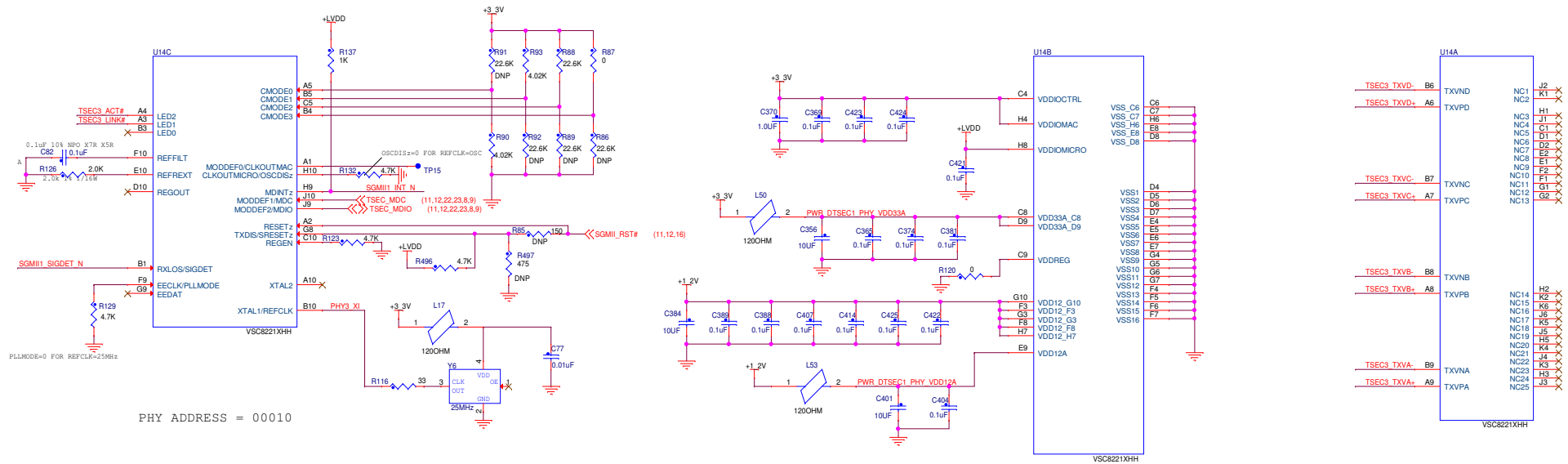


Transformer

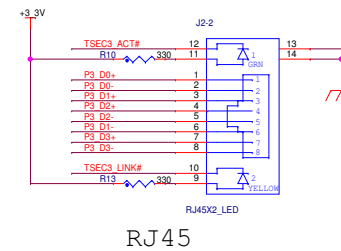


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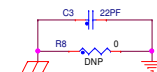
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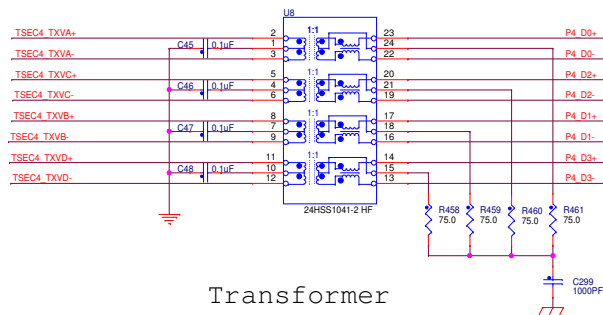
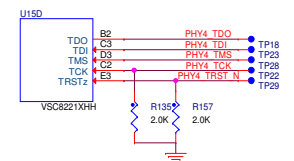
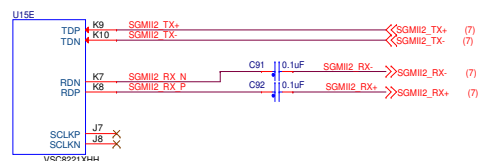
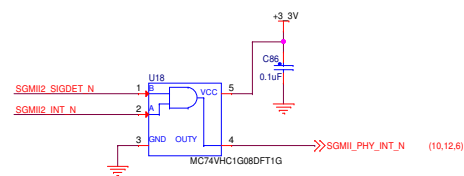
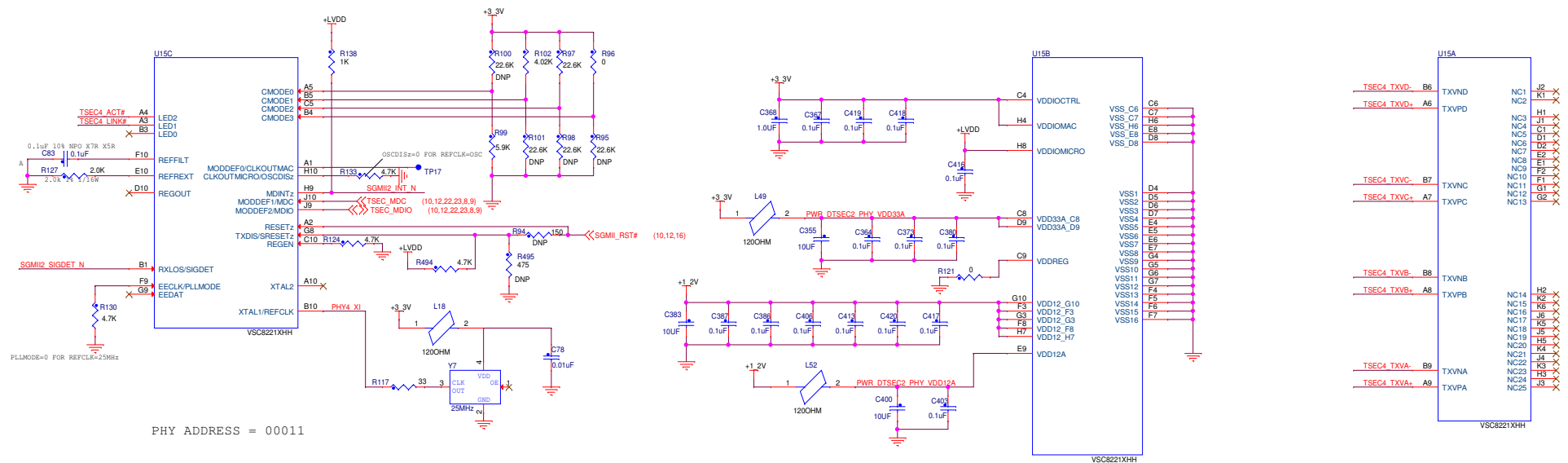
Transformer



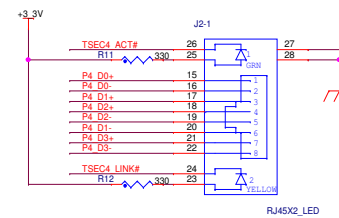
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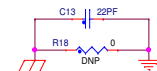
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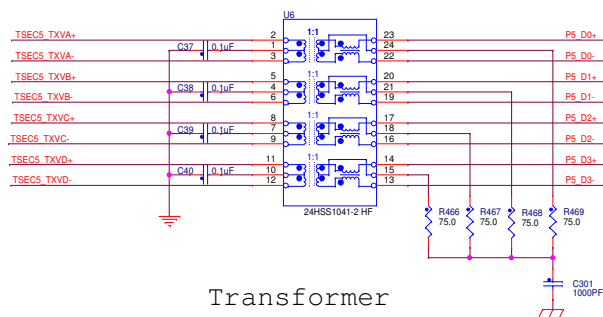
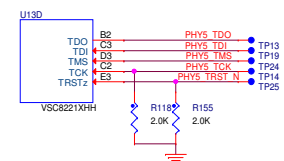
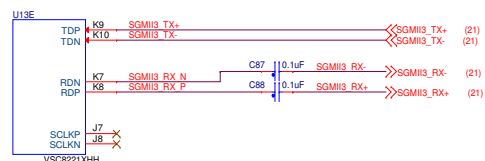
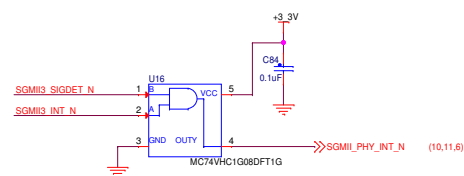
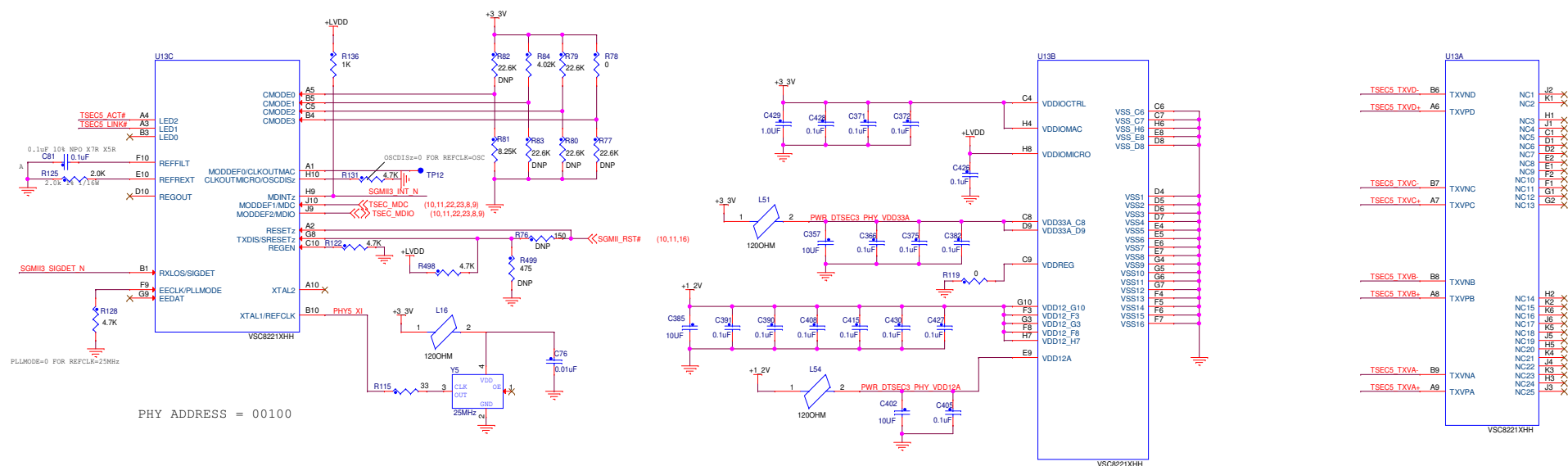
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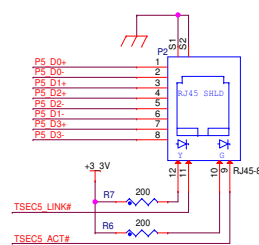
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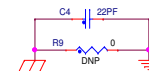
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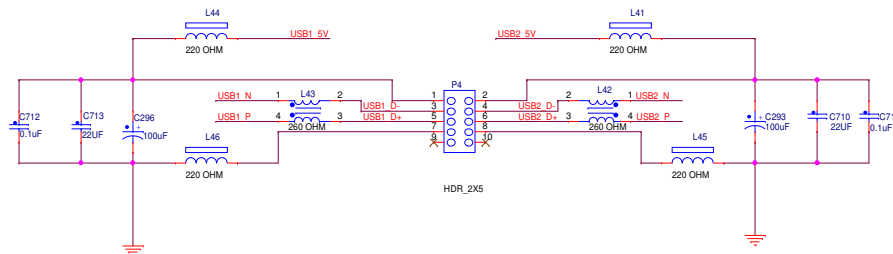
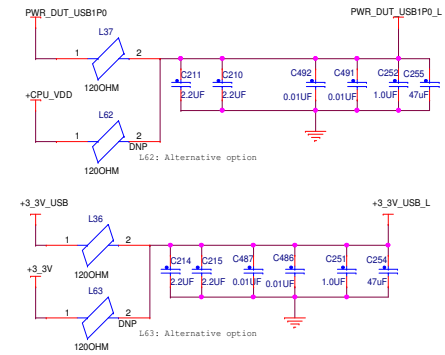


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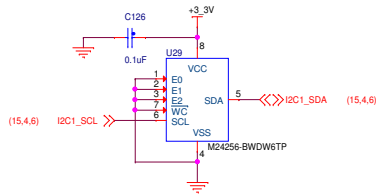


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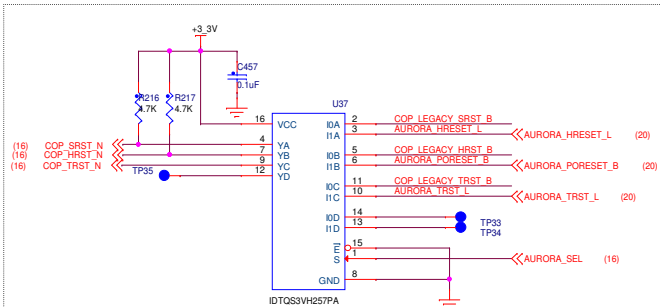
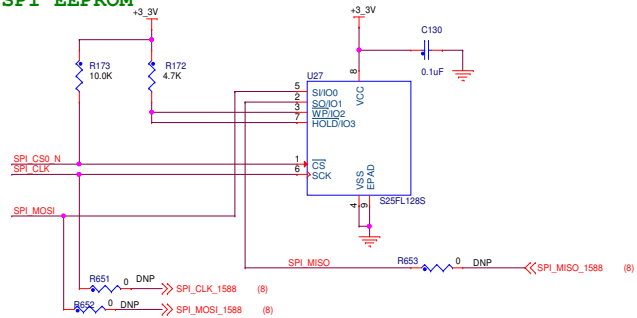


BOOT I2C1 EEPROM

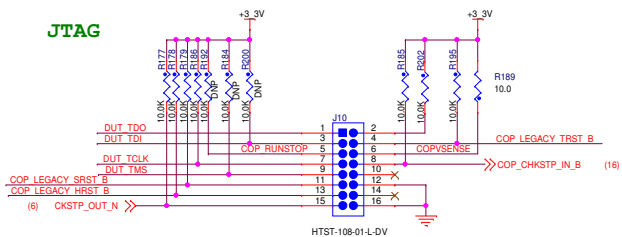


I2C1 ADDRESS:
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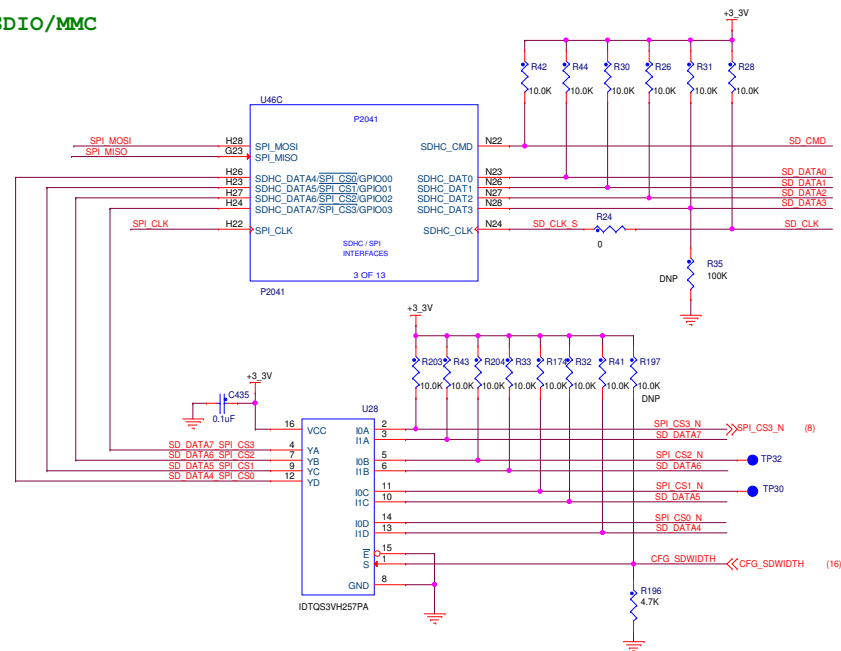
SPI EEPROM



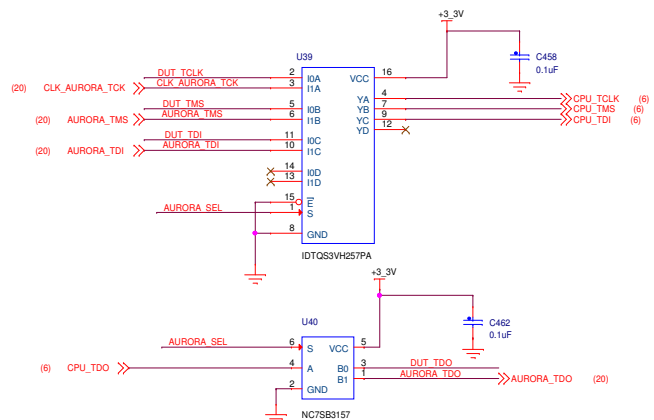
JTAG



SD/SDIO/MMC

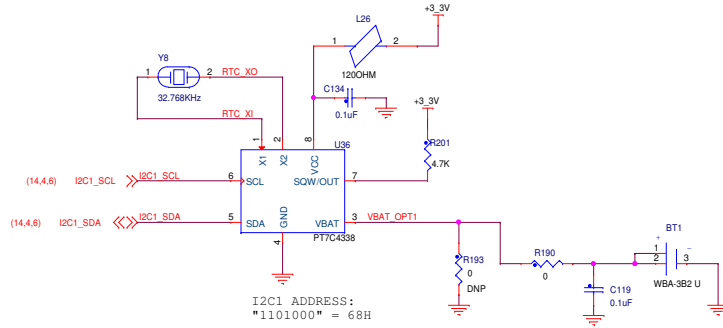


MUX

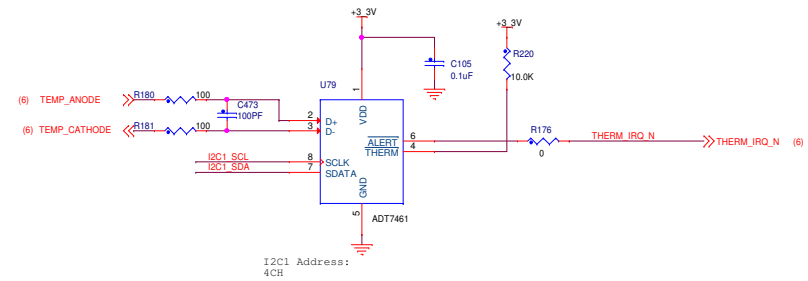


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Page Title:	PERIPHERALS 1		
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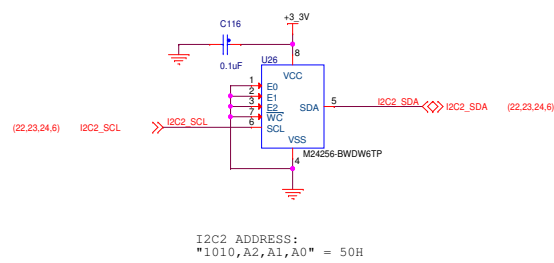
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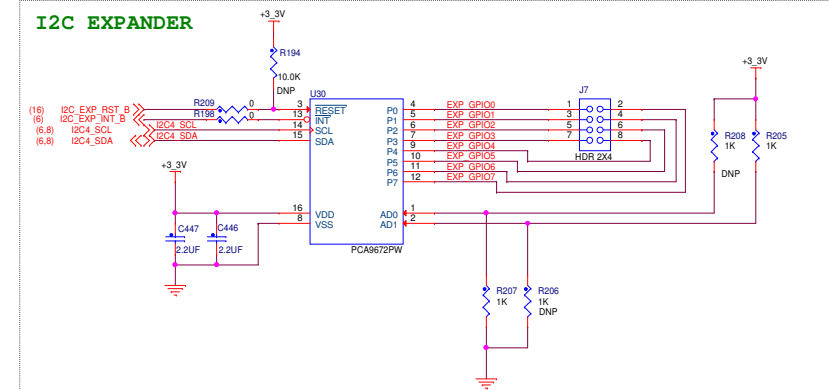
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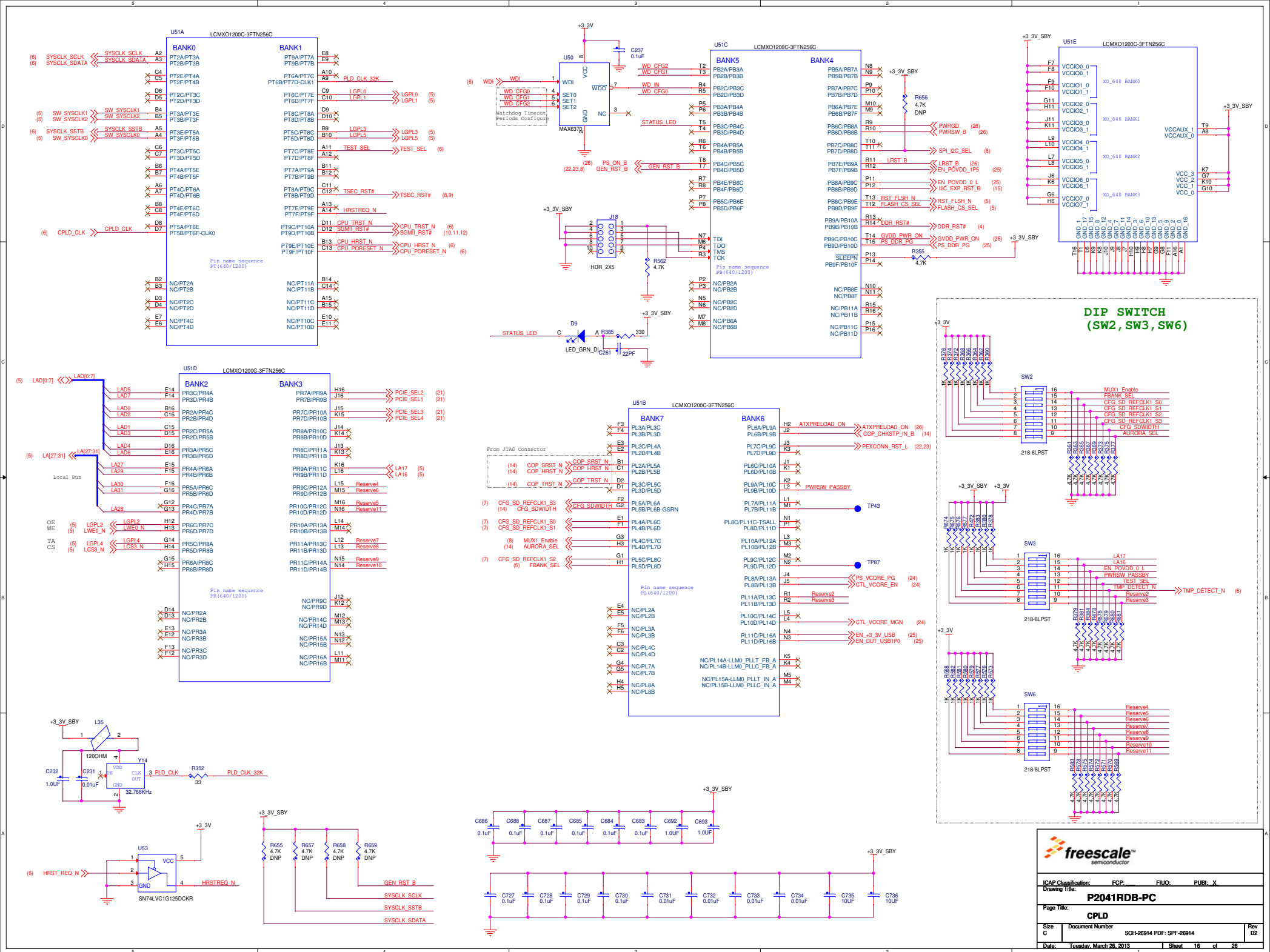
RDB EEPROM



I2C EXPANDER



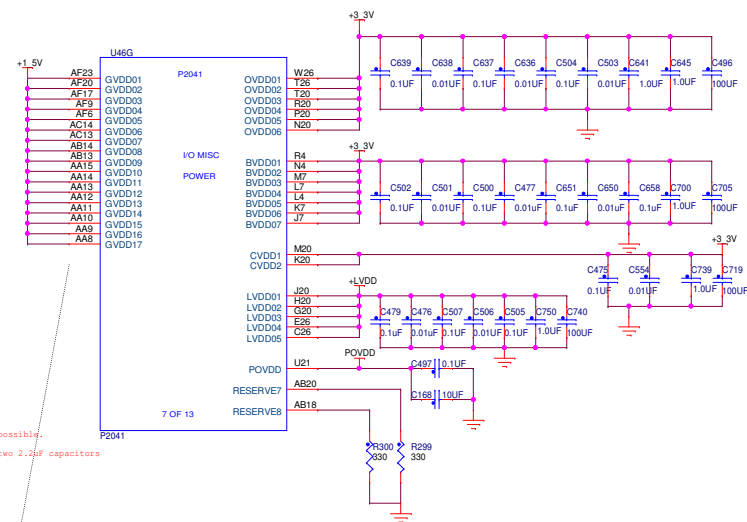
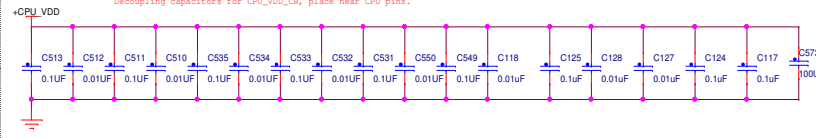
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P2041RDB-PC	
Page Title:	
I2C	
Size C	Document Number SCH-26914PDF: SPF-26914
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Decoupling capacitors for VDD_CA_PL are on the next page

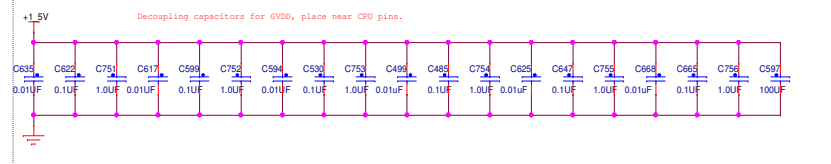
These parts must be placed as close as possible to the specific AVDD pins.

Decoupling capacitors for CPU_VDD_CB, place near CPU pins.

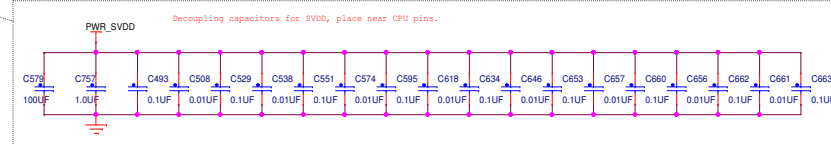


The filter circuit is placed as closely as possible to the AVDD_S8Sn balls to ensure it filters out as much noise as possible. The ground connection must be near the AVDD_S8Sn balls. The 0.003uF capacitor is closest to the balls, followed by two 2.2uF capacitors and finally the 100uF capacitor to the board supply plane.

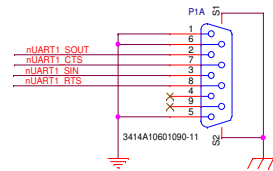
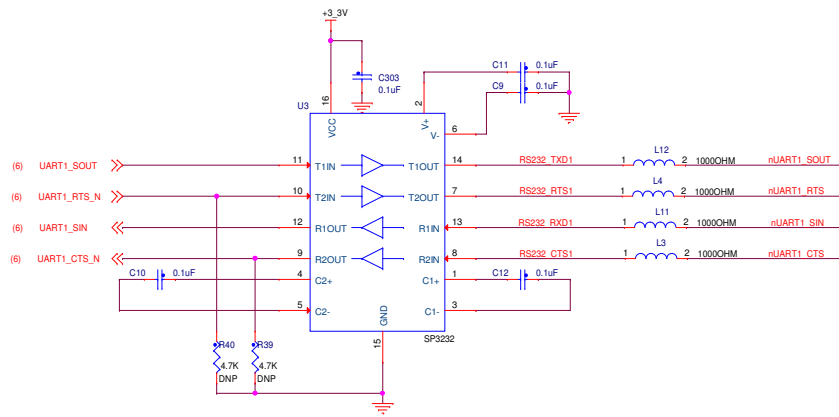
Decoupling capacitors for GVD2, place near CPU pins.



Decoupling capacitors for SVDD, place near CPU pins.

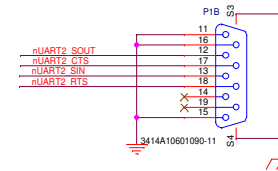
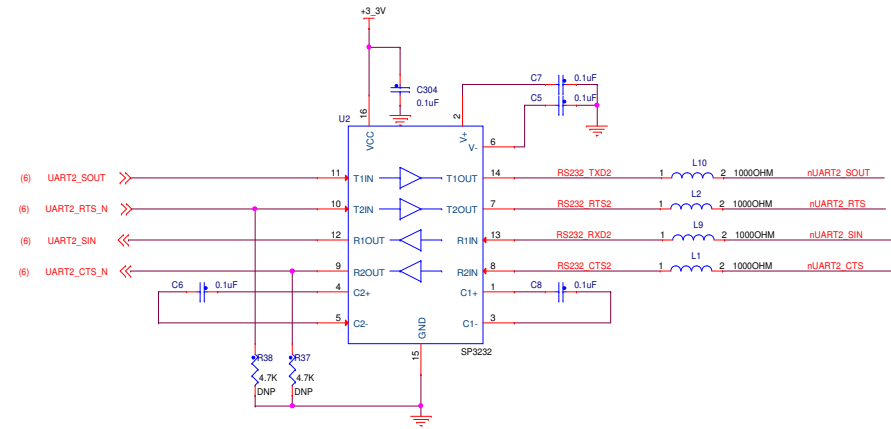


RS232



TOP

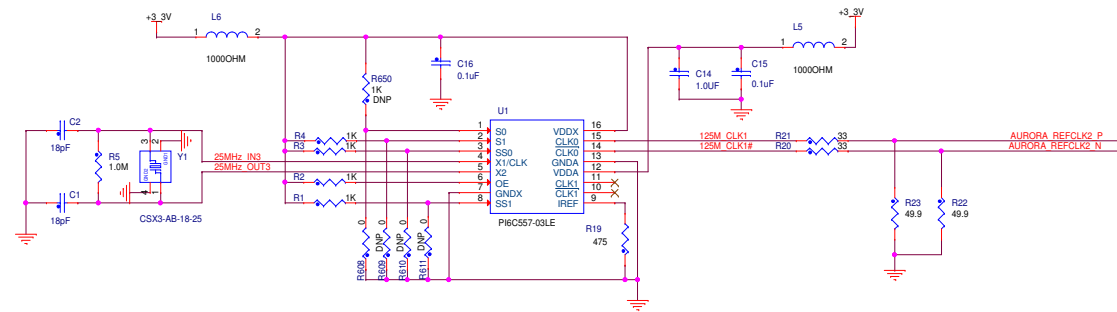
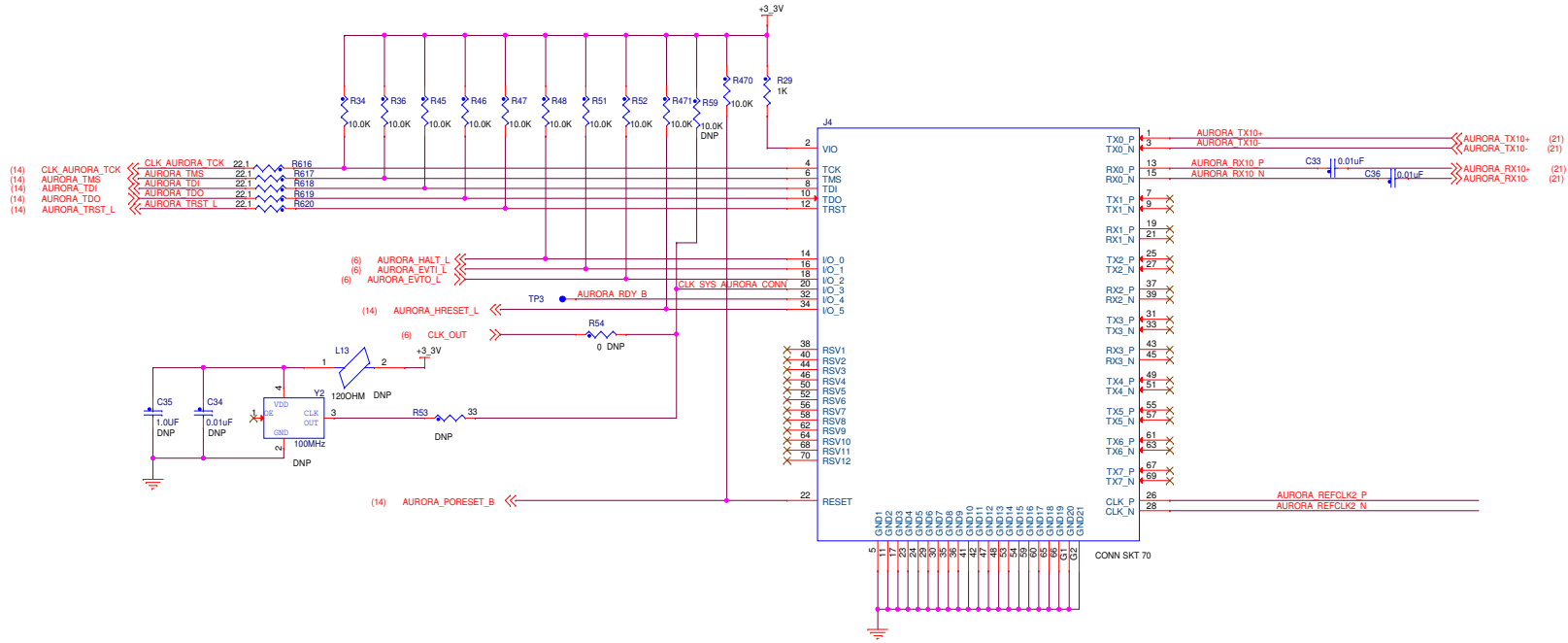
Screen on panel: TOP UART0
default console display port

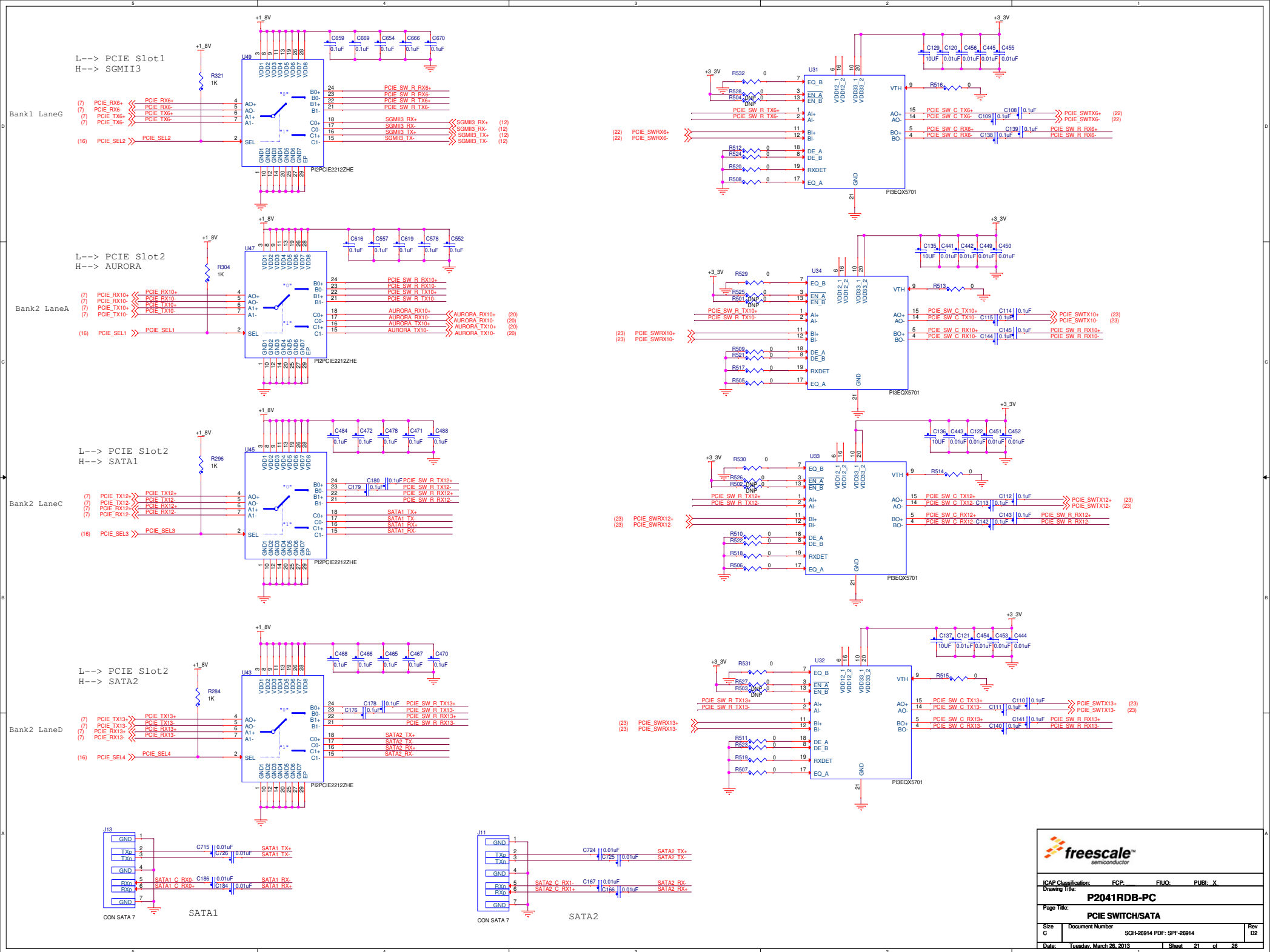


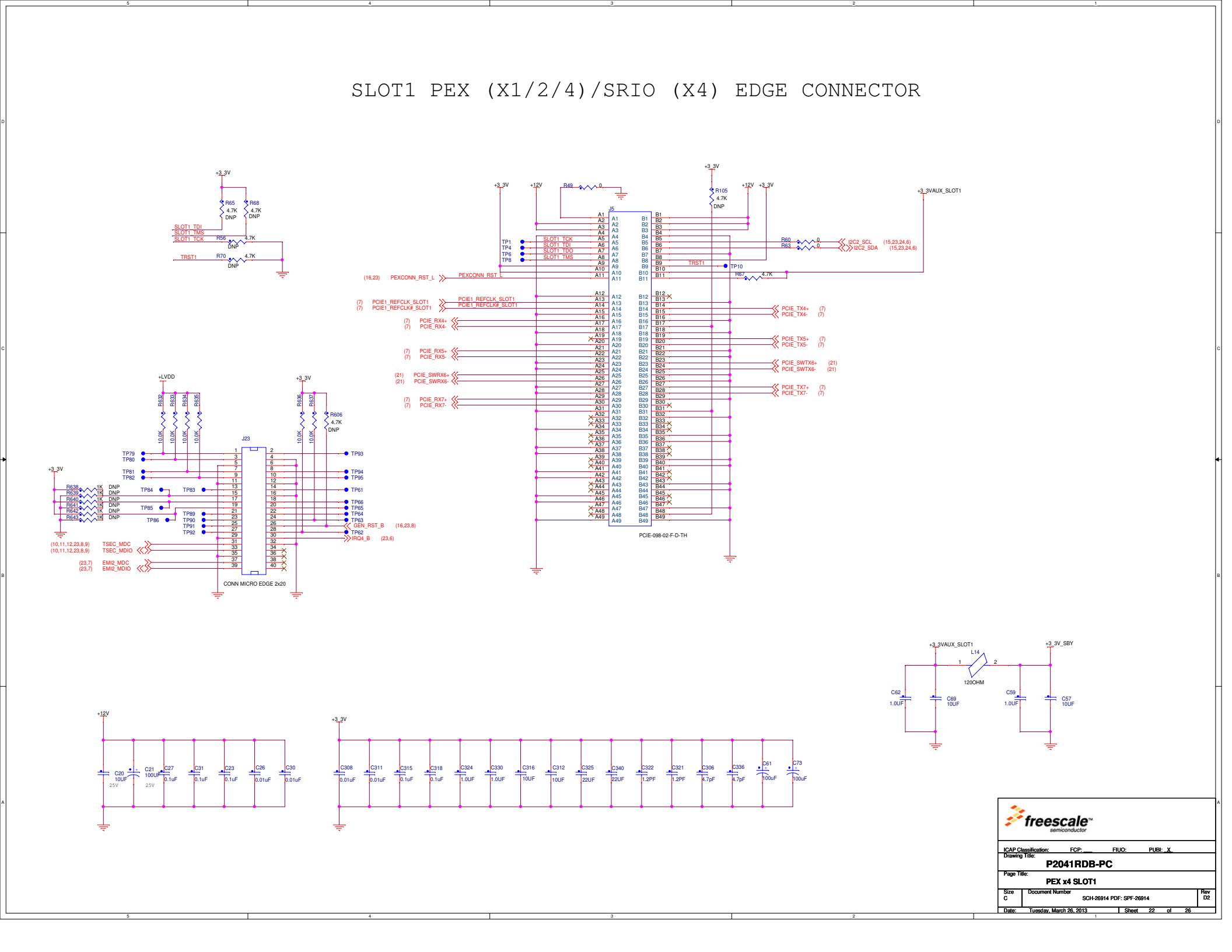
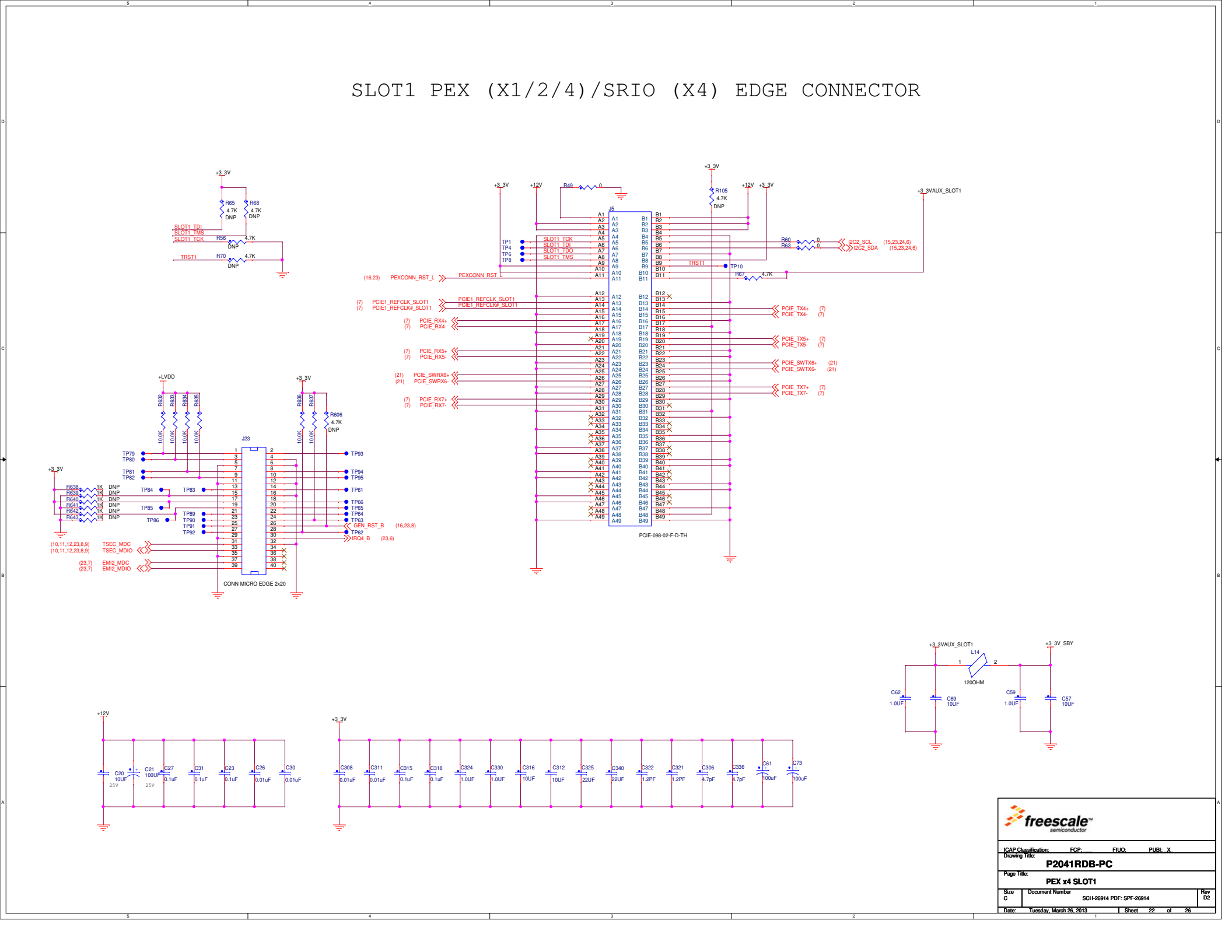
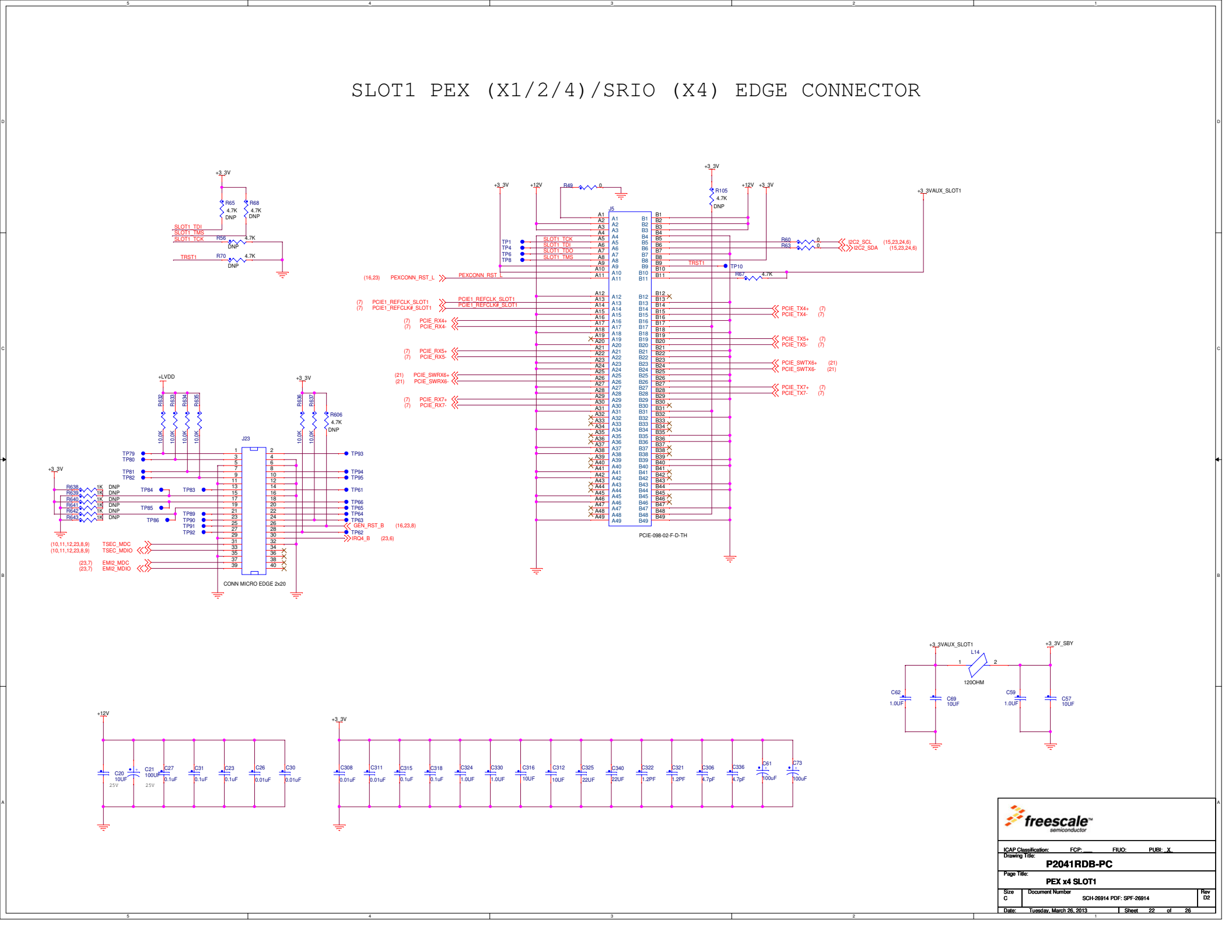
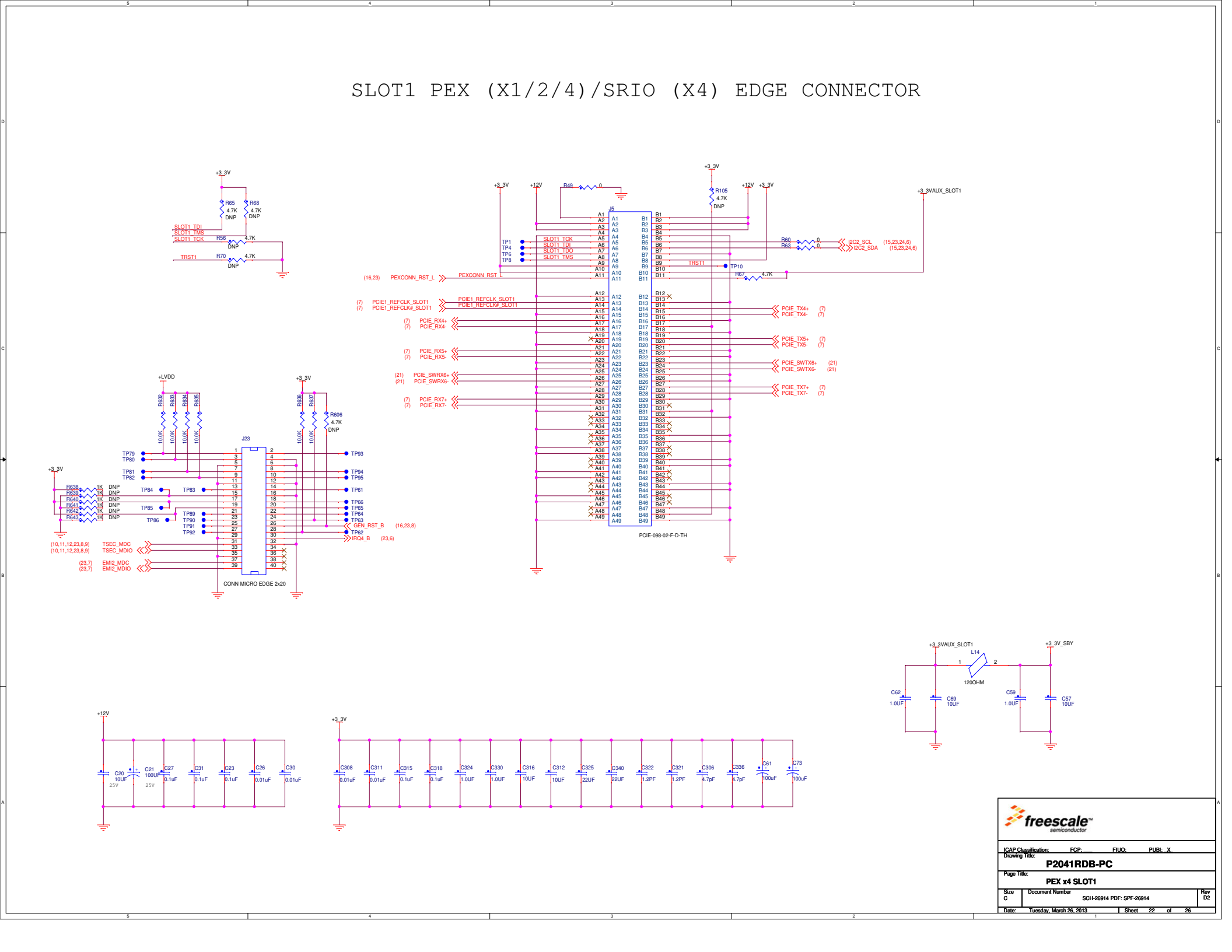
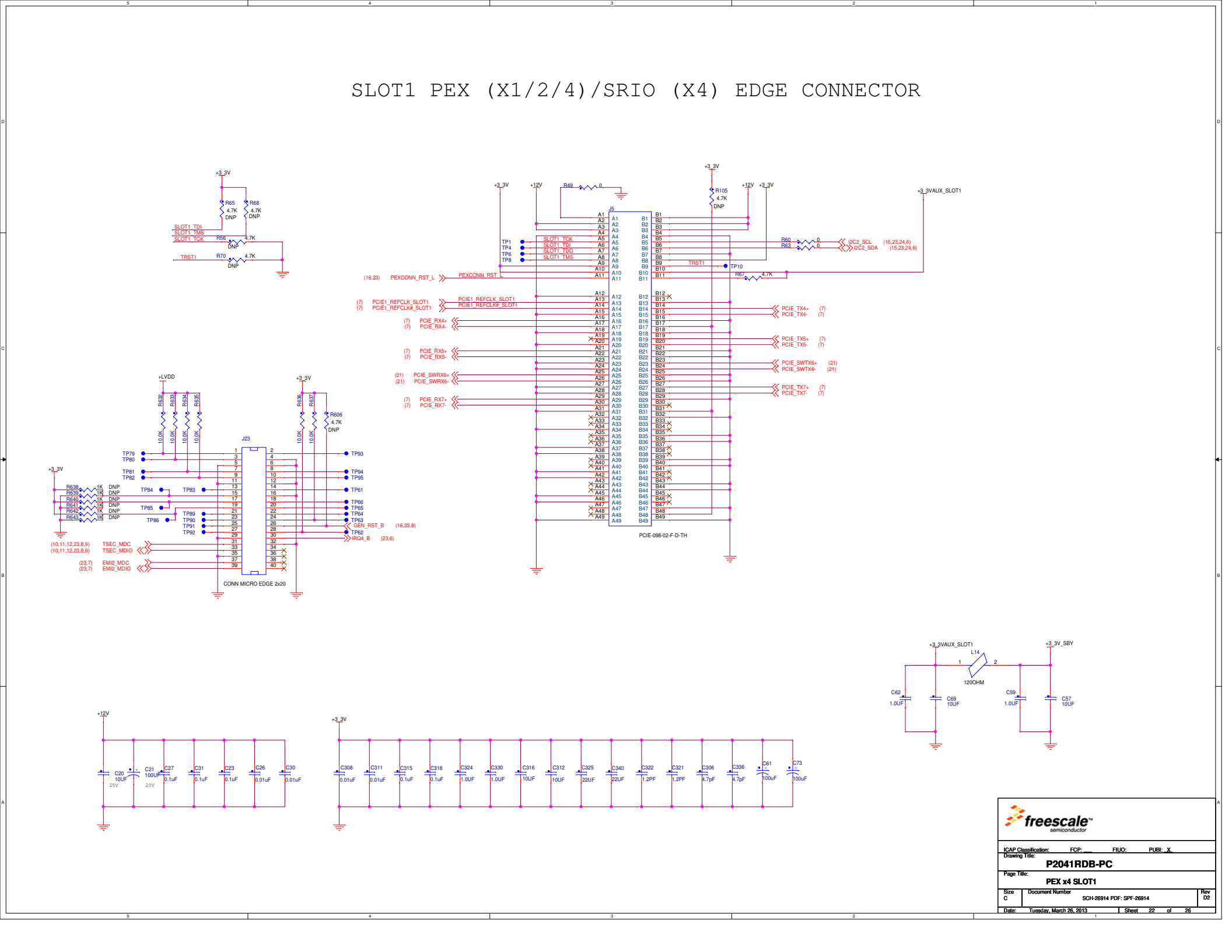
Bottom

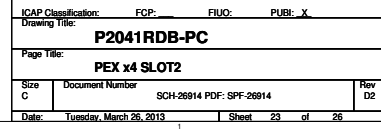
Screen on panel: BOT UART1

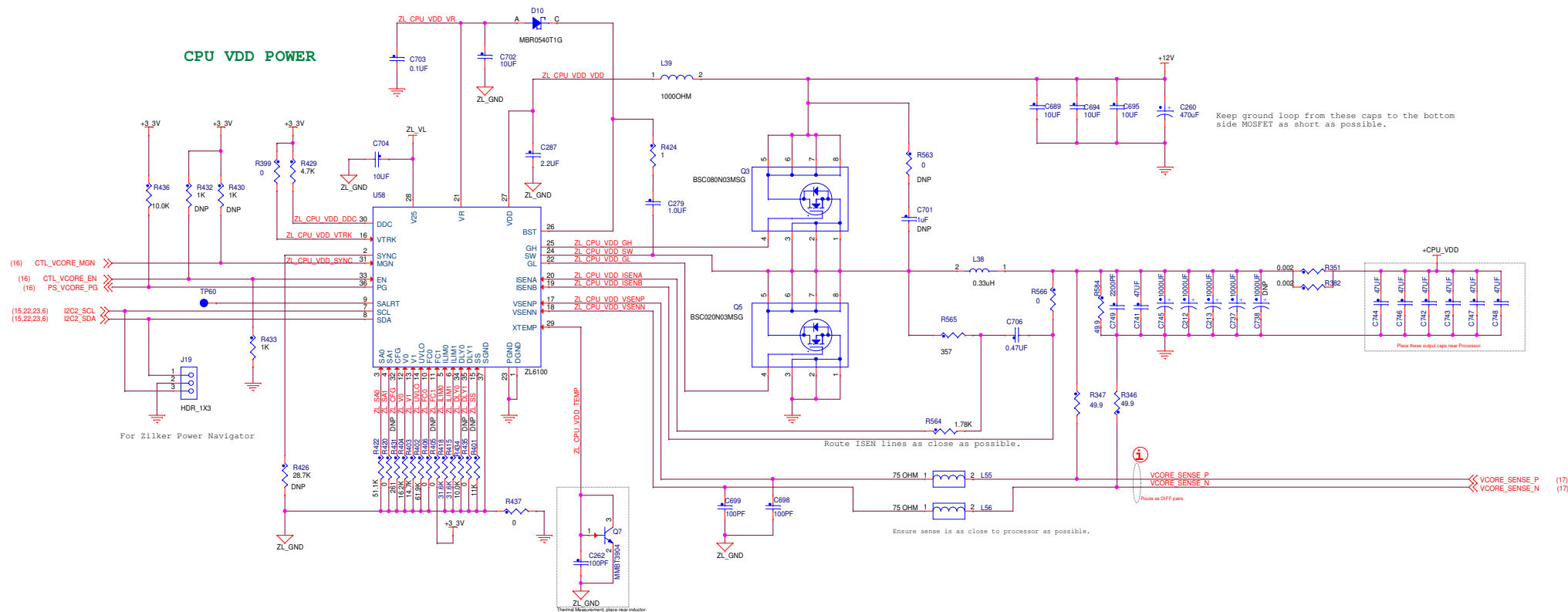
AURORA CONNECTOR -- SERDES





[illegible]

[illegible]

 **ZL6100 PINSTRAP CONFIGURATION**

SA(0:1) - I2CADDR:	0X11
CFG - Config:	Auto-detect
VB(1) - Vout1m:	1.1V (For rev1.0 Silicon) 1.0V (For rev1.1 Silicon)
UVLO - UNDERVOLT:	10.5V
FCID(1) - Compensation:	See spec.
ILIMP(1) - ILimit:	Low duty cycle, High FSW 30MV THRESHOLD 9 VIOLATIONS ALLOWED
DLTP(1:2) - SoftStart:	0ms delay
SS - SoftStart:	5ms ramp
FSW - SWITCH FREQ:	515 KHz

SHUTDOWN IF OUTPUT CURRENT IS AT 30.87A

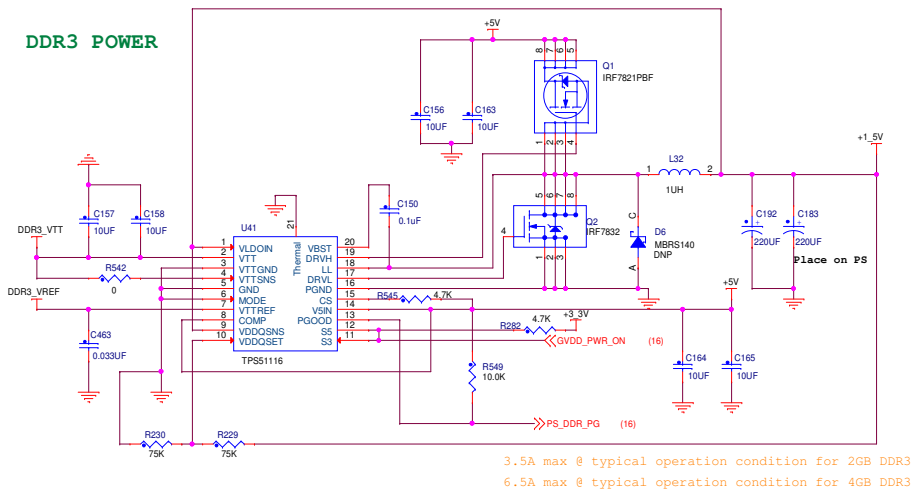
INDUCTOR DCR CURRENT SENSING METHOD

Note: Resistors are used in lieu of NC/GND/VL for maximum configuration flexibility.

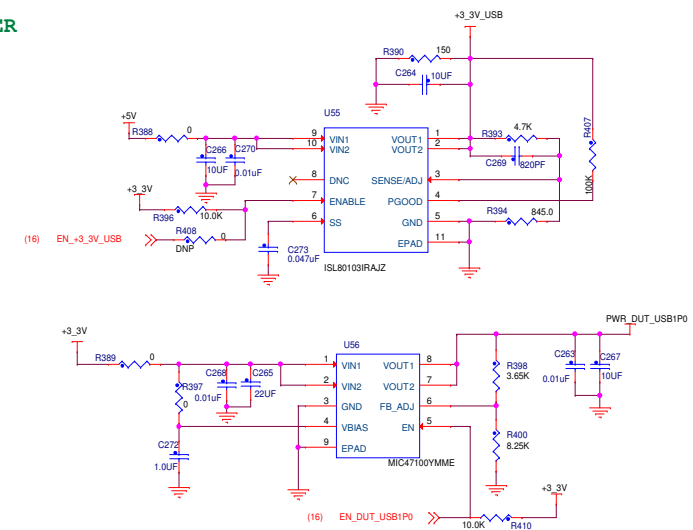
THE POPULATED 50 OHM OUTPUT
LOAD WILL DRAW STATIC CURRENT OF
20 MA @ 1.0V AND 22MA @ 1.1V

SGND AND PGND/GND GROUND UNIFICATION ARE TIED
TOGETHER AT LOW SIDE OF FET SOURCE PINS

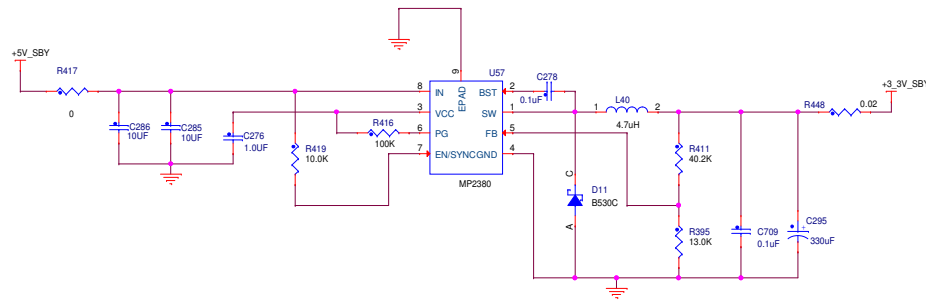
DDR3 POWER



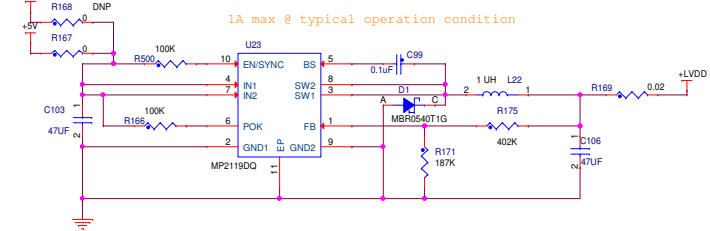
USB POWER



HOT 3.3V

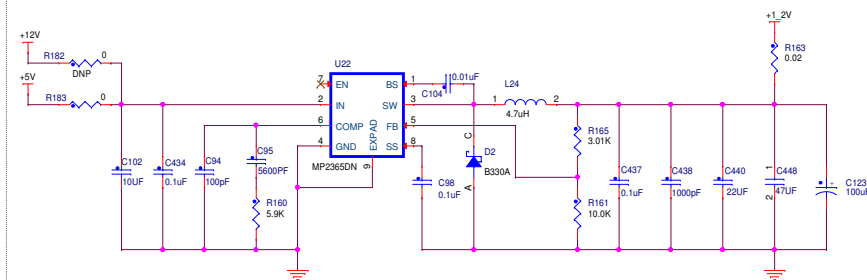


2.5V: ETHERNET PHY



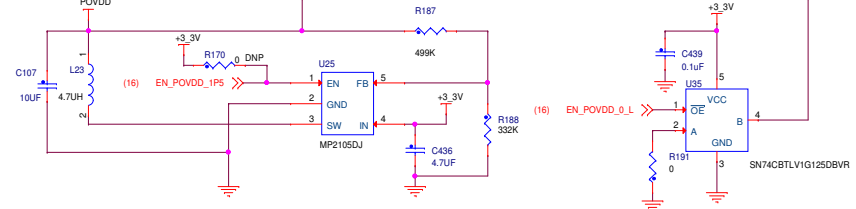
1.2V: ETHERNET PHY

2A max @ typical operation condition



1.5V Output For POVDD

750mA max @ typical operation condition



ICAP Classification: FCP: FIUC: PUR: X	
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