M5275EVB Evaluation Board

Table Of Contents:

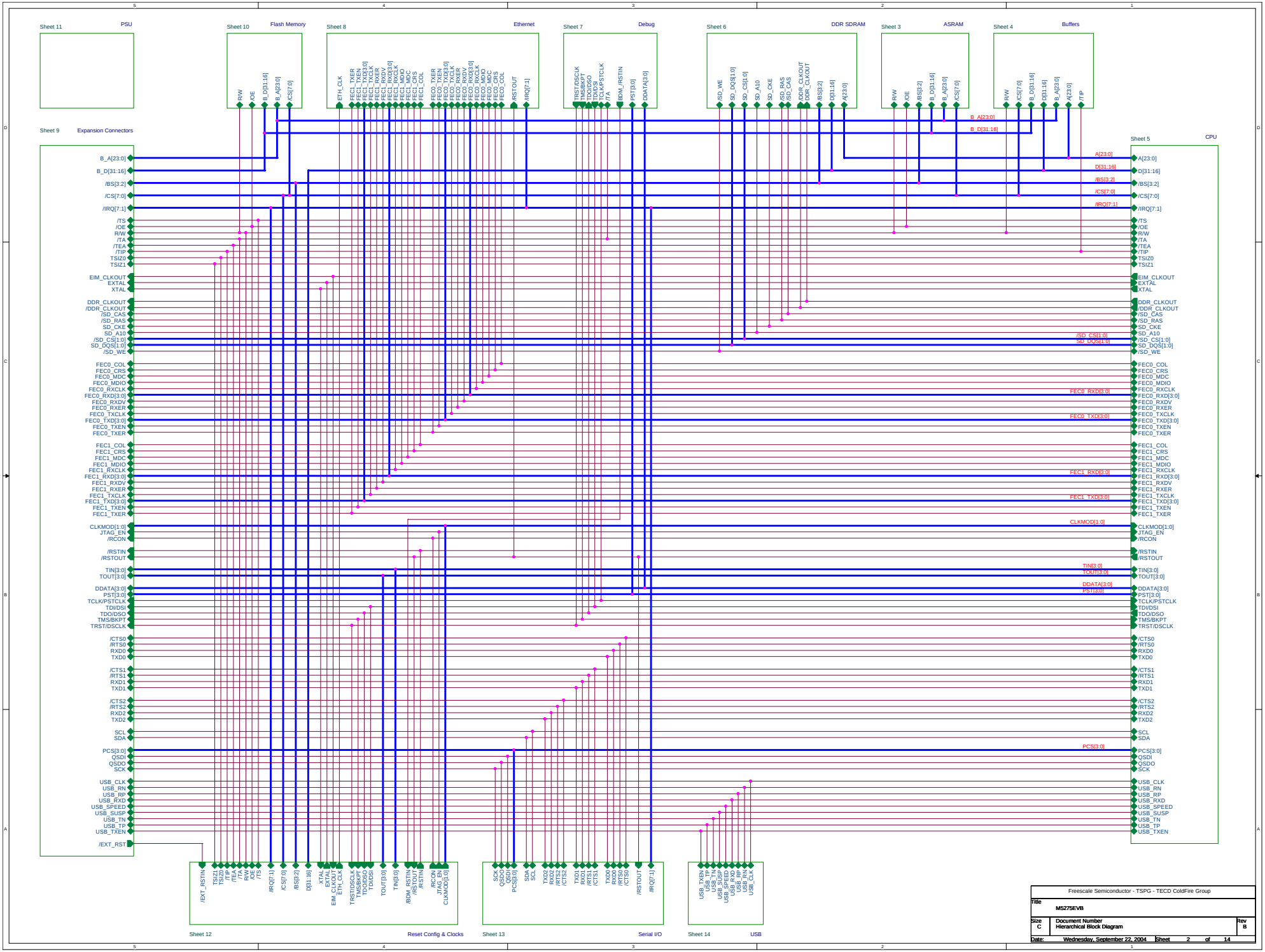
HIERARCHICAL INTERCONNECTS	SHEET 2
ASRAM MEMORY	SHEET 3
ADDRESS AND DATA BUS BUFFERS	SHEET 4
MCF5275 CPU	SHEET 5
DDR SDRAM MEMORY	SHEET 6
DEBUG	SHEET 7
ETHERNET INTERFACES	SHEET 8
EXPANSION CONNECTORS	SHEET 9
FLASH MEMORY	SHEET 10
POWER SUPPLY	SHEET 11
RESET CONFIGURATION & CLOCKING CIRCUITRY	SHEET 12
SERIAL I/O INTERFACES	SHEET 13
USB TRANSCEIVER	SHEET 14

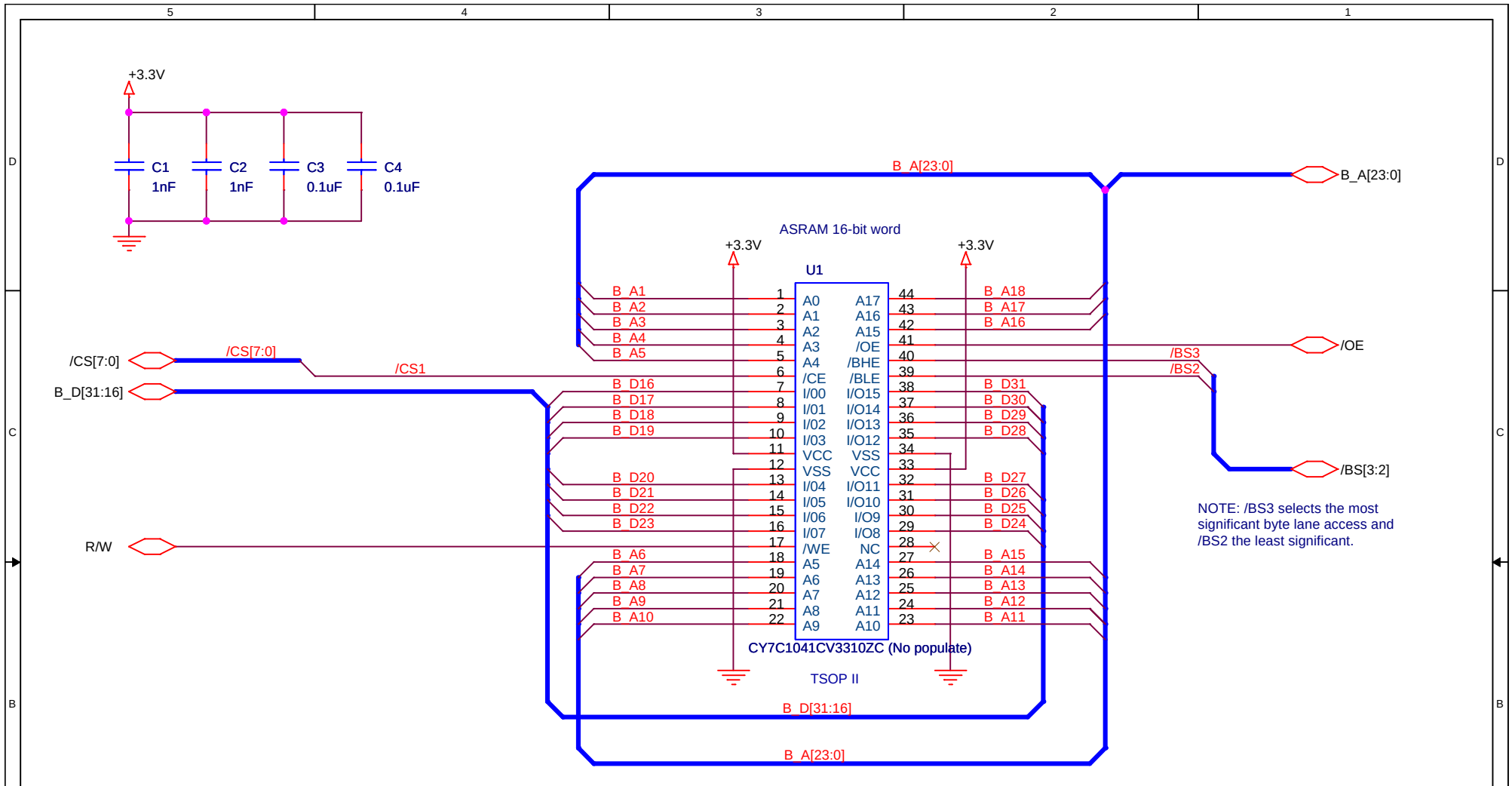
Revision Information

Rev	Date	Designer	Comments
0.7	13 May 04	PBH	Provisional release
0.8	16 June 04	PBH	Updated buffers/transceivers to be dual supply +2.5V & +3.3V
0.9	1 July 04	PBH	Added test points to all the DDR SDRAM signals.
A	21 July 04	PBH	Rev 1.0 released schematics for Rev 1.0 EVB
B	4 Aug 04	PBH	Rev B layout released to correct erroneous USB transceiver footprint
B	20 Oct 04	PBH	Removed C125 from the Vref supply to allow it to ramp quickly.
B	20 Jan 05	PBH	Corrected addressing on U12 32 Mbit Flash & comment on U27 USB transceiver.

Notes:

- All decoupling caps less than or equal to 0.1uF are COG SMD 0805 unless otherwise stated
- All decoupling caps greater than 0.1uF are X7R SMD 0805 unless otherwise stated
- All connectors are denoted Jx
- All jumpers are denoted JPx
- All Switches are denoted SWx
- All test points are denoted TPx
- All resistor packs (RPx) and resistors (Rx) are 1% tolerance unless stated otherwise


Sheet 11
PSU
Sheet 10
Flash Memory
Sheet 8
Ethernet
Sheet 7
Debug
Sheet 6
DDR SDRAM
Sheet 3
ASRAM
Sheet 4
Buffers
Sheet 9
Expansion Connectors
Sheet 5
CPU
Sheet 12
Reset Config & Clocks
Sheet 13
Serial I/O
Sheet 14
USB
B_A[23:0]
B_D[31:16]
/BS[3:2]
/CS[7:0]
/IRQ[7:1]
/TS
/OE
R/W
/TA
/TEA
/TIP
TSIZ0
TSIZ1
EIM_CLKOUT
EXTAL
XTAL
DDR_CLKOUT
/DDR_CLKOUT
/SD_CAS
/SD_RAS
SD_CKE
SD_A10
/SD_CS[1:0]
SD_DQS[1:0]
/SD_WE
FEC0_COL
FEC0_CRS
FEC0_MDC
FEC0_MDIO
FEC0_RXCLK
FEC0_RXD[3:0]
FEC0_RXDV
FEC0_RXER
FEC0_TXCLK
FEC0_TXD[3:0]
FEC0_TXEN
FEC0_TXER
FEC1_COL
FEC1_CRS
FEC1_MDC
FEC1_MDIO
FEC1_RXCLK
FEC1_RXD[3:0]
FEC1_RXDV
FEC1_RXER
FEC1_TXCLK
FEC1_TXD[3:0]
FEC1_TXEN
FEC1_TXER
CLKMOD[1:0]
JTAG_EN
/RCON
/RSTIN
/RSTOUT
TIN[3:0]
TOUT[3:0]
DDATA[3:0]
PST[3:0]
TCLK/PSTCLK
TDI/DSI
TDO/DSO
TMS/BKPT
TRST/DSCLK
/CTS0
/RTS0
RXD0
TXD0
/CTS1
/RTS1
RXD1
TXD1
/CTS2
/RTS2
RXD2
TXD2
SCL
SDA
PCS[3:0]
QSDI
QSDO
SCK
USB_CLK
USB_RN
USB_RP
USB_RXD
USB_SPEED
USB_SUSP
USB_TN
USB_TP
USB_TXEN
/EXT_RST
/ETH_CLK
/RSTOUT
/IRQ[7:1]
/ISD_WE
SD_DQS[1:0]
SD_CS[1:0]
SD_A10
SD_CKE
/SD_RAS
/SD_CAS
/DDR_CLKOUT
DDR_CLKOUT
/BS[3:2]
D[31:16]
A[23:0]
/TIP
Freescale Semiconductor - TSPG - TECD ColdFire Group
Title
M5275EVB
Size
C
Document Number
Hierarchical Block Diagram
Rev
B
Date:
Wednesday, September 22, 2004
Sheet
2
of
14



ASRAM is a 256K x 16bit (512KB) device

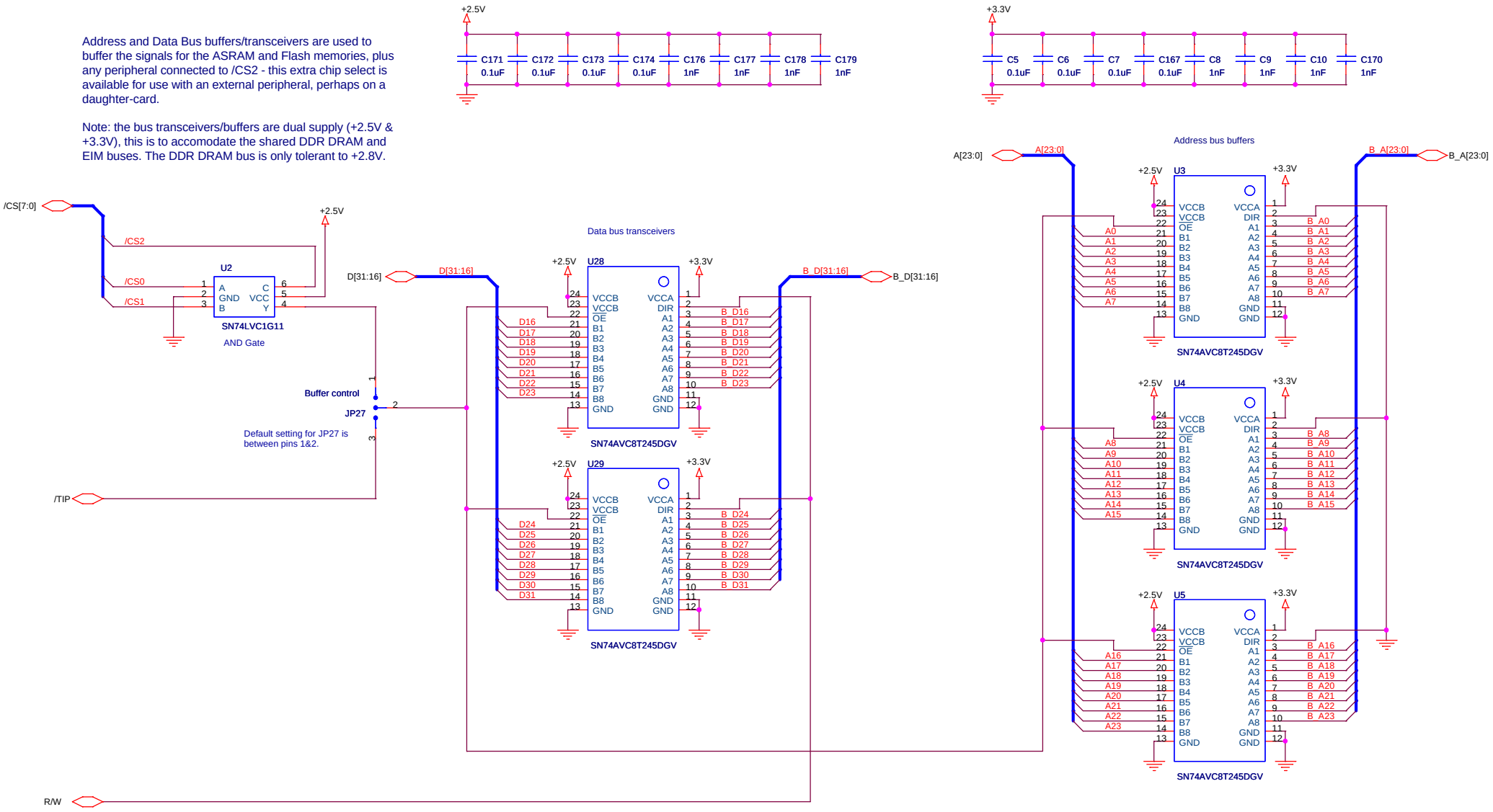
NOTE: Alternative ASRAM's with the same PCB footprint and functionality are :- Renesas HM62W16255HCJP-12

NOTE: Place the SMT footprint for the ASRAM's on the underside of the PCB close to the CPU U6.

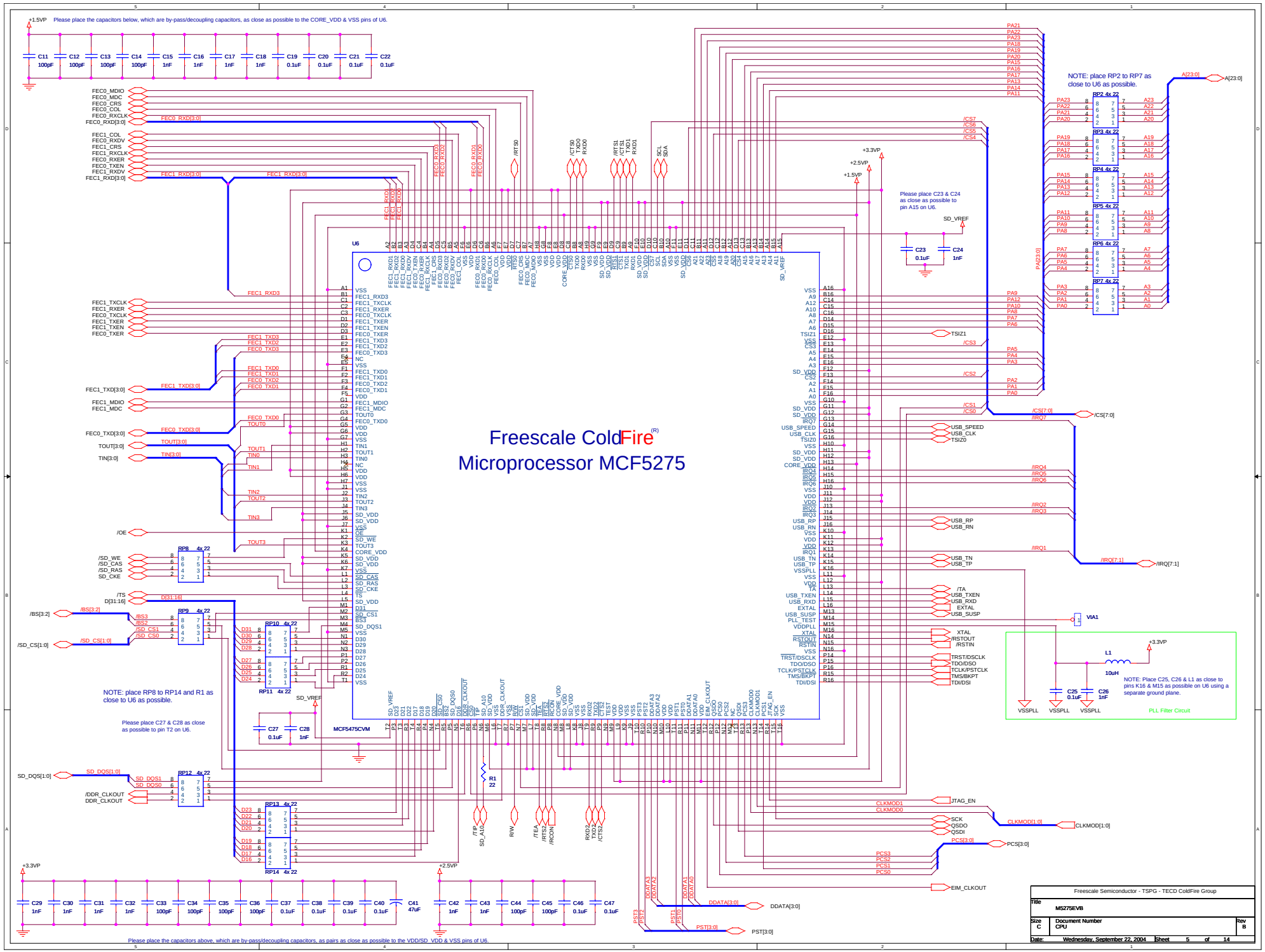
Freescale Semiconductor - TSPG - TECD ColdFire Group			
Title M5275EVB			
Size A	Document Number Asynchronous SRAM		Rev B
Date: Tuesday, December 07, 2004	Sheet 3 of 14		

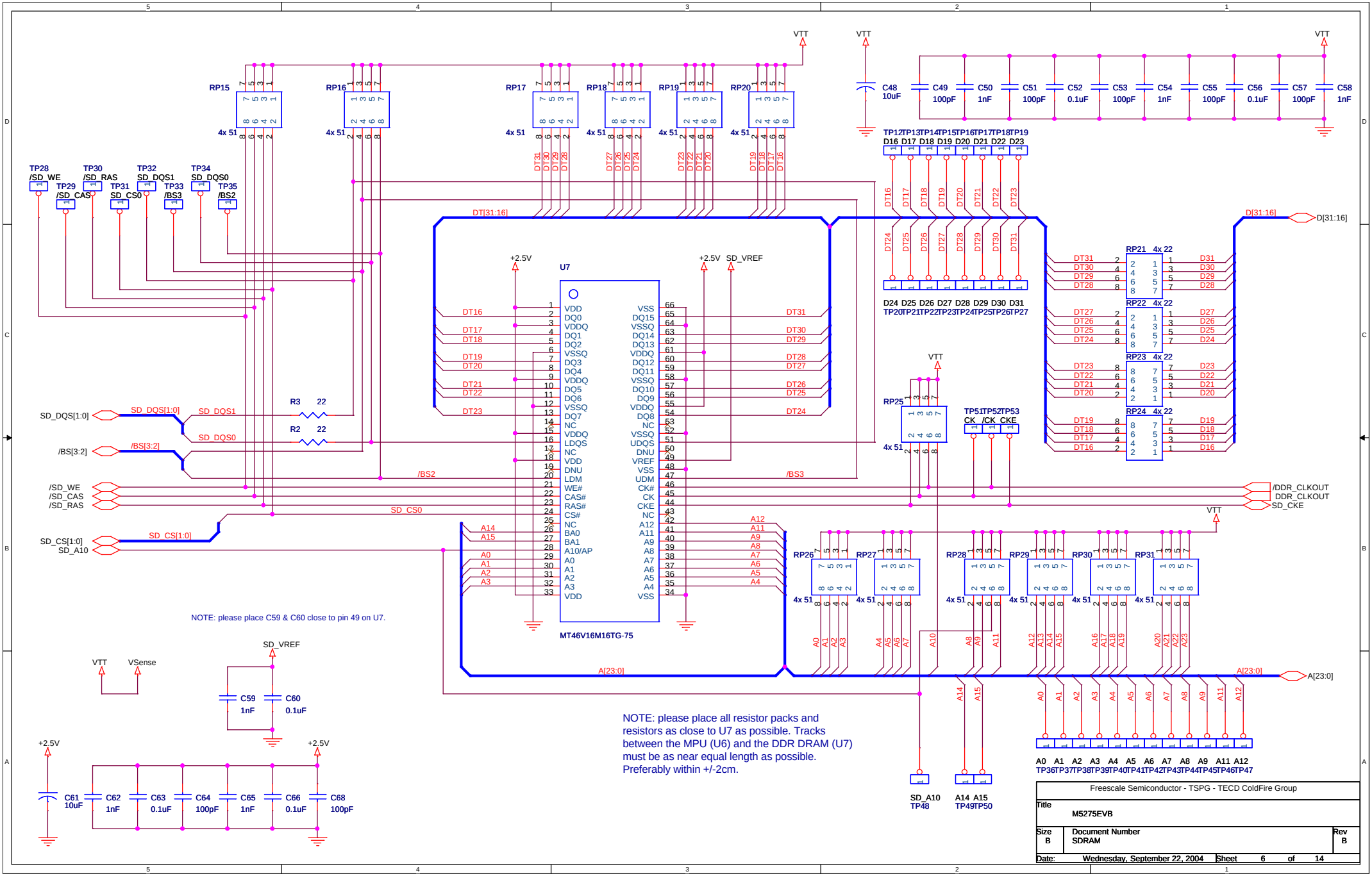
Address and Data Bus buffers/transceivers are used to buffer the signals for the ASRAM and Flash memories, plus any peripheral connected to /CS2 - this extra chip select is available for use with an external peripheral, perhaps on a daughter-card.

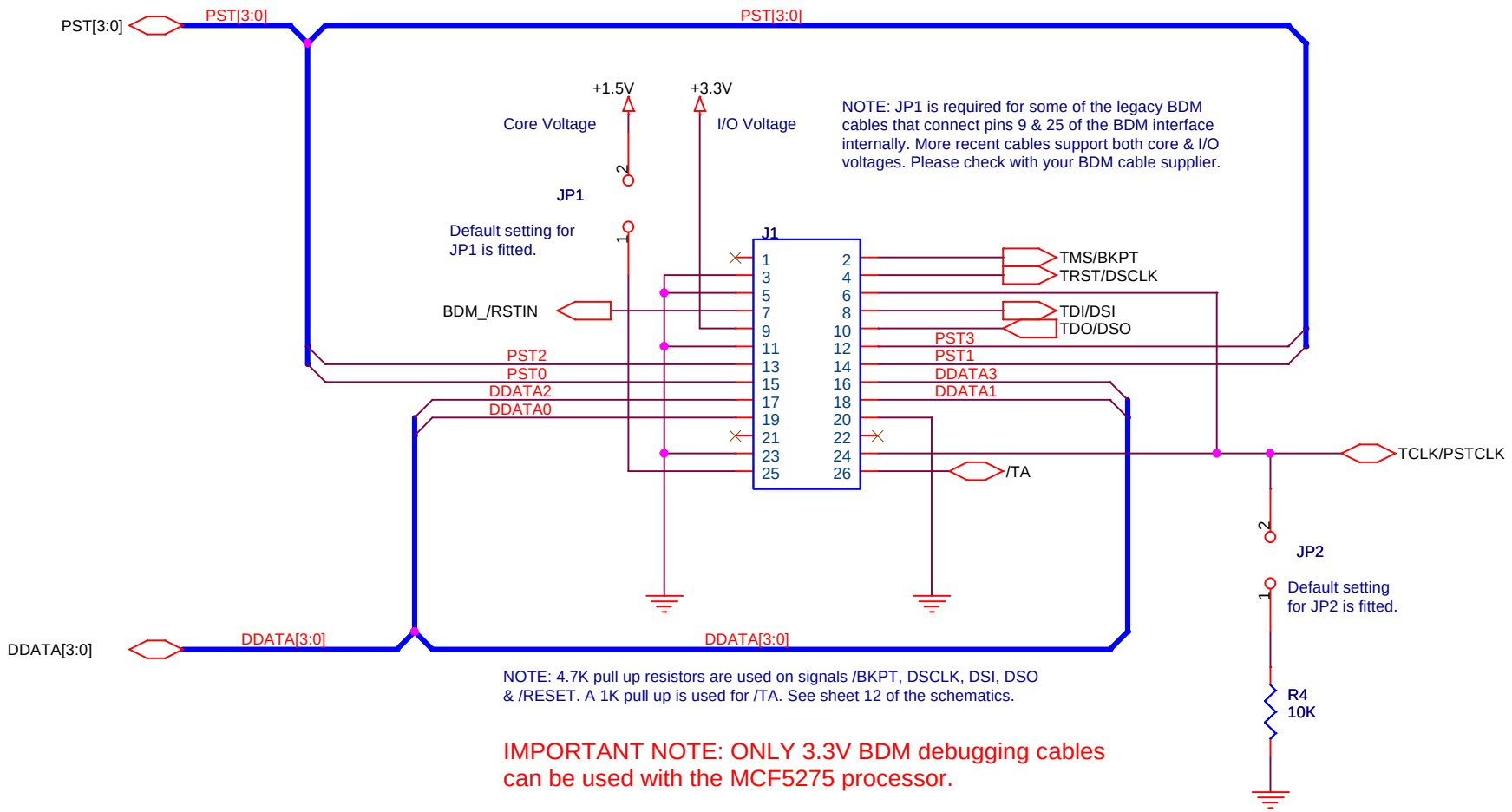
Note: the bus transceivers/buffers are dual supply (+2.5V & +3.3V), this is to accomodate the shared DDR DRAM and EIM buses. The DDR DRAM bus is only tolerant to +2.8V.



Freescale Semiconductor - TSPG - TECD ColdFire Group		
Title M5275EVB		
Size B	Document Number Buffers	Rev B
Date: Wednesday, September 22, 2004	Sheet 4 of 14	


Freescale ColdFire(R)
Microprocessor MCF5275
U6
MCF5475CVM
Please place the capacitors below, which are by-pass/decoupling capacitors, as close as possible to the CORE_VDD & VSS pins of U6.
NOTE: place RP2 to RP7 as close to U6 as possible.
Please place C23 & C24 as close as possible to pin A15 on U6.
Please place C27 & C28 as close as possible to pin T2 on U6.
NOTE: place RP8 to RP14 and R1 as close to U6 as possible.
NOTE: Place C25, C26 & L1 as close to pins K16 & M15 as possible on U6 using a separate ground plane.
PLL Filter Circuit
Please place the capacitors above, which are by-pass/decoupling capacitors, as pairs as close as possible to the VDD/SD_VDD & VSS pins of U6.
Freescale Semiconductor - TSPG - TECD ColdFire Group
Title
M5275EVB
Size C
Document Number CPU
Rev B
Date: Wednesday, September 22, 2004
Sheet 5 of 14

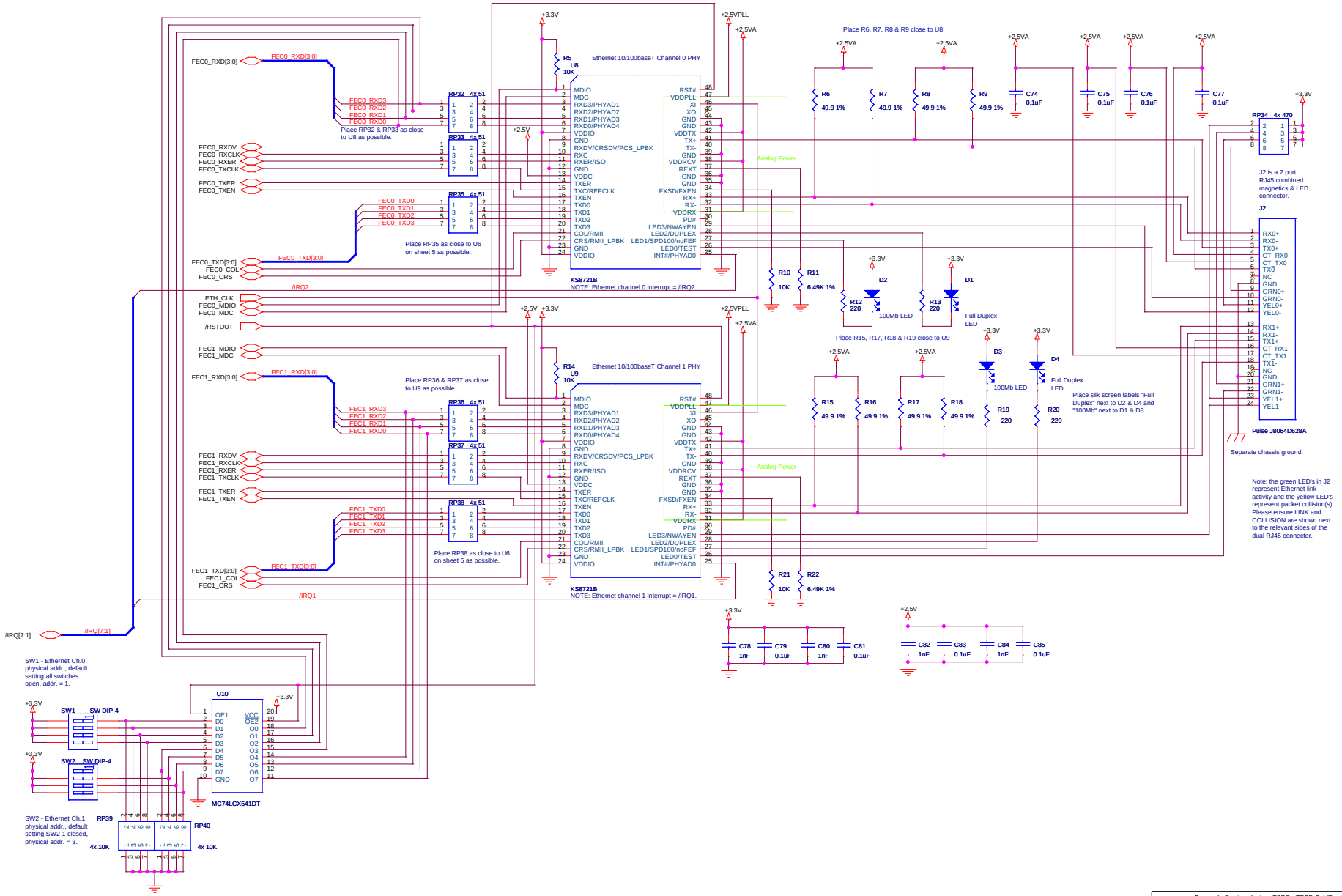

U7
MT46V16M16TG-75
RP15
RP16
RP17
RP18
RP19
RP20
RP21
RP22
RP23
RP24
RP25
RP26
RP27
RP28
RP29
RP30
RP31
4x 51
4x 22
C48 10uF
C49 100pF
C50 1nF
C51 100pF
C52 0.1uF
C53 100pF
C54 1nF
C55 100pF
C56 0.1uF
C57 100pF
C58 1nF
C59 1nF
C60 0.1uF
C61 10uF
C62 1nF
C63 0.1uF
C64 100pF
C65 1nF
C66 0.1uF
C68 100pF
R3 22
R2 22
VTT
VSense
SD_VREF
+2.5V
DT[31:16]
D[31:16]
A[23:0]
SD_DQS[1:0]
SD_DQS1
SD_DQS0
/BS[3:2]
/BS2
/BS3
/SD_WE
/SD_CAS
/SD_RAS
SD_CS0
SD_CS[1:0]
SD_A10
/DDR_CLKOUT
DDR_CLKOUT
SD_CKE
NOTE: please place C59 & C60 close to pin 49 on U7.
NOTE: please place all resistor packs and resistors as close to U7 as possible. Tracks between the MPU (U6) and the DDR DRAM (U7) must be as near equal length as possible. Preferably within +/-2cm.
Freescale Semiconductor - TSPG - TECD ColdFire Group
Title
M5275EVB
Size B
Document Number
SDRAM
Rev B
Date: Wednesday, September 22, 2004
Sheet 6 of 14



NOTE: 4.7K pull up resistors are used on signals /BKPT, DSCLK, DSI, DSO & /RESET. A 1K pull up is used for /TA. See sheet 12 of the schematics.

IMPORTANT NOTE: ONLY 3.3V BDM debugging cables can be used with the MCF5275 processor.

Freescale Semiconductor - TSPG - TECD ColdFire Group		
Title M5275EVB		
Size A	Document Number BDM/JTAG Debug Port	Rev B
Date: Wednesday, September 22, 2004	Sheet 7 of 14	

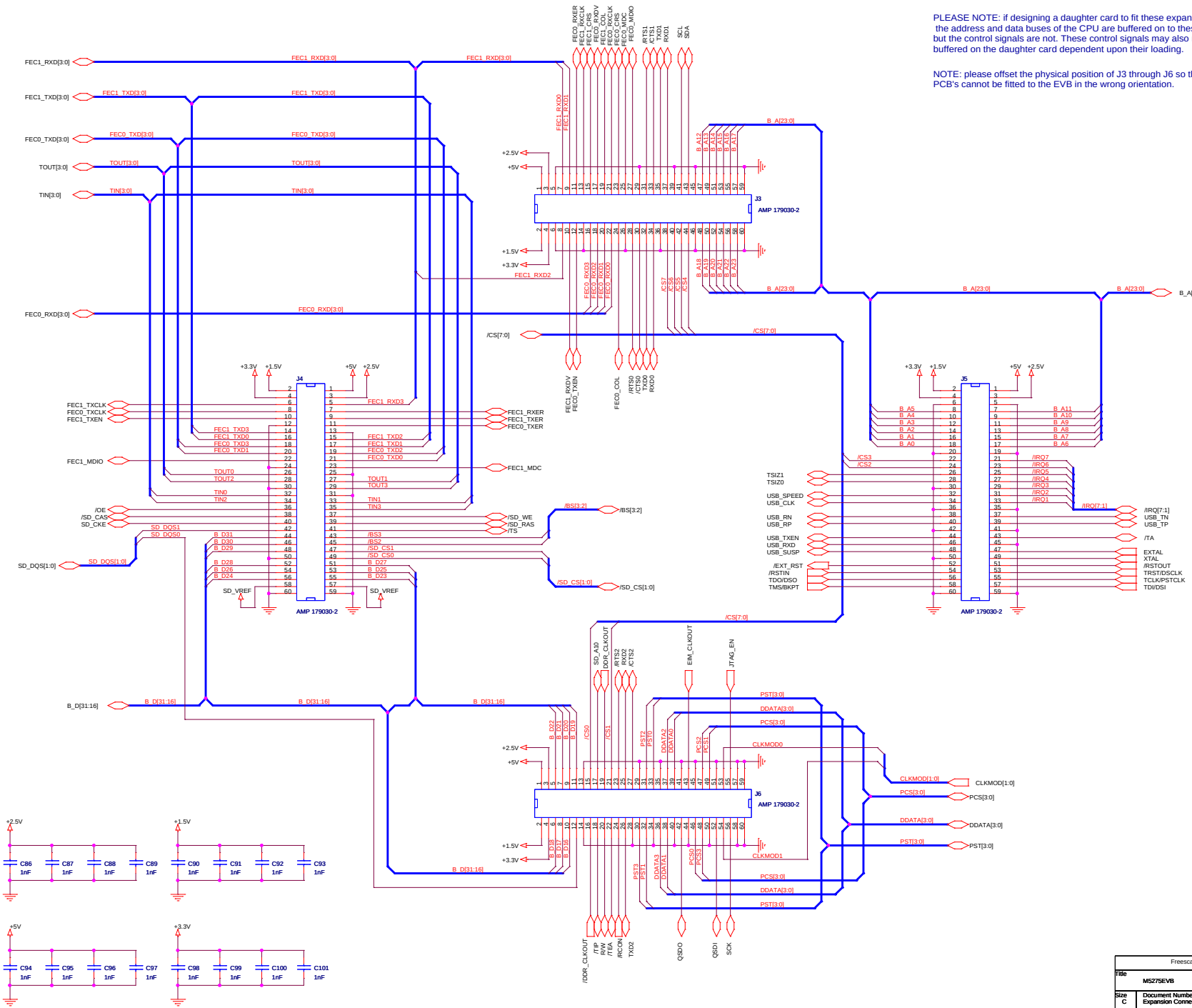


Freescale Semiconductor - TSPG - TECD ColdFire Group

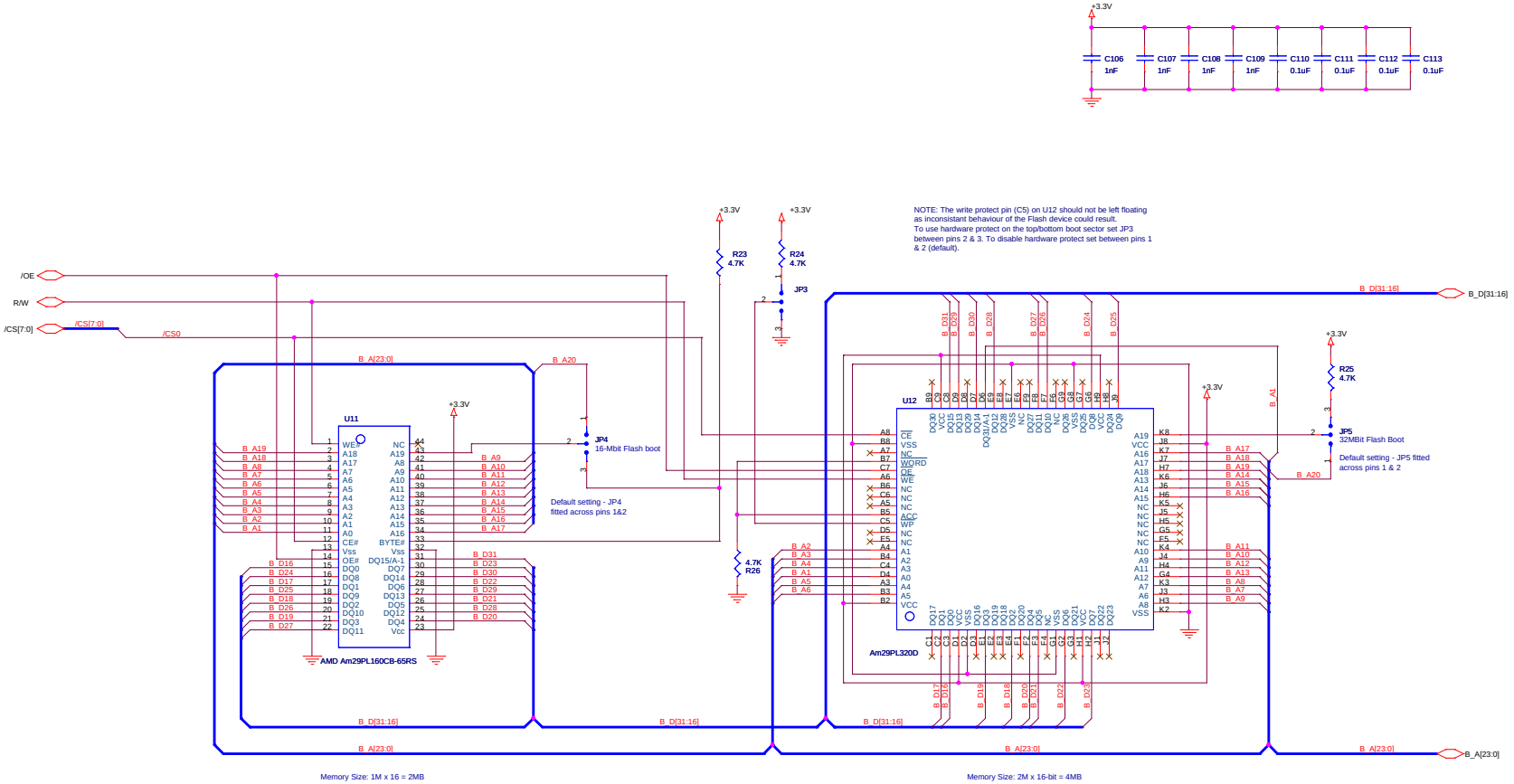
Title	M5275EVB	
Size C	Document Number 10/100BaseT Ethernet Transceiver	Rev B
Date: Wednesday, September 22, 2004	Sheet 8 of 14	

PLEASE NOTE: if designing a daughter card to fit these expansion connectors the address and data buses of the CPU are buffered on to these connectors, but the control signals are not. These control signals may also need to be buffered on the daughter card dependent upon their loading.

NOTE: please offset the physical position of J3 through J6 so that daughtercard PCB's cannot be fitted to the EVB in the wrong orientation.

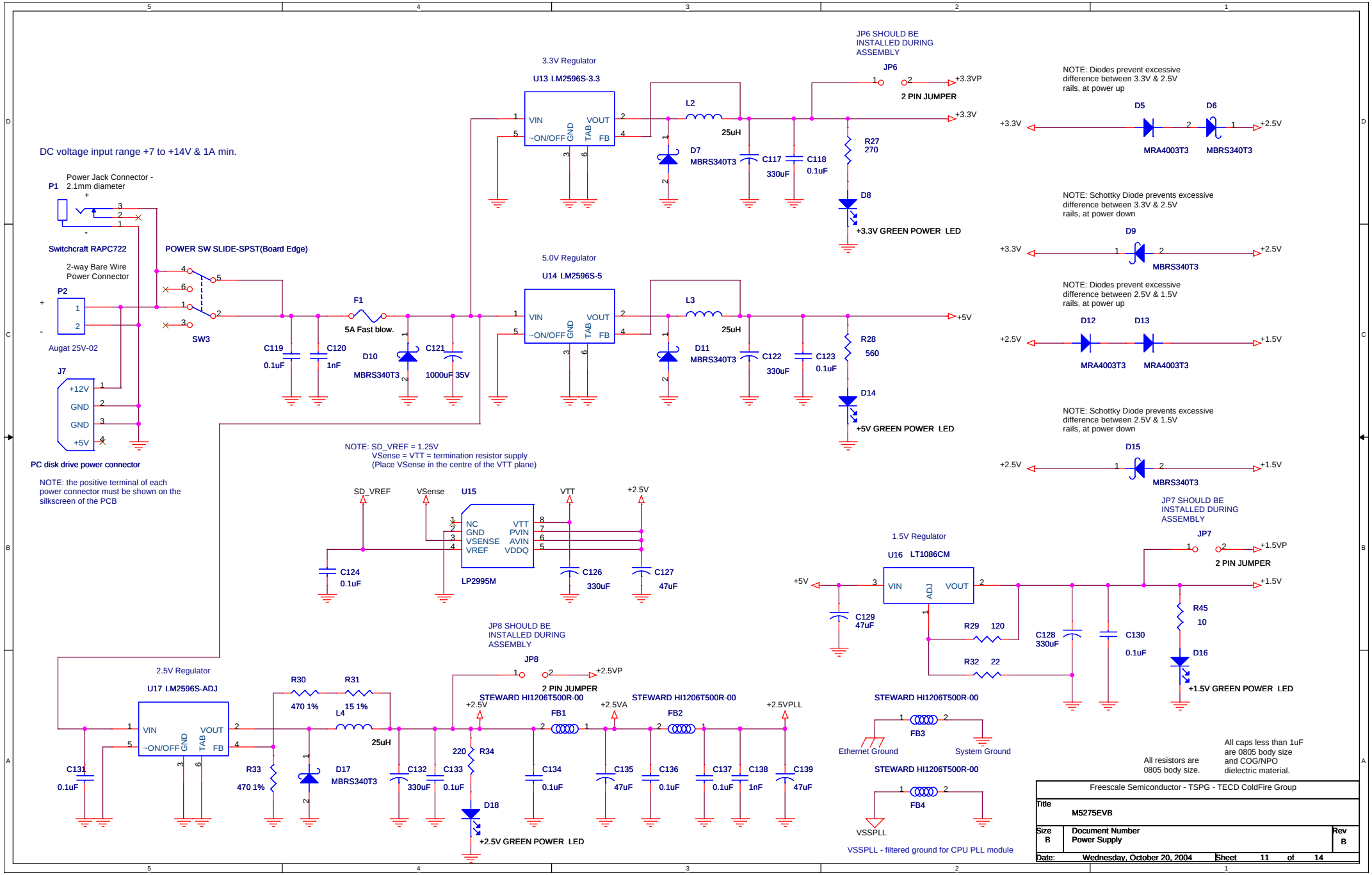


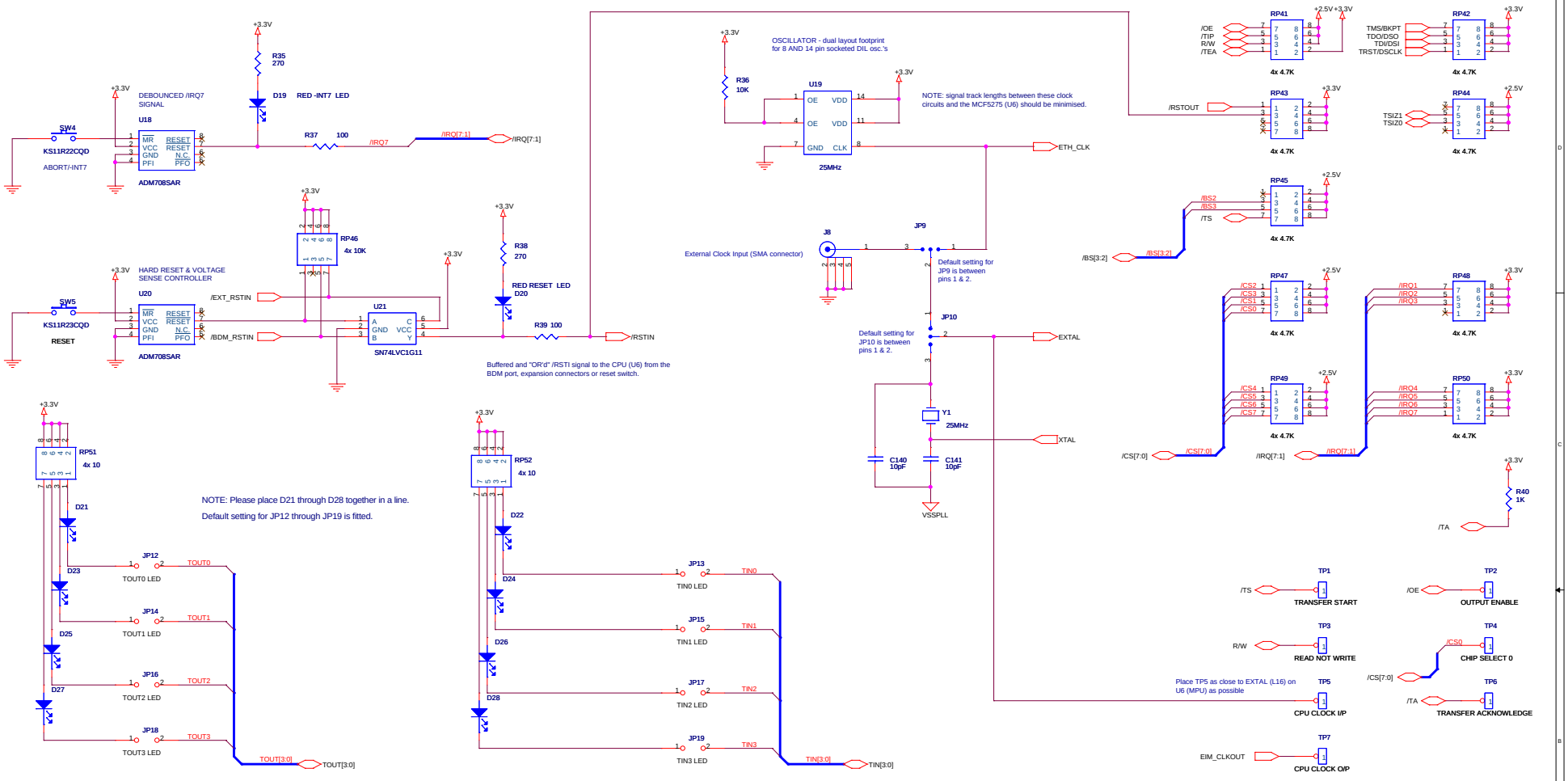
Freescale Semiconductor - TSPG - TECD ColdFire Group		
Title: M5275EVB		
Size: C	Document Number: Expansion Connectors	Rev: B
Date: Wednesday, September 22, 2004	Sheet 9 of 14	

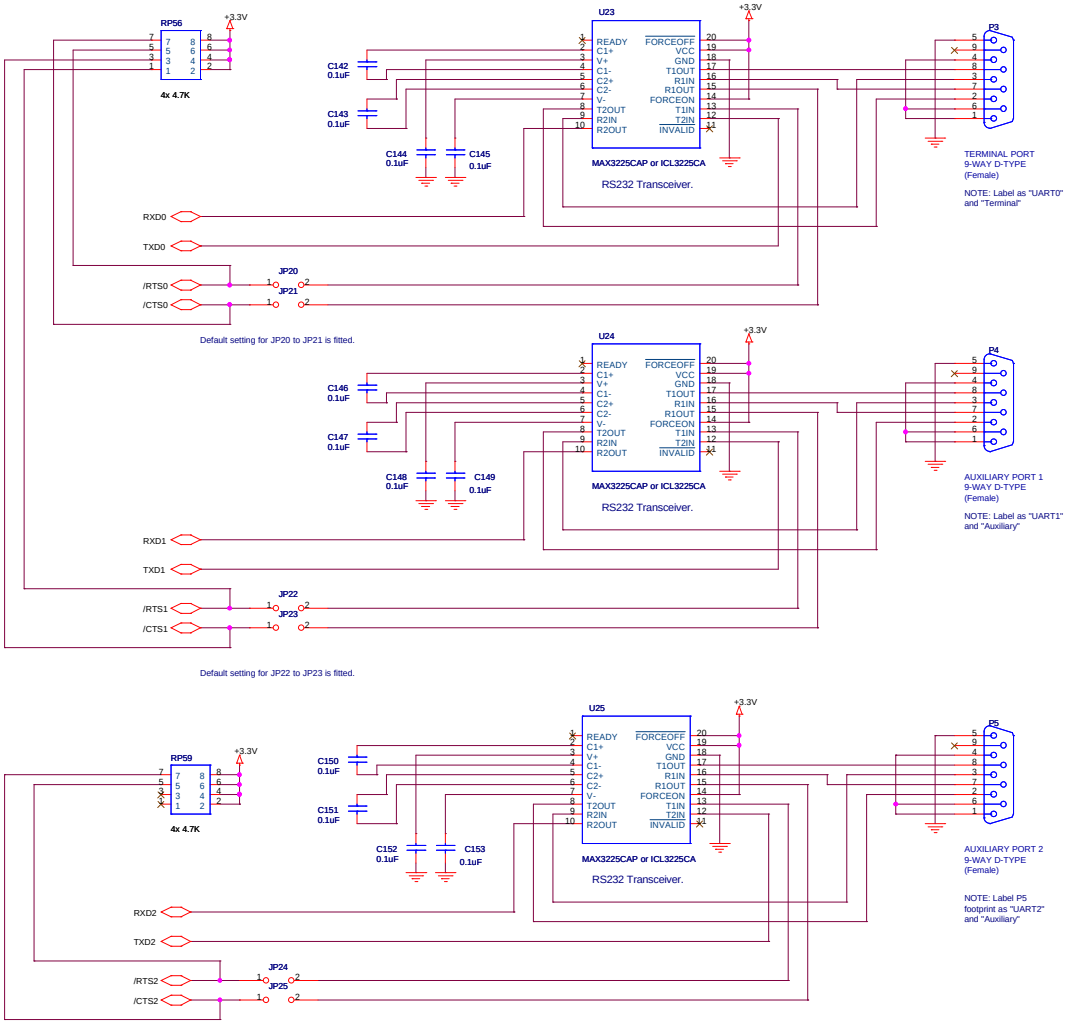


NOTE: only one of the footprints can/will be populated - BGA (U12) OR SSOP (U11)

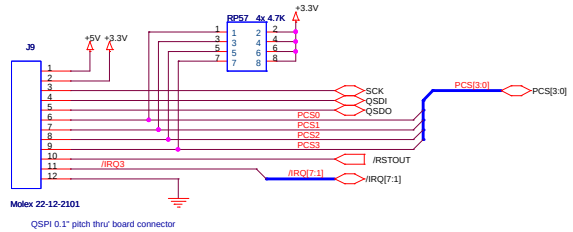
Freescale Semiconductor - TSPG - TECD ColdFire Group			
Title	M5275EVB		
Size C	Document Number Flash Memory		Rev B
Date: Thursday, January 20, 2005	Sheet 10 of 14		


DC voltage input range +7 to +14V & 1A min.
P1
Power Jack Connector - 2.1mm diameter
Switchcraft RAPC722
POWER SW SLIDE-SPST(Board Edge)
2-way Bare Wire Power Connector
P2
Augat 25V-02
J7
+12V
GND
GND
+5V
PC disk drive power connector
NOTE: the positive terminal of each power connector must be shown on the silkscreen of the PCB
SW3
C119 0.1uF
C120 1nF
F1
5A Fast blow.
D10 MBRS340T3
C121 1000uF 35V
3.3V Regulator
U13 LM2596S-3.3
VIN
VOUT
~ON/OFF
GND
TAB
FB
L2 25uH
D7 MBRS340T3
C117 330uF
C118 0.1uF
JP6 SHOULD BE INSTALLED DURING ASSEMBLY
JP6
2 PIN JUMPER
+3.3VP
+3.3V
R27 270
D8
+3.3V GREEN POWER LED
5.0V Regulator
U14 LM2596S-5
L3 25uH
D11 MBRS340T3
C122 330uF
C123 0.1uF
+5V
R28 560
D14
+5V GREEN POWER LED
NOTE: SD_VREF = 1.25V
VSense = VTT = termination resistor supply
(Place VSense in the centre of the VTT plane)
SD_VREF
VSense
U15
NC
GND
VSENSE
VREF
VTT
PVIN
AVIN
VDDQ
LP2995M
VTT
+2.5V
C124 0.1uF
C126 330uF
C127 47uF
2.5V Regulator
U17 LM2596S-ADJ
C131 0.1uF
R30 470 1%
R31 15 1%
L4 25uH
R33 470 1%
D17 MBRS340T3
C132 330uF
C133 0.1uF
JP8 SHOULD BE INSTALLED DURING ASSEMBLY
JP8
2 PIN JUMPER
+2.5VP
+2.5V
220 R34
D18
+2.5V GREEN POWER LED
STEWARD HI1206T500R-00
FB1
+2.5VA
FB2
+2.5VPLL
C134 0.1uF
C135 47uF
C136 0.1uF
C137 0.1uF
C138 1nF
C139 47uF
NOTE: Diodes prevent excessive difference between 3.3V & 2.5V rails, at power up
D5 MRA4003T3
D6 MBRS340T3
+3.3V
+2.5V
NOTE: Schottky Diode prevents excessive difference between 3.3V & 2.5V rails, at power down
D9 MBRS340T3
NOTE: Diodes prevent excessive difference between 2.5V & 1.5V rails, at power up
D12 MRA4003T3
D13 MRA4003T3
+1.5V
NOTE: Schottky Diode prevents excessive difference between 2.5V & 1.5V rails, at power down
D15 MBRS340T3
JP7 SHOULD BE INSTALLED DURING ASSEMBLY
JP7
2 PIN JUMPER
+1.5VP
+1.5V
1.5V Regulator
U16 LT1086CM
VIN
ADJ
VOUT
+5V
C129 47uF
R29 120
R32 22
C128 330uF
C130 0.1uF
R45 10
D16
+1.5V GREEN POWER LED
STEWARD HI1206T500R-00
FB3
Ethernet Ground
System Ground
FB4
VSSPLL
VSSPLL - filtered ground for CPU PLL module
All resistors are 0805 body size.
All caps less than 1uF are 0805 body size and COG/NPO dielectric material.
Freescale Semiconductor - TSPG - TECD ColdFire Group
Title
M5275EVB
Size B
Document Number
Power Supply
Rev B
Date: Wednesday, October 20, 2004
Sheet 11 of 14

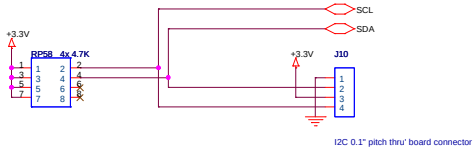

DEBOUNCED /IRQ7 SIGNAL
U18
SW4
KS11R22CQD
ABORT/-INT7
ADM708SAR
D19 RED -INT7 LED
R35 270
R37 100
/IRQ7
/IRQ[7:1]
HARD RESET & VOLTAGE SENSE CONTROLLER
U20
SW5
KS11R23CQD
RESET
/EXT_RSTIN
/BDM_RSTIN
RP46 4x 10K
U21
SN74LVC1G11
R38 270
RED RESET LED D20
R39 100
/RSTIN
Buffered and "OR'd" /RSTI signal to the CPU (U6) from the BDM port, expansion connectors or reset switch.
OSCILLATOR - dual layout footprint for 8 AND 14 pin socketed DIL osc.'s
R36 10K
U19
25MHz
NOTE: signal track lengths between these clock circuits and the MCF5275 (U6) should be minimised.
ETH_CLK
External Clock Input (SMA connector)
J8
JP9
Default setting for JP9 is between pins 1 & 2.
JP10
Default setting for JP10 is between pins 1 & 2.
EXTAL
XTAL
Y1 25MHz
C140 10pF
C141 10pF
VSSPLL
RP41 4x 4.7K
/OE
/TIP
R/W
/TEA
RP42 4x 4.7K
TMS/BKPT
TDO/DSO
TDI/DSI
TRST/DSCLK
RP43 4x 4.7K
/RSTOUT
RP44 4x 4.7K
TSIZ1
TSIZ0
RP45 4x 4.7K
/BS2
/BS3
/TS
/BS[3:2]
RP47 4x 4.7K
/CS2
/CS3
/CS1
/CS0
RP48 4x 4.7K
/IRQ1
/IRQ2
/IRQ3
RP49 4x 4.7K
/CS4
/CS5
/CS6
/CS7
RP50 4x 4.7K
/IRQ4
/IRQ5
/IRQ6
/IRQ7
/CS[7:0]
/IRQ[7:1]
R40 1K
/TA
RP51 4x 10
D21
D23
D25
D27
JP12
JP14
JP16
JP18
TOUT0 LED
TOUT1 LED
TOUT2 LED
TOUT3 LED
TOUT0
TOUT1
TOUT2
TOUT3
TOUT[3:0]
NOTE: Please place D21 through D28 together in a line.
Default setting for JP12 through JP19 is fitted.
RP52 4x 10
D22
D24
D26
D28
JP13
JP15
JP17
JP19
TIN0 LED
TIN1 LED
TIN2 LED
TIN3 LED
TIN0
TIN1
TIN2
TIN3
TIN[3:0]
TP1 TRANSFER START
TP2 OUTPUT ENABLE
TP3 READ NOT WRITE
TP4 CHIP SELECT 0
TP5 CPU CLOCK I/P
TP6 TRANSFER ACKNOWLEDGE
TP7 CPU CLOCK O/P
EIM_CLKOUT
Place TP5 as close to EXTAL (L16) on U6 (MPU) as possible
TP8 GROUND
TP9 GROUND
TP10 GROUND
TP11 GROUND
NOTE: Place TP8, TP9, TP10 & TP11 at the corners of the PCB to allow easy connection of 'scope probe ground leads.
OFF - SW6 - ON
Chip Config. Off 1 Chip Config. On *
JTAG Interface Enabled 2 BDM Interface Enabled *
Encoded Clock Mode 3 Encoded Clock Mode
Encoded Clock Mode 4 Encoded Clock Mode
Encoded Oper. Mode 5 Encoded Oper. Mode
Encoded Oper. Mode 6 Encoded Oper. Mode
Encoded Oper. Mode 7 Encoded Oper. Mode
Encoded Boot Device 8 Encoded Boot Device
Encoded Boot Device 9 Encoded Boot Device
Partial Bus Drive 10 Full Bus Drive *
Encoded Address Mode 11 Encoded Address Mode
Encoded Address Mode 12 Encoded Address Mode
RP53 4x 4.7K
RP54 4x 4.7K
RP55 4x 4.7K
IMPORTANT NOTE: THE /RSTOUT SIGNAL MUST BE USED TO DRIVE THE OUTPUT ENABLE PINS OF U22 TO ALLOW THE D16, D17, D19, D20, D21, D24, D25 & D26 SIGNALS TO BE LATCHED CORRECTLY BY THE MCF5274/5 FOR CONFIGURATION AT RESET.
/RCON
JTAG_EN
CLKMOD1
CLKMOD0
CLKMOD[1:0]
Closed/On SW6 Open/Off
Configuration DIP switch - Grayhill 78RB12
U22
SN74AVC8T245DGV
D16
D17
D26
D19
D20
D21
D24
D25
D[31:16]
Note: default setting for SW6 is all switches closed/on.
Important Note - all unconnected pull-up and pull-down resistor pack connections, on all schematics pages, need to be connected to an unmasked via.
Encoded Clock Mode
SW6-3 SW6-4 Mode
OFF OFF 1:1 PLL
OFF ON External Clock - (PLL disabled)
ON OFF Normal PLL operation (Ext. Crystal)
ON ON Normal PLL operation (Ext. Clock) *
Encoded Chip Operating Mode
SW6-5 SW6-6 SW6-7 Mode
ON ON ON Master *
ON ON OFF Reserved
ON OFF ON Reserved
ON OFF OFF Reserved
OFF X X Reserved
Encoded Boot Device (Port Size)
SW6-8 SW6-9 Mode
OFF OFF External (8-bit)
OFF ON External (32-bit)
ON OFF External (32-bit)
ON ON External (16-bit) *
Output Pad Drive Strength
SW6-10 Mode
OFF Partial
ON Full *
Encoded Address/Chip Select Mode
SW6-11 SW6-12 Mode
OFF OFF PF[7:5] = /CS[6:4]
OFF ON PF7 = /CS6, PF[6:5] = A[22:21]
ON OFF PF[7:6] = /CS[6:5], PF[5] = A21
ON ON PF[7:5] = A[23:21] *
NOTE: Please place these tables on the silkscreen on the topside of the PCB close to SW6, * = default setting.
Freescale Semiconductor - TSPG - TECD ColdFire Group
Title M5275EVB
Size C
Document Number Reset Configuration & Clock selection
Rev B
Date: Wednesday, January 12, 2005
Sheet 12 of 14



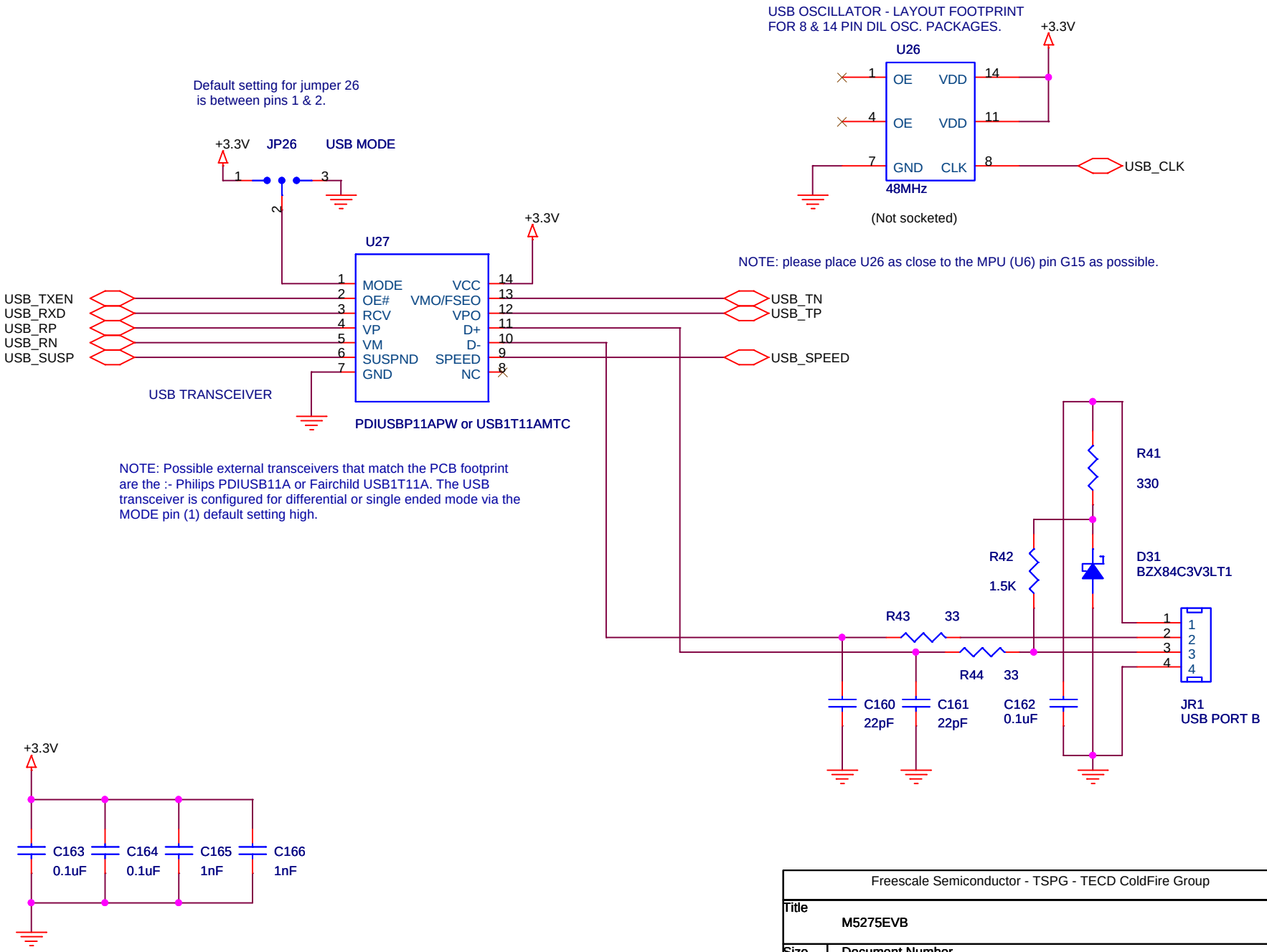
NOTE: J9, the QSPI connector, has additional signals (/RSTOUT & /IRQ3) connected to it to afford a wider range of functionality in any QSPI peripherals connected.



NOTE: the I2C bus on the MCF5275 processor is 3.3V tolerant only. If connection to a 5V system is required high frequency voltage level shifters will be required between the peripheral and processor.



Freescale Semiconductor - TSPG - TECD ColdFire Group		
Title M5275EVB		
Size C	Document Number Serial I/O	Rev B
Date: Wednesday, September 22, 2004	Sheet 13 of 14	



Freescale Semiconductor - TSPG - TECD ColdFire Group		
Title M5275EVB		
Size A	Document Number USB I/F	Rev B
Date: Thursday, January 20, 2005	Sheet 14 of 14	