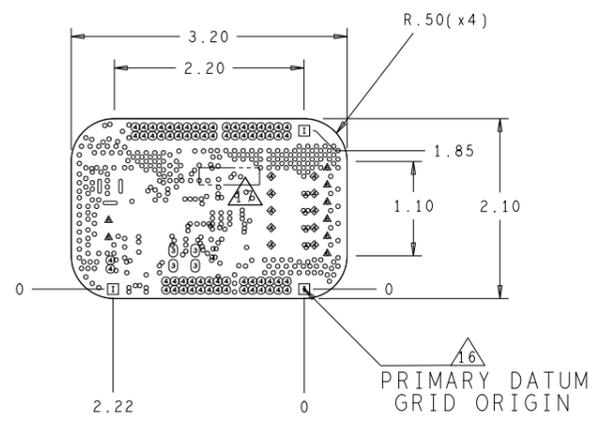


NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).
2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98
T_g - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
T_d - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
5. CHARACTERISTIC IMPEDANCE - NONE
6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .005"/.005"
7. PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
.05080-.232 MICRON (2-8 MICROINCH) OF GOLD OVER
2.540-6.350 MICRON (100-250 MICROINCH) OF NICKEL.
8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.
9. SOLDERMASK - GREEN COLOR, BOTH SIDES.
MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM FREESCALE.
10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.
11. ELECTRICAL TEST - 100% IPCD356.
12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.
13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS.
UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE.
14. TEARDROPS MAYBE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.
15. 2 SOLDER SAMPLES TO BE PROVIDED.
16. BASIC GRID INCREMENT AT 1:1 IS .0001.
17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
- MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0
18. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (Pb)
19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)
20. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP.
ALL HOLE LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM.
21. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS.
THE ADDITION OF RAILS AND .125' NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	11-20-14	A. M.
	B	PILOT RELEASE	04-15-15	A. M.
	C	PRODUCTION RELEASE	07-24-15	A. M.
	D	BOM UPDATE	09-15-15	A. M.
	E	BOM UPDATE	12-14-15	A. M.
	F	BOM UPDATE & ASSY FEEDBACK	01-21-16	A. M.



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
○	10.0	+0.0/-10.0	PLATED	348
⊙	39.0	+4.0/-0.0	PLATED	4
⊕	40.0	+3.0/-3.0	PLATED	64
⊖	40.0	+4.0/-2.0	PLATED	2
⊗	45.0	+3.0/-3.0	PLATED	10
△	63.0	+3.0/-3.0	PLATED	8
□	125.0	+3.0/-3.0	NON-PLATED	3
○	165.0x40.0	+3.0/-3.0	PLATED	1
□	165.0x40.0	+3.0/-3.0	PLATED	2

.063" THICK +/-10% FINISHED Cu WEIGHT

	LAYER 1	COMPONENT SIDE	1 oz.
	LAYER 2	SOLDER SIDE	1 oz.

DETAIL A
LAYER STACKUP
SCALE: NONE

PART NO. 170-28552		NXP SEMICONDUCTORS	
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6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA		TITLE: PRINTED WIRING BOARD FRDM-12XSF-EVB	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS ANGLES .XX .01 .0-30' .XXX .005 ✓ FMS ALL MACHINED SURFACES BREAK ALL SHARP EDGES AND CORNERS. REMOVE BURRS. UNDERLINED DIM. NOT TO SCALE. THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.	APPROVALS DRAWN neuronPro-RCC02C CHECKED ANDREW MacDONALD DESIGN ENGINEER THOMAS MAZEAUD	DATE 01-21-16 01-21-16 01-21-16	SIZE CAD FILE NAME DWG. NO. REV D LAY-28552 FAB-28555 E
SCALE 1/1		DO NOT SCALE DRAWING SHEET 1 OF 1	