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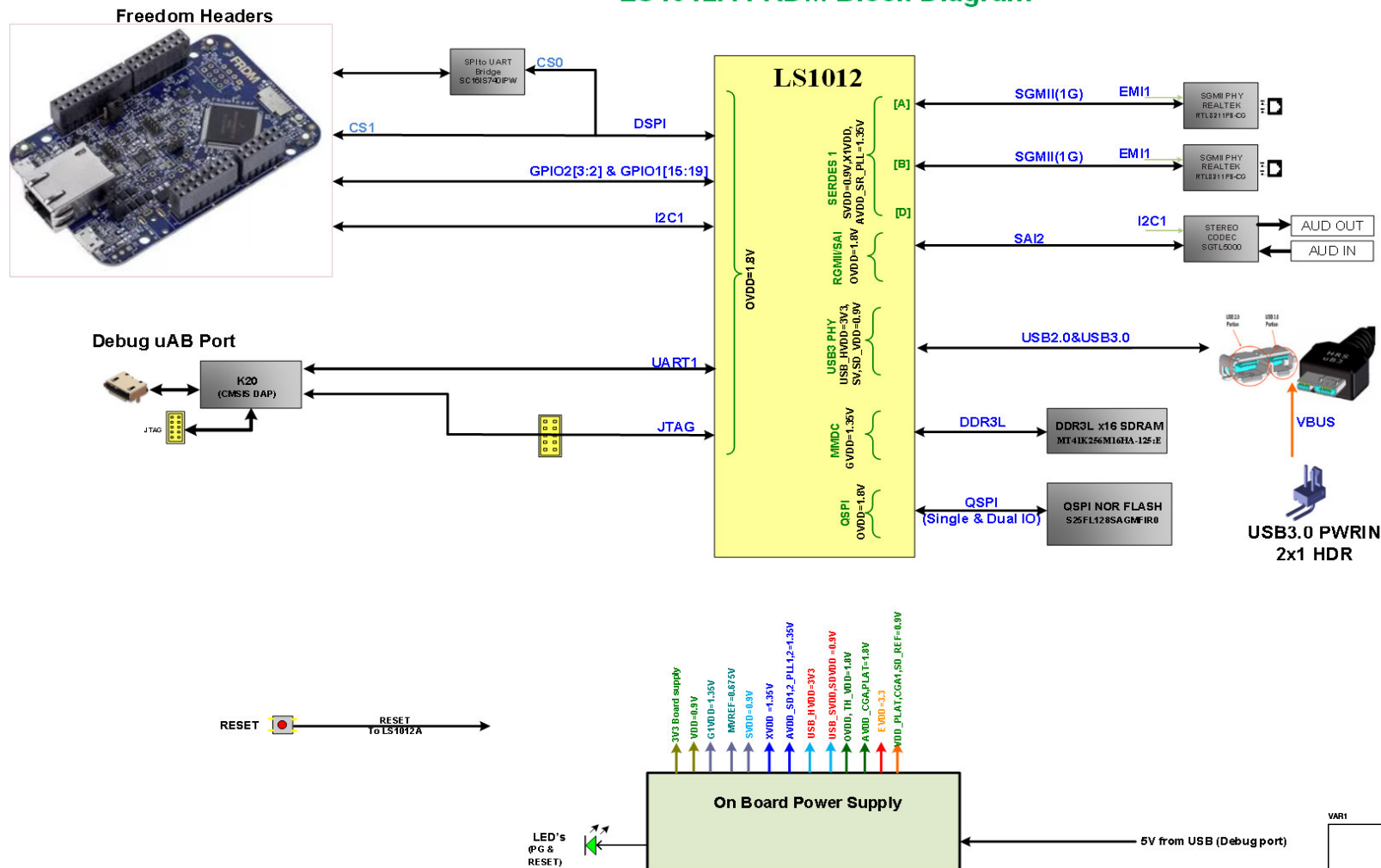
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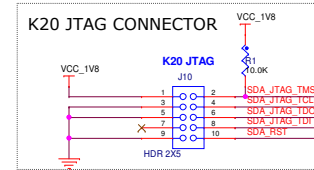
LS1012A FRDM REV - C

All information is subject to change without notice.
No warranty, expressed or applied, is made as to the accuracy of the information contained herein. This schematic is provided for reference purposes only. Contact your NXP representative to obtain the latest information on this product.

Rev	Date	Changes
X1	01/03/2016	First Release
A	14/04/2016	A85 Release
AX1	05/05/2016	A70 for ETH address change errata.
B	06/05/2016	A85 Release
BX1	02/08/2016	A70 Release; Rev B erratas fixed.
C	26/09/2016	A85 Release

LS1012A FRDM Block Diagram



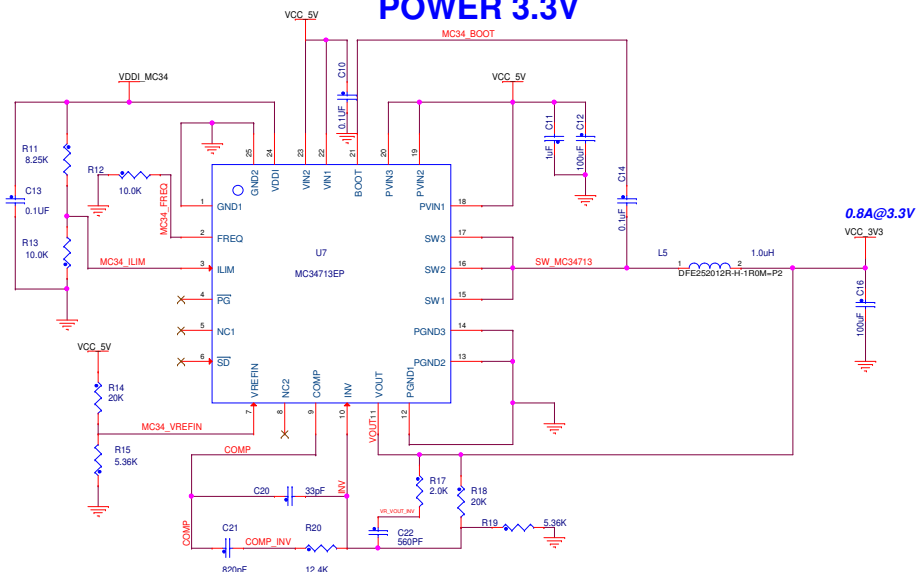


POWER IN

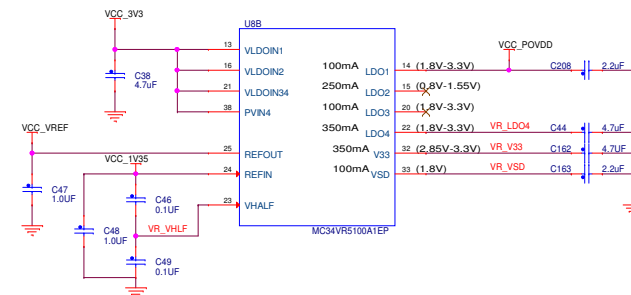
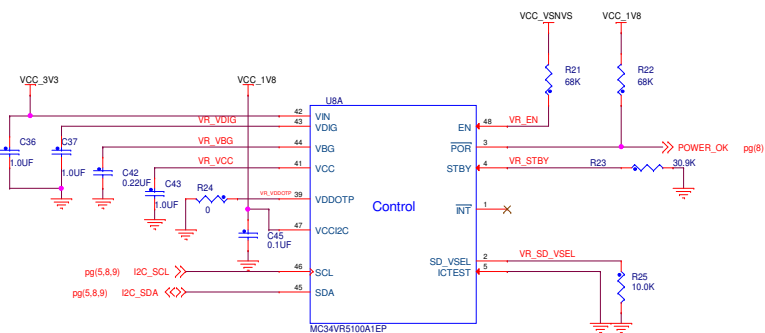
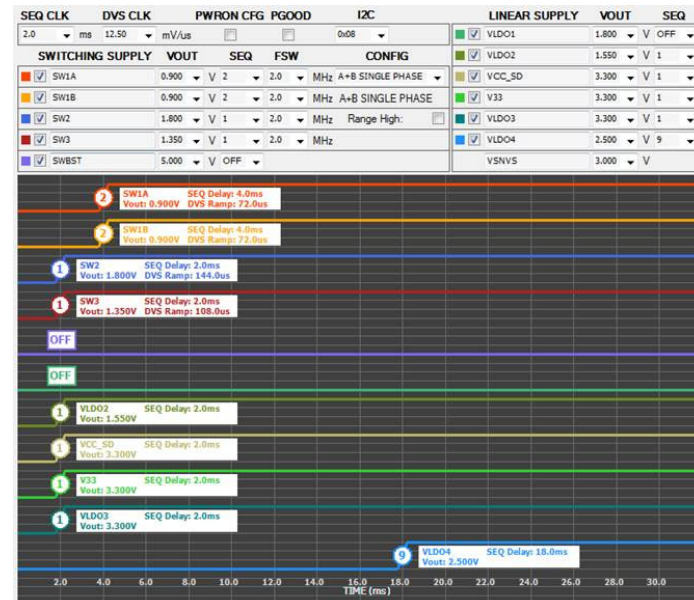
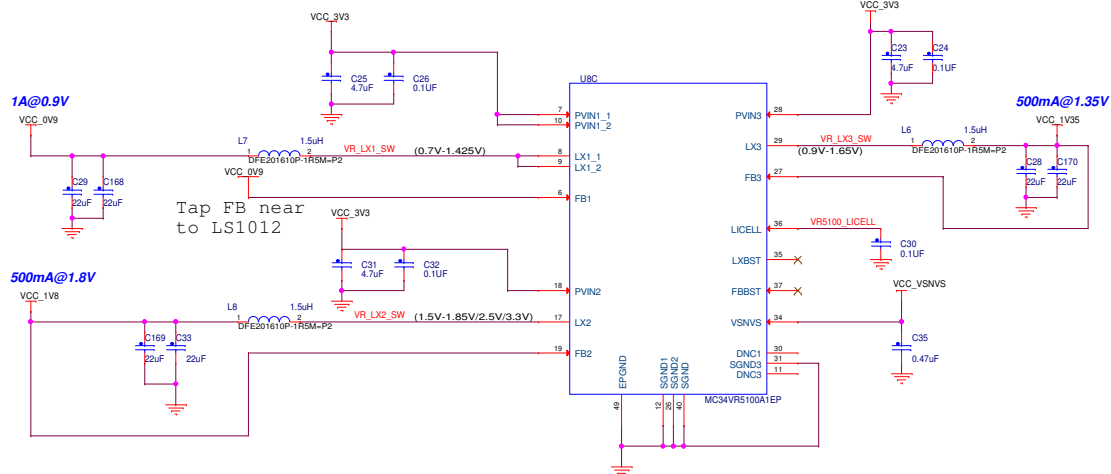
1A@5V (2 USB power ports on CMSIS USB port)



POWER 3.3V



VR5100



ICAP Classification: GP: X IUC: PUB: _____

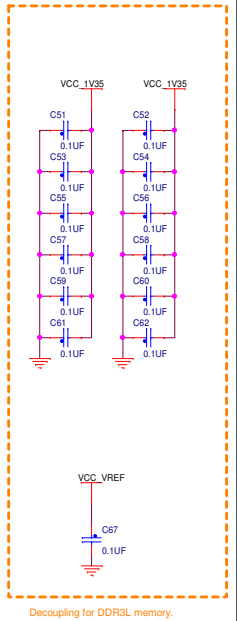
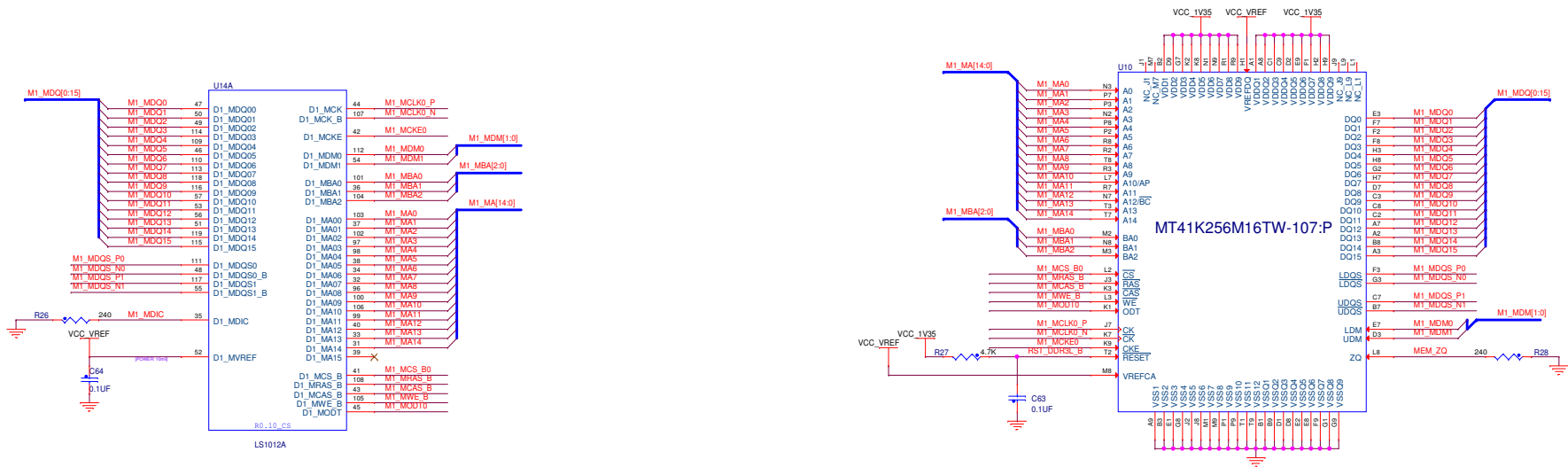
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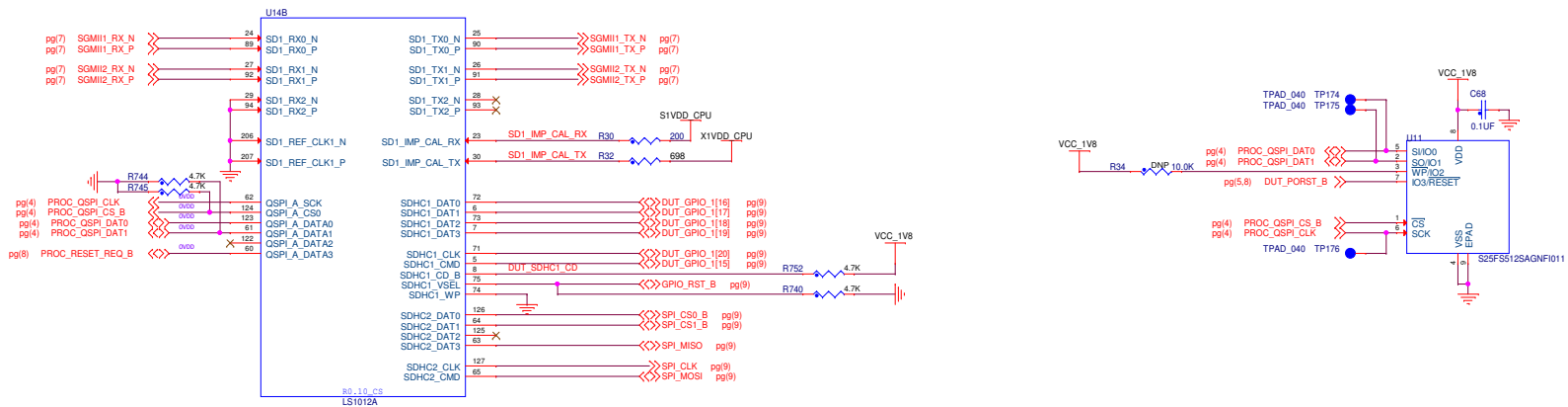
Size C Document Number SCH-29217 PDF: SPF-29217 Rev C

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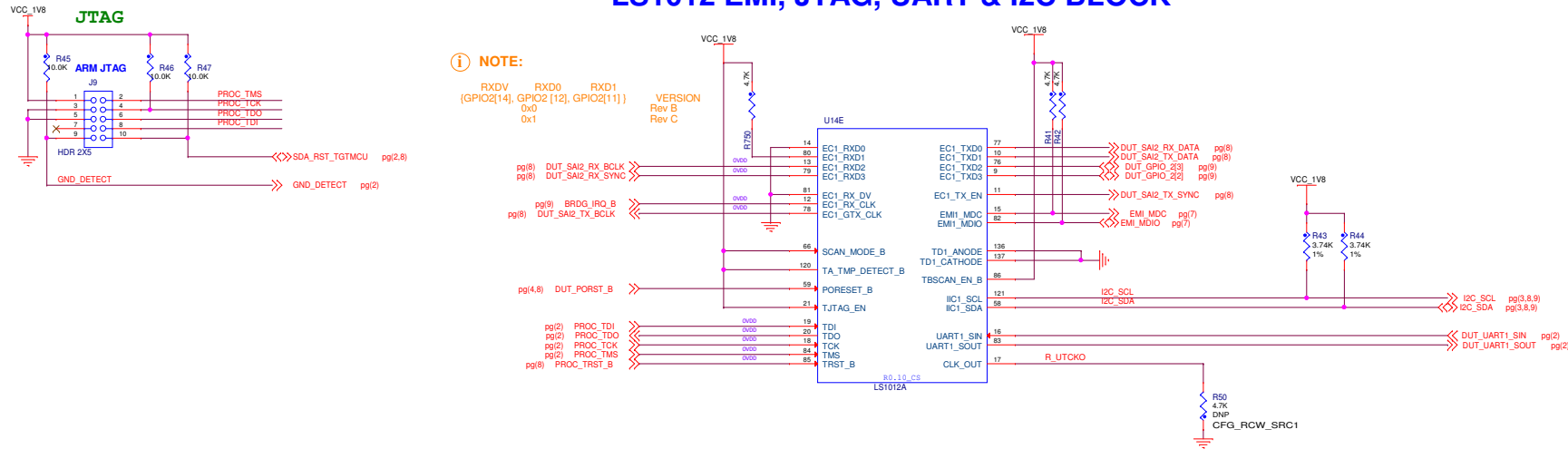
LS1012 DDR3L CONTROLLER BLOCK



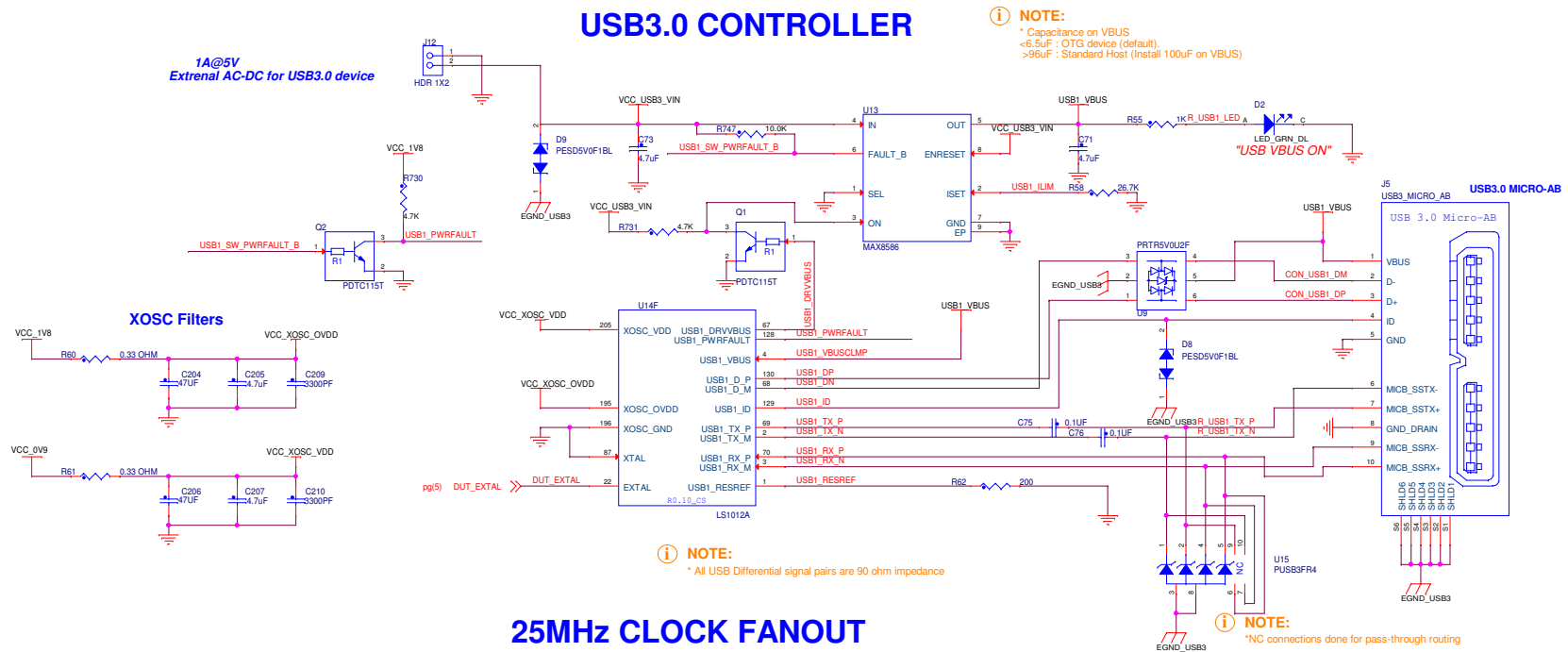
QSPI FLASH (512MBIT)



LS1012 EMI, JTAG, UART & I2C BLOCK

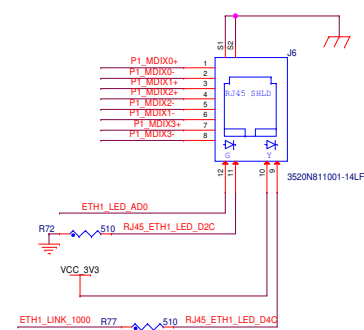
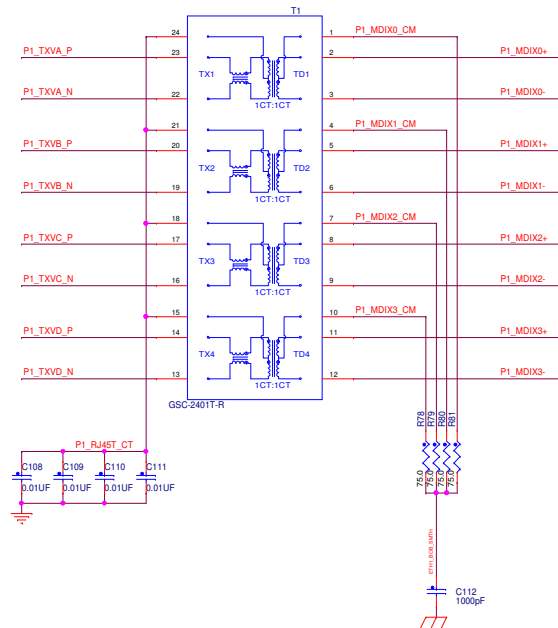
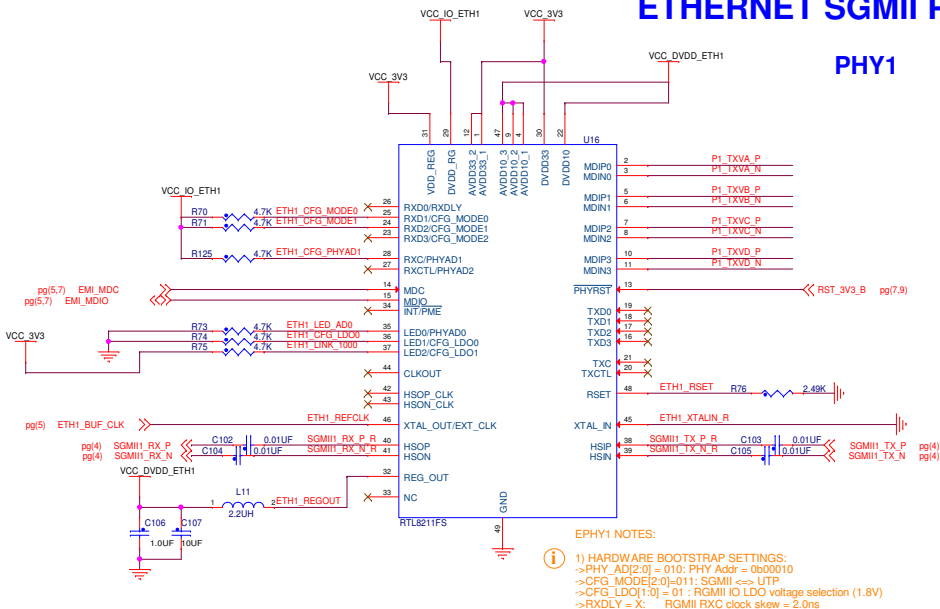


USB3.0 CONTROLLER

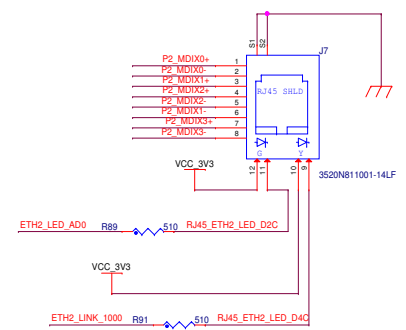
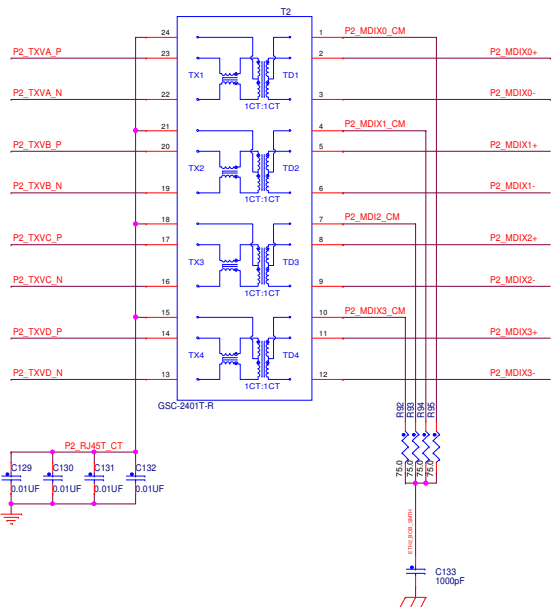
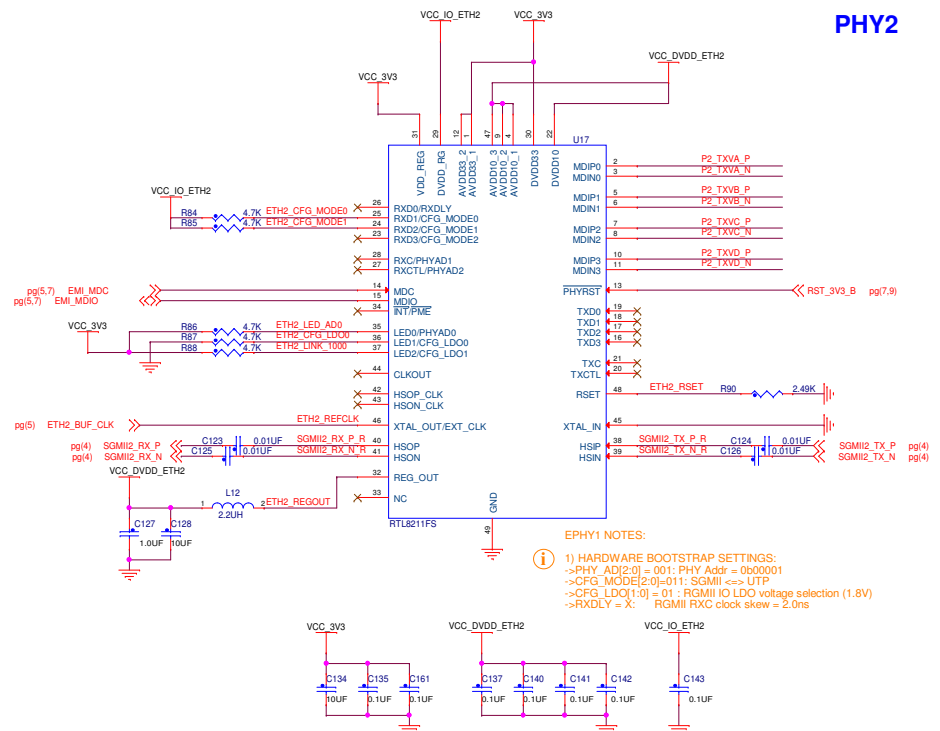


ETHERNET SGMII PHY INTERFACE

PHY1

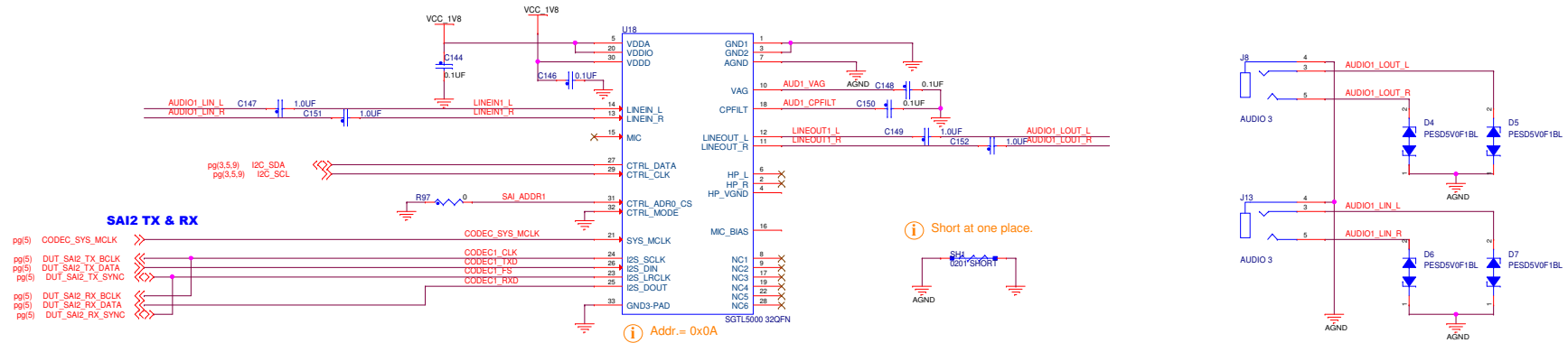


PHY2



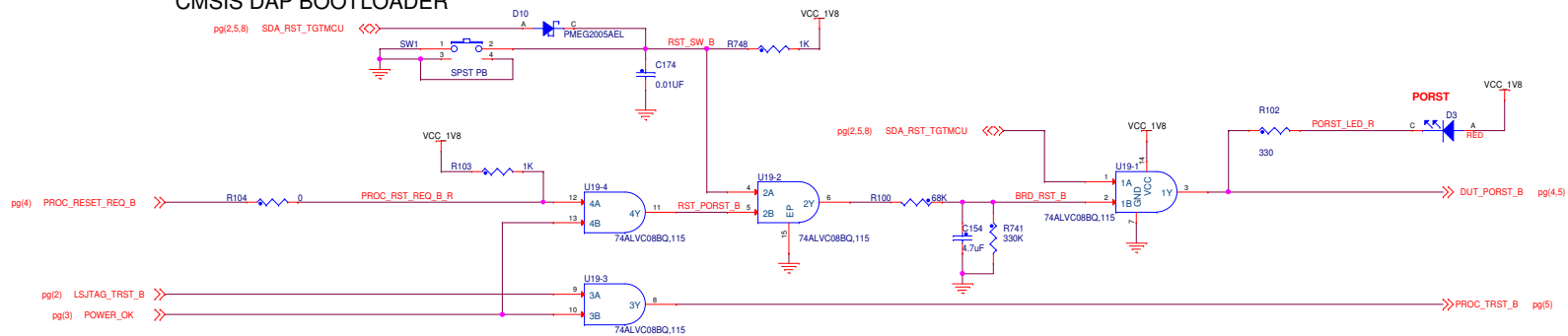
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Drawing Title: LS1012AFRDM			
Page Title: 07_ETHERNET PHYs			
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AUDIO CODEC



RESET

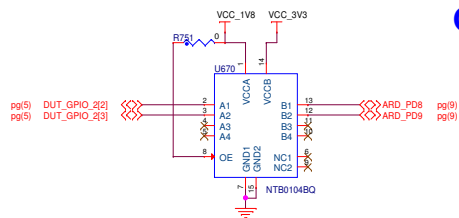
RESET SWITCH AND CMSIS DAP BOOTLOADER



VAR1



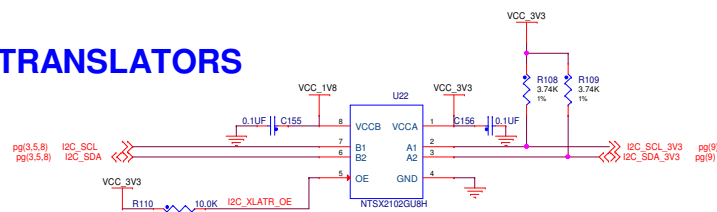
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Page Title: 08_AUDIO & RESET			
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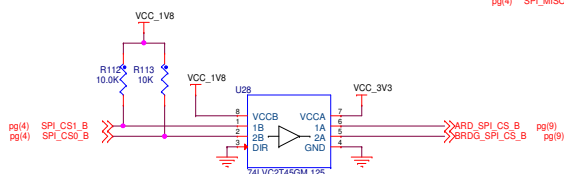
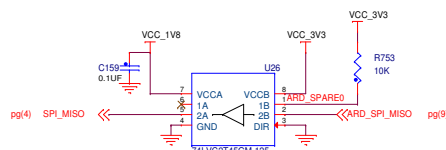
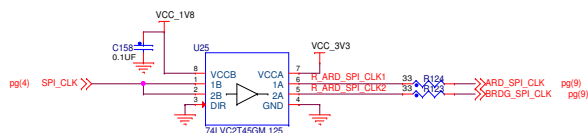
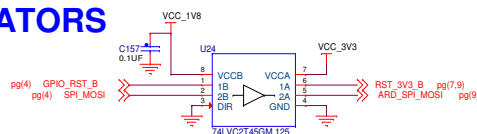
GPIOs

pg(4) DUT_GPIO_1[15] <-> ARD_PD1 pg(4,9)
 pg(4) DUT_GPIO_1[20] <-> ARD_PD2 pg(4,9)
 pg(4) DUT_GPIO_1[16] <-> ARD_PD4 pg(4,9)
 pg(4) DUT_GPIO_1[17] <-> ARD_PD5 pg(4,9)
 pg(4) DUT_GPIO_1[18] <-> ARD_PD6 pg(4,9)
 pg(4) DUT_GPIO_1[19] <-> ARD_PD7 pg(4,9)

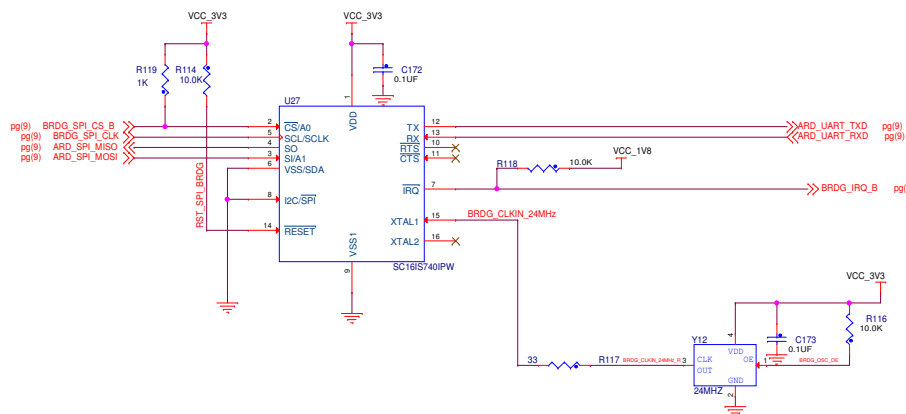
I2C TRANSATORS



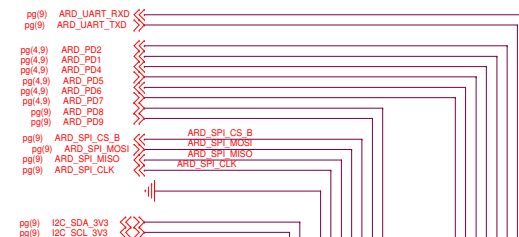
SPI TRANSATORS



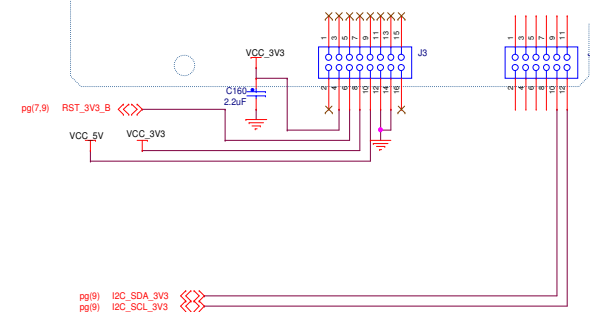
SPI TO UART BRIDGE



ARDUINO



FREEDOM PLATFORM COMPATIBILITY HEADERS



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