


Table of Contents	
2	Notes, Block Diagram
3	PN7642 VBGA64 MODULE

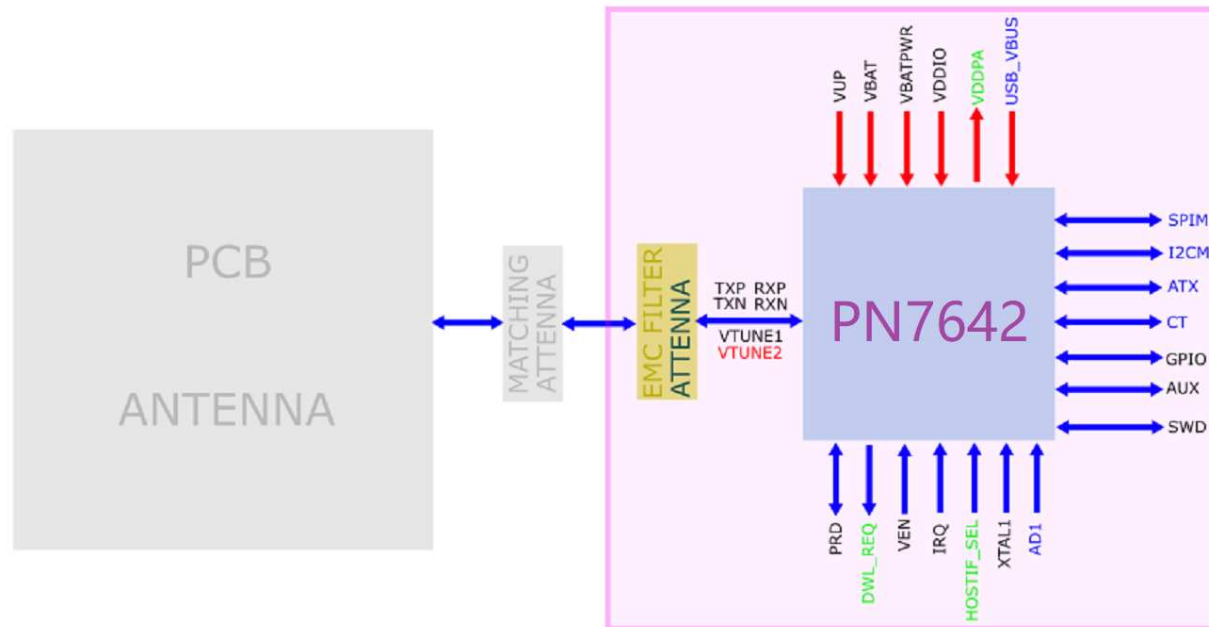
Revisions			
Rev	Description	Date	Approved
A	Release	11 FEB 22	Michael Neurohr
A1	DNP R4, C29, C13 Release (schematic update ONLY)	15 SEPT 22	Michael Neurohr

# PNEV7642MA


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C10,C13,C27,C29,R1,R4,R5,R7, R8,R9	DNP	03 PN7642 VBGA64 MODULE

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<small>Drawn by:</small> Jun Gao		<small>Page Title:</small> <b>Title Page</b>	
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<small>Date:</small> Thursday, September 15, 2022		<small>Sheet</small> 1	<small>Rev</small> A1
<small>of</small> 3			

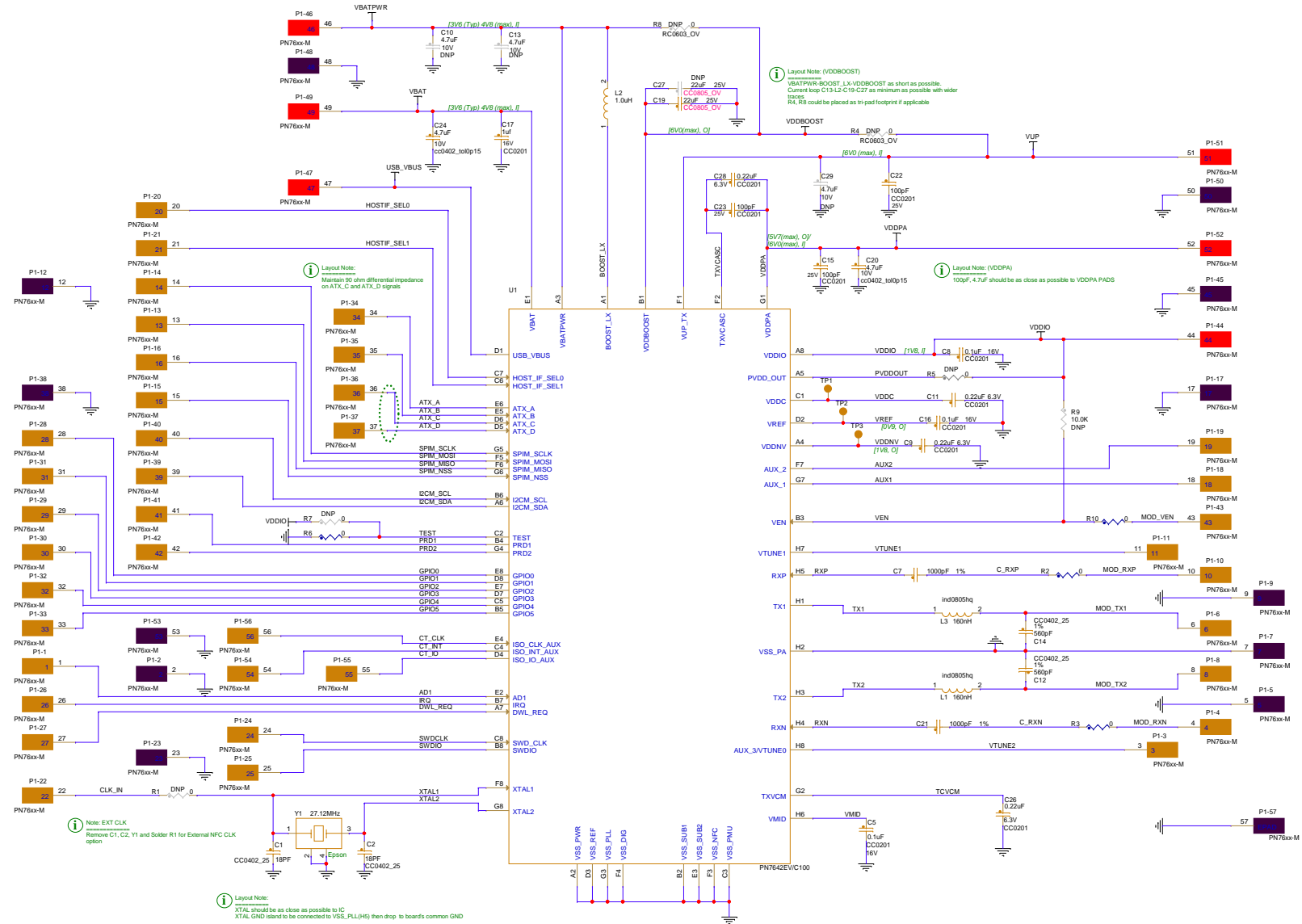
## PNEV7642MA: BLOCK DIAGRAM



1. Interrupted lines coded with the same letter or letter combinations are electrically connected.
2. Device type number is for reference only. The number varies with the manufacturer.
3. Special signal usage:  
 \_B Denotes - Active-Low Signal  
 <> or [] Denotes - Vectored Signals
4. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

		
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Drawing Title: PNEV7642MA		
Page Title: Notes, Block Diagram		
Size C	Document Number SCH-54814 PDF: SPF-54814	Rev A1
Date: Thursday, September 16, 2022	Sheet 2	of 3

# PN7642VBGA64 MODULE



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Drawing Title: PNEV7642MA

Page Title: PN7642VBGA64 MODULE

Size C Document Number SCH-54814 PDF: SPF-54814

Date: Thursday, September 16, 2022

Sheet 3 of 3

Rev A1