MOTOROLA
Semiconductor Products Sector

Verdi Rev 1B ReadMe

What is Verdi?

Verdi is the validation platform and a reference design for the MCF547x and MCF548x family of ColdFire processors. Verdi provides hardware to feature all the modules of the superset processor, the MCF5485. However, since all the derivatives of the family are pin-compatible, any member of the MCF547x/8x family can be populated on the validation platform.

Verdi Features

The features of Verdi include:

- MCF5485 or MCF5475 ColdFire processor
- 32Mbytes of DDR SDRAM on a 32-bit DIMM
- 32Mbytes of NOR Flash
- 512Kbytes of Fast Static RAM
- 2 - Ethernet ports
- 4 - 32-bit, 3.3V-only PCI card slots
- 2 – CAN ports (DB9 connectors)
- 2 – UART ports (DB9 connectors)
- Xilinx Spartan-2 FPGA and EEPROM

Verdi Rev1B Errata

There are several known errata on Verdi revision 1B. Most of these have been corrected with wired fixes and are implemented in revision 2B. The errata are explained below:

/RSTI – Processor Reset Input

To produce the correct /RSTI signal, the following changes were required:

- Short pins 4&5 of U22
- 4.7Kohm resistor between pins 7&9 of J2 (on underside)

Reset Configuration Enable

The reset configuration bits need to be driven when /RSTI is asserted (instead of /RSTO as shown on schematics). This was worked around as follows:

- Wire pin 1 of U25 to via on underside of board that connects to via on upper side of board next to TP7. Run wire on underside of board and through the hole in the corner of the board near U25
- Lift pin 20 of U26. Wire lifted pin to pin 1 of U26

Latche Enable for Flexbus Address Latches

The latches used on Verdi (16373 on schematic, 16374 populated) require an active high latch enable signal. The /TS signal provided by the Flexbus is the indication of a valid address on the bus, but this signal is active low. Therefore, it was necessary to use the Xilinx FPGA to correct the LE problem. The FPGA drives the address latch enable (ALE) on pin 69, which is connected to TIN1 of the processor. The changes necessary to wire TIN1 to the LE of the latches is as follows:

- Cut /TS trace between TP3 and pin 25 of U2 (cut close to TP3)
- Cut /TS trace on bottom of board near TP3
- Wire pin 1 of JP16 to pin 25 of U2
- Wire between TP3 and via going to J17 pin A4

This fix does result in another minor issue. The FPGA reads its program from the EEPROM U10 on startup. Therefore, the FPGA must be power-up and programmed before the processor can communicate with the Flash and SRAM devices on the Flexbus. Therefore, it is necessary to power-up the board and then press the Reset (RED) button to allow the processor to boot from Flash.

Access to all 32MB of Flash

Verdi was originally designed for two 16-bit Am29LV640M Flash devices which provided 16Mbytes of non-volatile memory. Due to Flash availability and lead-times, Verdi was populated with two 16-bit Am29LV128M devices which prove 32Mbytes. In order to access all the Flash memory, it was necessary to wire up an addition address line. This was accomplished as follows:

- Wire pin 13 of U2 to pin 2 of U8 and U9

Note that JP8 still controls the configuration of Flash address A21 (formerly the highest address line). In position 1-2, the jumper allows the routing of FB_A23 to the Flash address A21. This is the normal operation. In position 2-3, the jumper ties Flash address A21 high. This allows the user to boot from the second 8MB of Flash – useful for debugging user code without overwriting the dBUG ROM Monitor. In this position, the second and fourth 8MB block of Flash is accessible (0xFE800000 – 0xFE8FFFFF and 0xFF800000 – 0xFFFFFFFF).

PHY Address for U6 and U7

It was intended for the PHY address of U6 and U7 to be programmable via SW1 and SW2. However, the signals that these switches control need to be sampled by the PHY at reset and then tri-stated during normal operation. There is no circuitry on Verdi to disable these switches from driving following a reset. Therefore, all switches of SW1 and SW2 need to be left in the OFF position, disabling them from driving the PHY address lines at all times. The default address for the PHY will then be latched at reset. Both U6 and U7 will have an MII PHY address of 0x01. This is not an issue since each PHY is connected to only one of the FEC MII channels.

MTMOD Reset Values

For normal operation MTMOD[3:1] should be pulled down. Verdi Rev 1B has these signals pulled high.

USB and PLL Power Supply Filtering

The USB and PLL power supply filtering circuit has changed on later revisions of Verdi to match the recommended circuitry in the MCF547x/8x User's Manuals.

Ethernet Interface Impedance Matching

Several resistors (R13, R14, R15, R16, R23, R24, R25, and R26) on the Ethernet interface were mistakenly specified as 49.9 KΩ instead of 49.9 Ω +/- 1%.

PCI M66EN Signal

The M66EN signal on the PCI connectors should be monitored by the processor to determine if a 33MHz PCI card has been inserted into a 66MHz bus. On later revisions of Verdi, this signal is pulled high and tied to a GPI pin on the processor.