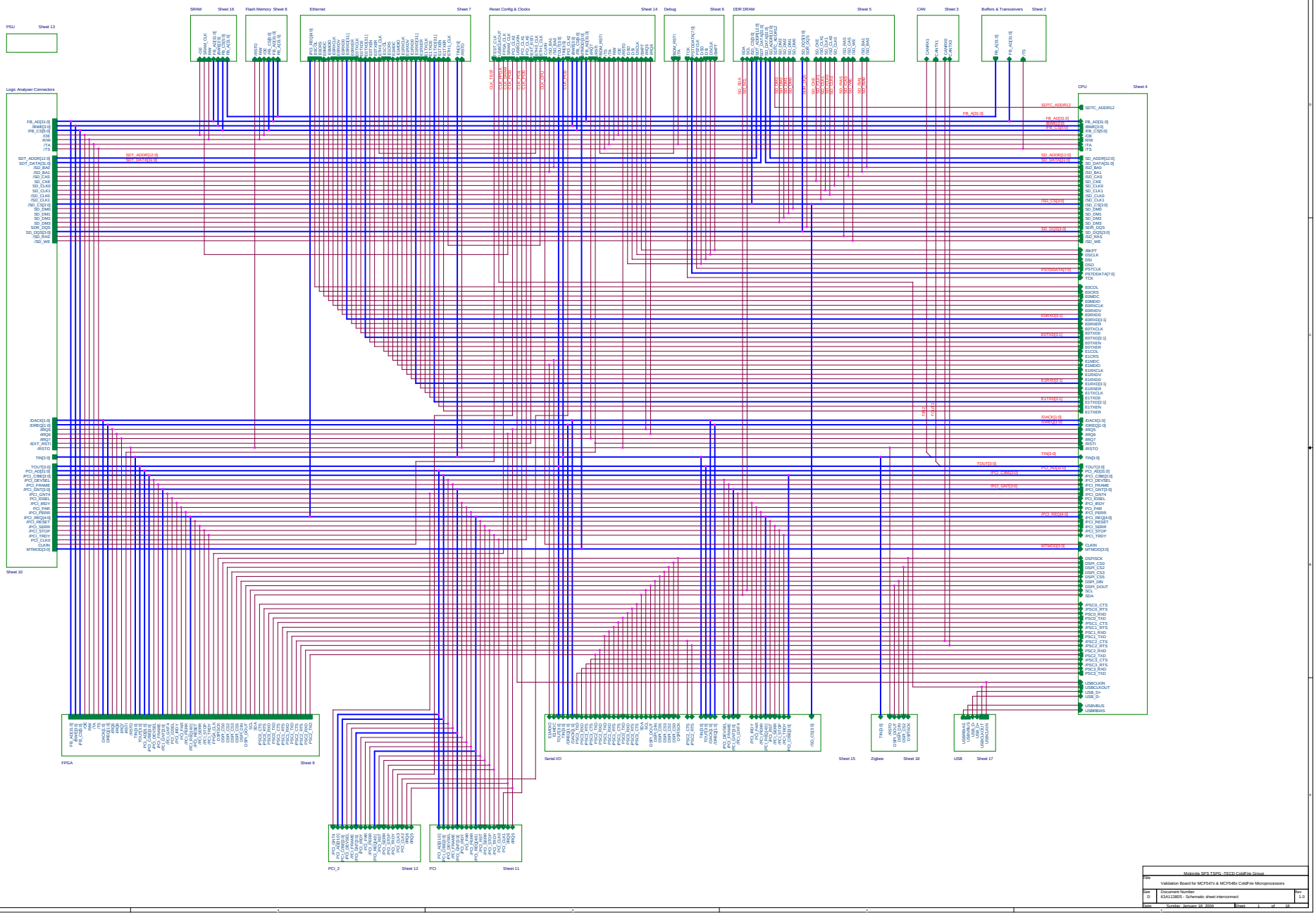
SRAM
Sheet 16
Flash Memory
Sheet 8
Ethernet
Sheet 7
Reset Config & Clocks
Sheet 14
Debug
Sheet 6
DDR DRAM
Sheet 5
CAN
Sheet 3
Buffers & Transceivers
Sheet 2
PSU
Sheet 13
Logic Analyser Connectors
Sheet 10
CPU
Sheet 4
FPGA
Sheet 9
Serial I/O
Sheet 15
Zigbee
Sheet 18
USB
Sheet 17
PCI_2
Sheet 12
PCI
Sheet 11
Motorola SPS TSPG -TECD ColdFire Group
Validation Board for MCF547x & MCF548x ColdFire Microprocessors
Document Number
63A113805 - Schematic sheet interconnect
Rev
1.0
Date:
Sunday, January 18, 2004
Sheet
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of
38

Address bus latches.

FB_A[31:0]

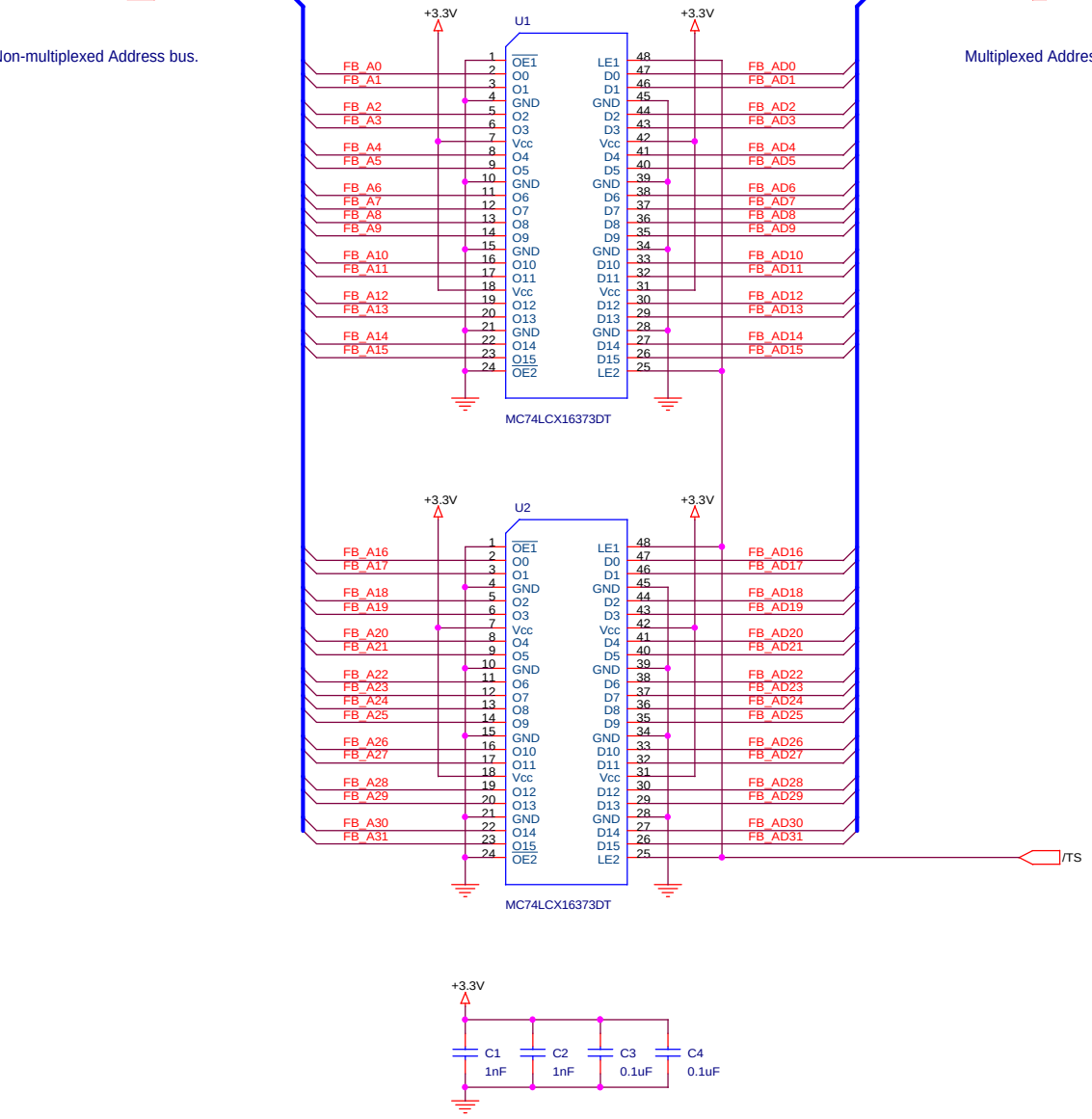
FB_A[31:0]

Non-multiplexed Address bus.

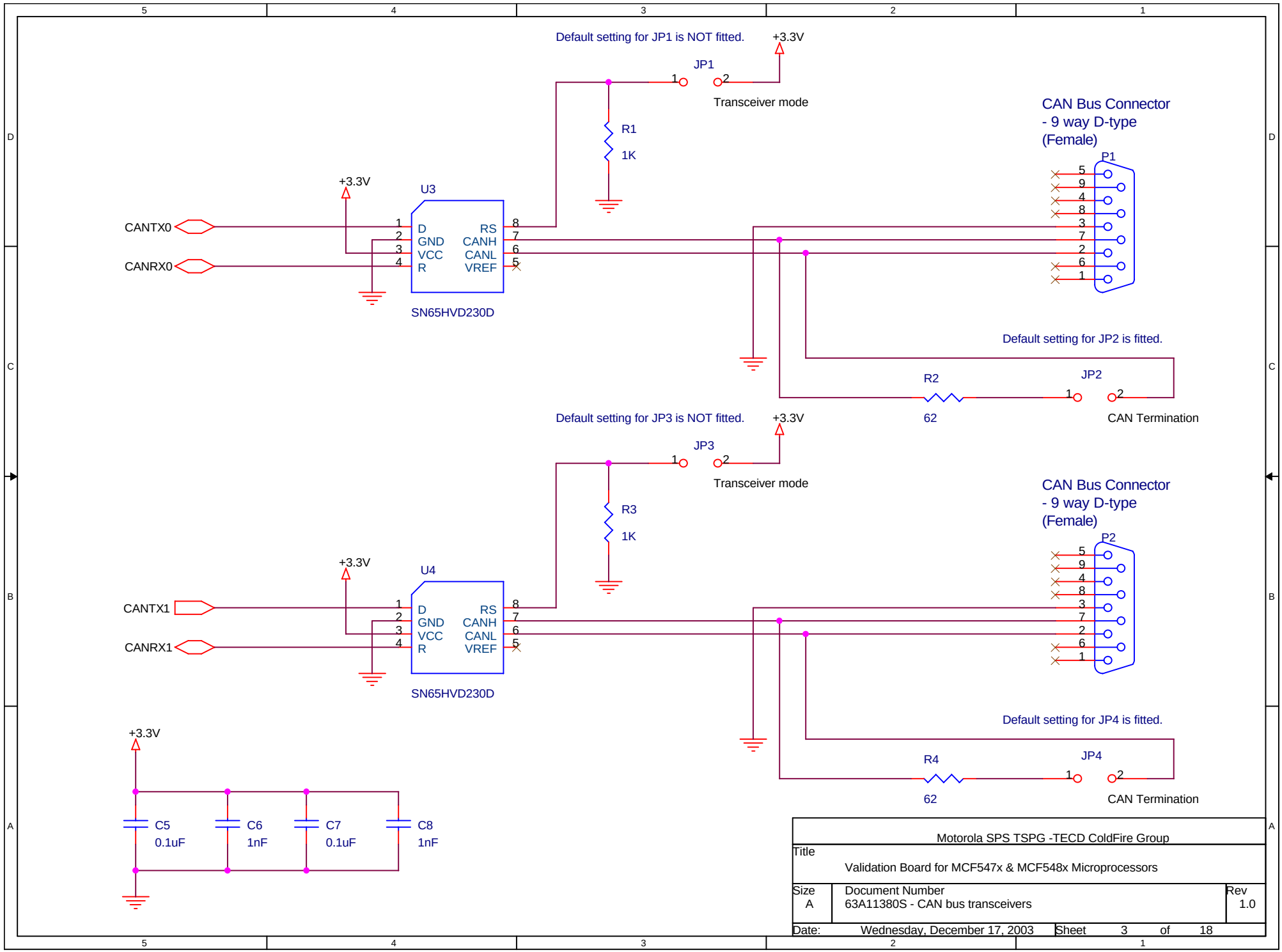
FB_AD[31:0]

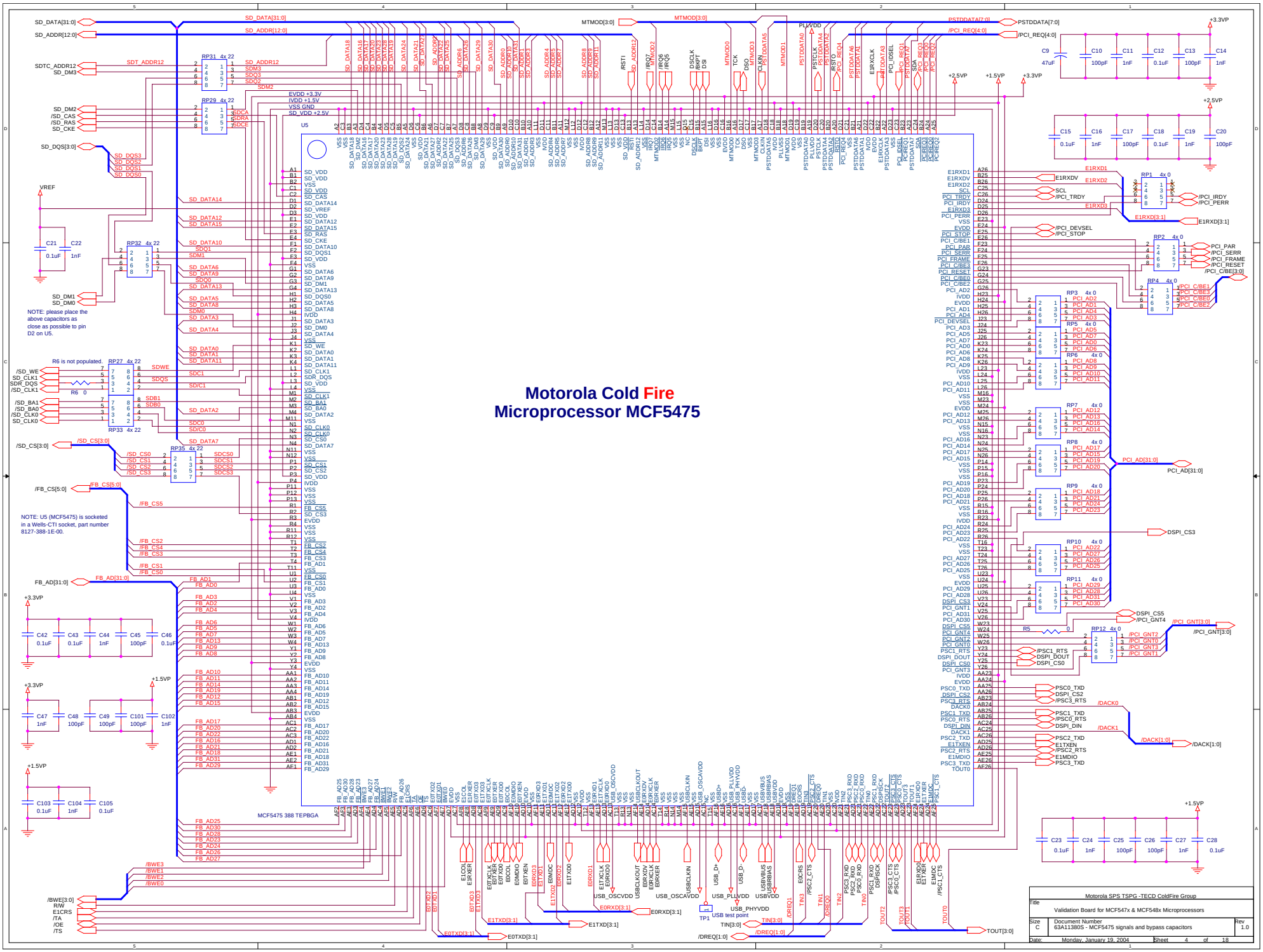
FB_AD[31:0]

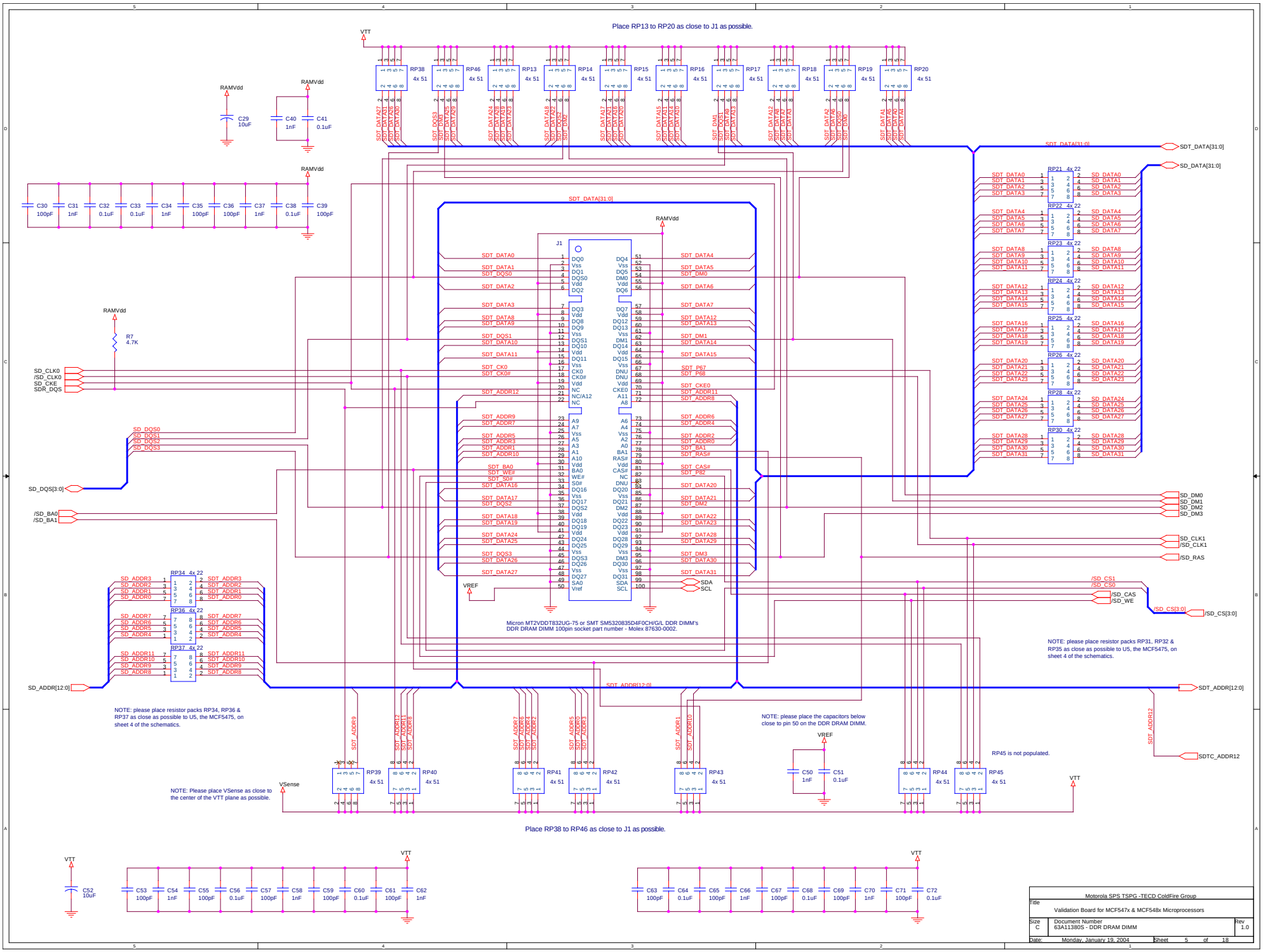
Multiplexed Address/Data bus from the CPU (sheet 4).



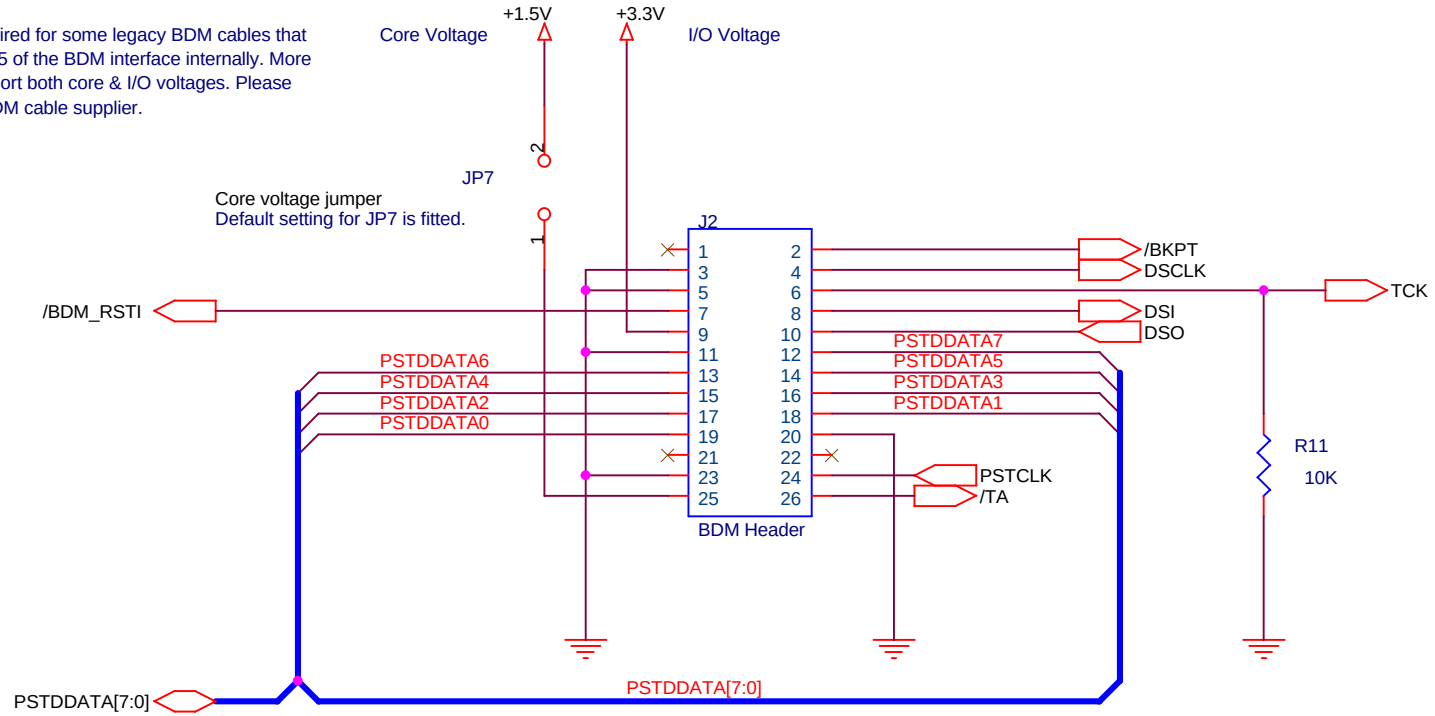
Motorola SPS TSPG -TECD ColdFire Group		
Title: Validation Board for MCF547x & MCF548x Microprocessors		
Size: B	Document Number: 63A11380S - Flex bus address latches	Rev: 1.0
Date: Wednesday, November 26, 2003	Sheet 2 of 18	


Default setting for JP1 is NOT fitted.
+3.3V
JP1
1
2
Transceiver mode
R1
1K
CAN Bus Connector
- 9 way D-type
(Female)
P1
+3.3V
U3
CANTX0
CANRX0
1
2
3
4
D
GND
VCC
R
RS
CANH
CANL
VREF
8
7
6
5
SN65HVD230D
Default setting for JP2 is fitted.
R2
62
JP2
CAN Termination
Default setting for JP3 is NOT fitted.
+3.3V
JP3
Transceiver mode
R3
1K
CAN Bus Connector
- 9 way D-type
(Female)
P2
+3.3V
U4
CANTX1
CANRX1
SN65HVD230D
Default setting for JP4 is fitted.
R4
62
JP4
CAN Termination
+3.3V
C5
0.1uF
C6
1nF
C7
0.1uF
C8
1nF
Motorola SPS TSPG -TECD ColdFire Group
Title
Validation Board for MCF547x & MCF548x Microprocessors
Size
A
Document Number
63A11380S - CAN bus transceivers
Rev
1.0
Date:
Wednesday, December 17, 2003
Sheet
3
of
18


Motorola Cold Fire
Microprocessor MCF5475
MCF5475 388 TEPBGA
U5
NOTE: please place the above capacitors as close as possible to pin D2 on U5.
NOTE: U5 (MCF5475) is socketed in a Wells-CTI socket, part number 8127-388-1E-00.
R6 is not populated.
Motorola SPS TSPG -TECD ColdFire Group
Validation Board for MCF547x & MCF548x Microprocessors
Document Number 63A11380S - MCF5475 signals and bypass capacitors
Rev 1.0
Monday, January 19, 2004
Sheet 4 of 18


Place RP13 to RP20 as close to J1 as possible.
VTT
RAMVdd
C29 10uF
C40 1nF
C41 0.1uF
C30 100pF
C31 1nF
C32 0.1uF
C33 0.1uF
C34 1nF
C35 100pF
C36 100pF
C37 1nF
C38 0.1uF
C39 100pF
RP38 4x 51
RP46 4x 51
RP13 4x 51
RP14 4x 51
RP15 4x 51
RP16 4x 51
RP17 4x 51
RP18 4x 51
RP19 4x 51
RP20 4x 51
SDT_DATA[31:0]
SD_DATA[31:0]
RP21 4x 22
RP22 4x 22
RP23 4x 22
RP24 4x 22
RP25 4x 22
RP26 4x 22
RP28 4x 22
RP30 4x 22
J1
R7 4.7K
SD_CLK0
/SD_CLK0
SD_CKE
SDR_DQS
SD_DQS[3:0]
/SD_BA0
/SD_BA1
SD_ADDR[12:0]
SDT_ADDR[12:0]
VREF
SDA
SCL
Micron MT2VDDT832UG-75 or SMT SM5320835D4F0CH/G/L DDR DIMM's
DDR DRAM DIMM 100pin socket part number - Molex 87630-0002.
RP34 4x 22
RP36 4x 22
RP37 4x 22
NOTE: please place resistor packs RP34, RP36 & RP37 as close as possible to U5, the MCF5475, on sheet 4 of the schematics.
NOTE: please place resistor packs RP31, RP32 & RP35 as close as possible to U5, the MCF5475, on sheet 4 of the schematics.
/SD_CS1
/SD_CS0
/SD_CAS
/SD_WE
/SD_CS[3:0]
SD_DM0
SD_DM1
SD_DM2
SD_DM3
SD_CLK1
/SD_CLK1
/SD_RAS
RP39 4x 51
RP40 4x 51
RP41 4x 51
RP42 4x 51
RP43 4x 51
RP44 4x 51
RP45 4x 51
RP45 is not populated.
NOTE: please place the capacitors below close to pin 50 on the DDR DRAM DIMM.
C50 1nF
C51 0.1uF
VSense
NOTE: Please place VSense as close to the center of the VTT plane as possible.
SDTC_ADDR12
Place RP38 to RP46 as close to J1 as possible.
C52 10uF
C53 100pF
C54 1nF
C55 100pF
C56 0.1uF
C57 100pF
C58 1nF
C59 100pF
C60 0.1uF
C61 100pF
C62 1nF
C63 100pF
C64 0.1uF
C65 100pF
C66 1nF
C67 100pF
C68 0.1uF
C69 100pF
C70 1nF
C71 100pF
C72 0.1uF
Motorola SPS TSPG -TECD ColdFire Group
Title
Validation Board for MCF547x & MCF548x Microprocessors
Size C
Document Number 63A11380S - DDR DRAM DIMM
Rev 1.0
Date: Monday, January 19, 2004
Sheet 5 of 18

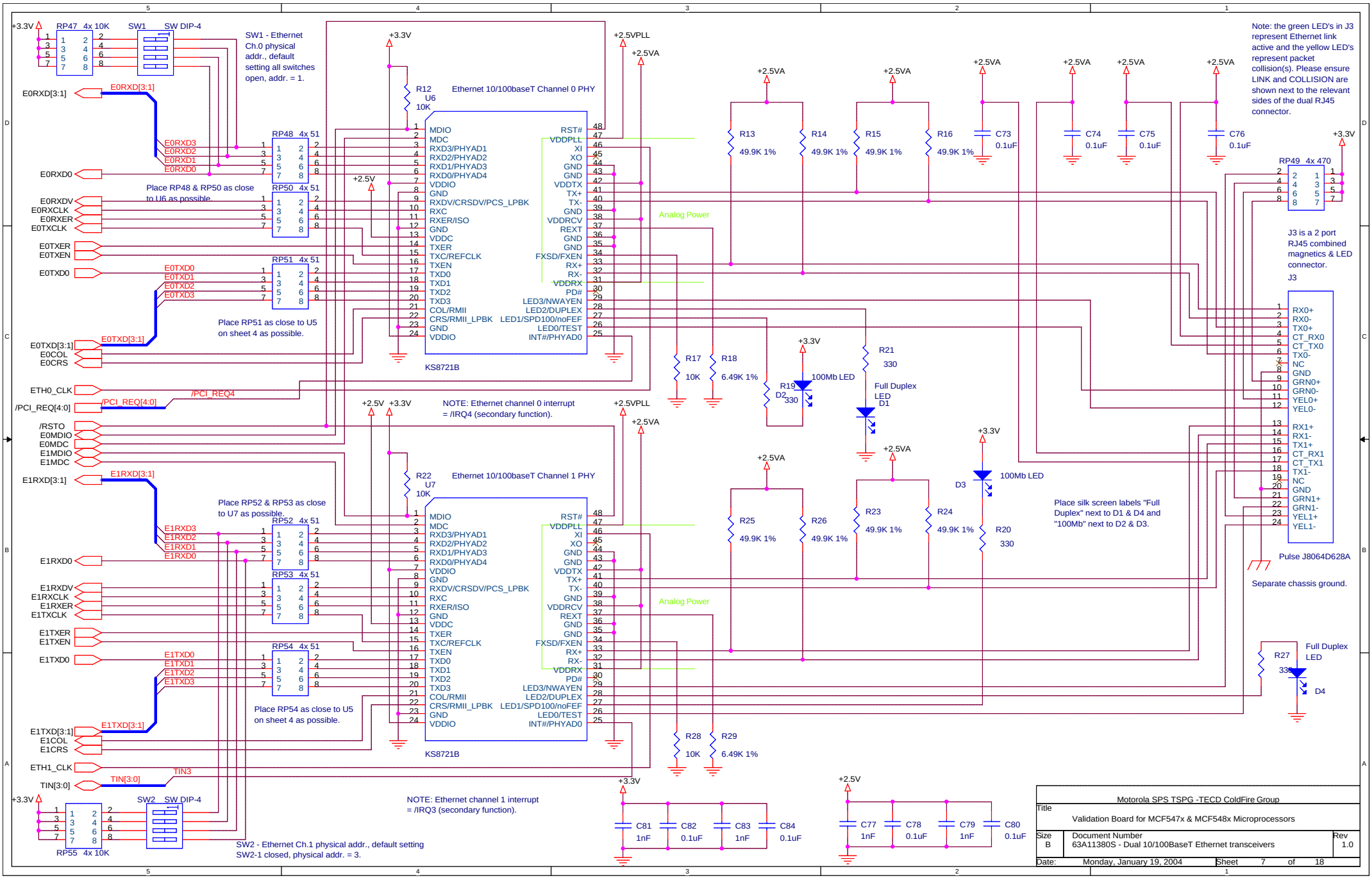
NOTE: JP7 is required for some legacy BDM cables that connect pins 9 & 25 of the BDM interface internally. More recent cables support both core & I/O voltages. Please check with your BDM cable supplier.

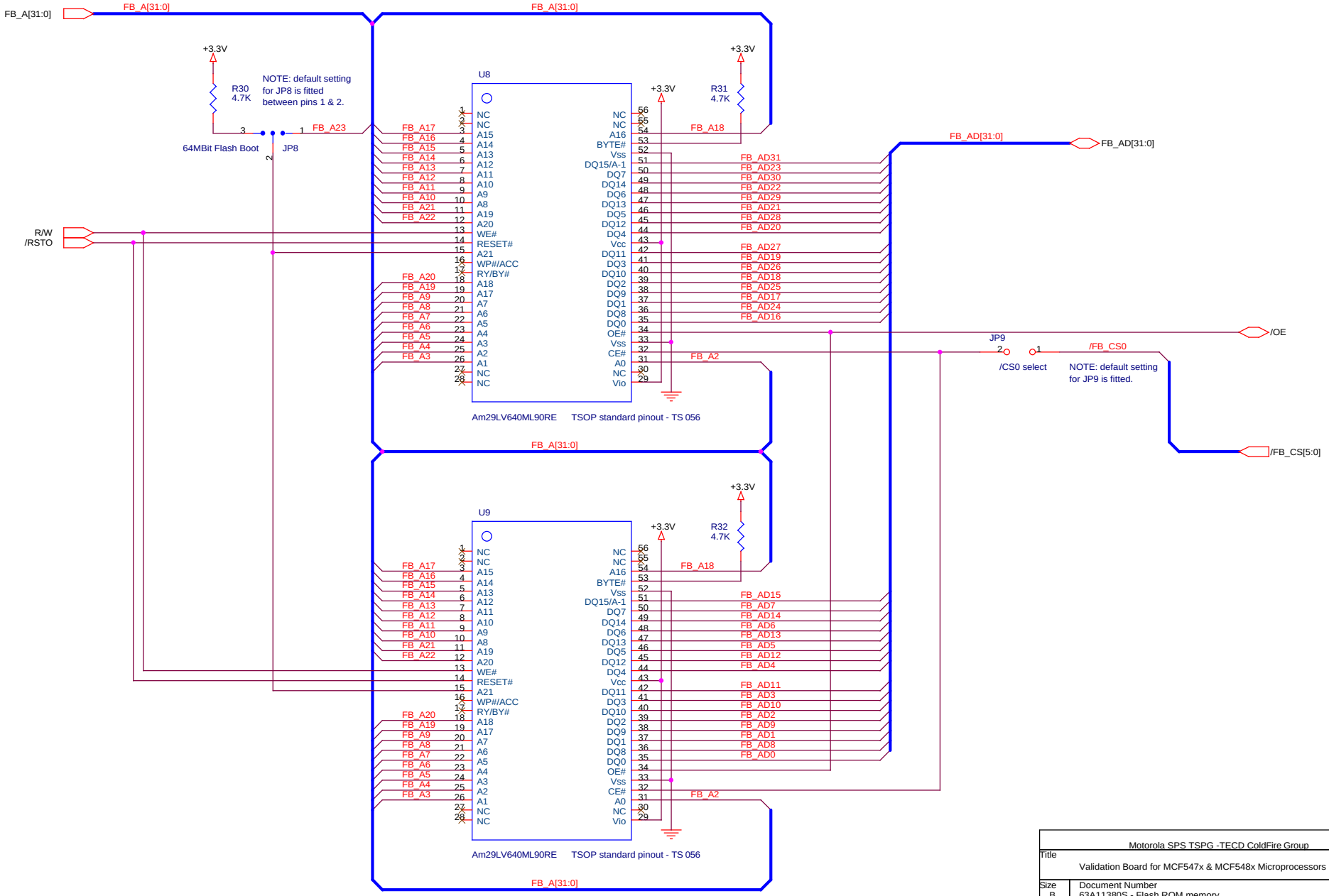


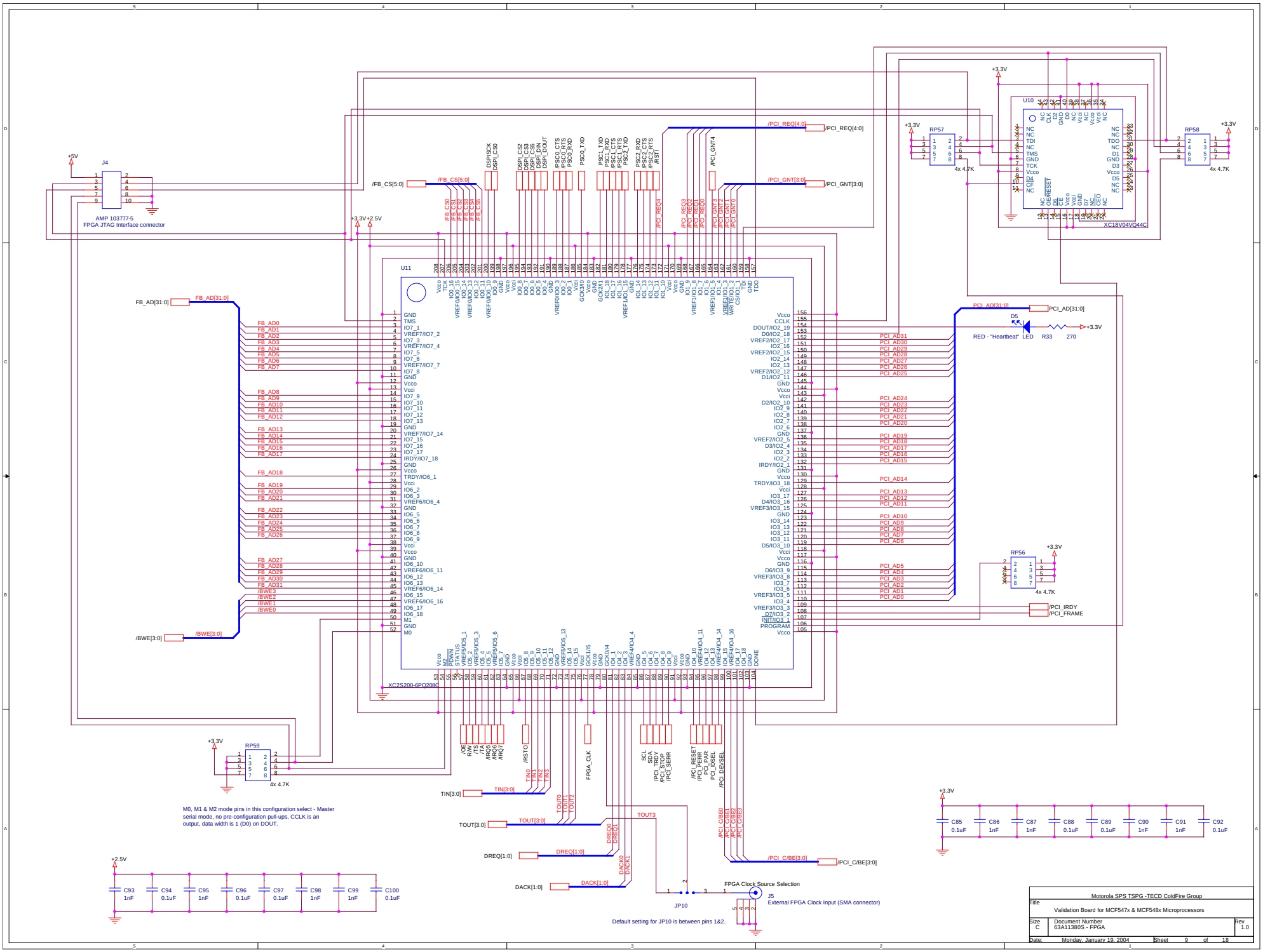
NOTE: 4.7K pull up resistors are used on signals /BKPT, DSCLK, DSI, DSO & /RSTI. A 1K pull up is used for -TA. See page 14 of the schematics.

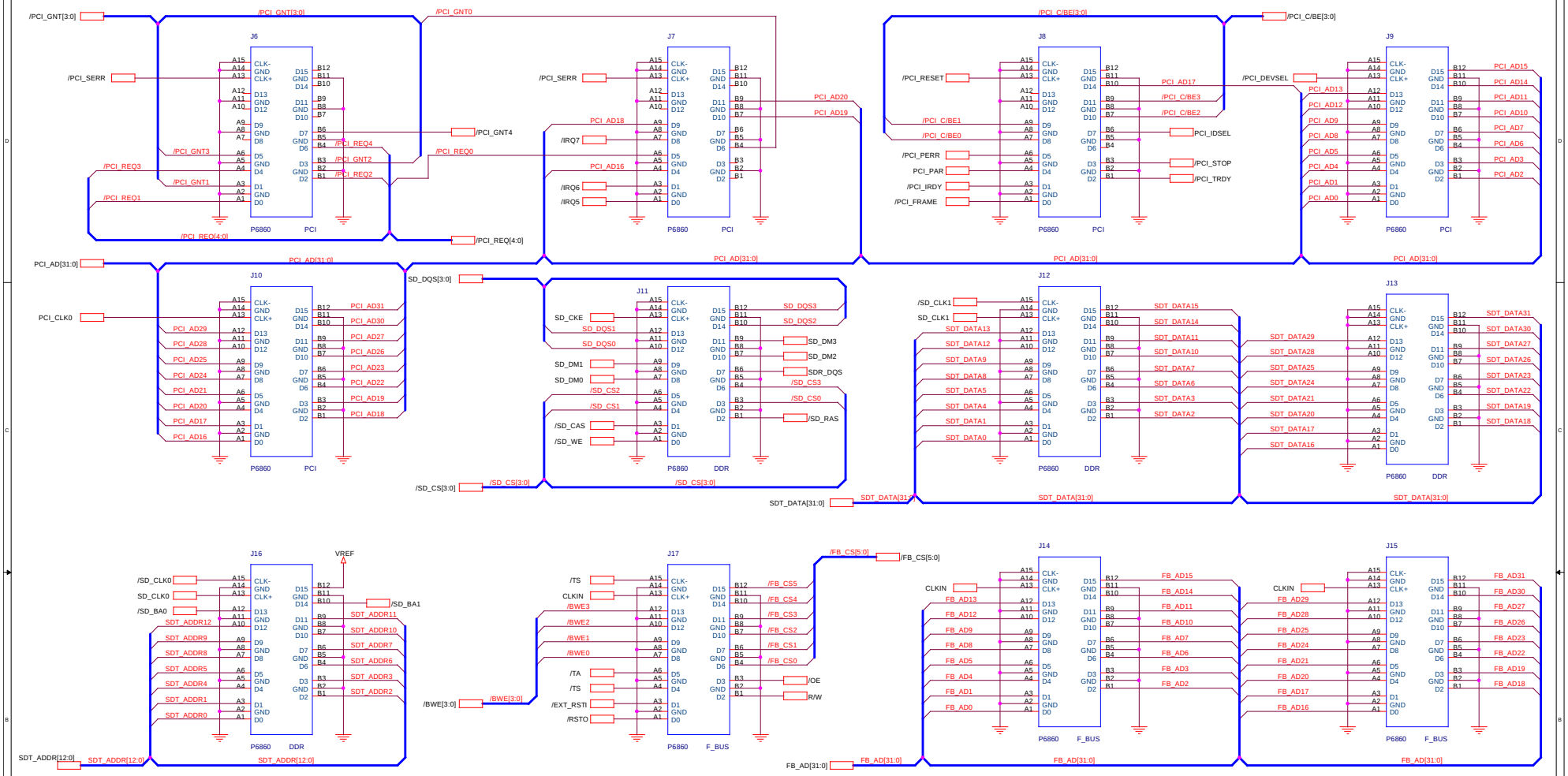
IMPORTANT NOTE: ONLY 3.3V BDM debugging cables can be used with MCF547x/8x processors.

Motorola SPS TSPG -TECD ColdFire Group		
Title: Validation Board for MCF547x & MCF548x Microprocessors		
Size: A	Document Number: 63A11380S - BDM/JTAG connector	Rev: 1.0
Date: Wednesday, December 17, 2003	Sheet 6 of 18	


RP47 4x 10K
SW1 SW DIP-4
SW1 - Ethernet Ch.0 physical addr., default setting all switches open, addr. = 1.
Ethernet 10/100baseT Channel 0 PHY
KS8721B
Place RP48 & RP50 as close to U6 as possible.
Place RP51 as close to U5 on sheet 4 as possible.
NOTE: Ethernet channel 0 interrupt = /IRQ4 (secondary function).
Ethernet 10/100baseT Channel 1 PHY
KS8721B
Place RP52 & RP53 as close to U7 as possible.
Place RP54 as close to U5 on sheet 4 as possible.
NOTE: Ethernet channel 1 interrupt = /IRQ3 (secondary function).
SW2 SW DIP-4
RP55 4x 10K
SW2 - Ethernet Ch.1 physical addr., default setting
SW2-1 closed, physical addr. = 3.
Analog Power
Note: the green LED's in J3 represent Ethernet link active and the yellow LED's represent packet collision(s). Please ensure LINK and COLLISION are shown next to the relevant sides of the dual RJ45 connector.
J3 is a 2 port RJ45 combined magnetics & LED connector.
J3
100Mb LED
Full Duplex LED
Place silk screen labels "Full Duplex" next to D1 & D4 and "100Mb" next to D2 & D3.
Pulse J8064D628A
Separate chassis ground.
Motorola SPS TSPG -TECD ColdFire Group
Validation Board for MCF547x & MCF548x Microprocessors
63A11380S - Dual 10/100BaseT Ethernet transceivers
Monday, January 19, 2004


FB_A[31:0]
+3.3V
R30
4.7K
NOTE: default setting
for JP8 is fitted
between pins 1 & 2.
64MBit Flash Boot
JP8
FB_A23
R/W
/RSTO
U8
U9
NC
A15
A14
A13
A12
A11
A10
A9
A8
A19
A20
WE#
RESET#
A21
WP#/ACC
RY/BY#
A18
A17
A7
A6
A5
A4
A3
A2
A1
BYTE#
Vss
DQ15/A-1
DQ7
DQ14
DQ6
DQ13
DQ5
DQ12
DQ4
Vcc
DQ11
DQ3
DQ10
DQ2
DQ9
DQ1
DQ8
DQ0
OE#
CE#
A0
Vio
R31
4.7K
R32
4.7K
FB_A18
FB_A2
FB_AD[31:0]
FB_AD31
FB_AD23
FB_AD30
FB_AD22
FB_AD29
FB_AD21
FB_AD28
FB_AD20
FB_AD27
FB_AD19
FB_AD26
FB_AD18
FB_AD25
FB_AD17
FB_AD24
FB_AD16
FB_AD15
FB_AD7
FB_AD14
FB_AD6
FB_AD13
FB_AD5
FB_AD12
FB_AD4
FB_AD11
FB_AD3
FB_AD10
FB_AD2
FB_AD9
FB_AD1
FB_AD8
FB_AD0
Am29LV640ML90RE
TSOP standard pinout - TS 056
JP9
/CS0 select
/FB_CS0
NOTE: default setting
for JP9 is fitted.
/OE
/FB_CS[5:0]
Motorola SPS TSPG -TECD ColdFire Group
Validation Board for MCF547x & MCF548x Microprocessors
Size B
Document Number
63A11380S - Flash ROM memory
Rev 1.0
Date: Wednesday, December 17, 2003
Sheet 8 of 18


J4
AMP 103777-5
FPGA JTAG Interface connector
U11
XC2S200-6PQ208C
U10
XC18V04VQ44C
RP57
RP58
RP56
RP59
4x 4.7K
D5
RED - "Heartbeat" LED
R33
270
/FB_CS[5:0]
FB_AD[31:0]
/BWE[3:0]
/PCI_REQ[4:0]
/PCI_GNT[3:0]
PCI_AD[31:0]
/PCI_IRDY
/PCI_FRAME
/PCI_C/BE[3:0]
TIN[3:0]
TOUT[3:0]
DREQ[1:0]
DACK[1:0]
FPGA_CLK
M0, M1 & M2 mode pins in this configuration select - Master serial mode, no pre-configuration pull-ups, CCLK is an output, data width is 1 (D0) on DOUT.
JP10
Default setting for JP10 is between pins 1&2.
FPGA Clock Source Selection
J5
External FPGA Clock Input (SMA connector)
C85 0.1uF
C86 1nF
C87 1nF
C88 0.1uF
C89 0.1uF
C90 1nF
C91 1nF
C92 0.1uF
C93 1nF
C94 0.1uF
C95 1nF
C96 0.1uF
C97 0.1uF
C98 1nF
C99 1nF
C100 0.1uF
Motorola SPS TSPG -TECD ColdFire Group
Validation Board for MCF547x & MCF548x Microprocessors
Document Number 63A11380S - FPGA
Rev 1.0
Monday, January 19, 2004
Sheet 9 of 18



Motorola SPS TSPG -TECD ColdFire Group		
Title: Validation Board for the MCF547x & MCF548x Microprocessors		
Size: C	Document Number: 63A11380S - Logic Analyser connectors	Rev: 1.0
Date: Saturday, January 17, 2004	Sheet 10 of 18	

NOTE: PCI slot 1 uses /PCI_REQ1 & /PCI_GNT1 signals and PCI slot 2 uses /PCI_REQ2 & /PCI_GNT2 signals. PCI slot 1 has IDSEL connected to PCI_AD17 and PCI slot 2 has IDSEL connected to PCI_AD18. Both PCI connectors are setup for 3.3V operation and +/-12V is supplied via P3 to each PCI connector. Finally, JTAG is unusable on both PCI connectors.

2-way Bare Wire Power Connector
P3
Augat 25V-02

/PCI_GNT[3:0]
/PCI_REQ[4:0]
/IRQ6
/IRQ5
/PCI_C/BE[3:0]
PCI_AD[31:0]

RP60 4x 10K
RP61 4x 10K

J20 Universal 32-bit PCI Connector
PCI Slot 1
PCI socket part number - AMP 145167-4

J21 Universal 32-bit PCI Connector
PCI Slot 2
PCI socket part number - AMP 145167-4

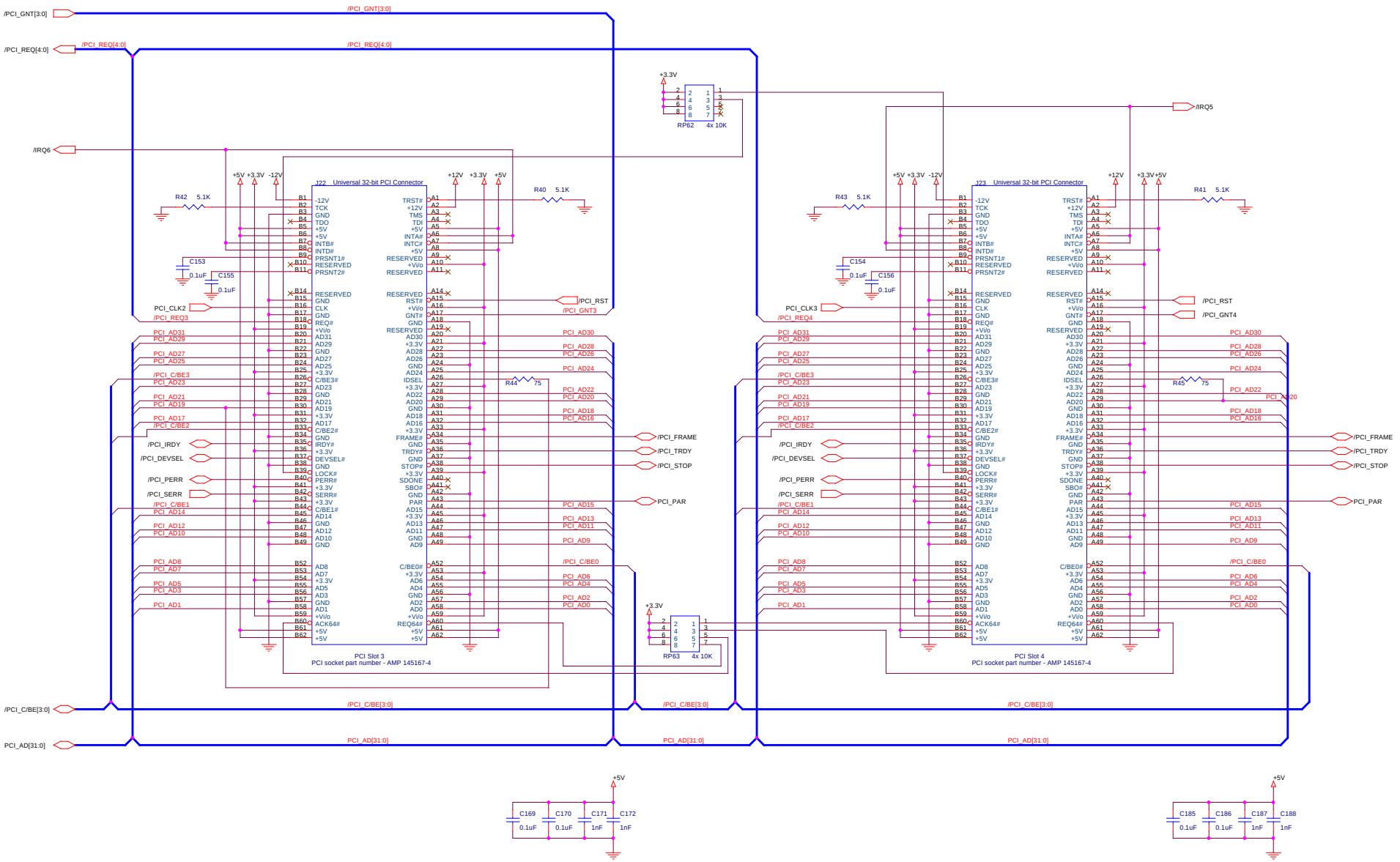
R36 5.1K
R34 5.1K
R37 5.1K
R35 5.1K
R38 75
R39 75

C117 0.1uF
C119 0.1uF
C118 0.1uF
C120 0.1uF

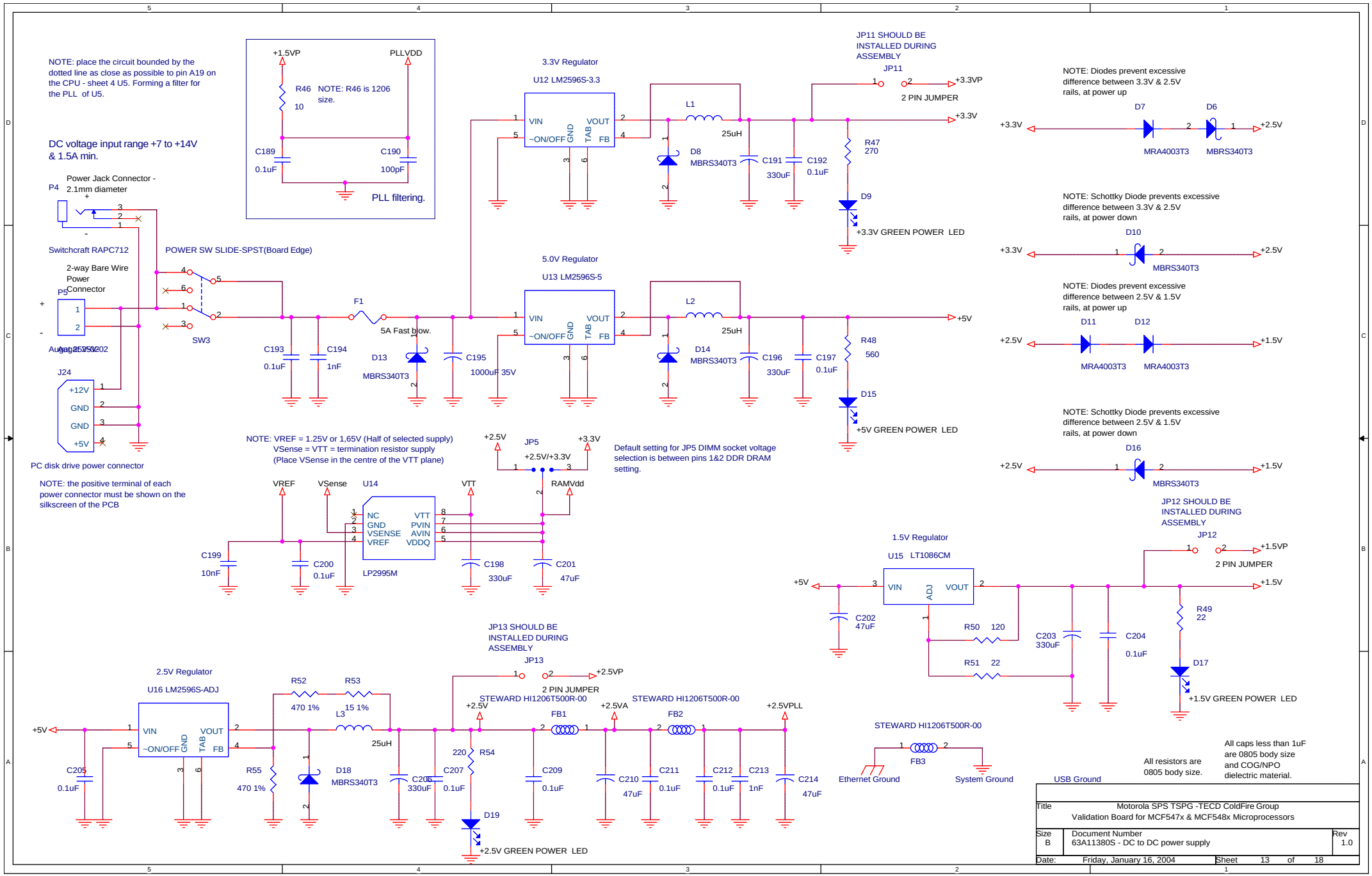
C121 C122 C123 C124 C125 C126 C127 C128 C129 C130 C131 C132 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 1nF 1nF 1nF 1nF 1nF 1nF
C133 C134 C135 C136 0.1uF 0.1uF 1nF 1nF
C137 C138 C139 C140 C141 C142 C143 C144 C145 C146 C147 C148 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 1nF 1nF 1nF 1nF 1nF 1nF
C149 C150 C151 C152 0.1uF 0.1uF 1nF 1nF

	Motorola SPS TSPG -TECD ColdFire Group
Title	Validation Board for MCF547x & MCF548x Microprocessors
Size C	Document Number 63A11380S - 2x PCI bus connectors
Rev	1.0
Date:	Friday, November 28, 2003
Sheet	11 of 18

NOTE: PCI slot 3 uses /PCI_REQ3 & /PCI_GNT3 signals and PCI slot 4 uses /PCI_REQ4 & /PCI_GNT4 signals. PCI slot 3 has IDSEL connected to PCI_AD19 and PCI slot 4 has IDSEL connected to PCI_AD20. Both PCI connectors are setup for 3.3V operation and +/-12V is supplied via P3 (sheet 11) to each PCI connector. Finally, JTAG is unusable on both PCI connectors.



Motorola SPS TSPG -TECD ColdFire Group		
Title: Validation Board for MCF547x & MCF548x Microprocessors		
Size: C	Document Number: 63A11380S - Second 2x PCI bus connectors	Rev: 1.0
Date: Sunday, January 18, 2004	Sheet 12 of 18	


NOTE: place the circuit bounded by the dotted line as close as possible to pin A19 on the CPU - sheet 4 U5. Forming a filter for the PLL of U5.
DC voltage input range +7 to +14V & 1.5A min.
+1.5VP
PLLVDD
R46 10
NOTE: R46 is 1206 size.
C189 0.1uF
C190 100pF
PLL filtering.
P4
Power Jack Connector - 2.1mm diameter
Switchcraft RAPC712
POWER SW SLIDE-SPST(Board Edge)
SW3
P5
2-way Bare Wire Power Connector
J24
+12V
GND
GND
+5V
PC disk drive power connector
NOTE: the positive terminal of each power connector must be shown on the silkscreen of the PCB
F1
5A Fast blow.
3.3V Regulator
U12 LM2596S-3.3
VIN
VOUT
~ON/OFF
GND
TAB
FB
L1
25uH
D8 MBRS340T3
C191 330uF
C192 0.1uF
R47 270
D9
+3.3V GREEN POWER LED
JP11 SHOULD BE INSTALLED DURING ASSEMBLY
JP11
2 PIN JUMPER
+3.3VP
+3.3V
5.0V Regulator
U13 LM2596S-5
L2
25uH
D14 MBRS340T3
C196 330uF
C197 0.1uF
R48 560
D15
+5V GREEN POWER LED
+5V
C193 0.1uF
C194 1nF
D13 MBRS340T3
C195 1000uF 35V
NOTE: VREF = 1.25V or 1,65V (Half of selected supply)
VSense = VTT = termination resistor supply
(Place VSense in the centre of the VTT plane)
U14
VREF
VSense
VTT
NC
GND
VSENSE
VREF
PVIN
AVIN
VDDQ
LP2995M
C199 10nF
C200 0.1uF
C198 330uF
C201 47uF
JP5
+2.5V/+3.3V
RAMVdd
Default setting for JP5 DIMM socket voltage selection is between pins 1&2 DDR DRAM setting.
NOTE: Diodes prevent excessive difference between 3.3V & 2.5V rails, at power up
D7 MRA4003T3
D6 MBRS340T3
NOTE: Schottky Diode prevents excessive difference between 3.3V & 2.5V rails, at power down
D10 MBRS340T3
NOTE: Diodes prevent excessive difference between 2.5V & 1.5V rails, at power up
D11 MRA4003T3
D12 MRA4003T3
NOTE: Schottky Diode prevents excessive difference between 2.5V & 1.5V rails, at power down
D16 MBRS340T3
JP12 SHOULD BE INSTALLED DURING ASSEMBLY
JP12
2 PIN JUMPER
+1.5VP
+1.5V
1.5V Regulator
U15 LT1086CM
ADJ
C202 47uF
R50 120
R51 22
C203 330uF
C204 0.1uF
R49 22
D17
+1.5V GREEN POWER LED
JP13 SHOULD BE INSTALLED DURING ASSEMBLY
JP13
2 PIN JUMPER
+2.5VP
2.5V Regulator
U16 LM2596S-ADJ
R52 470 1%
R53 15 1%
L3
25uH
R55 470 1%
D18 MBRS340T3
C205 0.1uF
C206 330uF
C207 0.1uF
220
R54
D19
+2.5V GREEN POWER LED
STEWARD HI1206T500R-00
FB1
FB2
FB3
+2.5V
+2.5VA
+2.5VPLL
C209 0.1uF
C210 47uF
C211 0.1uF
C212 0.1uF
C213 1nF
C214 47uF
Ethernet Ground
System Ground
USB Ground
All resistors are 0805 body size.
All caps less than 1uF are 0805 body size and COG/NPO dielectric material.
Title
Motorola SPS TSPG -TECD ColdFire Group
Validation Board for MCF547x & MCF548x Microprocessors
Size B
Document Number
63A11380S - DC to DC power supply
Rev 1.0
Date: Friday, January 16, 2004
Sheet 13 of 18

Ethernet osc. - dual layout footprint for 8 and 14 pin DIL socketed osc.'s

DEBOUNCED -INT7 SIGNAL

U18

S1

KS11R22CQD

ABORT/-INT7

ADM708SAR

D20 RED -INT7 LED

R56 270

R58 100

/IRQ7

HARD RESET & VOLTAGE SENSE CONTROLLER

U21

S2

KS11R23CQD

RESET

ADM708SAR

D21 RED RESET LED

R59 270

R60 10K

R61 100

U22

MC74AC08DT

/BDM_RSTI

/EXT_RSTI

/RSTI

Buffered and OR'd /RSTI signal to the CPU sourced from the BDM port, expansion connectors or reset switch.

RP64 4x 4.7K

/OE
R/W
/TS
/RSTO

RP65 4x 4.7K

DSO
DSI
DSCLK
/BKPT

RP67 4x 4.7K

MTMOD3
MTMOD2
MTMOD1

MTMOD[3:0]

RP68 4x 4.7K

/BWE3
/BWE2
/BWE1
/BWE0

/BWE[3:0]

RP70 4x 4.7K

/SD_BA0
/SD_BA1
/FB_CS5
/FB_CS4

RP71 4x 10K

/IRQ6
/IRQ5

RP72 4x 4.7K

/FB_CS3
/FB_CS2
/FB_CS1
/FB_CS0

/FB_CS[5:0]

NOTE: 1K pull-up on /FB_TA signal to create sharp rising edge on termination of an external /FB_TA.

R62 1K

/TA

NOTE: Pull-up's for some of the the CPU control signals are shown above. The rest of the pull-ups are shown on sheet 15, Serial I/O.

TIN[3:0]

JP15 TIN0 Isolation D22
JP16 TIN1 Isolation D23
JP17 TIN2 Isolation D24
JP18 TIN3 Isolation D25

RP73 4x 270

Kingbright AA3528YC yellow LED's

NOTE: Please place D22 to D29 together in a line.

TOUT[3:0]

JP19 TOUT0 Isolation D26
JP20 TOUT1 Isolation D27
JP21 TOUT2 Isolation D28
JP22 TOUT3 Isolation D29

RP78 4x 270

Kingbright AA3528MBC blue LED's

TP3 /TS FLEX BUS TRANSFER START
TP4 /OE FLEX BUS OUTPUT ENABLE
TP5 R/W FLEX BUS READ NOT WRITE
TP6 /FB_CS0 FLEX BUS CHIP SELECT 0
/FB_CS[5:0]
TP7 CPU RESET I/P
TP8 /TA FLEX BUS TRANSFER ACKNOWLEDGE
TP9 /RSTO CPU RESET O/P
TP10 USBCLKIN USB CLOCK I/P
TP11 /IRQ7
TP12 USBCLKOUT USB CLOCK O/P
TP13 GROUND
TP14 GROUND
TP15 GROUND
TP16 GROUND

NOTE: Place TP13, TP14, TP15 & TP16 at the corners of the PCB to allow easy connection of 'scope probe ground leads.

Important Note - all unconnected pull-up and pull-down resistor pack connections, on all schematics pages, need to be connected to an unmasked via.

RP75 4x 4.7K
RP76 4x 4.7K
RP77 4x 4.7K

Closed/On SW4 Open/Off

FB_AD0
FB_AD1
FB_AD2
FB_AD3
FB_AD4
FB_AD5
FB_AD8
FB_AD9
FB_AD10
FB_AD11
FB_AD12
MTMOD0

Configuration DIP switch - Grayhill 78RB12

NOTE: switch bank SW4 default setting = all switches open/off.

RP79 4x 4.7K

IMPORTANT NOTE: THE /RSTO SIGNAL MUST BE USED TO DRIVE THE OUTPUT ENABLE PINS OF U25 & U26 TO ALLOW THE FB_AD0 to FB_AD5 & FB_AD8 to FB_AD12, plus MTMOD0 SIGNALS TO BE LATCHED CORRECTLY BY THE CPU FOR CONFIGURATION AT RESET.

U25 MC74LCX541DT

U26 MC74LCX541DT

FB_AD[31:0]

MTMOD[3:0]

C221 1nF
C222 0.1uF
C223 1nF
C224 0.1uF

OFF - SW4 - ON

Port size conf.	SW4-1	Port size conf.
Port size conf.	SW4-2	Port size conf. - 16bit default setting SW1 = 0, SW2 = 1.
Auto Ack. conf.	SW4-3	Auto Ack. conf. - default AA enabled 63 wait states.
Byte enable conf.	SW4-4	Byte enable conf. - default BE signals assert for read & write cycles.
Flexbus conf.	SW4-5	Flexbus conf. - default - PCI_AD[31:0] used for PCI & AD[31:0] for Flex bus addr. & data
Flexbus size conf.	SW4-6	Flexbus size conf.- default BWE[1:0] = FB_AD[1:0] & BWE[3:2] = TSIZ[1:0]
Divide ratio encoding	SW4-7	Divide ratio encoding - default value = 00011 for FB_AD[12:8]
Divide ratio encoding	SW4-8	Divide ratio encoding - default clock ratio is 1:2 external:core
Divide ratio encoding	SW4-9	Divide ratio encoding - CLKIN PCI & Flexbus range 41.66 to 66.66MHz for MCF547x (41.66 to 50.00MHz for MCF548x)
Divide ratio encoding	SW4-10	Divide ratio encoding - Internal XLB & SDRAM bus range 83.33 to 133.33MHz for MCF547x (83.33 to 100.00MHz for MCF548x)
Divide ratio encoding	SW4-11	Divide ratio encoding - Core frequency range - 166.66 to 266.66MHz for MCF547x (166.66 to 200MHz for MCF548x)
BDM/JTAG Mode	SW4-12	BDM/JTAG mode - default is BDM mode, MTMOD = 0.

NOTE: Please place this table on the silkscreen on the topside of the PCB close to SW4.

C215 10nF
C216 0.1uF

Place RP66 & RP69 as close to U19 & U20 as possible. Also, ensure clock traces are as near equal in length as possible to the CPU, FPGA, PCI connectors & SRAM.

TP2 CPU CLOCK I/P

RP66 4x 22

FPGA_CLK
CLKIN
TEST_CLK
SRAM_CLK

U19 MPC905D

RP69 4x 22

PCI_CLK3
PCI_CLK2
PCI_CLK1
PCI_CLK0

U20 MPC905D

PCI & System socketed osc. - dual layout footprint for 8 and 14 pin DIL osc.'s

U17

R57 10K

66MHz

JP14 Jumper 3 way

Default setting for JP14 is across pins 1&2.

J25

External Clock Input (SMA connector)

C217 10nF
C218 0.1uF

Place RP74 as close to U24 as possible. Also, ensure clock traces are as near equal in length as possible to the Ethernet transceivers (PHY's).

ETH1_CLK
ETH0_CLK

RP74 4x 22

U24 MPC905D

U23

R63 10K

25MHz

Ethernet socketed osc. - dual layout footprint for 8 and 14 pin DIL osc.'s

C219 10nF
C220 0.1uF

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NOTE: place U28 (IRDA transceiver) on the edge of the EVB.

Default setting for JP23 & 24 is fitted.

UART2 TxD Isolation

UART2 RxD Isolation

Default setting for JP25 is between pins 1&2.

IRDA mode select

TFDU6102

NOTE: the I2C bus on the MCF547x/8x processor is 3.3V tolerant only. If connection to a 5V system is required high frequency voltage level shifters will be required between the peripheral and processor.

Serial EEPROM address =2 on I2C bus.

AT24C02AN-10TI-2.7
2Kb Serial EEPROM

SAMTEC MTMM-126-04-G-D-148

0.1" pitch BERG connector

NOT POPULATED AT ASSEMBLY.

MAX3225CAP or ICL3225CA

RS232 Transceiver.

TERMINAL PORT
9-WAY D-TYPE
(Female)

Default setting for JP26 & JP27 is fitted.

UART0 /RTS Isolation

UART0 /CTS Isolation

AUXILIARY PORT
9-WAY D-TYPE
(Female)

Default setting for JP28 & JP29 is fitted.

UART1 /RTS Isolation

UART1 /CTS Isolation

QSPI connector 0.1 pitch

NOT POPULATED AT ASSEMBLY.

NOTE: Pull-up's for some of the the CPU control signals. The rest of the pull-ups are shown on sheet 14, Reset, Configuration & Clocks.

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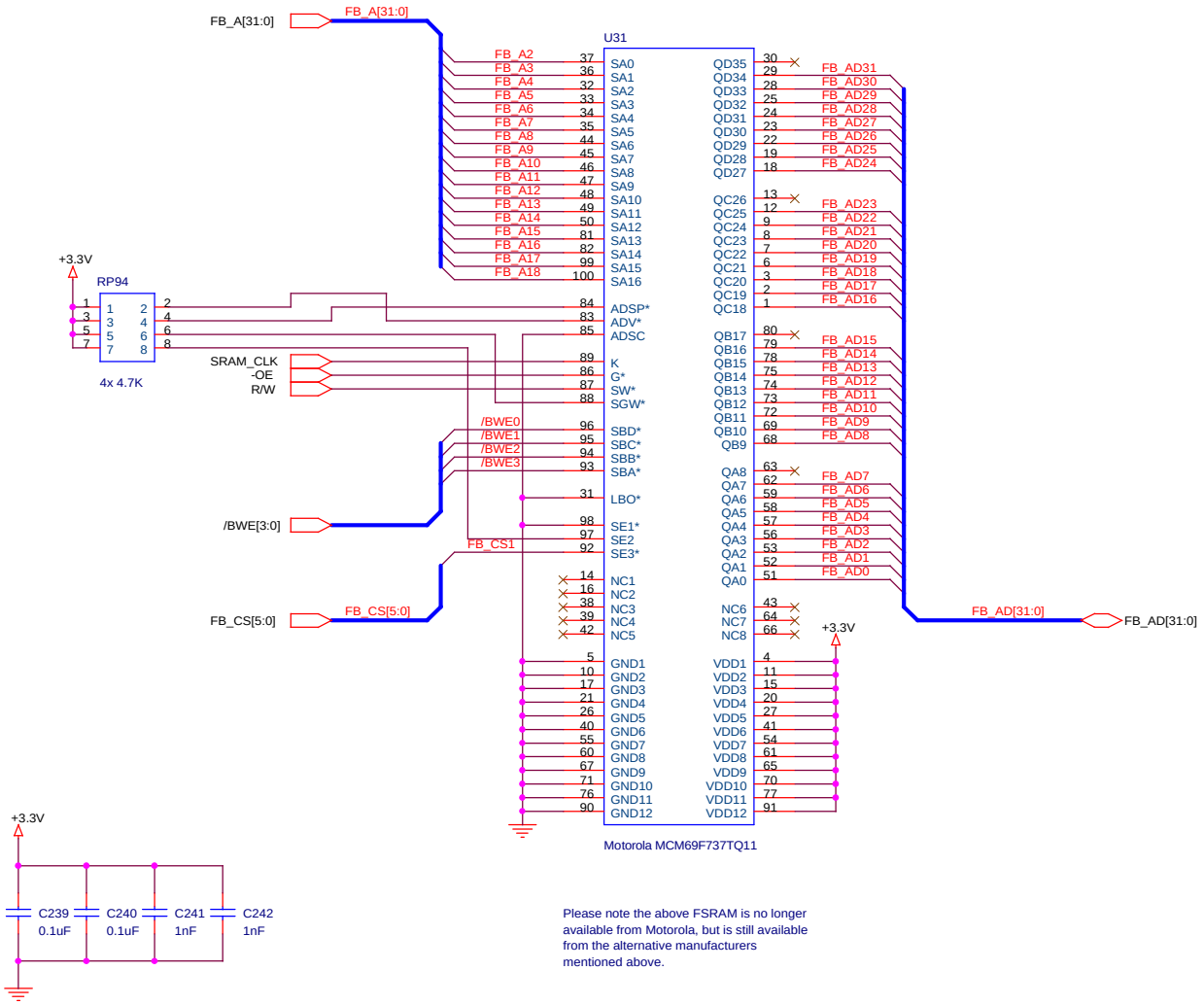
NOTE: Alternative FSRAM's with the same PCB footprint and functionality are :- Samsung K7B403625M, Cypress CY7C1345B, IDT 71V3577 & Micron MT58L128L36F1.



Please note the above FSRAM is no longer available from Motorola, but is still available from the alternative manufacturers mentioned above.

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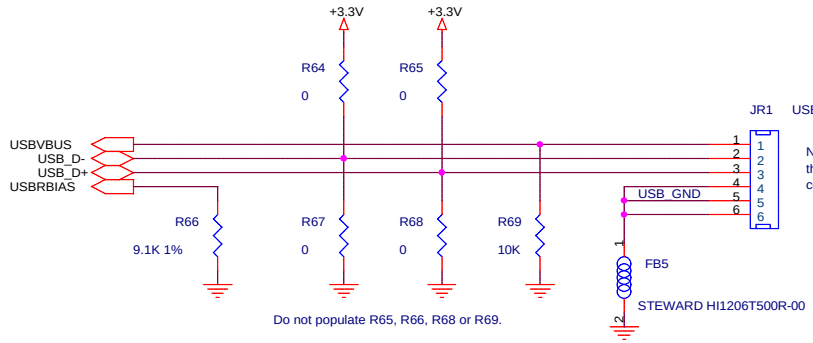
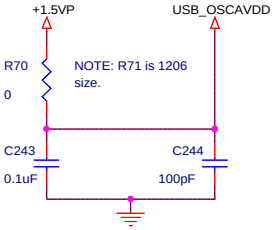
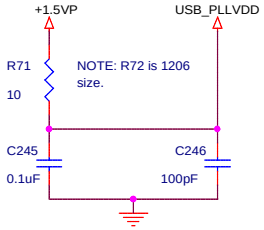
NOTE: there must be a 90ohm differential phase impedance between signals USB_D- & USB_D+. Please couple these traces as soon as they leave U5 (sheet4) through to JR1.



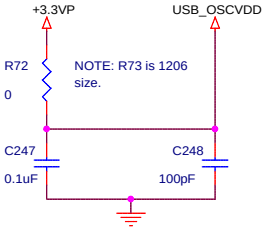
NOTE: please ensure that the USB connector shield is connected to USB ground.



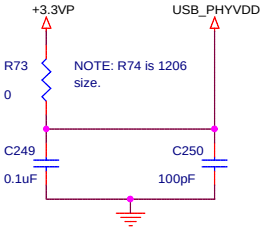
NOTE: place the circuit above as close as possible to pin AD15 on the MCF5475, CPU - U5, sheet 4. As this is the filter for USB_OSCAVDD.



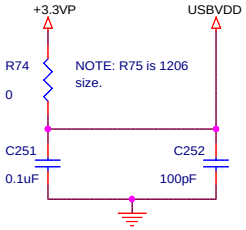
NOTE: place the circuit above as close as possible to pin AD16 on the MCF5475, CPU - U5, sheet 4. As this is the filter for USB_PLLVDD.



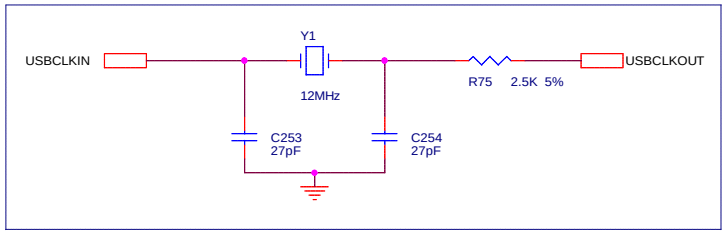
NOTE: place the circuit above as close as possible to pin AC13 on the MCF5475, CPU - U5, sheet 4. As this is the filter for USB_OSCVDD.



NOTE: place the circuit above as close as possible to pin AC16 on the MCF5475, CPU - U5, sheet 4. As this is the filter for USB_PHYVDD.



NOTE: place the circuit above as close as possible to pins AE18 on the MCF5475, CPU - U5, sheet 4. As this is the filter for USBVDD.



NOTE: place the circuit bounded by the dotted line as close as possible to pins AF14 & AF15 on the MCF5475, CPU - U5, sheet 4.

Motorola SPS TSPG -TECD ColdFire Group

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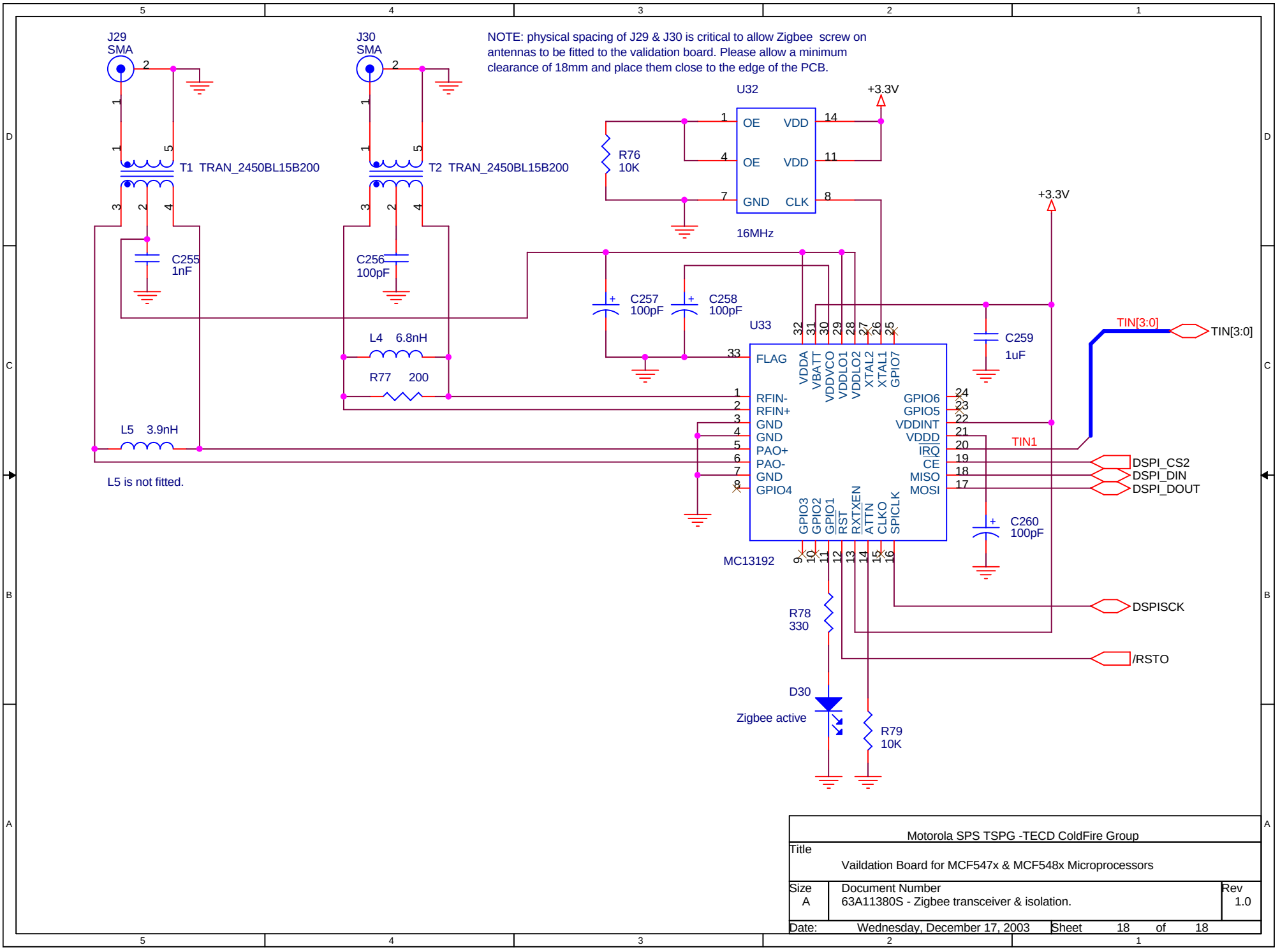

Motorola SPS TSPG -TECD ColdFire Group		
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Size: A	Document Number: 63A11380S - Zigbee transceiver & isolation.	Rev: 1.0
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