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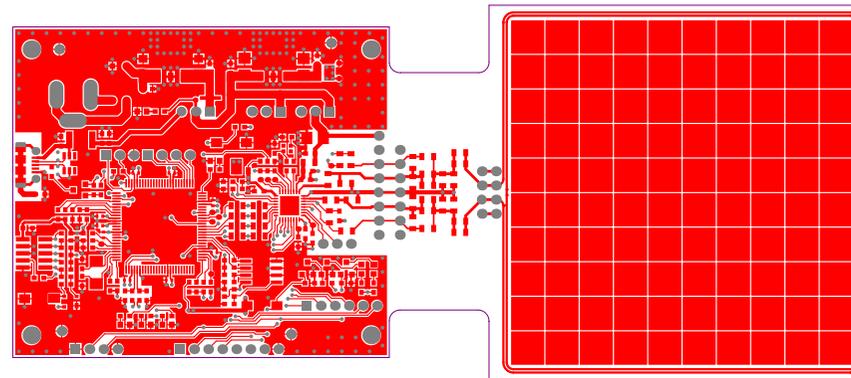
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Title: CLEV6630B	
Date: 11.05.2017	Revision: V2.0
File: CLEV6630B_V2.0.PcbDoc	Designed by:
NXP	

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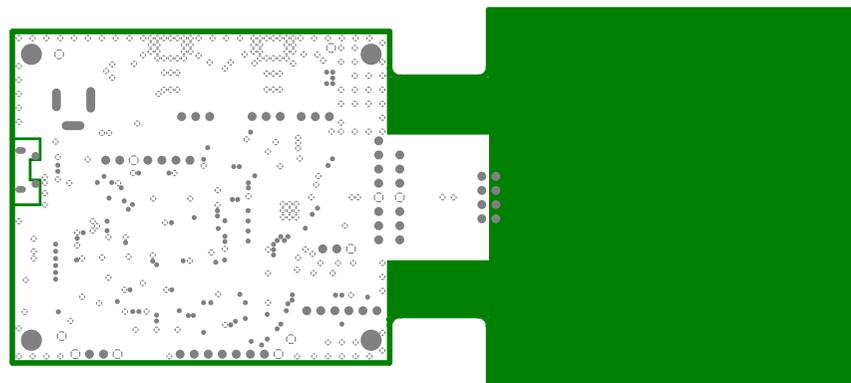
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Date: 11.05.2017	Revision: V2.0
File: CLEV6630B_V2.0.PcbDoc	Designed by:
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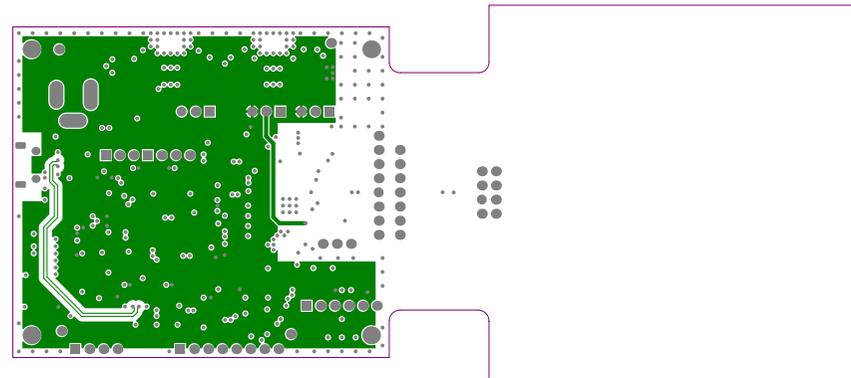
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Date: 11.05.2017	Revision: V2.0
File: CLEV6630B_V2.0.PcbDoc	Designed by:
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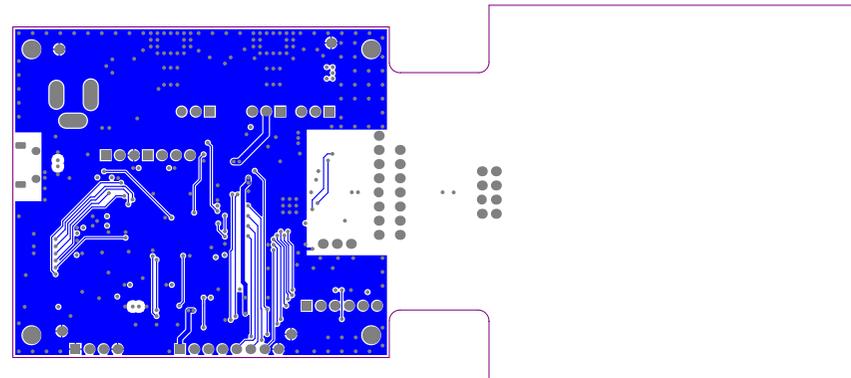
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Date: 11.05.2017	Revision: V2.0
File: CLEV6630B_V2.0.PcbDoc	Designed by:
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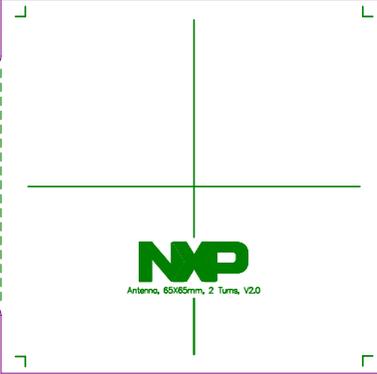
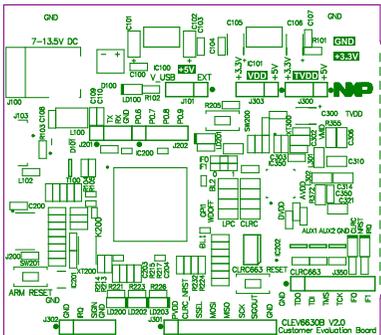
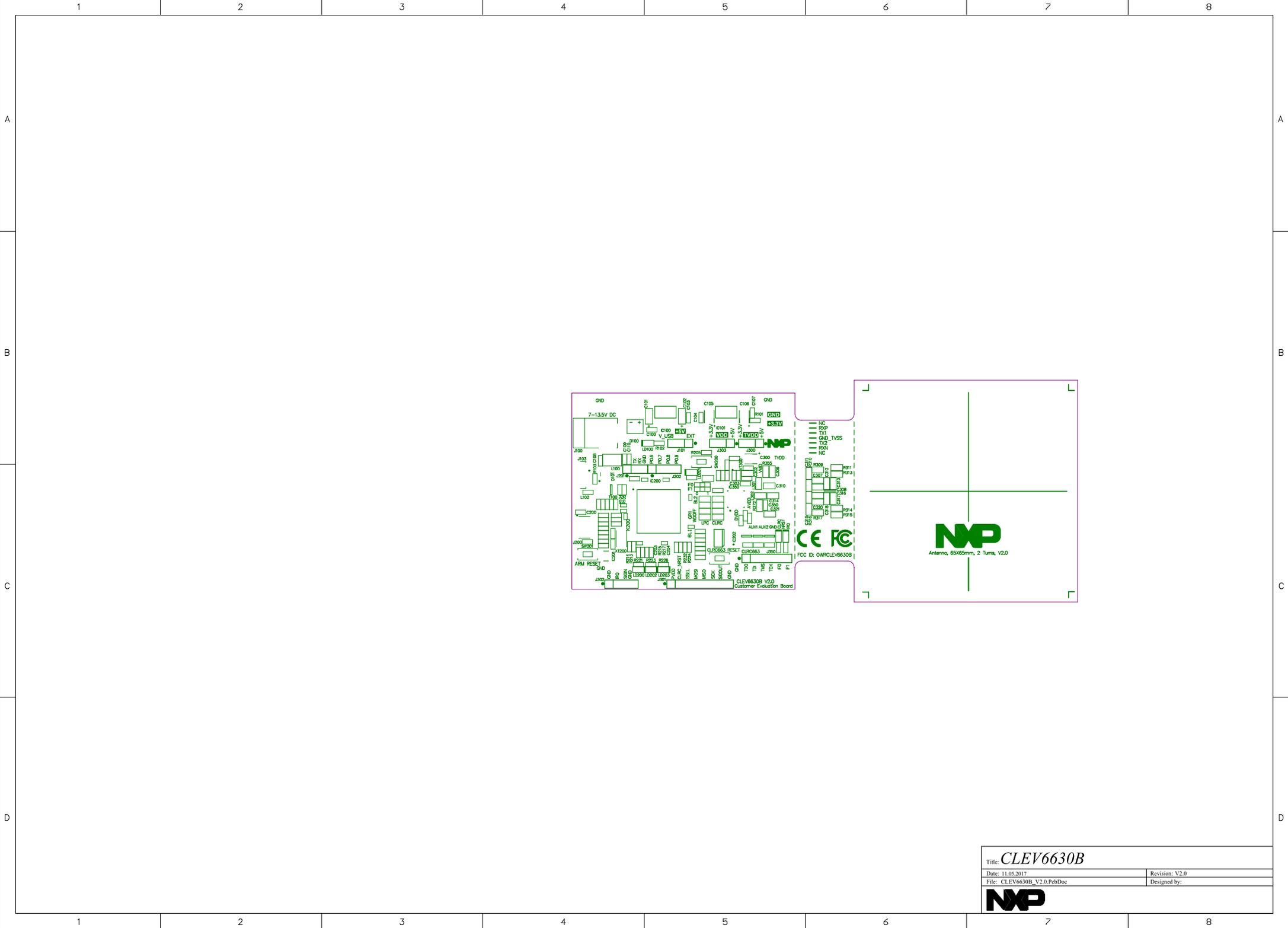
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Date: 11.05.2017	Revision: V2.0
File: CLEV6630B_V2.0.PcbDoc	Designed by:
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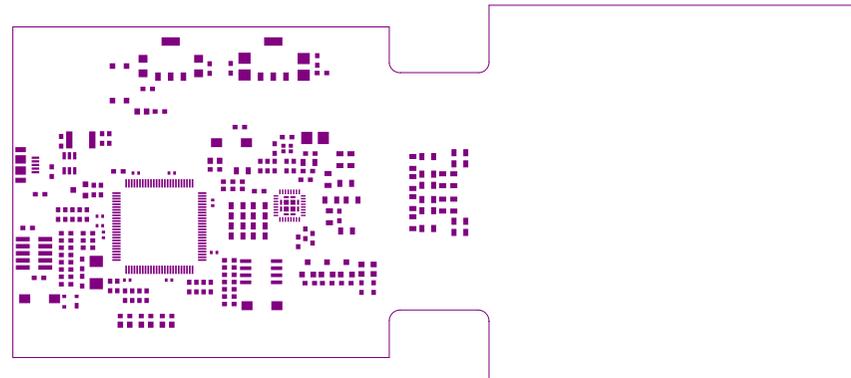
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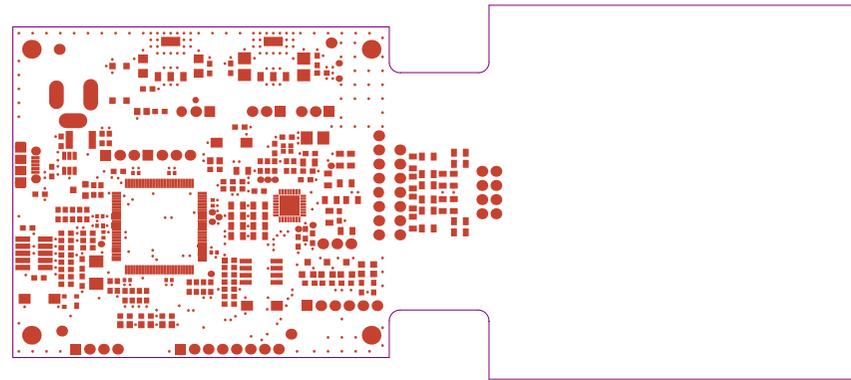
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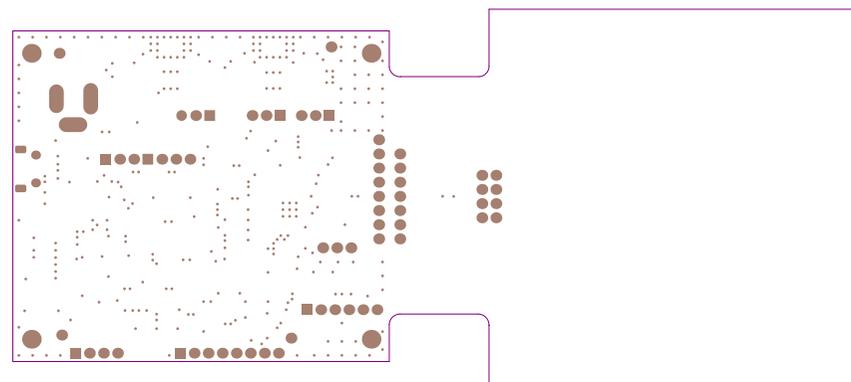
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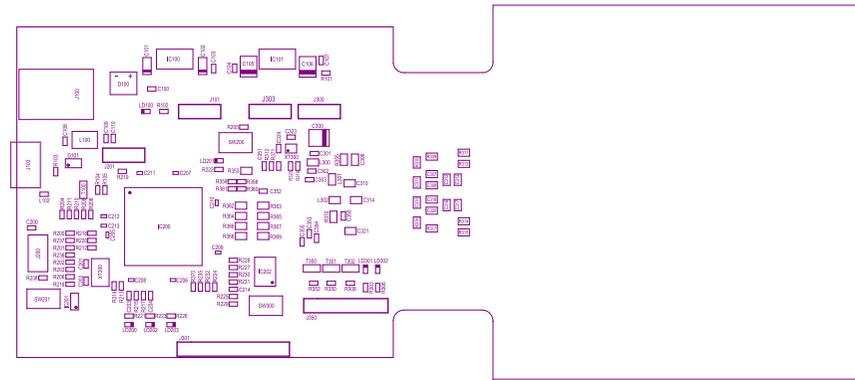
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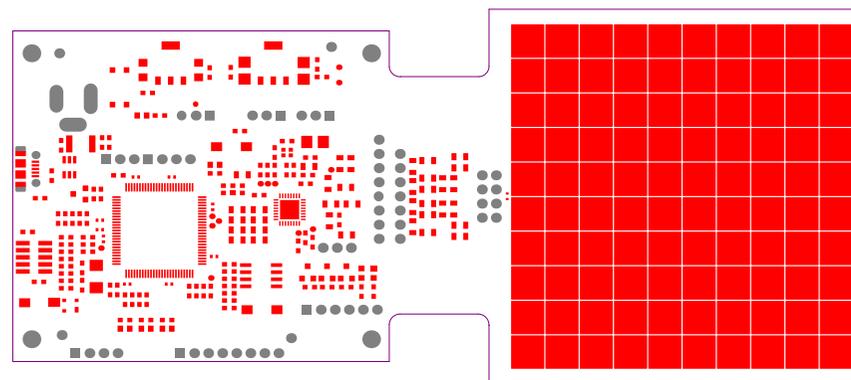
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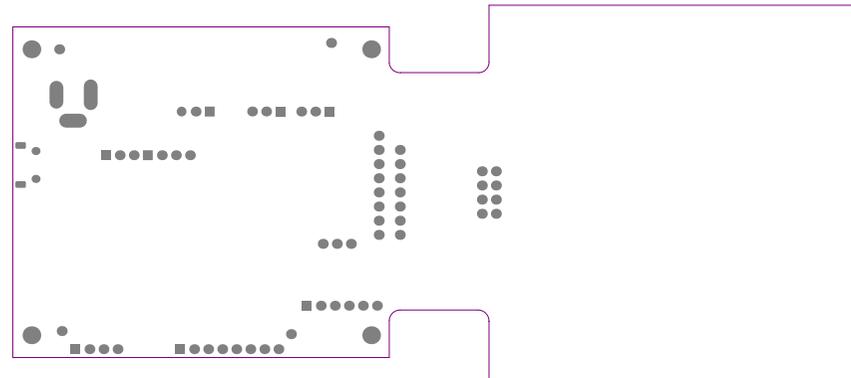
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Master Drawings:

- material: FR4, Tg: 150
- thickness: 1,6mm (min 1,44, max 1,7mm)
- layer stackup: - Top Cu: 35um
 - prepreg 0,14mm
 - Internal Plane1 Cu: 35um
 - core 1,0mm
 - MidLayer1 Cu: 35um
 - prepreg 0,14mm
 - Bottom Cu: 35um
- min. hole metallization: 20um
- surface finishing: ENIG
- solder mask: - in accordance with IPC-SM-840
 - Liquid Photo Imageable (LPI)
 - color: BLUE
 - unless otherwise defined (in gerber), solder mask overlap on SMT pads is not allowed

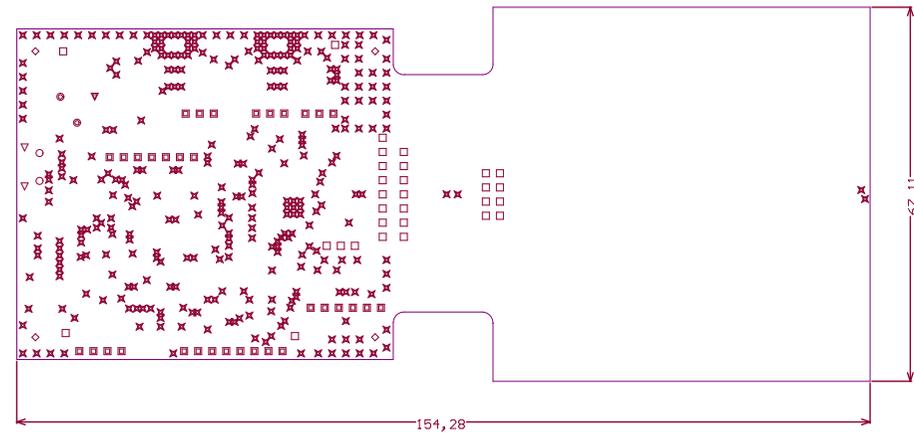
- silk screen: Yes, White
- impedance control: Yes, see table below
- board must meet the acceptable level of IPC-A-800, Class 2, current revision.
- bow and twist: - max. 0,75% SMT boards
 - max. 1,5% THT boards
- point of origin (0,0): bottom left corner
- board is designed on 0,050 mm grid
- primary side: Top layer

Impedance table:

	Differential pair 90 [ohm]
	Width / Spacing [mm]
Layer1	0,22 / 0,3
Layer2	
Layer3	0,18 / 0,40
Layer4*	0,22 / 0,3

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
▽	1	1,000mm (39,37mil)	PTH	Slot
▽	2	0,400mm (23,62mil)	PTH	Slot
○	2	0,800mm (39,37mil)	PTH	Round
○	2	1,000mm (39,37mil)	PTH	Slot
◇	4	3,200mm (126,00mil)	NPTH	Round
□	30	1,000mm (39,37mil)	PTH	Round
■	34	1,016mm (40,00mil)	PTH	Round
✕	334	0,300mm (11,81mil)	PTH	Round
	409 Total			

*Slot definitions : Routed Path Length = Calculated from tool_start centre position to tool_end centre position.
 Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout



Title: **CLEV6630B**

Date: 11.05.2017	Revision: V2.0
File: CLEV6630B_V2.0.PcbDoc	Designed by:

