

MIMXRT1180-EVK

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1. Unless Otherwise Specified:

All resistors are in ohms, 1/16 Watt,0402
All capacitors are in uF,0402
All voltages are DC
All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

Revision History

Rev. Code	Date	By	Description
X1	2021-07-06	Shawn Shi	Draft version
A	2021-11-15	Shawn Shi	Initial Release
B	2022-03-18	Shawn Shi	1. Add one more GPIO interrupt button. 2. Re-assign CANx_TX/CANx_RX to IOMUX without Boot mode config function. 3. Consolidate MDC/MDIO of all 5 ethernet PHY using the same pinout. 4. Add dedicate buffer for all system reset logic control. 5. Replace audio codec chip WM8960(To be EOL) with WM8962. 6. Replace OCT Flash from MX25UM51345GXD100 to MT35XU512ABA2G12-0AAT.
C	2023-03-17	Shawn Shi	1. Changed HyperRAM from S27KL0642DPBH020 to W957A8MFYA5K. 2. Changed ADC_VREF external option to VDD_1V8. 3. Remove route of MCULINK_TRG_RST to MCU_JTAG_nTRST. 4. Change ENET2&ENET3 signals to be enabled, so 5 ENET are available as default. 5. Change HyperRAM to be enabled and disable SDRAM by default. 6. Change ENET1_INT_B,ENET1_RST_B to 1V8 pullup. 7. Enable the ISP Automatic Control using jumper setting instead of 0ohm resitors. 8. Add jumper J105 for WIFI_WAKE_B_3V3 signal, default open. 9. Populate R782, R783 and R778.
C1	2023-05-05	Shawn Shi	1. Reserve 1pc RGMII/RMII connector for PHY daughter card extension. 2. Reserve LPSPi option to enable new radio features/functionally. 3. Replace EEprom with 24LC32A.
C2	2023-06-20	Shawn Shi	1. Add level shifter for ENET1_INT_B,ENET3_INT_B,ENET1_RST_B,ENET3_RST_B. 2. Correct PN from MIMXRT1189CVM8A to MIMXRT1189CVM8B. 3. Assign SD1_VSELECT to GPIO_AD_34. 4. Change DECAP over VDDA_1P8_IN to 1uF.
C3	2023-10-11	Shawn Shi	No layout change 1. Replace HyperRAM with W956A8MBYA5K. 2. Replace SINC_ADC with AMC1106M05DWV. 3. DNP R142 for ECAT_LINK. 4. Change JP7 default setting to OPEN.
C4	2025-02-28	Shawn Shi	1. Change RT1180 silicon from MIMXRT1189CVM8B to MIMXRT1189CVM8C. 2. Add notes on Page15 & Page19, No POE function supported.

Jumper Setting

REF DES	JUMPER(DEFAULT)	PAGE NAME
J1,J3	1-2	03 Main Power
J4,J135	1-2	04 Power Domain
J6,J9,J12,J14,J77	1-2	05 MIMXRT1180 Part1
J11	2-3	05 MIMXRT1180 Part1
J76	1-2	08 SD Card
J57	2-3	08 SD Card
J58,J59,J75	2-3	09 FLEXSPI Flash
J97,J98,J99,J100	1-2	13 SAI
J65,J72	2-3	17 PHY2_RGMII
J63,J73	2-3	18 PHY3_RGMII
J78,J79	1-2	23 M.2 Socket
J90,J91,J93	1-2	24 Boot
JP6	1-2	25 MCU-Link


3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
_B Denotes - Active-Low Signal
<> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

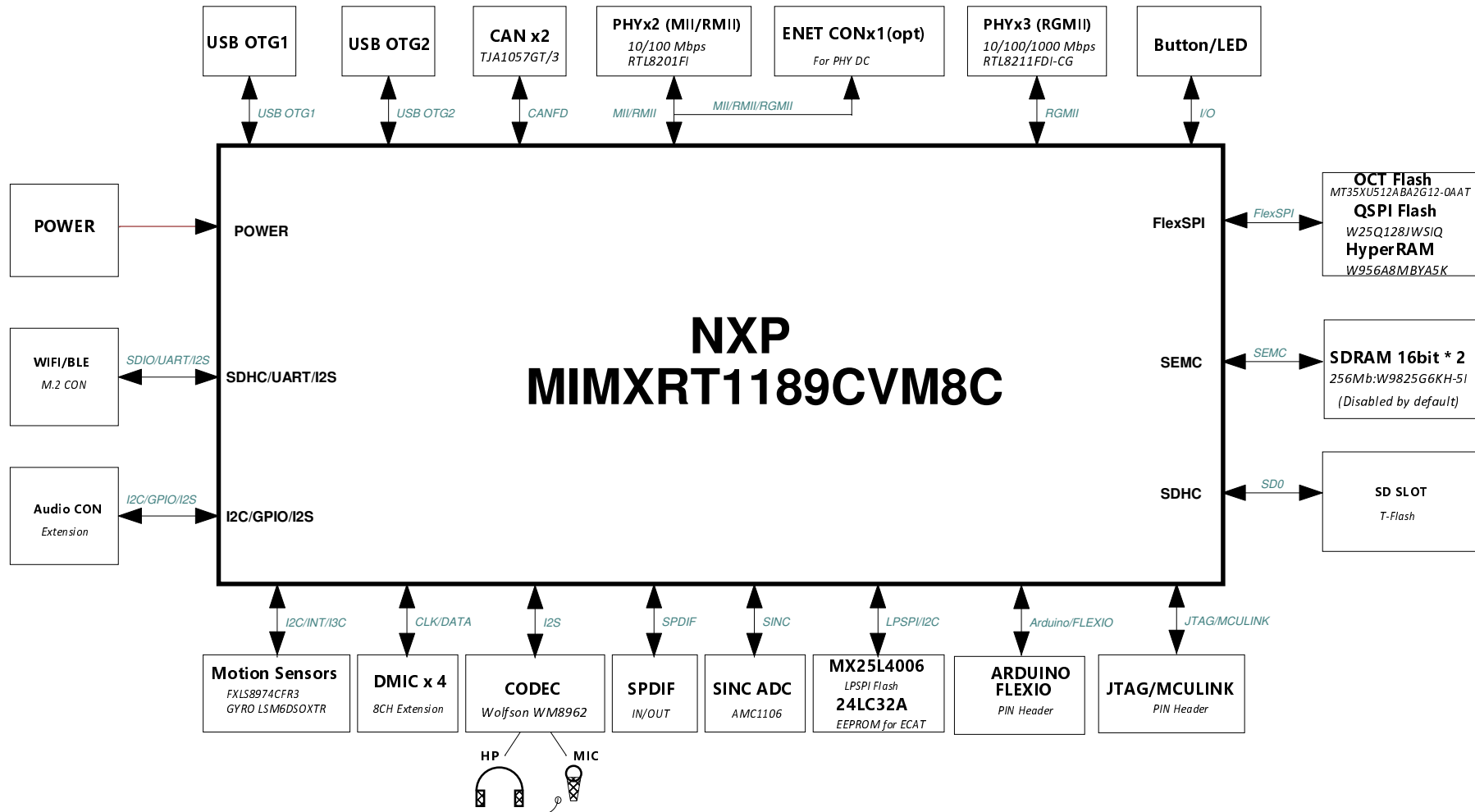
Switch Setting

REF DES	SWITCH(DEFAULT)	PAGE NAME
SW5	off.off.off.on	24 Boot

		Microcontroller Product Group 6501 William Cannon Drive West Austin, TX 78735-8598	
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ICAP Classification: CP:		EUC: PUB:	
Designer: Shawn Shi	Drawing Title: MIMXRT1180-EVK		
Drawn by: Shawn Shi	Page Title: Cover		
Approved: Yes	Size C	Document Number SCH-50577, PDF: SPF-50577	Rev C4
Date: Tuesday, April 15, 2025		Sheet 1 of 31	

MIMXRT1180-EVK

Block Diagram RevC4



ICAP Classification:	CP:	I/O:	PUR:
Drawing Title:	MIMXRT1180-EVK		
Page Title:	Block Diagram		
Size C	Document Number	SCH-50577, PDF: SPF-50577	Rev C4
Date:	Monday, March 03, 2025	Sheet 2 of 31	

Main Power

Reverse Voltage Protection

Over-Voltage Protection

The diagram illustrates the main power supply circuit for a device, featuring two primary protection sections: Reverse Voltage Protection and Over-Voltage Protection.

Reverse Voltage Protection: This section includes a barrel connector (J2) with pins for DC_5V_IN, SLK+DC_5V_IN, and GND. The input is filtered by a 1µF capacitor (C3) and a 5A/32V fuse (F1). The circuit then passes through a diode bridge (D1, MMSZ5V1ST1G) to protect against reverse voltage. The output is connected to the 5V_USB_OTG1 and 5V_USB_OTG2 pins of the USB connector (J1).

Over-Voltage Protection: This section monitors the 5V supply for over-voltage conditions. It uses a voltage divider (R3, R4) to sense the 5V line. The sensed voltage is compared against a reference (D2, MMBT3906TT1G) and a threshold (D3, MMBT3906TT1G). If an over-voltage condition is detected, the circuit triggers the 5V_USB_OTG2 pin to go low, which is connected to the 5V_SDA_PSW pin of the USB connector (J1).

SW1 (2-3/5-6) -> 5V ON
SW1 (1-2/4-5) -> 5V OFF

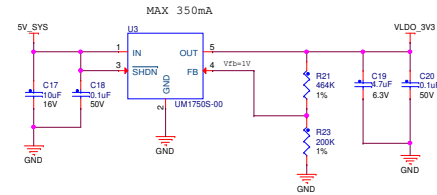
The circuit also includes a 5V_SDA_PSW pin connected to the 5V_USB_OTG2 pin of the USB connector (J1). The 5V_USB_OTG1 pin is connected to the 5V_SDA_PSW pin. The 5V_USB_OTG2 pin is connected to the 5V_SDA_PSW pin. The 5V_SDA_PSW pin is connected to the 5V_SDA_PSW pin. The 5V_SDA_PSW pin is connected to the 5V_SDA_PSW pin.

[illegible]

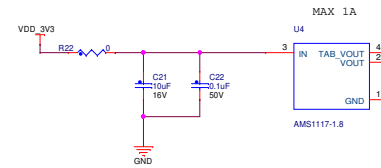
Four circuit diagrams are shown, each representing a test point (TP3, TP4, TP5, and TP6) connected to ground (GND) through a 10k resistor. Each diagram includes a note: "SILK = GND".

ICAP Classification:		CP:	IUO:	PUB:
Drawing Title:				
MIMXRT1180-EVK				
Page Title:				
Main Power				
Size C	Document Number SCH-50577, PDF: SCH-50577			Rev C4
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3V3 LDO for BBSM

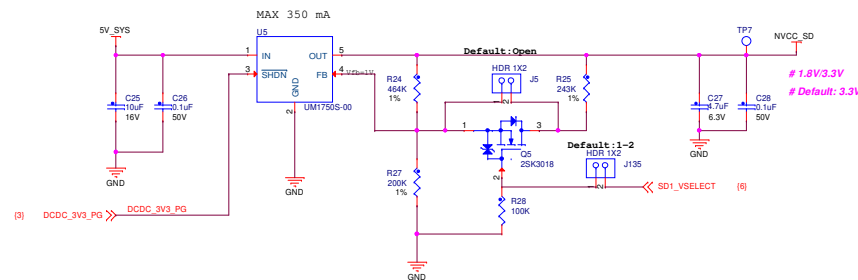


1V8 LDO

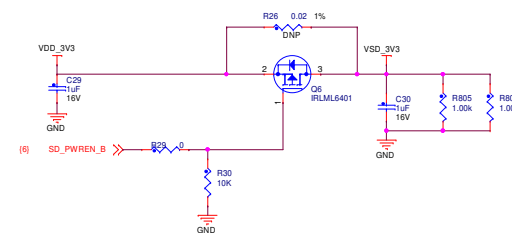


Flash VCC Option
1.8V default

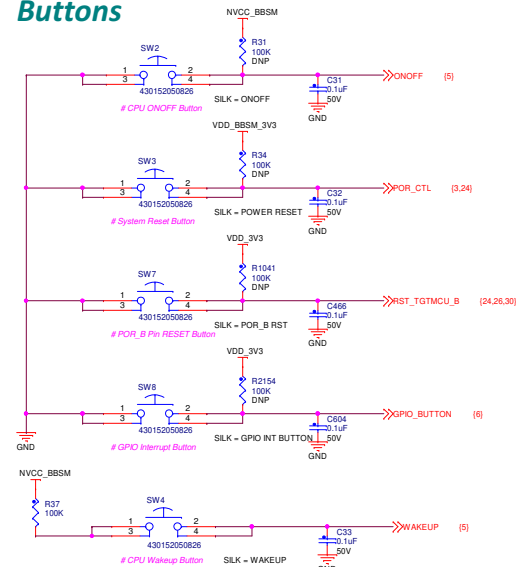
NVCC_SD <SD3.0>



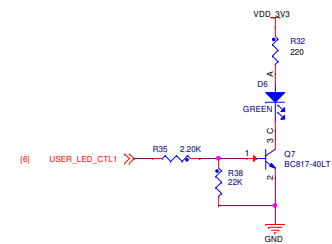
SD Card Power Switch



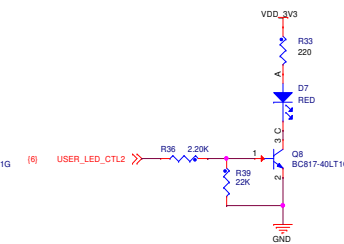
Buttons



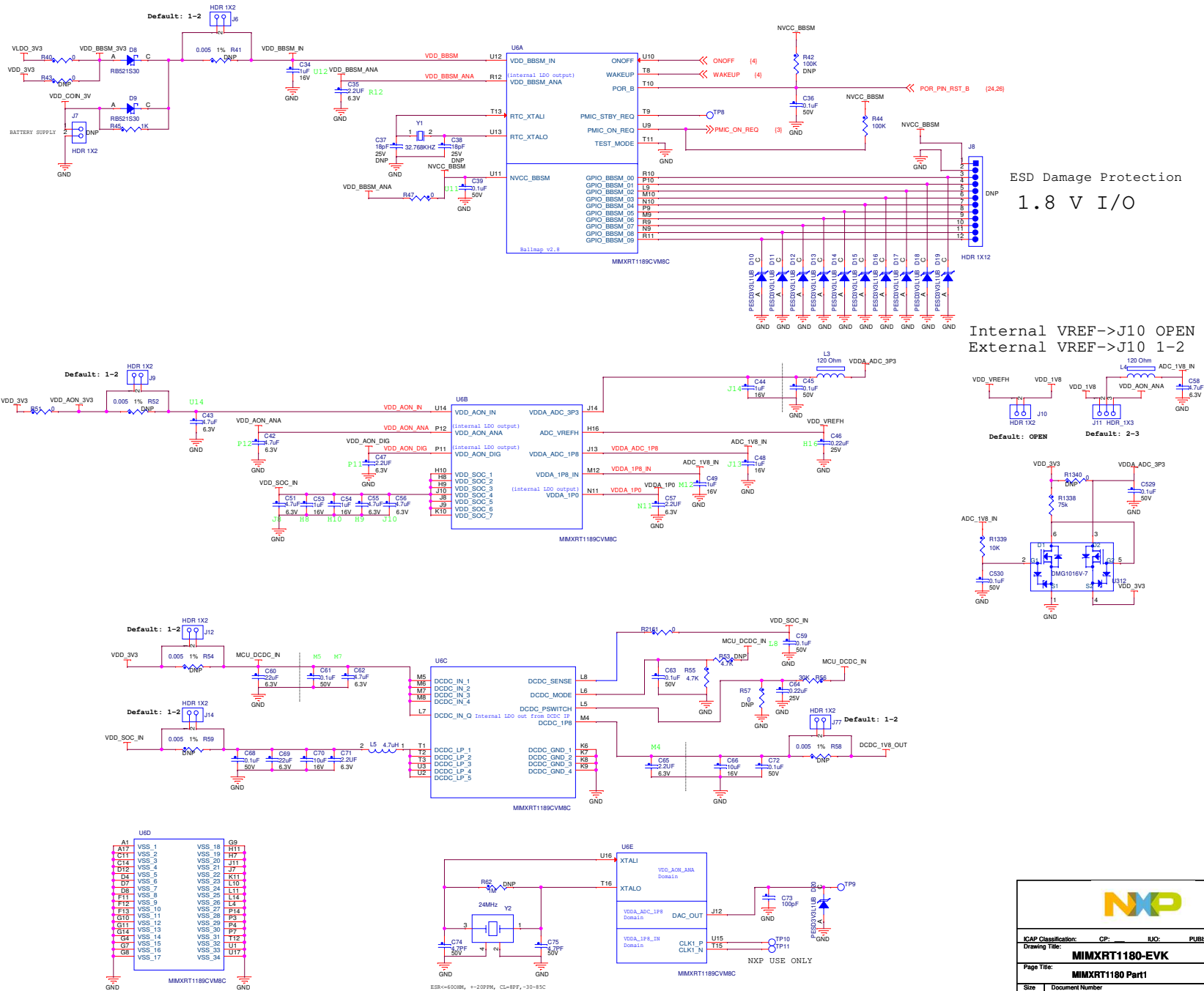
USER LED1



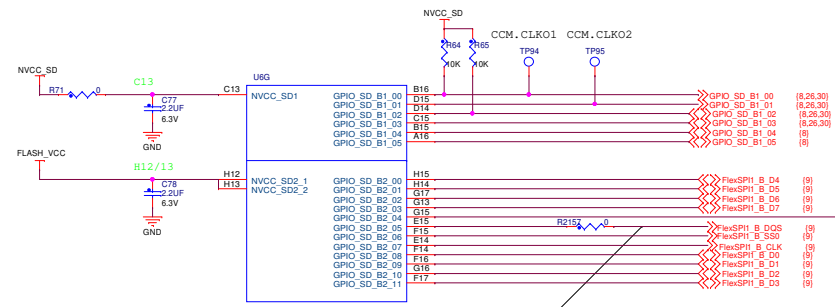
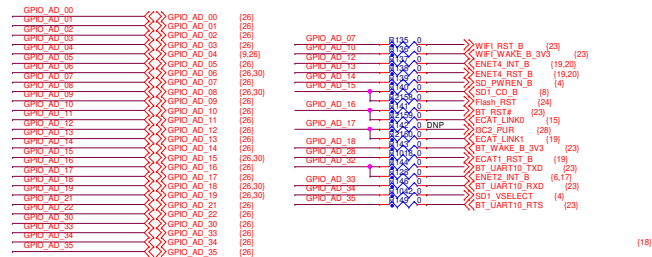
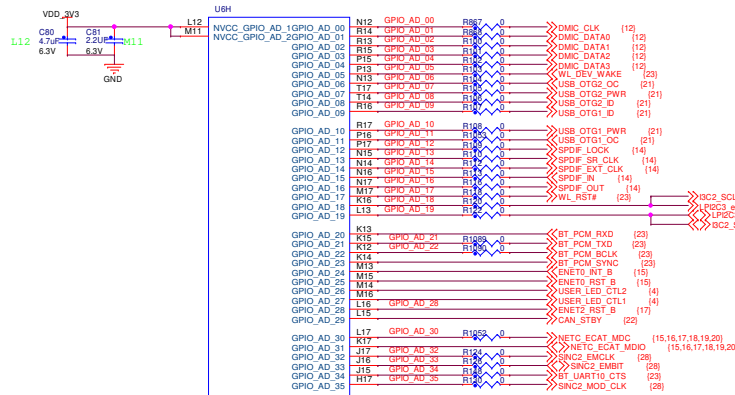
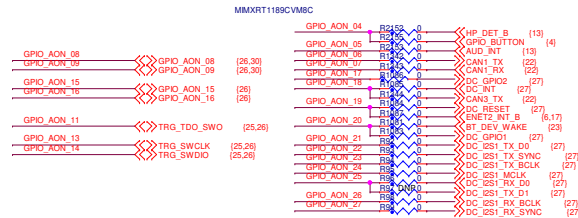
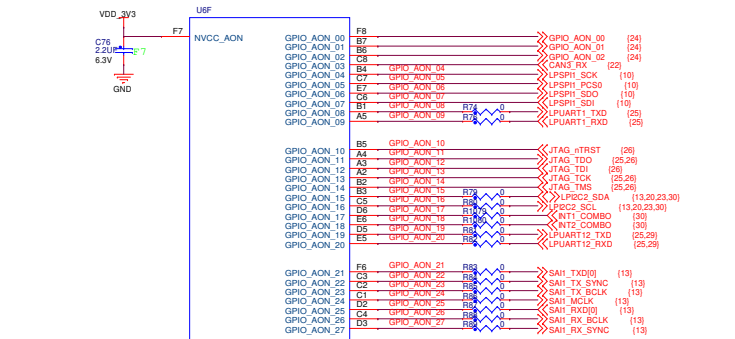
USER LED2



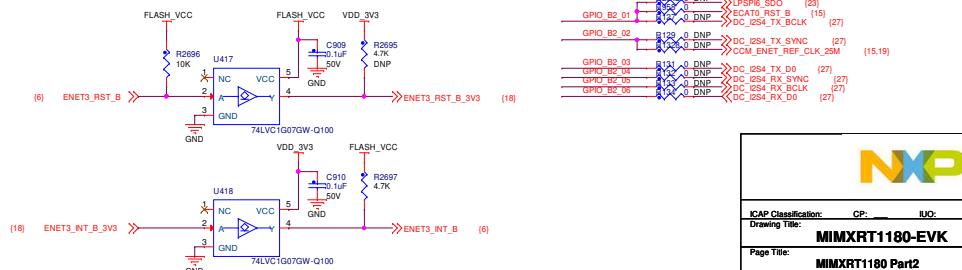
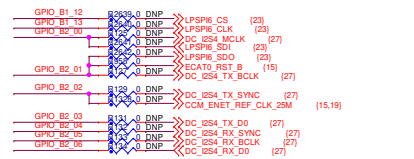
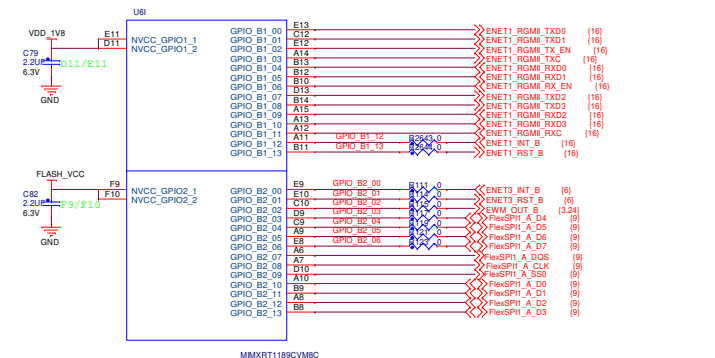
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Page Title:	Power Domain		
Size C	Document Number	SCH-50577, PDF: SPF-50577	Rev C4
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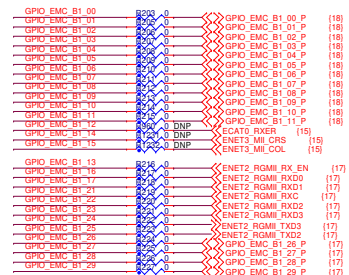
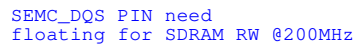


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MIMXRT1180-EVK				
Page Title:				
MIMXRT1180 Part1				
Size	Document Number	SCH-50577, PDF: SPF-50577		Rev
C				C4
Date:		Friday, February 28, 2025	Sheet	5 of 31

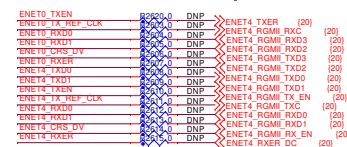
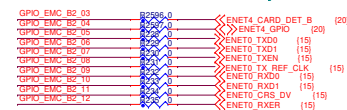


Floating FlexSPI_DQS PIN for QSPI Flash RW @133MHz
(R2157 should be placed close to MCU pin)

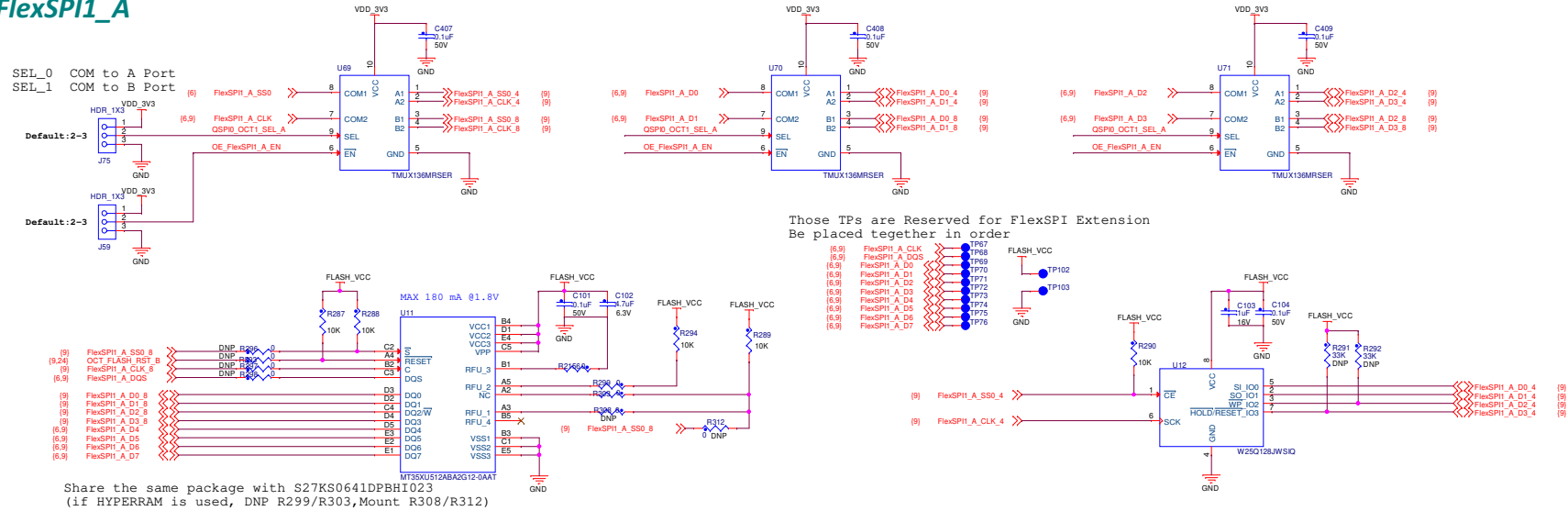




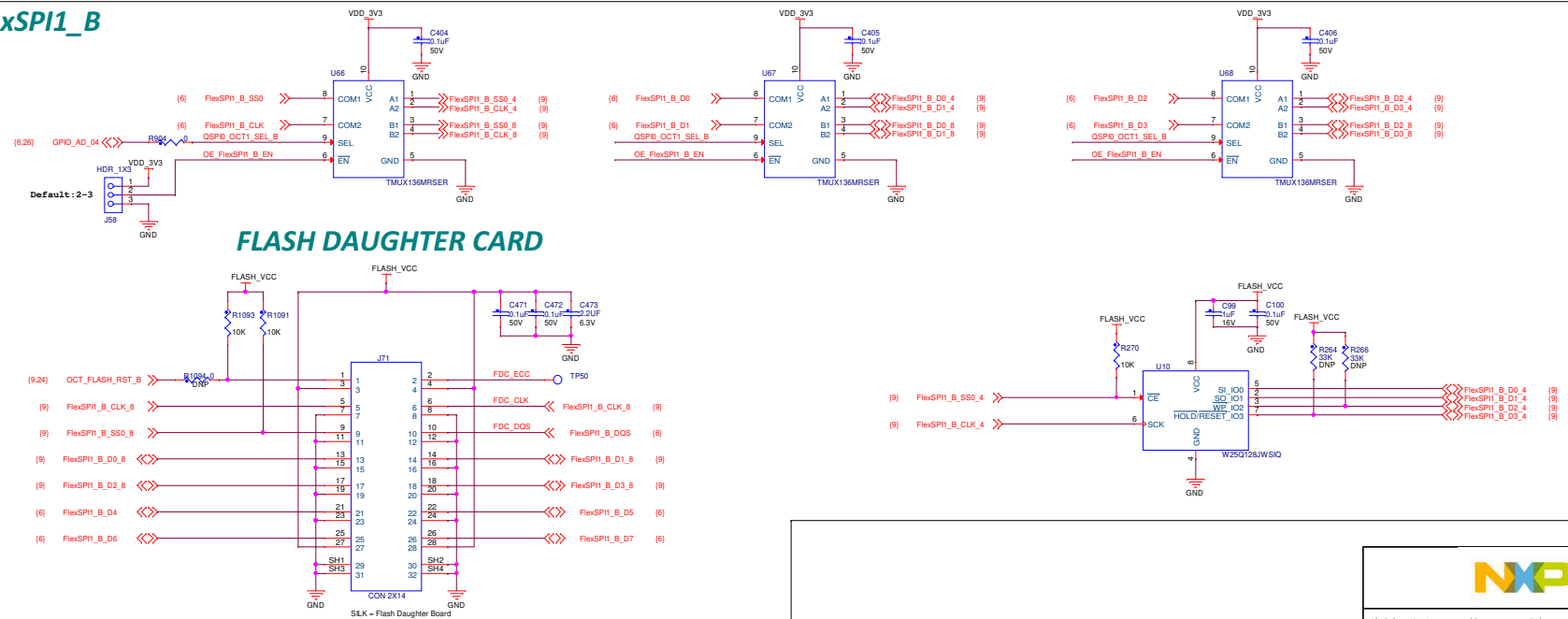
ENET0&ENET4 RMII Multiplex



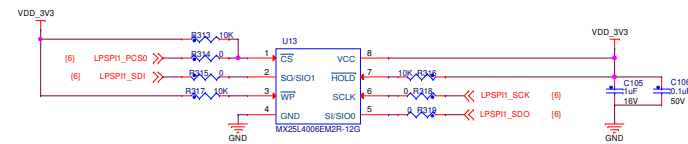
FlexSPI1_A



FlexSPI1_B

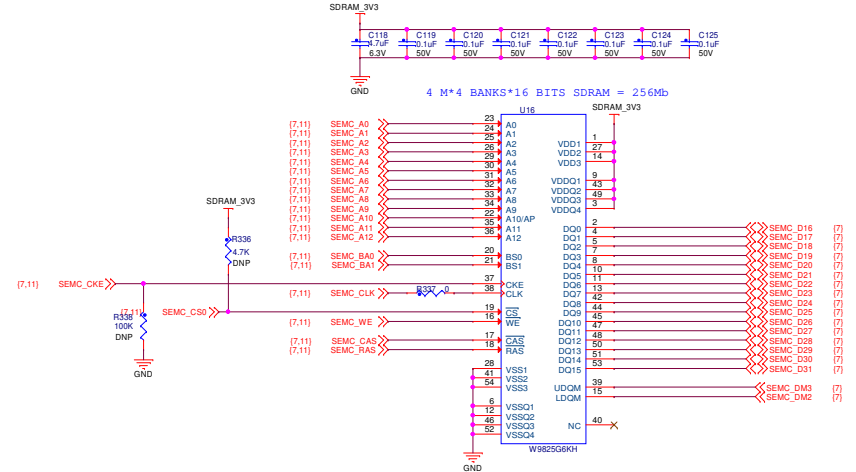
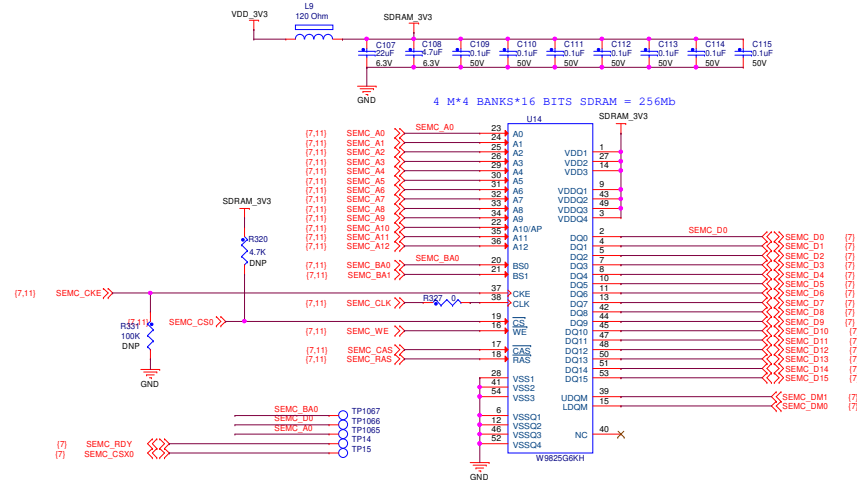


LPSPi Flash(Secondary Boot)

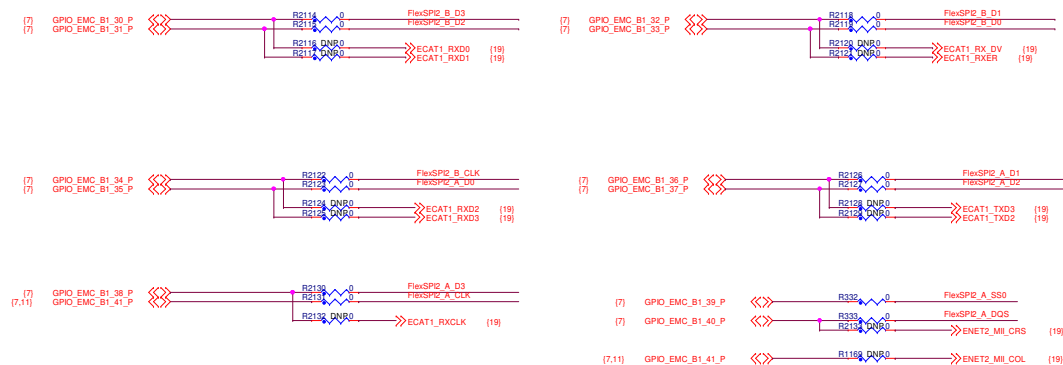


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Drawing Title:	MIMXRT1180-EVK		
Page Title:	LPSPi Flash		
Size C	Document Number SCH-50577, PDF: SPF-50577	Rev C4	
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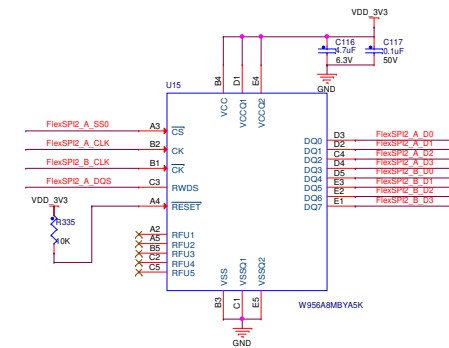
SDRAM



Signal Multiplex



HyperRAM(64Mb)



ICAP Classification: CP: IUO: PUB:

Drawing Title: **MIMXRT1180-EVK**

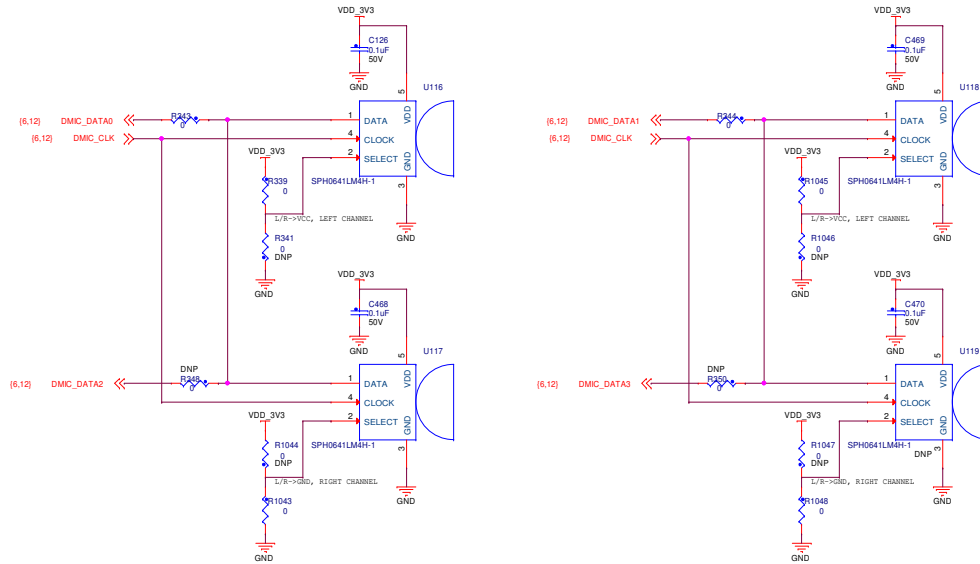
Page Title: **SDRAM_opt/HyperRAM**

Size C	Document Number SCH-50577, PDF: SPF-50577
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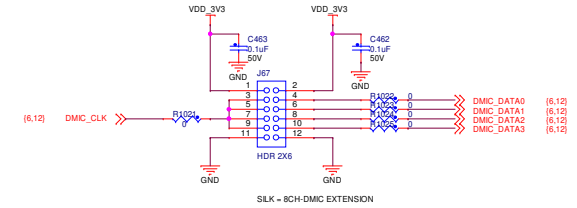
Date:	Friday, February 28, 2025	Sheet	11	of	31
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Board DMIC

Notes: Placing the mic under PCB which is opening to face the user

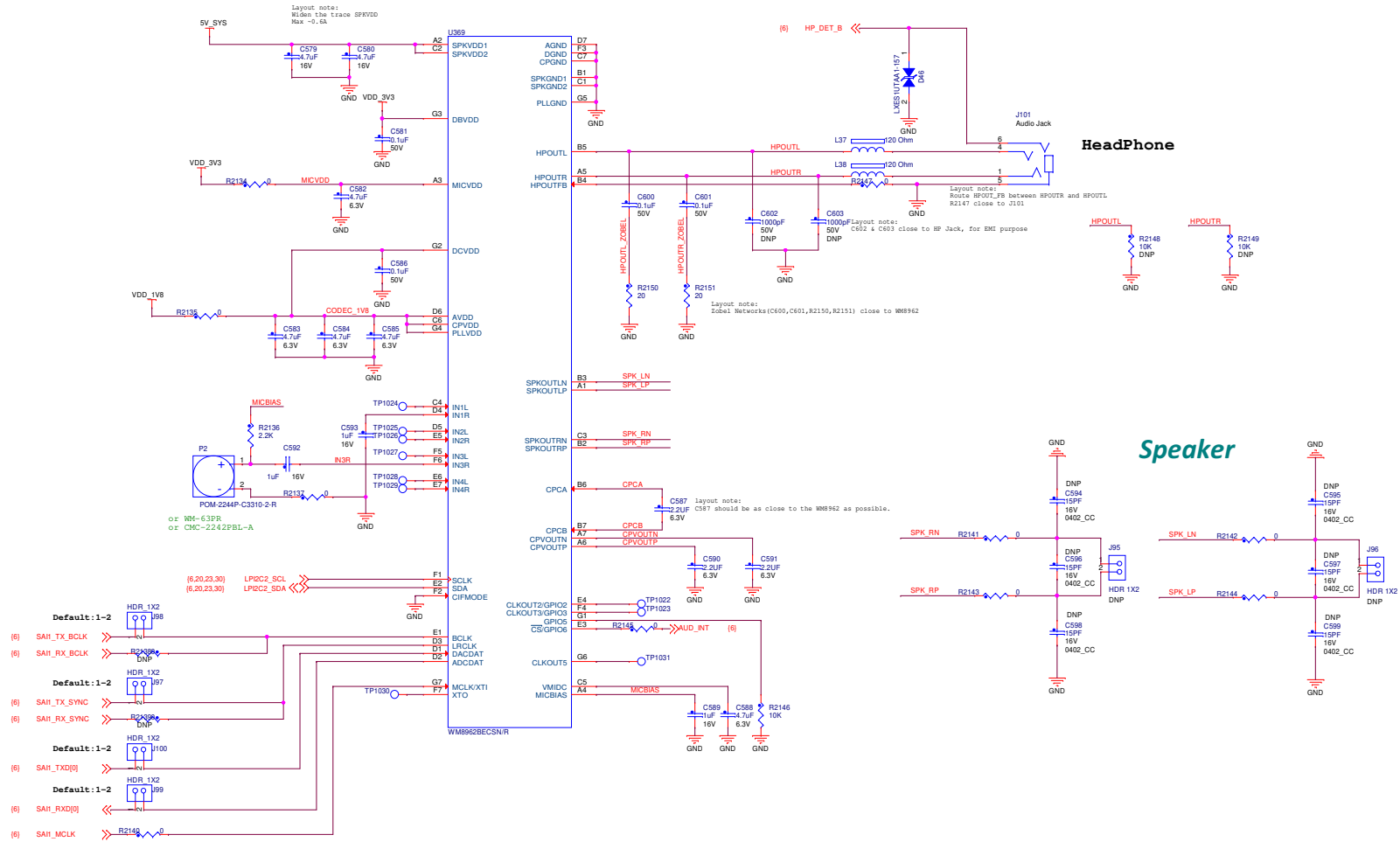


8CH-DMIC Extension

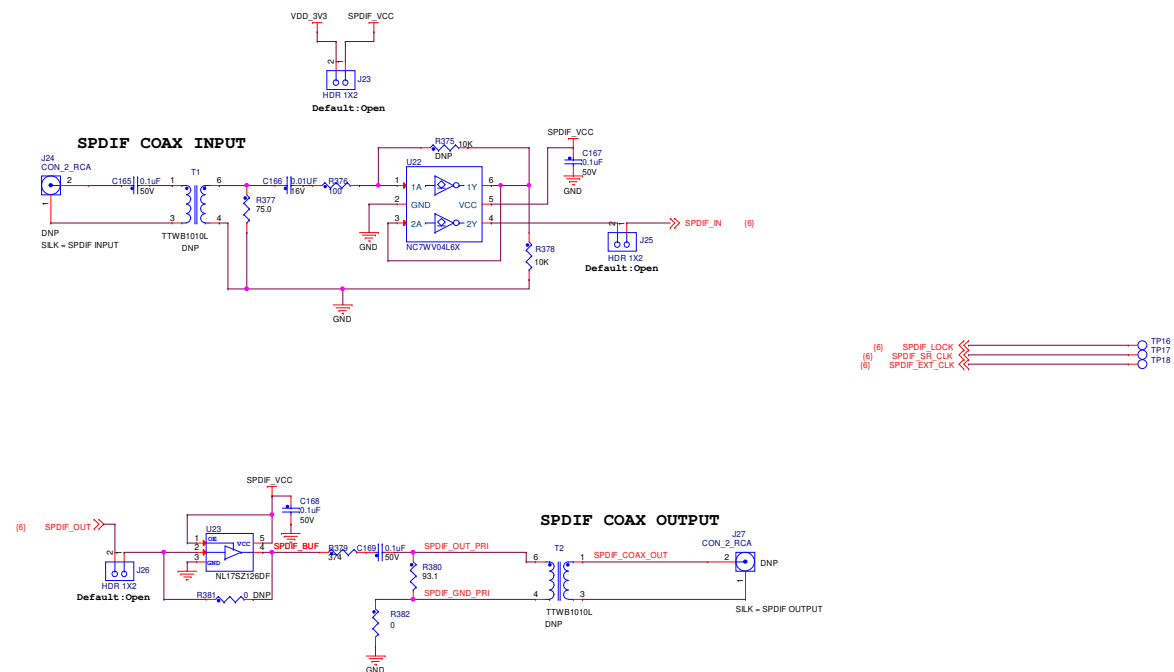


ICAP Classification:	CP:	I/O:	PUBL:
Drawing Title:	MIMXRT1180-EVK		
Page Title:	DMIC		
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Audio Codec



SPDIF Interface



ICAP Classification:	CP:	NO:	PUBL:
Drawing Title:	MIMXRT1180-EVK		
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C			C4
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10/100Mbps Ethernet Circuit

RXD3(RMII REF_CLK Direction)
REF_CLK Input mode:1(Default)
REF_CLK Output mode:0

RXDV(MII/RMII Mode Config)
RMII mode:1 (Default)
MII mode:0

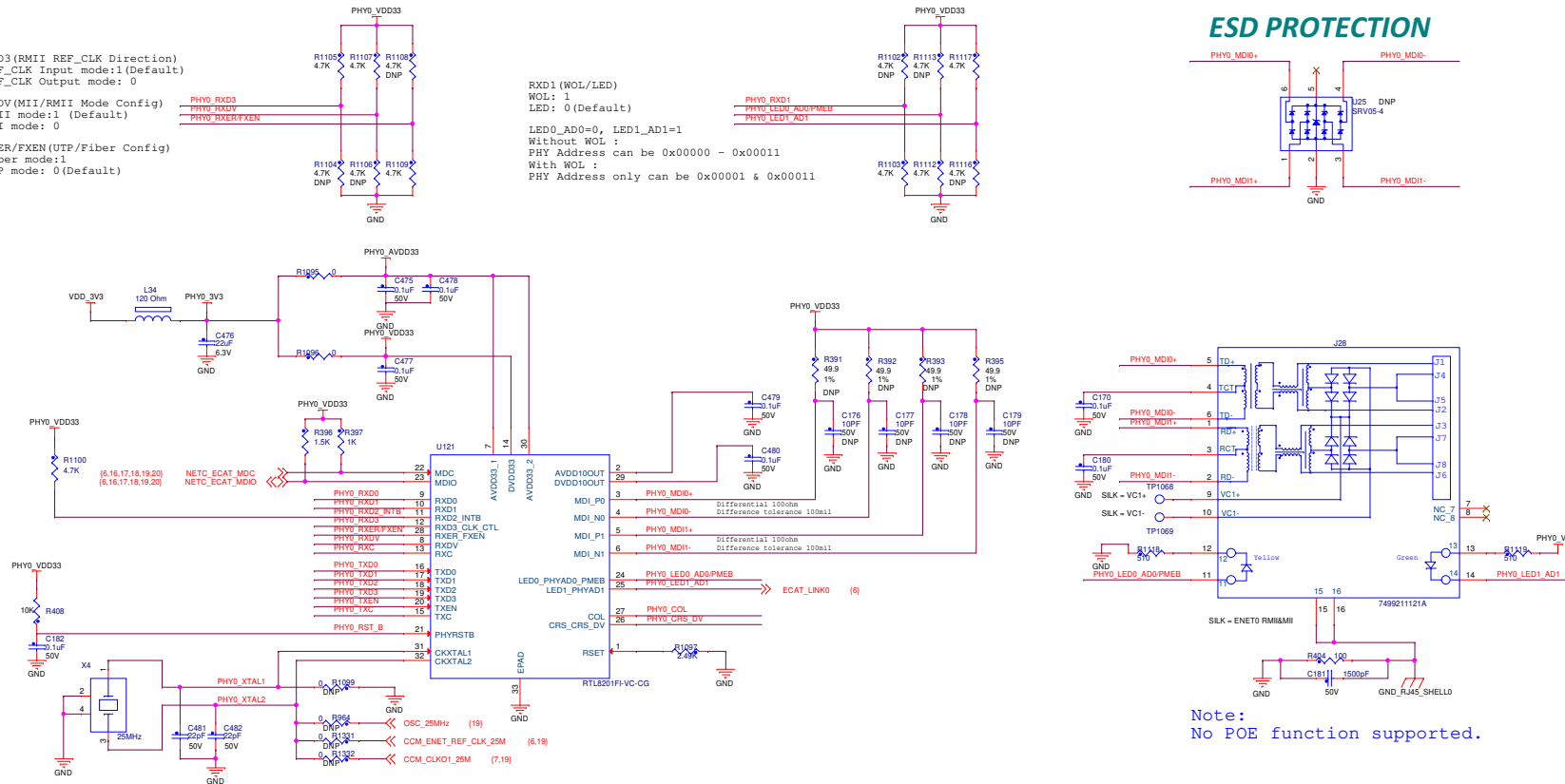
RXER/FXEN(UTP/Fiber Config)
Fiber mode:1
UTP mode:0(Default)

RXD1(WOL/LED)
WOL:1
LED:0(Default)

LED0_AD0=0, LED1_AD1=1

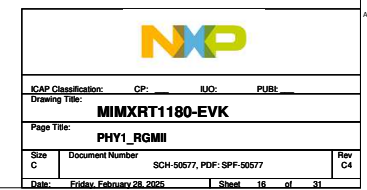
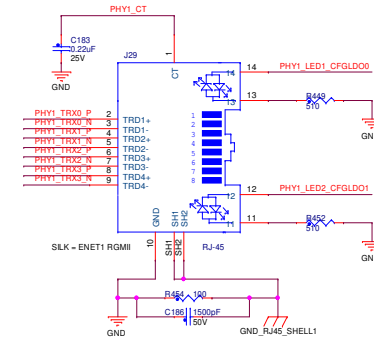
Without WOL :
PHY Address can be 0x00000 - 0x00011

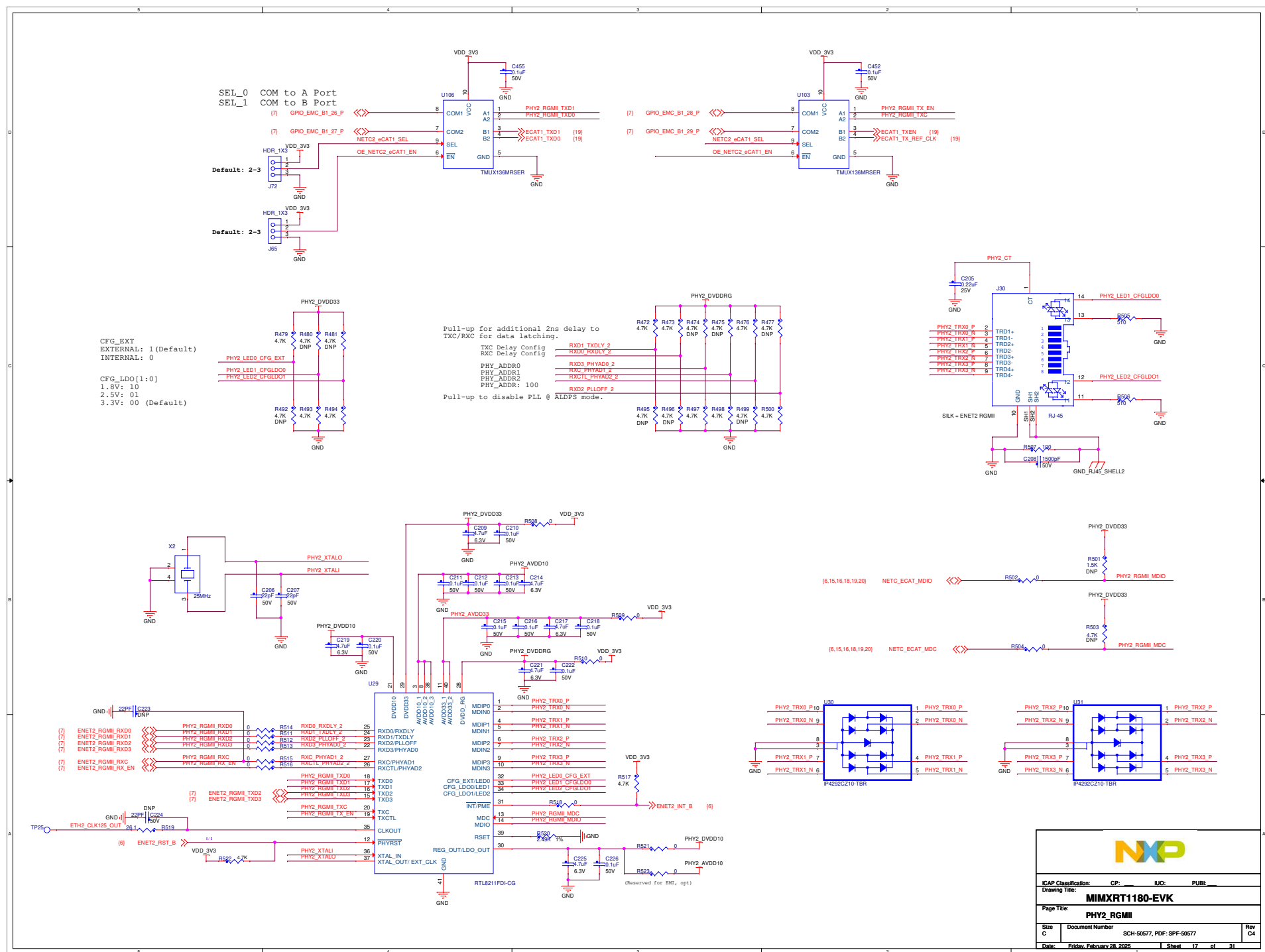
With WOL :
PHY Address only can be 0x00001 & 0x00011



Signal	Direction	Pin	Signal	Direction	Pin
ENET1_RGMII_TXC	TX	R881	ECAT_SYNC0	TX	30
ENET1_RGMII_TX_EN	TX	R882	ECAT_SYNC1	TX	30
ENET1_RGMII_TXD0	TX	R883	ECAT_ACT0	TX	30
ENET1_RGMII_TXD1	TX	R884	ECAT_ACT1	TX	30

The schematic diagram shows the PHY1 LED driver circuit. It is powered by PHY1_DVDD33 and connected to GND. The circuit includes resistors R434 (4.7K), R435 (4.7K DNP), R436 (4.7K), R437 (4.7K DNP), R438 (4.7K), and R439 (4.7K DNP). The output lines are PHY1_LED0_CFG_EXT, PHY1_LED1_CFGLDO0, and PHY1_LED2_CFGLDO1.





ICAP Classification:	GP:	IIQ:	PUR:
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Drawing Title: **MINYPT1100 E/MK**

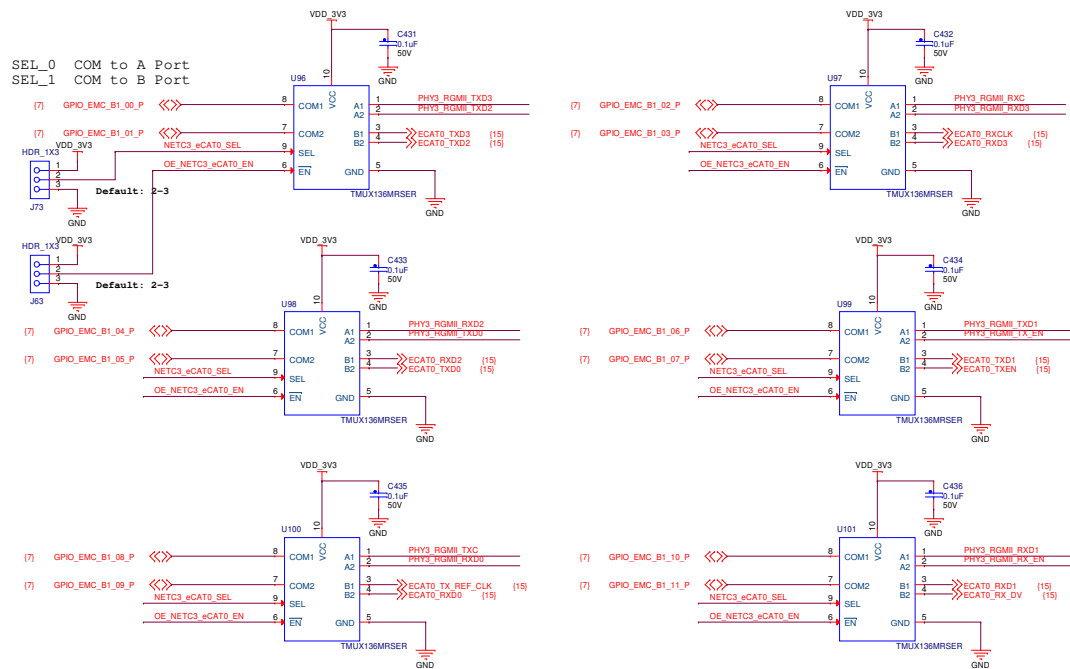
MIMXR11180-EVK

Page Title: PHY2_RGMI

Size	Document Number
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C	SCH-50577, PDF: SPF-50577
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Pull-up for additional 2ns delay to TXC/RXC for data latching.

```
TXC Delay Config
RXC Delay Config
```

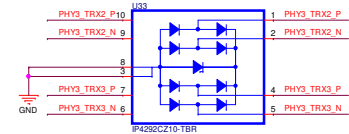
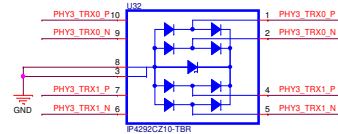
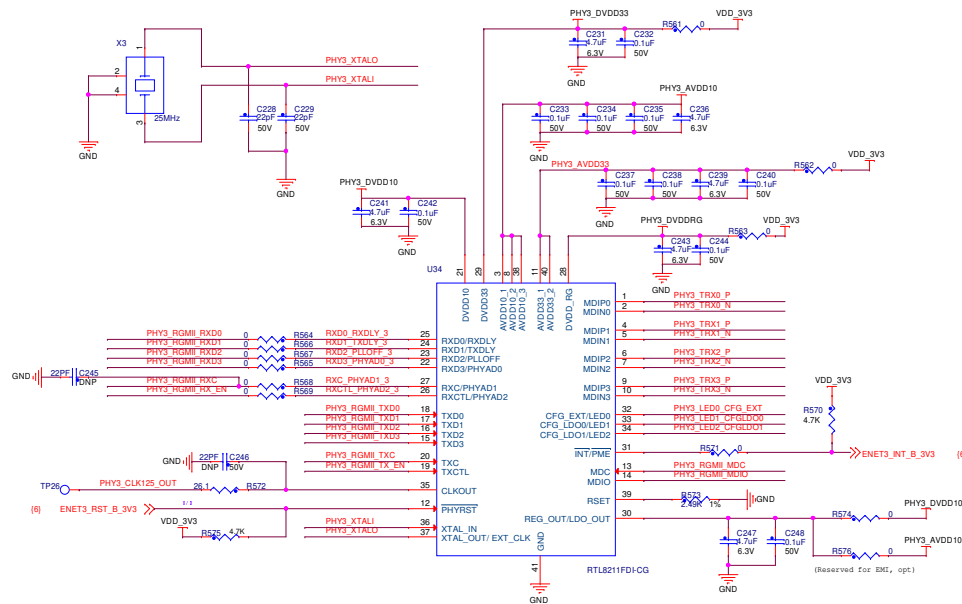
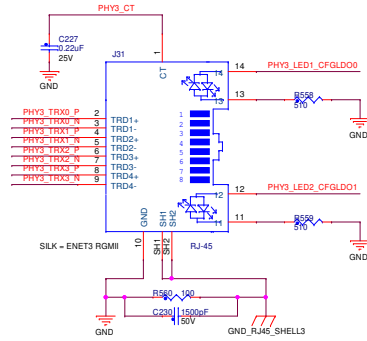
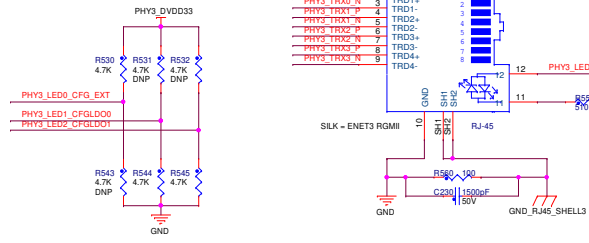
PHY_ADDR0
PHY_ADDR1
PHY_ADDR2

```
PHY_ADDR: 111
```

TABLE 4. CO-ORDINATE TABLE OF THE MODELS

```
CFG_EXT
EXTERNAL: 1 (Default)
INTERNAL: 0
```

```
CFG_LDO[1:0]
1.8V: 10
2.5V: 01
3.3V: 00 (Default)
```



ICAP Classification: CP: IUO: PUBt:

Drawing Title: **MIMXRT1180-EVK**

Page Title: PHY3_RGMII

Size	Document Number
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Date: Friday, February 28, 2025 Sheet 18 of 31

10/100Mbps Ethernet Circuit

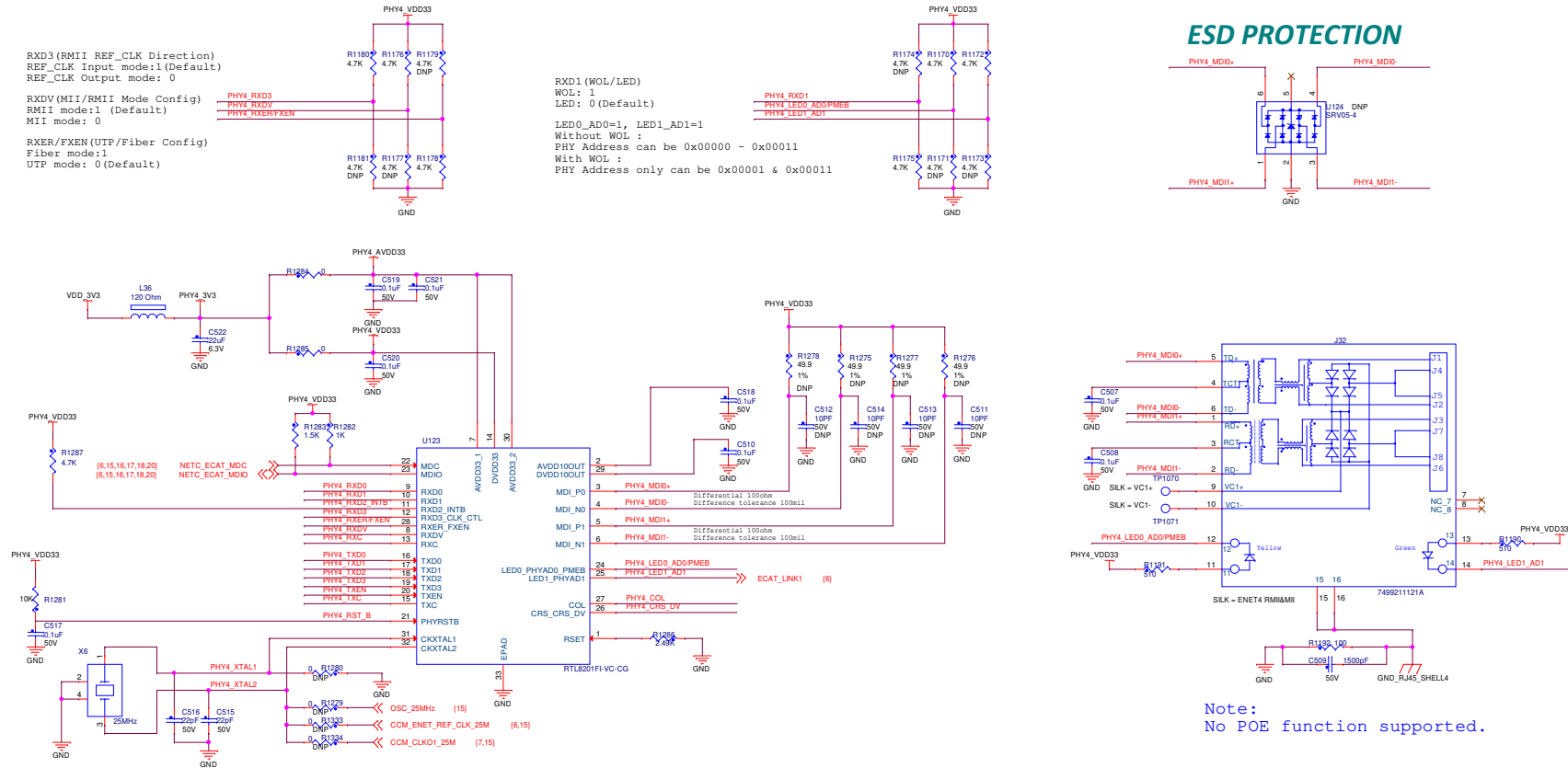
RXD3(RMII REF_CLK Direction)
REF_CLK Input mode:1(Default)
REF_CLK Output mode: 0

RXDV(MII/RMII Mode Config)
RMII mode:1 (Default)
MII mode: 0

RXER/FXEN(UTP/Fiber Config)
Fiber mode:1
UTP mode: 0(Default)

RXD1(WOL/LED)
WOL: 1
LED: 0(Default)

LED0_AD0=1, LED1_AD1=1
Without WOL :
PHY Address can be 0x00000 - 0x00011
With WOL :
PHY Address only can be 0x00001 & 0x00011

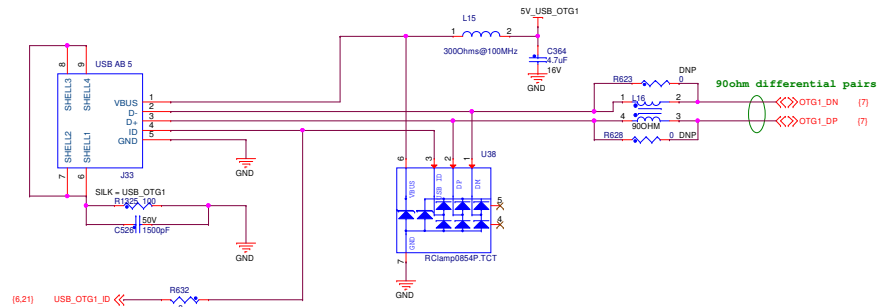




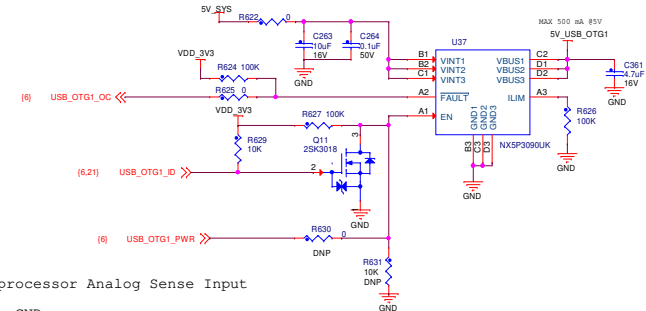
KAD Classification:	CR:	UIC:	DUP:
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Drawing Title: **MIMXBT1100_EWK**

USB OTG1



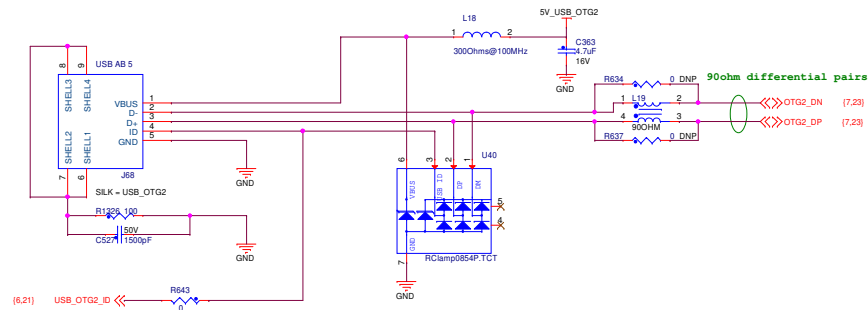
USB1 Power



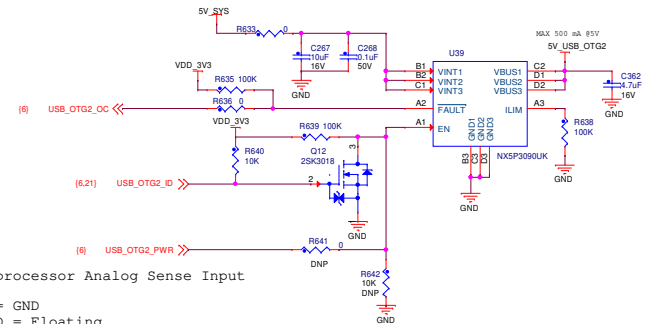
USB ID is a processor Analog Sense Input

Host --> ID = GND
Device --> ID = Floating

USB OTG2



USB2 Power



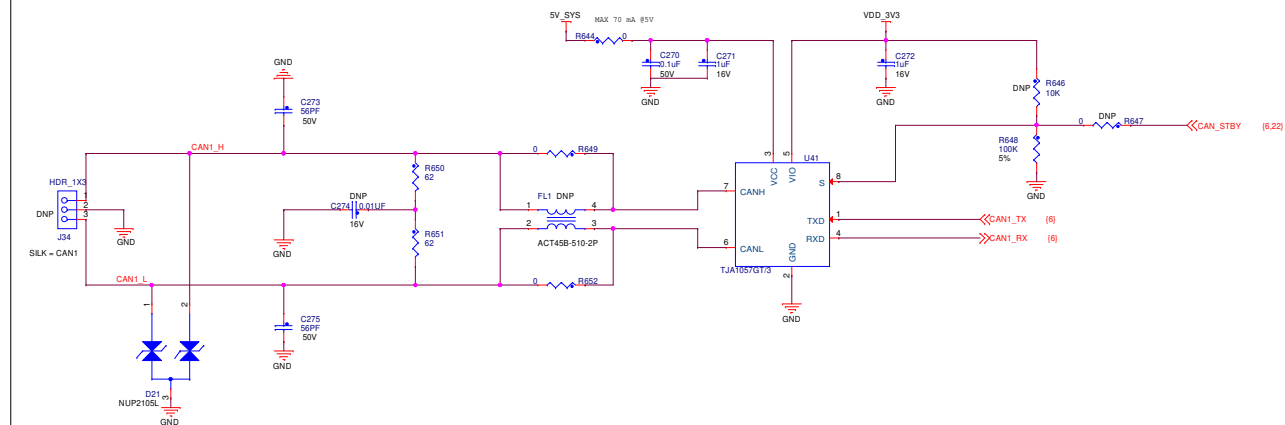
USB ID is a processor Analog Sense Input

Host --> ID = GND
Device --> ID = Floating

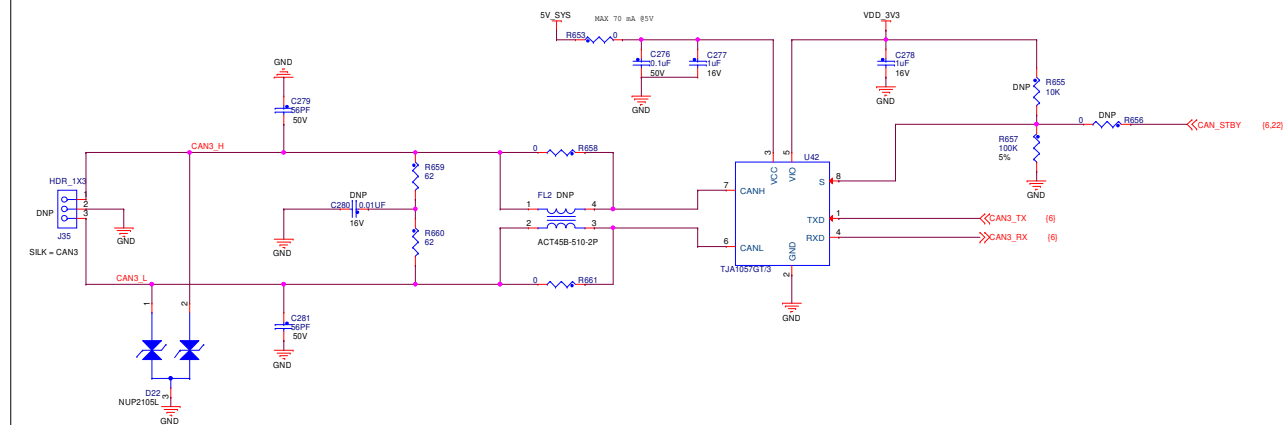


ICAP Classification:		CP:	I/O:	PUBL:
Drawing Title:		MIMXRT1180-EVK		
Page Title:		USB		
Size C	Document Number	SCH-50677, PDF: SPF-50677		Rev C4
Date:	Friday, February 28, 2025	Sheet	21	of 31

CAN1 Bus



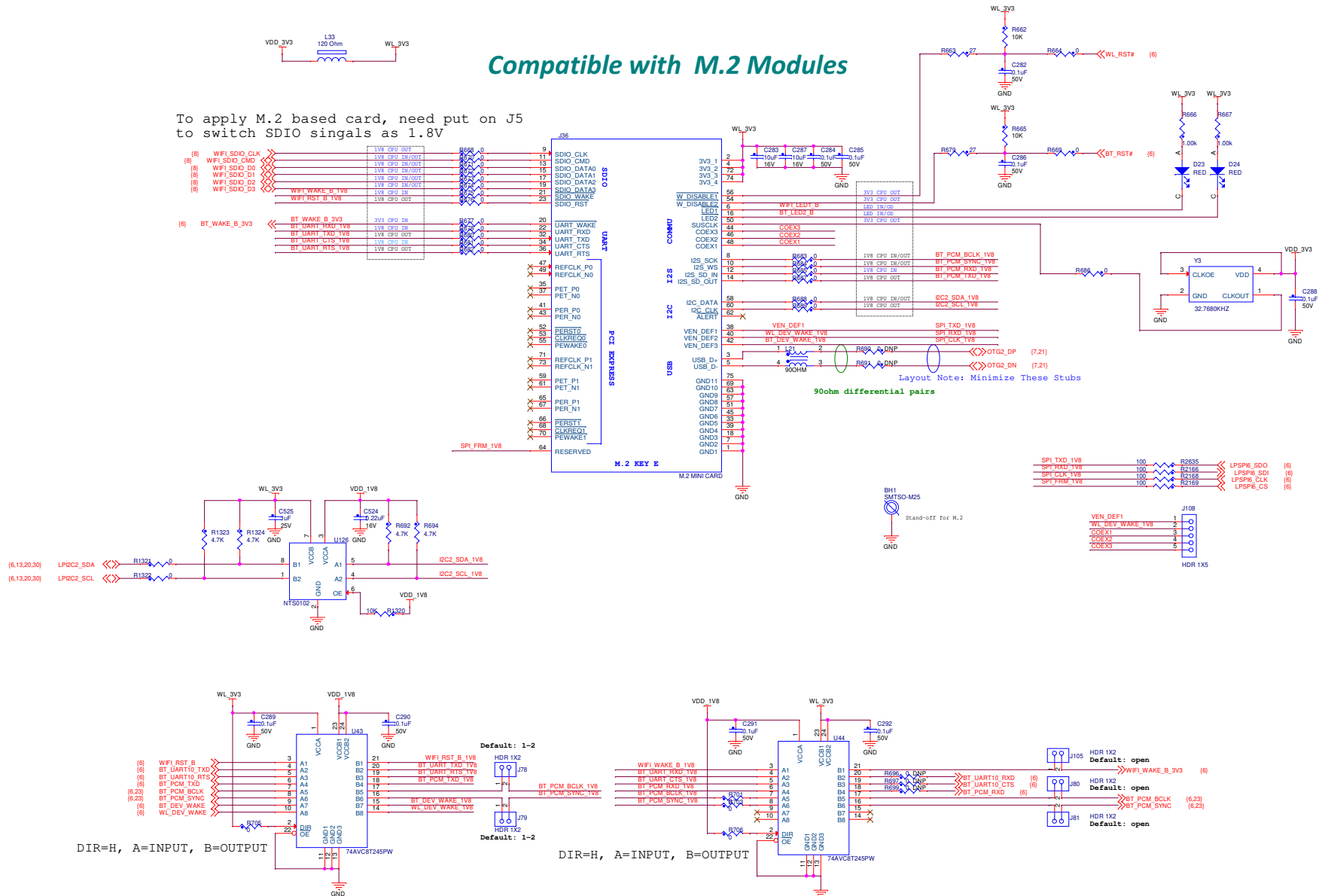
CAN3 Bus



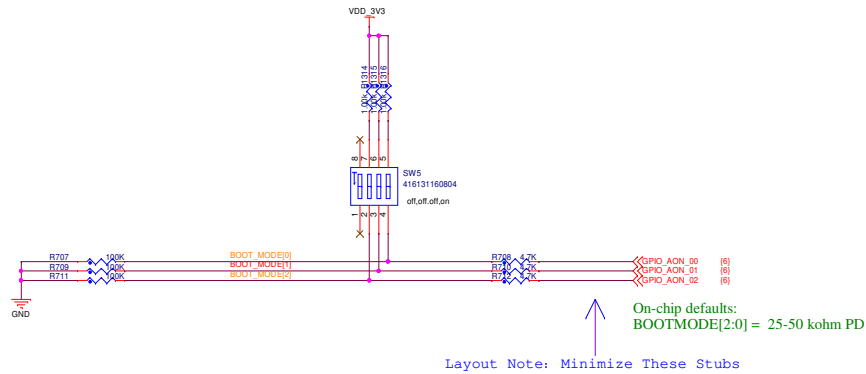
ICAP Classification:	CP:	NO:	PUBL:
Drawing Title:	MIMXRT1180-EVK		
Page Title:	CAN		
Size	Document Number	SCH-50577, PDF: SPF-50577	Rev
C			C4
Date:	Friday, February 28, 2025	Sheet	22 of 31

Compatible with M.2 Modules

To apply M.2 based card, need put on J5 to switch SDIO signals as 1.8V



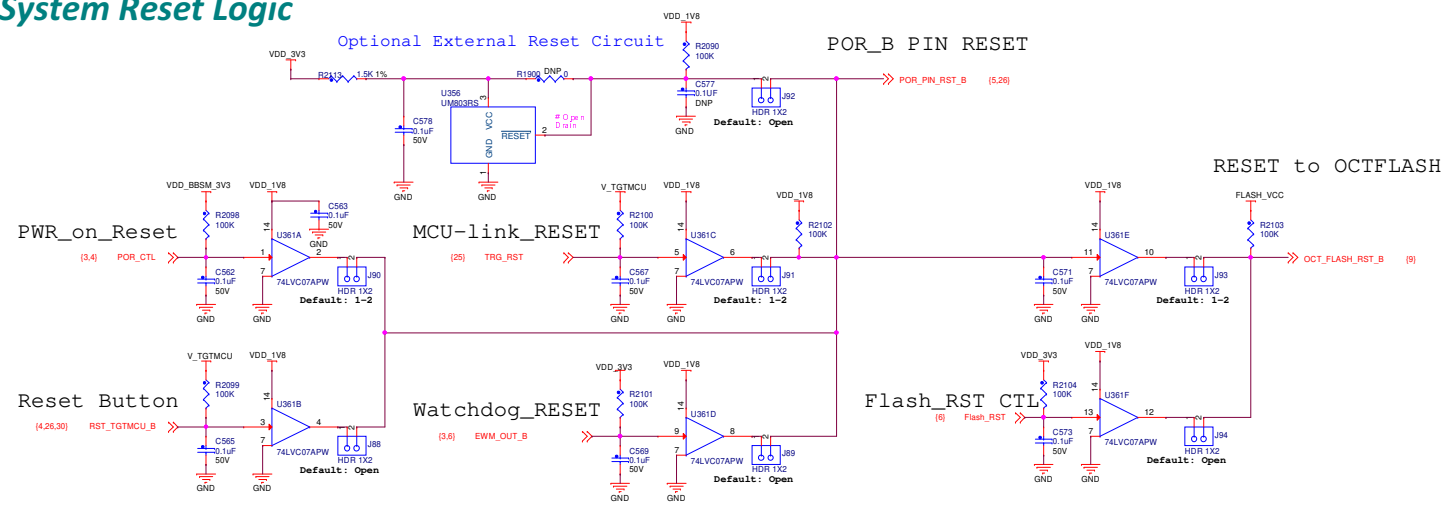
External Boot Switch



Boot Mode pin settings

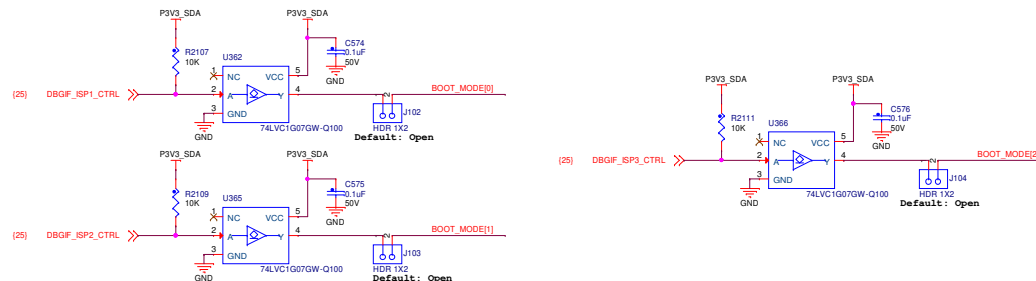
BOOT_MODE[2:0]	Boot Type
000(SW5-x000)	Boot from Internal Fuses
001(SW5-x001)	Serial Downloader (USB1 or LPUART1)
010(SW5-x010)	USDHC2 8-bit 1.8V eMMC 5.1
011(SW5-x011)	uSDHC1 4-bit SD 3.0
100(SW5-x100)	FlexSPI Quad SPI Serial NOR (or Octal SPI NOR in Quad SPI NOR mode)
101(SW5-x101)	FlexSPI Quad SPI Serial NAND 2k page (or Octal SPI NAND in Quad SPI NOR mode)
110(SW5-x110)	FlexSPI Quad SPI Serial NAND 4k page (or Octal SPI NAND in Quad SPI NOR mode)
111(SW5-x111)	Test Mode

System Reset Logic

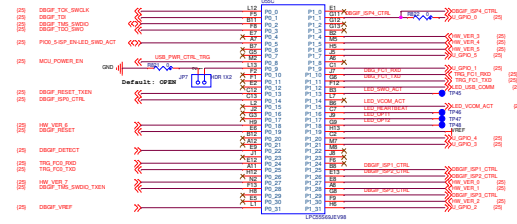
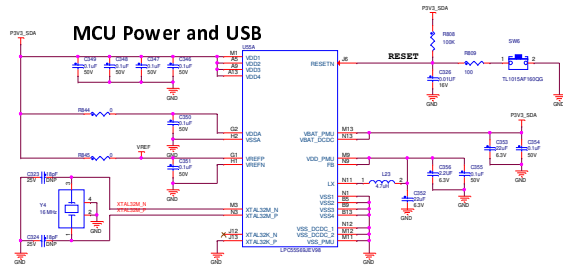


ISP Control for Factory Automation

Note: If ISP Automatic Control is used, You need to configure SW5 to be x111 first



MCU Power and USB



Both JTAG and SWD are supported for debug

(6) JTAG_nTRST
(16) JTAG_TDI
(6,25) JTAG_TMS
(6,25) JTAG_TCK
(6,25) JTAG_TDO

(5,24) POR_PN_RST_B

VDD_3V3

D25 RB521S30

R713 10K DNP

R714 10K DNP

R715 10K DNP

R716 10K DNP

R717 10K DNP

R718 100

JTAG_VREF

JTAG_TSTRST

JTAG_TDI

JTAG_TMS

JTAG_TCK

JTAG_TDO

JTAG_TDO0

JTAG_DE

JTAG_CLOCK

1 37

2 JTAG_FMS

3

4

5

6

7

8

9

10

11

12

13

14

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20

BH25420B301
SILK = JTAG(SWD)

R719 10K DNP

R720 10K DNP

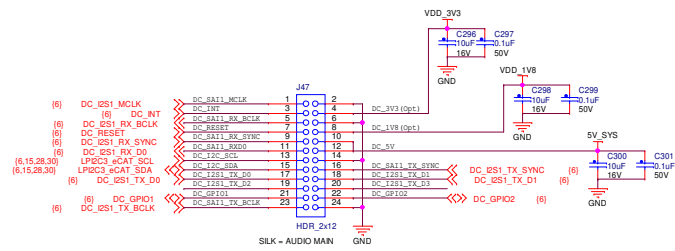
R721 10K

GND

FLEXIO HEADER

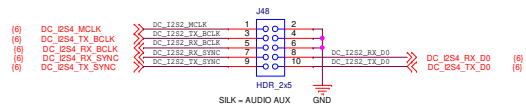
Arduino & MC Interface

AUDIO MAIN CONN

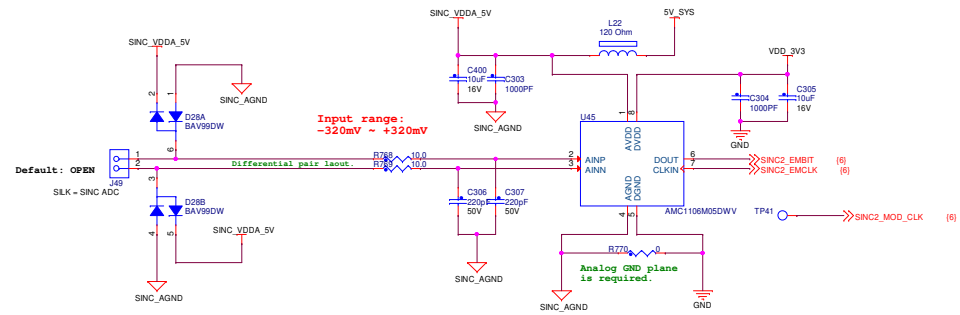


AUDIO AUX CONN

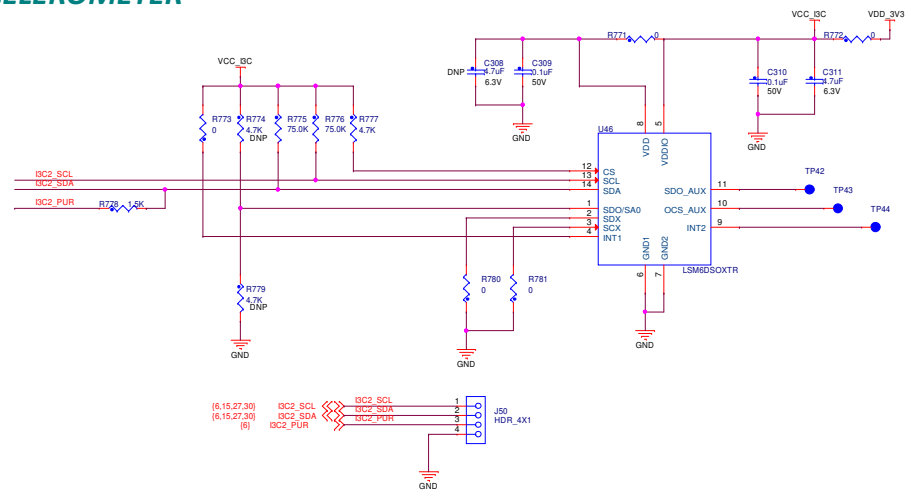
If Audio aux conn (J48) is used, please mount resistors below,
R125,R127,R129,R131,R132,R133,R134



SINC ADC



I3C GYRO&ACCELEROMETER



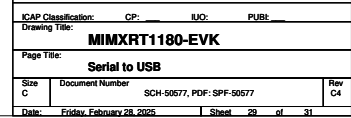
ICAP Classification:	CP: _____	IUO: _____	PUBt: _____
Drawing Title: _____			

Drawing Title: **MIMXRT1180-EVK**

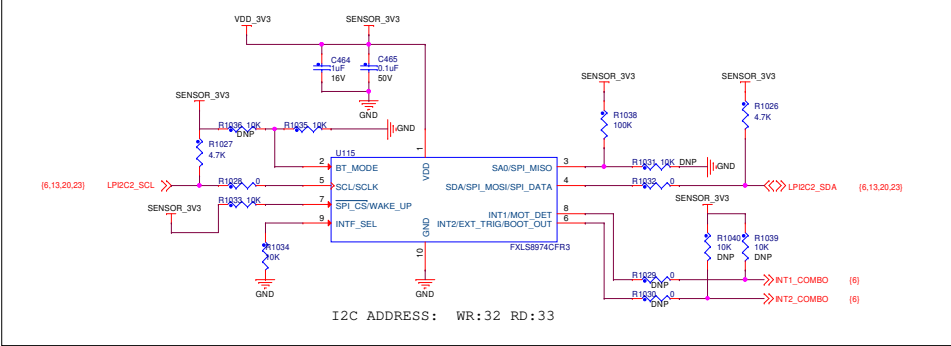
SINC&I3C	
Size C	Document Number SCH-50577, PDF: SPF-50577

Date: Friday, February 28, 2025	Sheet 28 of 31
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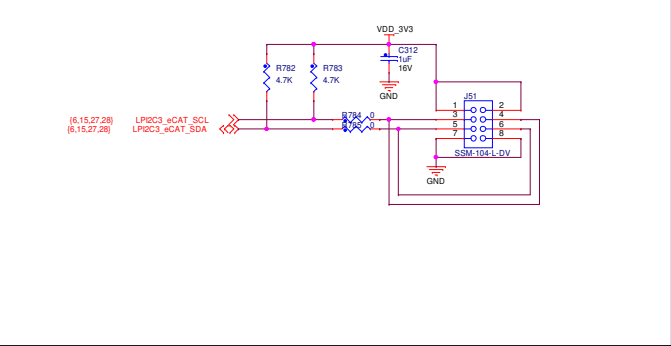
Rev
C4

[illegible]

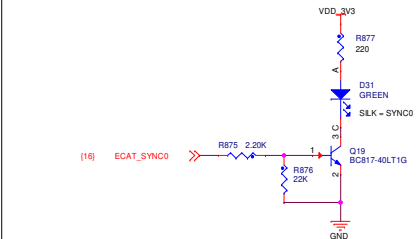
Accelerometer



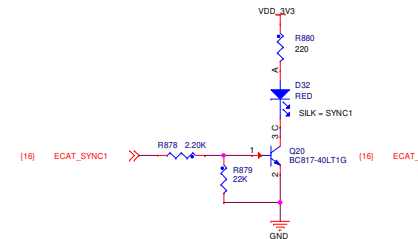
I2C CONN Extension



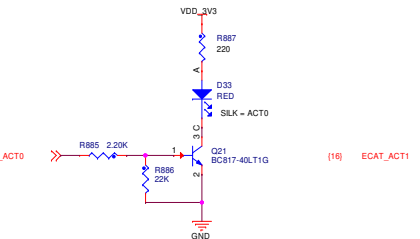
USER LED3



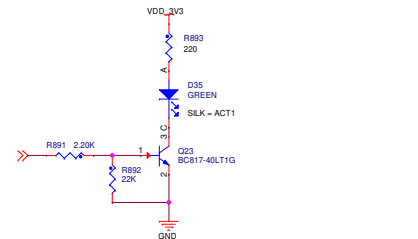
USER LED4



USER LED5

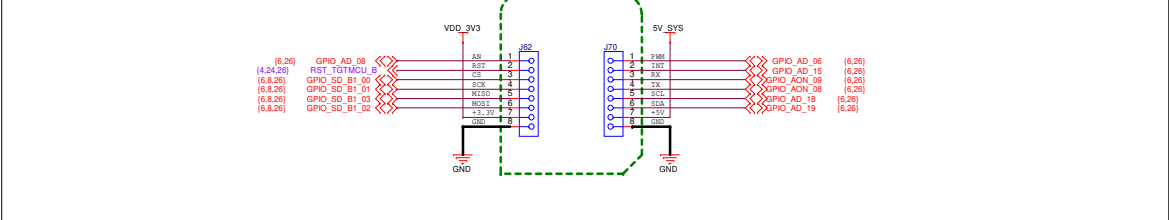


USER LED6



Mikroe Click Connectors

(Signals are shared with Arduino.)



	Resistors and Switch Option List				
USE CASE1	PHY0 RMII	PHY1 RGMII	PHY2 RGMII	PHY3 RGMII	PHY4 RMII
	Default setting	Default setting	Default setting	Default setting	Default setting
USE CASE2	PHY0 MII	PHY1 RGMII	PHY2 RGMII	PHY3 RGMII	PHY4 MII
	DNP R959, R1229, R1230. R1122, R1235, R1233, R1234, R1240, R1239, R1237, R1238, R405, R1236 Populate R960, R1231, R1232, R1259, R1260, R1261, R1262, R1263, R1264, R1265, R1266, R1267, R1268, R1269, R1270, R1271, R1272, R1273, R1274 U96, U97, U98, U99, U100 and U101 Switch to signal path B	Default setting	Default setting	Default setting	DNP R1289, R1292, R1290, R1291, R1293, R1294, R1295, R1296, R1288, R1313 Populate R1297 R1298, R1299, R1300, R1302 R1301, R1303, R1304, R1305, R1307, R1306, R1308, R1310, R1309, R1311, R1312, R2116, R2117, R2120,R2121, R2124, R2125, R2128, R2129, R2132, R2133, R1169 U103, U106 Switch to signal path B