**8CH-DMIC Board**

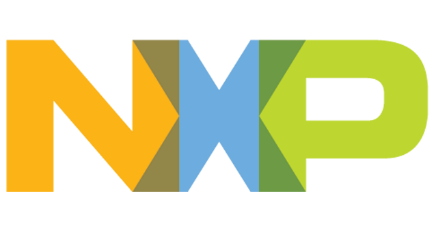
**Microcontrollers**

**Systems & Applications Engineering /**

**LPC Ecosystems**

**Revision B**

**July 15, 2021**

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**R****evision History**

|  |  |  |  |
| --- | --- | --- | --- |
| **Rev. No.** | **Date (Submitted by)** | **Sections Affected** | **Substantial Changes** |
| 0.1 | June-3-2020 (Amish, Chun, Al) |  | Initial version |
| 0.2 | June-8-2020 (Amish, Chun, Al, Brendon) |  | DMIC header connection updates (put GPIO signal names). Silkscreen label updates for MICs and LEDs |
| 0.3 | September-8-2020, Al |  | Changed function to support 8 DMIC’s. Defined multiple physical configurations. Defined clk/data connections for each configuration. |
| 0.4 | October 7, 2020, Al |  | Added notes on component placement and added 3-mic linear config |
| 0.5 | October 27, 2020, Al |  | Added LED configuration to diagram |
| 0.6 | Nov 17 2020, Amish |  | Made some minor updates below. |
| 0.7 | Jan 22 2021, Amish |  | Updated the name of the board |
| A | Feb 26, 2021 Al |  | Released to Rev A. and added operational voltage range. |
| B | July 15, 2021, Al |  | Change jumper requirements to allow more clk routing flexibility for CLK01, CLK23, CLK45, and CLK67 |

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# Introduction

## Scope

This document outlines requirements for 8 channel DMIC plug-in board, with multiple physical configurations, which can be connected to the MCU EVK boards supporting the DMIC connector.

## Overview of the document

This document is formed as a combined requirements and high-level design document. The high-level requirements are listed at a system level and for each module/part of the system respectively.

The document is outlined according to the grouping of the requirements. Each part of the document then contains an elaboration of the matching requirement(s) and a high-level design of the module/part wherever applicable.

The main scope of the document is to state the hardware design requirements. In addition to this there are a number of requirements pertaining documentation and other platform deliverables.

The document is written using the IETF RFC 2119 [RFC2119] recommendations for interpreting the key words "SHALL", "SHALL NOT", "REQUIRED", "SHOULD", "SHOULD NOT", "RECOMMENDED", "MAY", and "OPTIONAL".

# Acronyms and Abbreviations

| **Acronym or Term** | **Definition** |
| --- | --- |
| ADC  BLE  CE  CPU | Analog to Digital Converter  Bluetooth Low Energy  Consumer Electronics  Central Processing Unit |
| FCC  NCL  FRDM | Federal Communications Commission  NXP Controlled Library  Freedom System |
| GPIO | General Purpose Input/Output |
| IEEE | Institute of Electrical and Electronics Engineers |
| LED | Light Emitting Diode (plural) |
| MCU  NVM | Microcontroller Unit  Non-Volatile Memory |
| OOBE  PCB | Out of Box Experience  Printed Circuit Board |
| PWM  RF | Pulse Width Modulation  Radio Frequency |
| RoHS | Restriction of the Use of Certain Hazardous Substances |
| SMAC | Simple Medium Access Controller |
| SMA | Sub-Miniature A Connector |
| SPI | Serial Peripheral Interface |
| TWR | Tower System |
| TWRPI | Tower Plug In |
| UART | Universal Asynchronous Receiver Transmitter |
| USB | Universal Serial Bus |
| WEEE | Waste Electrical and Electronic Equipment |
|  |  |
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|  |  |
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|  |  |

# Hardware Requirements

## General Hardware Requirements

**REQ-1:** Development boards design documentation shall be available. This includes Schematics, Source files (Allegro as preference), 274-x Gerbers, BOM (as an excel spreadsheet), and PDF file for each of them.

**REQ-2:** All development boards shall comply with the **RoHS directive**.

**REQ-3:** All development boards shall comply with the **WEEE directive**.

**REQ-4:** All development boards shall comply with the **CE standards**.

**REQ-5:** All Printed Circuit Boards will be of a nominal standard thickness of 0.064 inches.

**REQ-6:** For 4-layer design, the PCB shall be FR4 board. Following figure shows the required stack-up for a 4-layer board. Layer 1 and 4 should be ground planes. Layer 2 and 3 are signal/power planes.

**REQ-7:** All hardware related documentation shall be open source.

REQ-8: EC, FCC and ARIB certification shall be available to release production.

## DMIC Plug-in Board

The DMIC plug-in board will allow a single, double, triple, quad, hexagonal, hexagonal (with center mic), and octal DMIC solution. As an example, this can be used in conjunction with the MIMXRT6XX/B0-EVK board for B0 silicon revision.

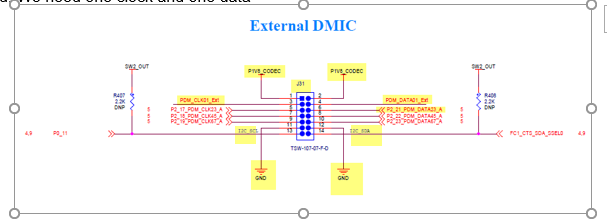
### DMIC connection to the EVK board

**REQ-9**:The DMIC plug-in board should be able to connect to a 5x2 0.1” header (as an example, please refer to J31 connector on the MIMXRT6XX/B0-EVK) to support 8 DMIC solution.

Please see picture below.

Highlighted signals below (power, GND, PDM signals, I2C signals) are the signals which will be interfaced to.

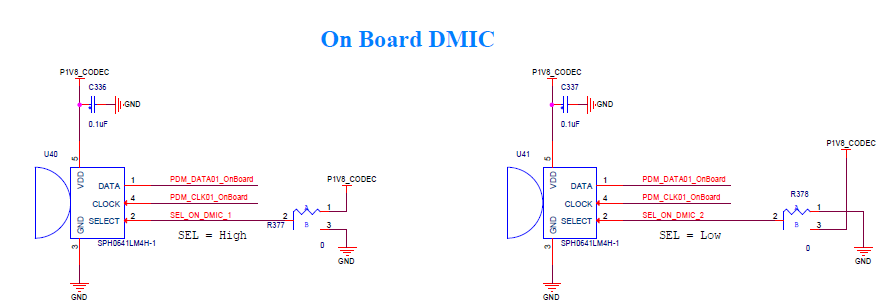
NOTE: While the MIMXRT6XX/B0-EVK shows power of 1.8V, the DMIC plug-in board shall be capable of operating from a voltage range of 1.8V to 3.6V.



On the DMIC plug-in board, instead of I2C signal names for J31.13 and J31.15, please use the GPIO names (PIO0\_11 which gets connected to I2C\_SCL signal on the EVK board and PIO0\_10 which gets connected to I2C\_SDA signal on the EVK board).

### Components

**REQ-10:** Use the same components we used for the on-board DMIC board (example below from RT685/B0 Rev E board) on the MIMXRT6XX/B0-EVK board with exception to use SPH0644LM4H-1 instead. Please see picture below.



**REQ-11**: Please ensure to comply with SPH0644LM4H-1 specifications on board cleaning after re-flow. This needs to be brought to attention to manufacturer/assembly.

**REQ-12:** We need a total of 11 mics on plug-in board to support all physical configurations. At most, 8 will be in use simultaneously.

### Signal connections

**REQ-13:**

* Clk01 shall go the DMIC’s that can use Dat01 signals
* Clk23 shall have a jumper selection to source DMIC’s using Dat23 from either Clk23 from input connector or from Clk01 from the input connector.
* Clk45 shall have a jumper selection to source DMIC’s using Dat45 from either Clk45 from input connector or from Clk01 from the input connector.
* Clk67 shall have a jumper selection to source DMIC’s using Dat67 from either Clk67 from input connector or from Clk45 from the Clk45 jumper selection. Depending on Clk45 jumper, Clk67 can come from Clk67, Clk45, or Clk01.

**REQ-14:** The following configurations and signal connections shall be supported. D01 indicates Clk01 and Data01 signals, (See REQ-13 for Clkxx adjustments). Polarity will be settable per MIC.

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Conf | MIC0 | MIC1 | MIC2 | MIC3 | MIC4 | MIC5 | MIC6 | MIC7 | MIC8 | MIC9 | MIC10 |
| 2MIC | D01 |  |  | D01 |  |  |  |  |  |  |  |
| 3MICA | D01 |  |  | D01 |  |  |  |  |  | D23 |  |
| 3MICB | D01 |  | D01 |  | D23 |  |  |  |  |  |  |
| 3MICC | D01 |  |  | D01 |  |  | D23 |  |  |  |  |
| 4MICA | D01 |  | D01 |  | D23 |  | D23 |  |  |  |  |
| 4MICB |  | D01 | D01 |  |  |  |  | D23 | D23 |  |  |
| 5MIC |  | D01 | D01 |  |  |  |  | D23 | D23 |  | D45 |
| 6MIC | D01 | D01 | D23 | D23 | D45 | D45 |  |  |  |  |  |
| 7MIC | D01 | D01 | D23 | D23 | D45 | D45 | D67 |  |  |  |  |
| 8MIC | D01 | D01 | D23 | D23 | D45 | D45 | D67 |  |  |  | D67 |

### Layout

**REQ-15:** The layout needs to be a circular layout. Please see picture below for positioning and numbering. Picture is top view. Microphones are installed on the bottom of board.

**REQ-16:** Microphone spacing is per diagram.

**REQ-17:** The DMIC plug-in board design plugs-into the EVK board, the mics needs to be placed on bottom of board which means we have a through-hole on top where voice comes from the top.

**REQ-18:** To avoid the issue of component height interfering with the sound propagation, components shall be placed on bottom of board so the microphone sound holes on top will not be obstructed.

**REQ-19:** Usesame mic ordering, placement, and labeling as shown in the picture below.

A picture containing diagram

Description automatically generated

### LEDs

**REQ-20:** There shall be 6 LEDs on **top** of the plug-in adapter board. Placement is as per the above diagram. The LEDs should driven by an I2C to GPIO converter IC, controlled by I2C signals on the J31 connector and will be controlled by the RT685 device**.** These LEDs should be blue with appropriate resistors used to provided similar brightness from each, although multi-color is also acceptable. A power-on LED will be placed on top of the board next to the interface connector.

### Printed Circuit Board (PCB)

**REQ-21**: The board shall be a 4-layer PCB. If the board designer feels that additional layers will make for a better board design, then more layers may be considered. However, increasing from 4-layer plan will require approval.

### Mechanical Enclosure

**REQ-22:** Enclosure is not required.

### Board Markings

**REQ-23:** Back side of the PCB should include NXP logo in the primary silkscreen, QR code and certification logos in secondary silkscreen and a sticker with schematic / design version.

**REQ-24:** Front side of the PCB should include NXP logo and board part-number graved in copper and component naming in silkscreen.

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### Silkscreen

**REQ-25**: All components shall be labelled with their reference designator on the silkscreen. The silkscreen shall not include any internal project code names and shall include a product code of the form 8CH-DMIC

Please label the MICs and LEDs on the silkscreen with big font.

# Software Requirements

## Compliance Test Software Requirements

**REQ-26:** Compliance software shall be delivered from NXP for RF compliance testing.

## Production Test Software Requirements

**REQ-27:** Test software shall be reviewed and updated accordingly to reflect the new features being added. Need to be able to test each of the 11 DMIC’s with software.

# Platform Approvals

|  |  |
| --- | --- |
| **Title** | **Manager** |
| Software Lead | Jason Martin |
| IC Applications Leads | Amish Desai / Chun Chu |
| IC BU | Brendon Slade |
| IC Architect | Al Morrow |
| Marketing | Bart V |

# Supplemental notes

1. None