S32K118EVB-Q064

CUSTOMER EVB

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Revisions

Rev	Description	Designer	Date	Approved
X1				TBD
A	Prototype	J.Sanchez		
B	Final Release	J.Sanchez		

CAUTION:

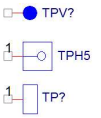
This schematic is provided for reference purposes only. As such, NXP does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the NXP S32K family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

3 Different test points used in design:

TPVx - Through Hole Pad small

TPHx - Through Hile Pad Large (for standard 0.1" header). Also used on IO Matrix (IOMx)

TPX - Surface Mount Wire Loop



Notes:

- All components and board processes are to be ROHS compliant
- All connectors and headers are denoted Jx/Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
  2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughtout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

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ICAP Classification: CP: ___ IUO: ___ PUBI: X__

Designer: Osvaldo Romero	Drawing Title: XS32K118EVB-Q064	
Drawn by: Jesus Sanchez	Page Title: TITLE PAGE	
Approved: APPROVER	Size B	Document Number SCH-29945 PDF: SPF-29945 / Rev B
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1. Unless Otherwise Specified:
   All resistors are in ohms, 1% and 5 %
   All capacitors are in uF, 10% , 20 % and 5%
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

ICAP Classification: CP: ___ IUO: ____ PUBI: _X__

Drawing Title:
XS32K118EVB-Q064

Page Title:
Notes and Block Diagram

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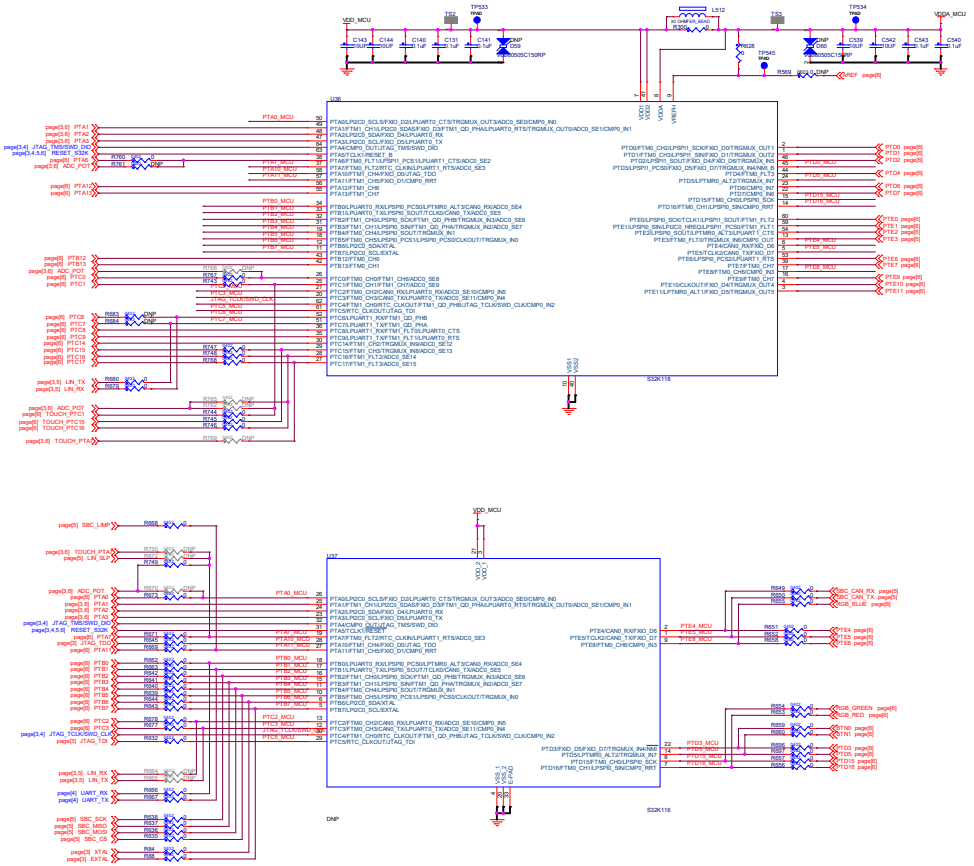

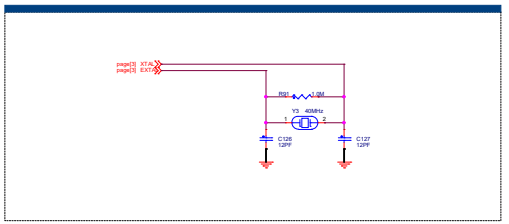

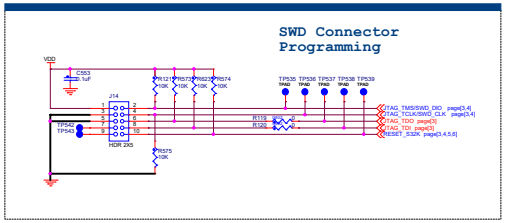

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Drawing Title:	XS32K118EVB-Q064
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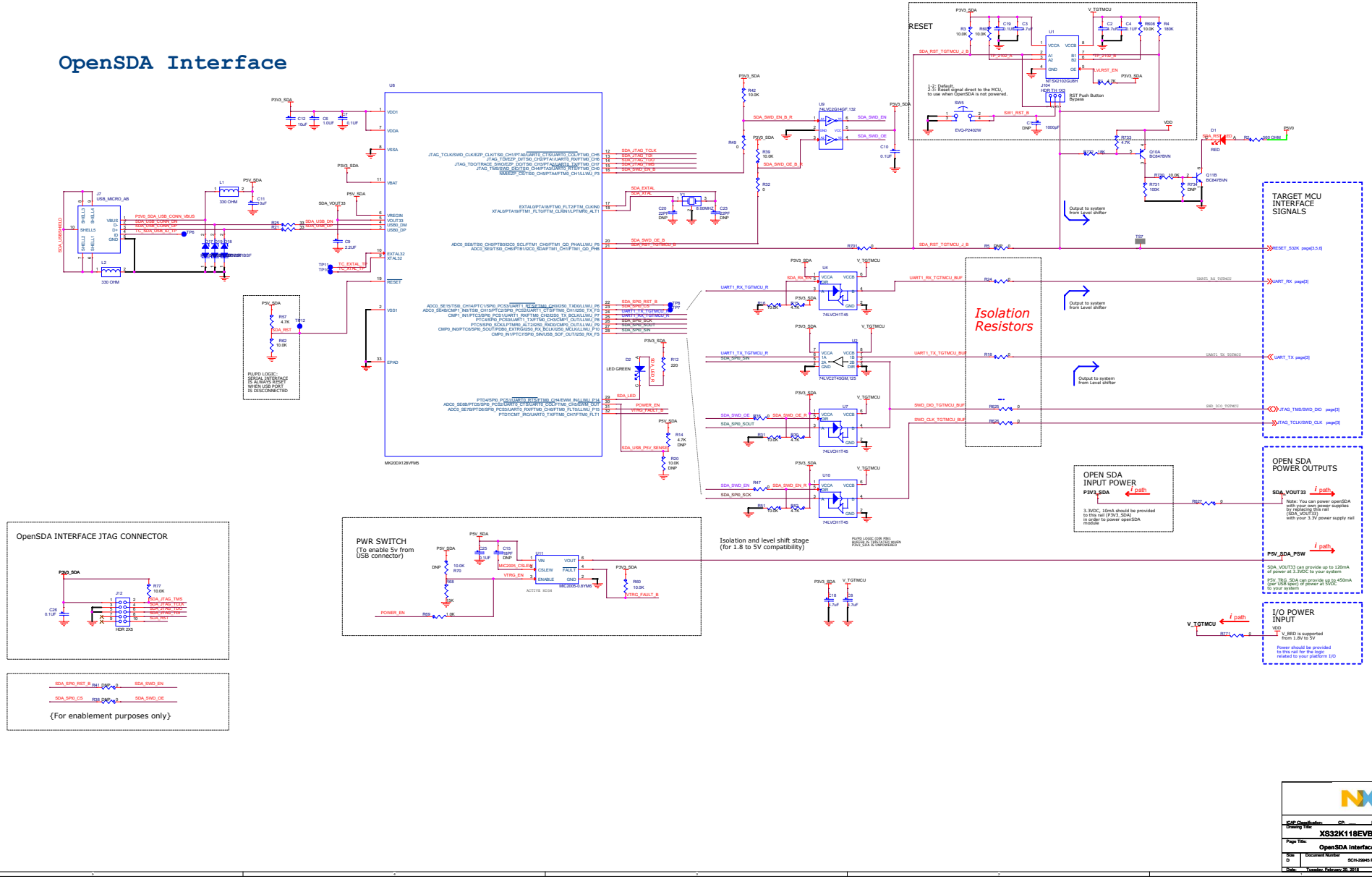
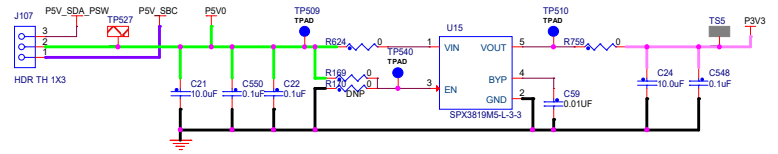
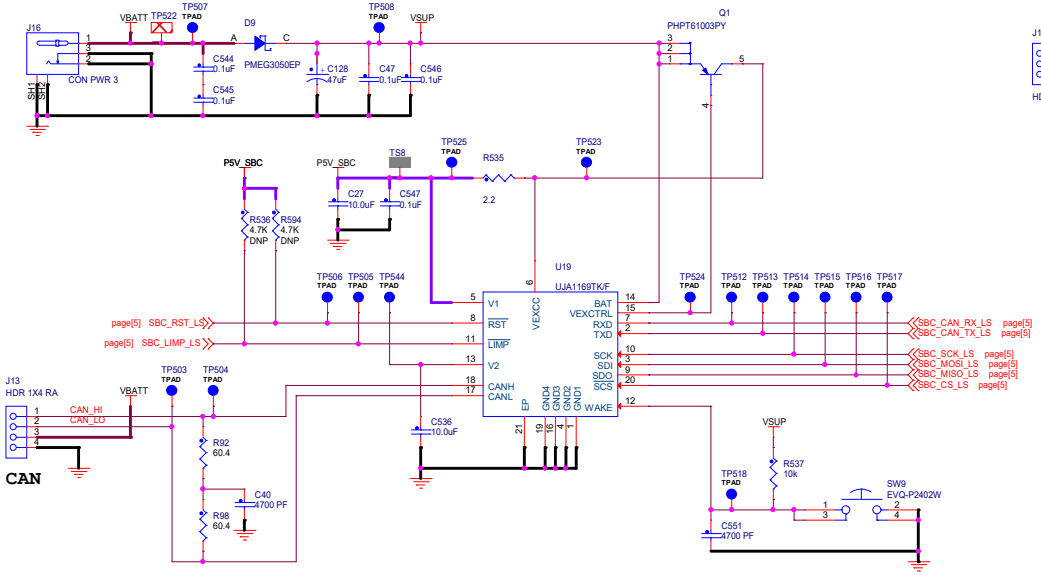
OpenSDA Interface

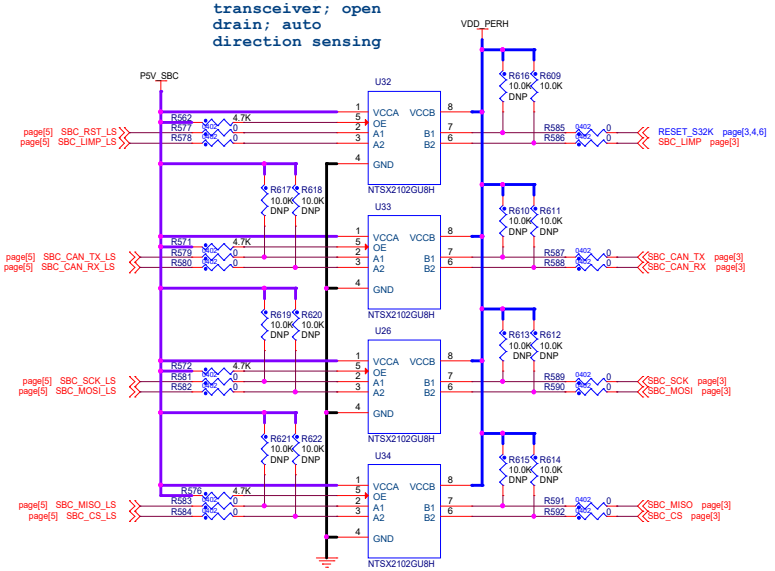


3.3V LDO Power Supply

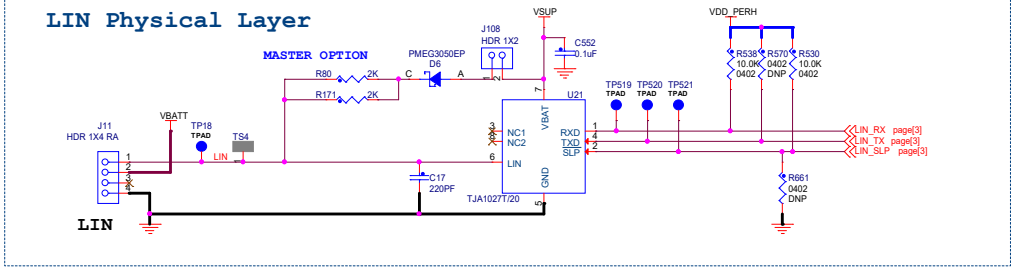




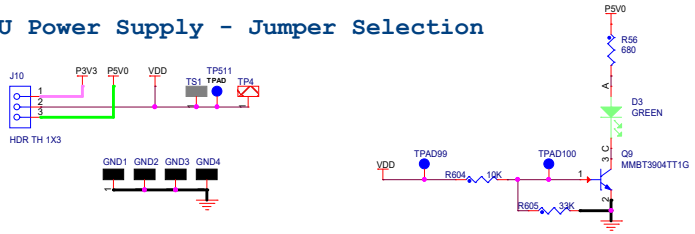
Dual supply translating transceiver; open drain; auto direction sensing



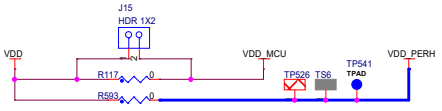
LIN Physical Layer



MCU Power Supply - Jumper Selection



MCU Current Measurement



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Drawing Title:	XS32K118EVB-Q064
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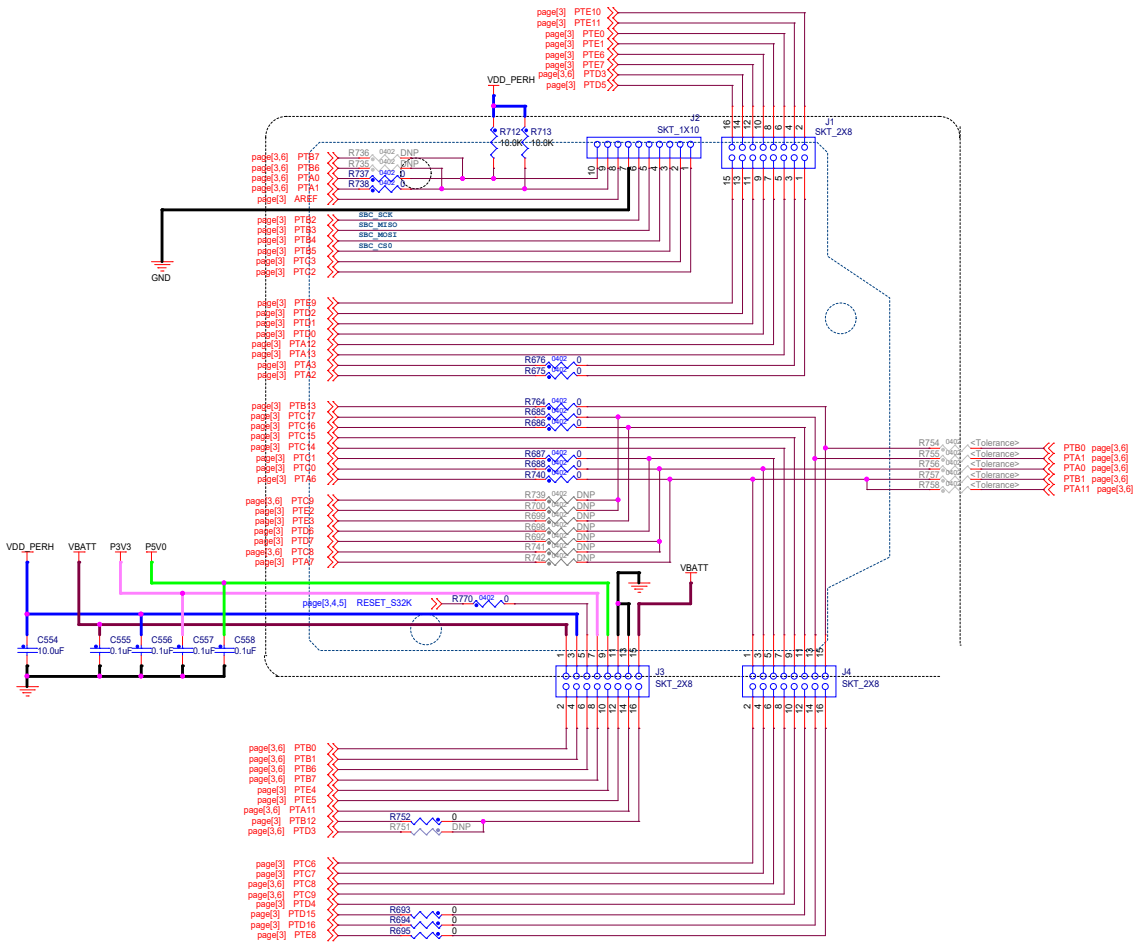
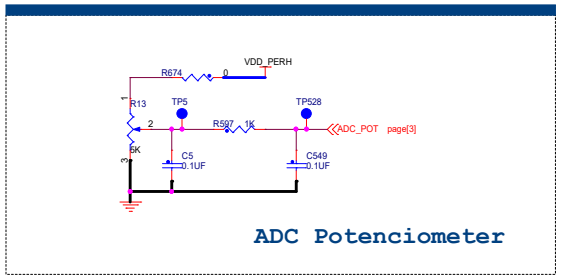
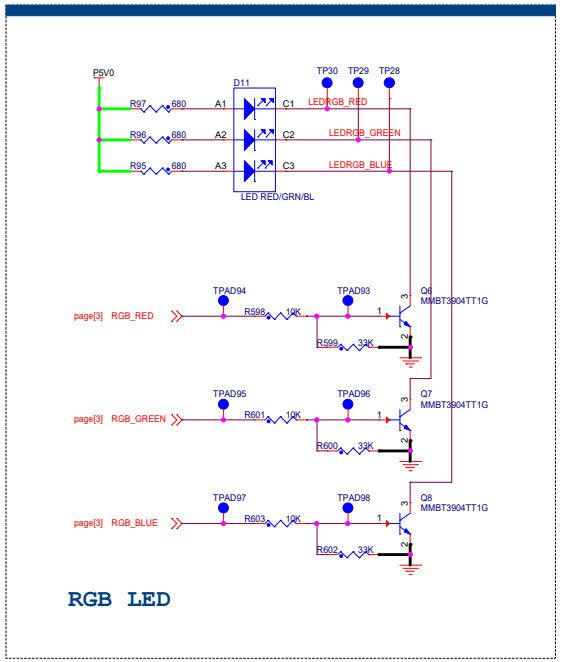
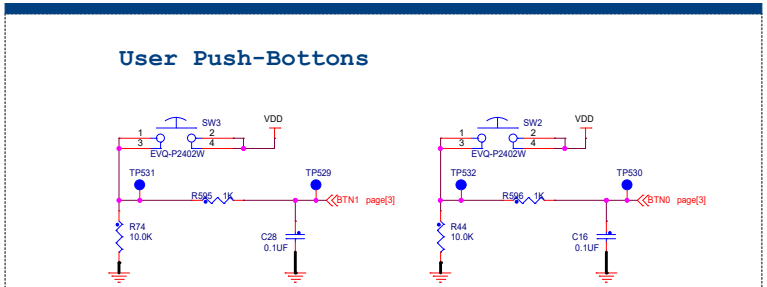




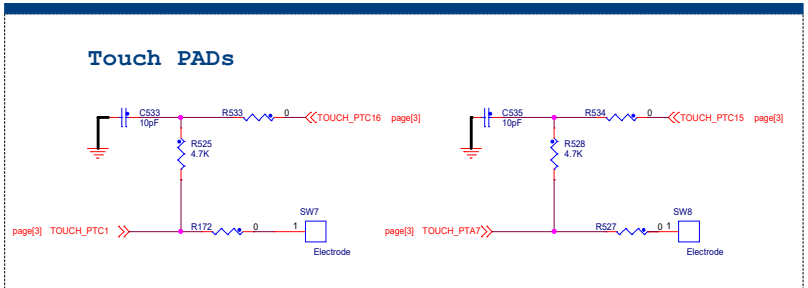
ADC Potenciometer



RGB LED



User Push-Bottons



Touch PADs

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Page Title: **I/O Headers**

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