NXP DSC DESIGNED FOR DIGITAL POWER CONVERSION APPLICATIONS

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SECURE CONNECTIONS FOR A SMARTER WORLD

PUBLIC

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- Benefits of digital controlled power conversion system
- DSC highlighted features for digital power applications
- Typical digital power use case introduction

Benefits of Digital Controlled Power Conversion System

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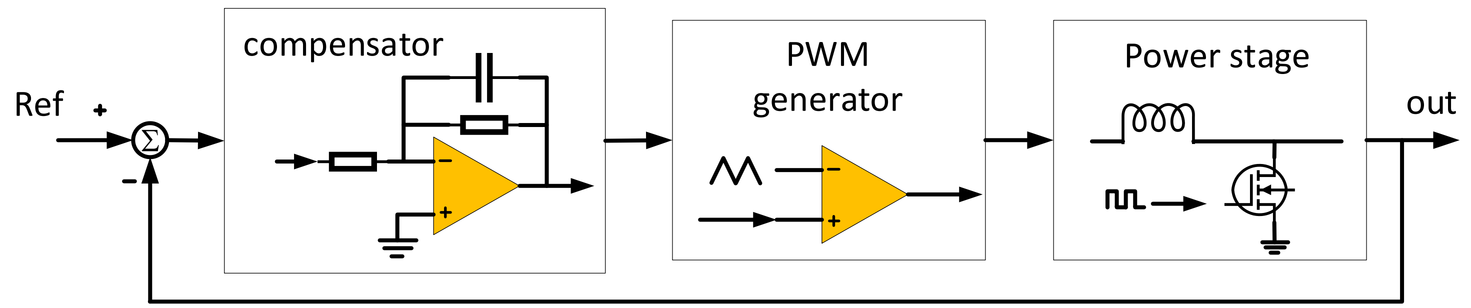
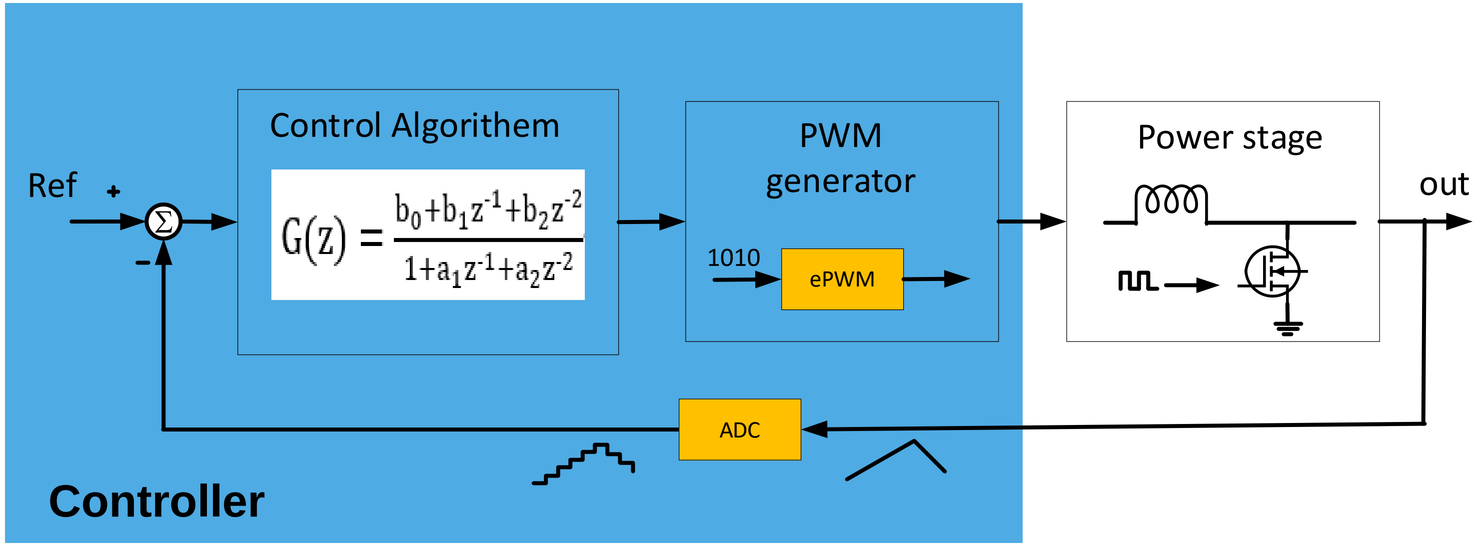
DIGITAL VS. ANALOG CONTROL IN POWER CONVERSION SYSTEM

Analog control



Digital control



Digital control depends on translation of primary measurements of analogue signals into digital values, then the control is hardware independent.

BENEFITS OF DIGITAL CONTROL

Improved flexibility

- ✓ Easy customization
- ✓ Easy to update
- ✓ Easy to implement adaptive control and nonlinear control
- ✓ Suitable for various topologies

High efficiency and power density

- ✓ According to line and load change, intelligently adjust the power stage operation to optimize efficiency in real time
- ✓ Smooth automatic switching between digital and analog control in one controller can improve standby efficiency

Cost effective

- ✓ Integrated control hardware, fewer devices can perform more complex functions
- ✓ future update without board change

Smart and Reliable

- ✓ Monitoring provides powerful protection for power system
- ✓ Energy internet, integrate the communication function with the power part

DSC Highlighted Features for Digital Power Applications

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DSC HIGHLIGHTED FEATURES FOR DIGITAL POWER APPLICATIONS

Featured Peripheral Resources

- Up to 2x 8-channel eFlexPWM module
- 2 x 8-channel 12-bit cyclic ADC
- Inter-Module Crossbar with Event Generation function
- Up to 4x High Speed Comparators with integrated 6/8-bit DAC ref.
- Multiple function QuadTimer
- Two Periodic Interval Timers
- Up to 2x 12-bit DAC

High Speed & Low Power Consumption

- 32-bit 56800EX core up to 100Mz, providing full 32-bit compatibility
- 21-bit PWM with NanoEdge high resolution, 312ps PWM frequency, duty cycle and deadtime resolution
- High speed ADCs capture events real-time, maximum ADC clock frequency of 25MHz
- Less than 0.3mA/MHz at full speed run

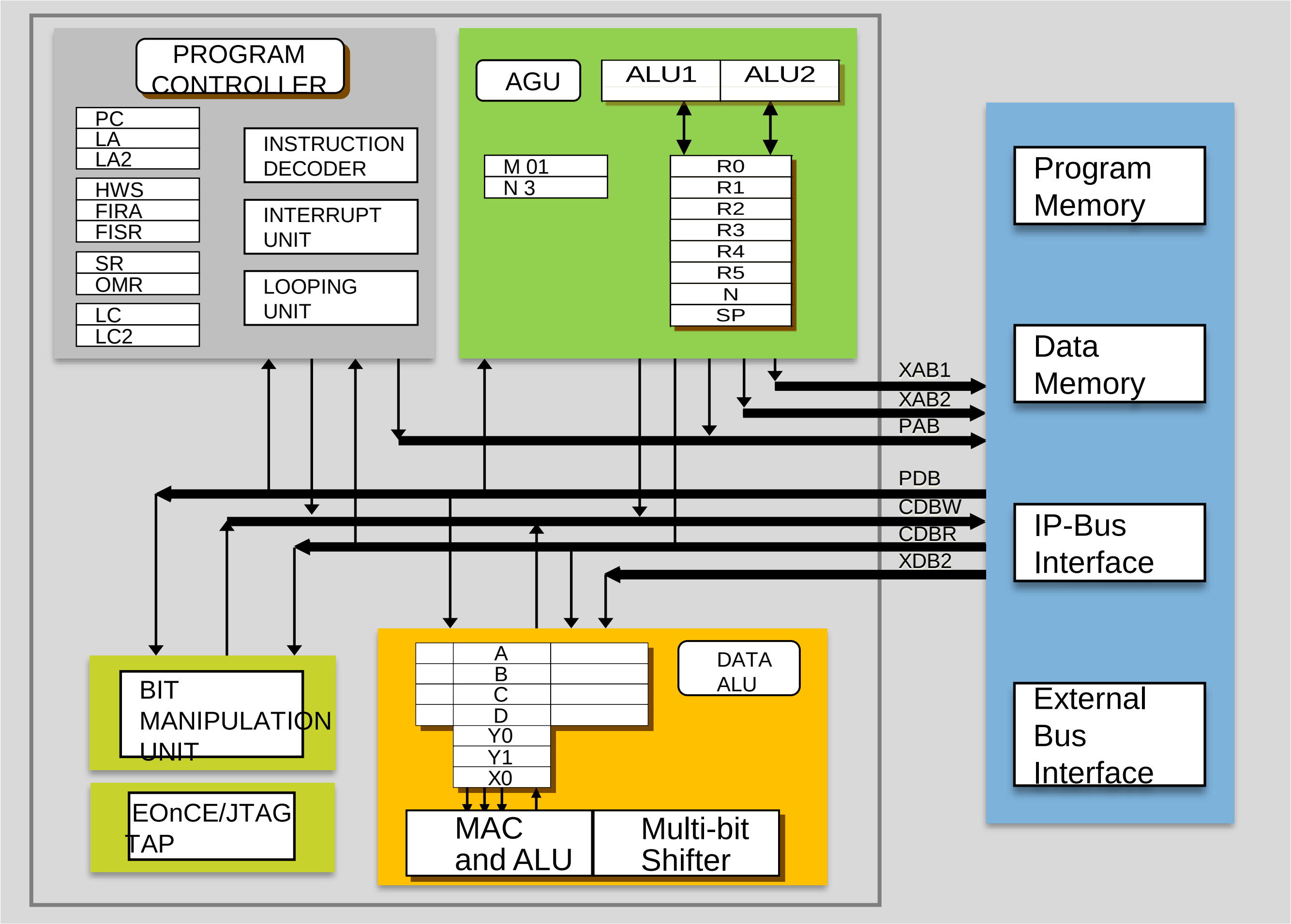
Flexible Sync & Trigger

- eFlexPWM different submodules can be flexible synced with each other
- eFlexPWM each submodule can generate 6 trigger signals
- ADC sync signal can be from PWM, Comparator, Qtimer, PIT or AOI
- Flexibility with the crossbar to simplify pin out and peripherals interconnection

Outstanding Support

- Enhanced customer experience via integrated tools and reference designs
- Code reusable across the complete portfolio
- Extensive software libraries provide quick project ramp up
- Local support expert team

56800EX CORE ARCHITECTURE



Program Controller (PC)

- Hardware loop support
- Nested Interrupt, priority control

Address Generation Unit (AGU)

- All registers have shadowed registers, effectively reduce context save/restore time during exception

Bit Manipulation (BMU):

- New bit manipulation instr. BFSC

Arithmetic Logic Unit (ALU):

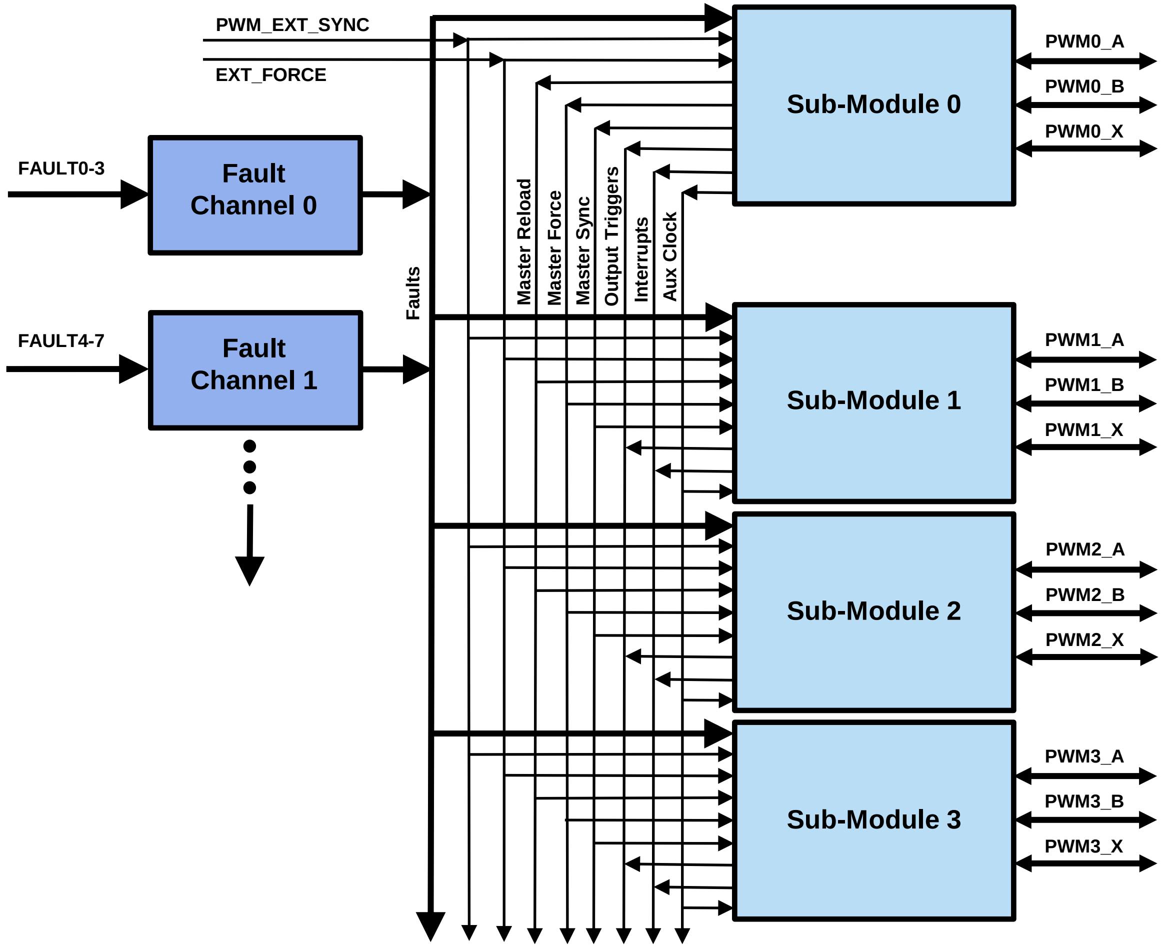
- single-cycle 32 x 32-bit -> 64-bit MAC
- 32-bit fractional and integer arithmetic
- Logic multi-bit shifter
- Bit-reverse addressing mode, supporting FFT

Bus architecture customized for DSP applications

- 1x 16bit Instr. + 1x 32bit data + 1x 16bit data bus
- Concurrent instruction fetches
- Dual data accesses in single cycle

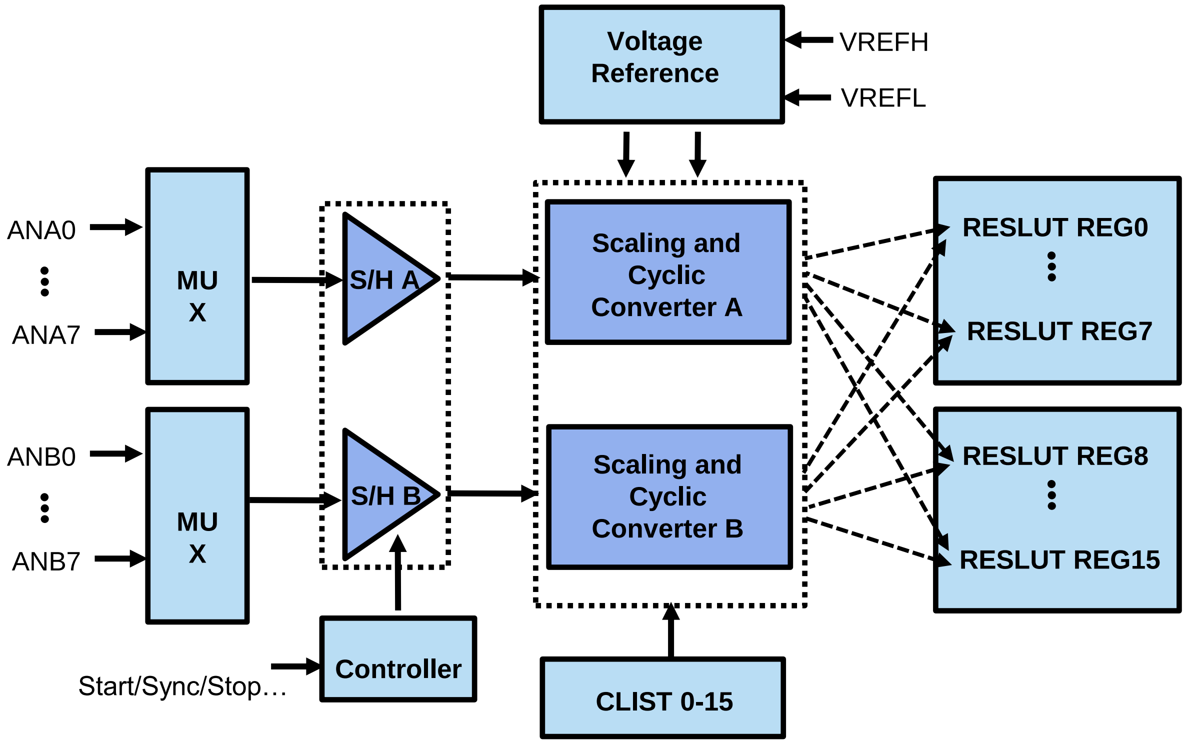
EFLEXPWM – 312PS HIGH RESOLUTION PWM

- 312ps resolution, suitable for digital power applications
- Flexible PWM control and multiple modes
  - Center, edge-aligned, and asymmetrical PWMs
  - Complementary PWM pairs
  - Phase shifted & double switching PWM outputs
  - Independent control of both edges of each PWM output
  - Full and half cycle reload capability
  - Individual software control for each PWM output
- Synchronization & Trigger
  - Support for synchronization to external hardware or other PWM
  - Multiple output trigger events can be generated per PWM cycle
- Safety
  - Fault inputs can be assigned to control multiple PWM outputs
  - Programmable filters for fault inputs
  - Fault automatic clearing
  - Independent top and bottom deadtime insertion
- Multiple functions support
  - Channels not used for PWM generation can be used for input capture functions, dual independent capture engines



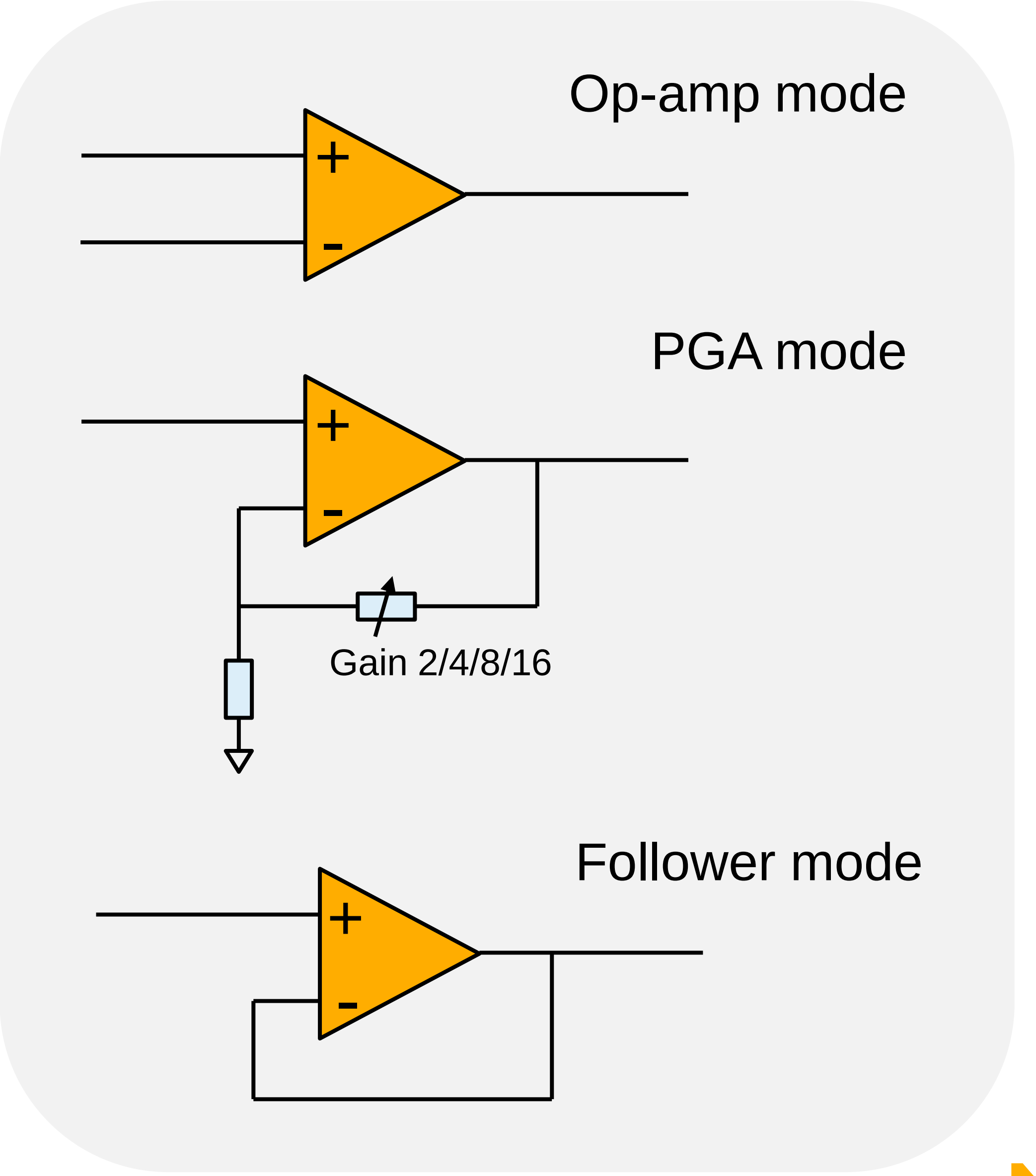
12-BIT HIGH SPEED CYCLIC ADC

- High input impedance, suitable for current sensing
- Max. 300ns conversion rate, up to 6.67 MSPS when two ADC work simultaneously (parallel mode)
- Flexible trigger mode include once, triggered or loop scan
- Can be synchronized to other peripherals by internal Crossbar, such as the PWM
- Improved Accuracy
  - Integrated PGA (x1, x2, x4) for small signal detection
  - Optional sample correction by pre-programmed offset
  - Support single-end and differential mode
- Multiple Functions
  - Optional interrupts at end of scan if there’s an out of high/low limit or there is a zero-crossing event



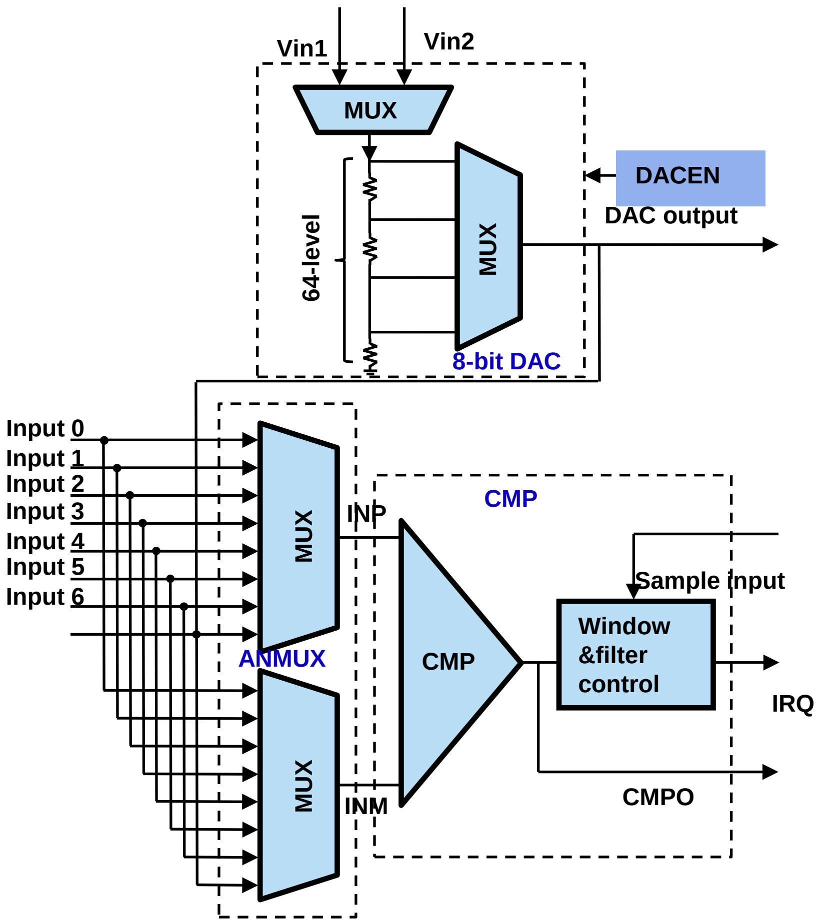
MULTI-MODE OPAMP

- 8MHz GBP, suitable for fast and accurate voltage and current sensing in power conversion and motor control applications
- Suitable for low side detection, output rail-to-rail
- work in three modes:
  – Op-amp mode
  – PGA mode (Gain 2/4/8/16)
  – Follower mode
- Output directly connect to ADC and ACMP input

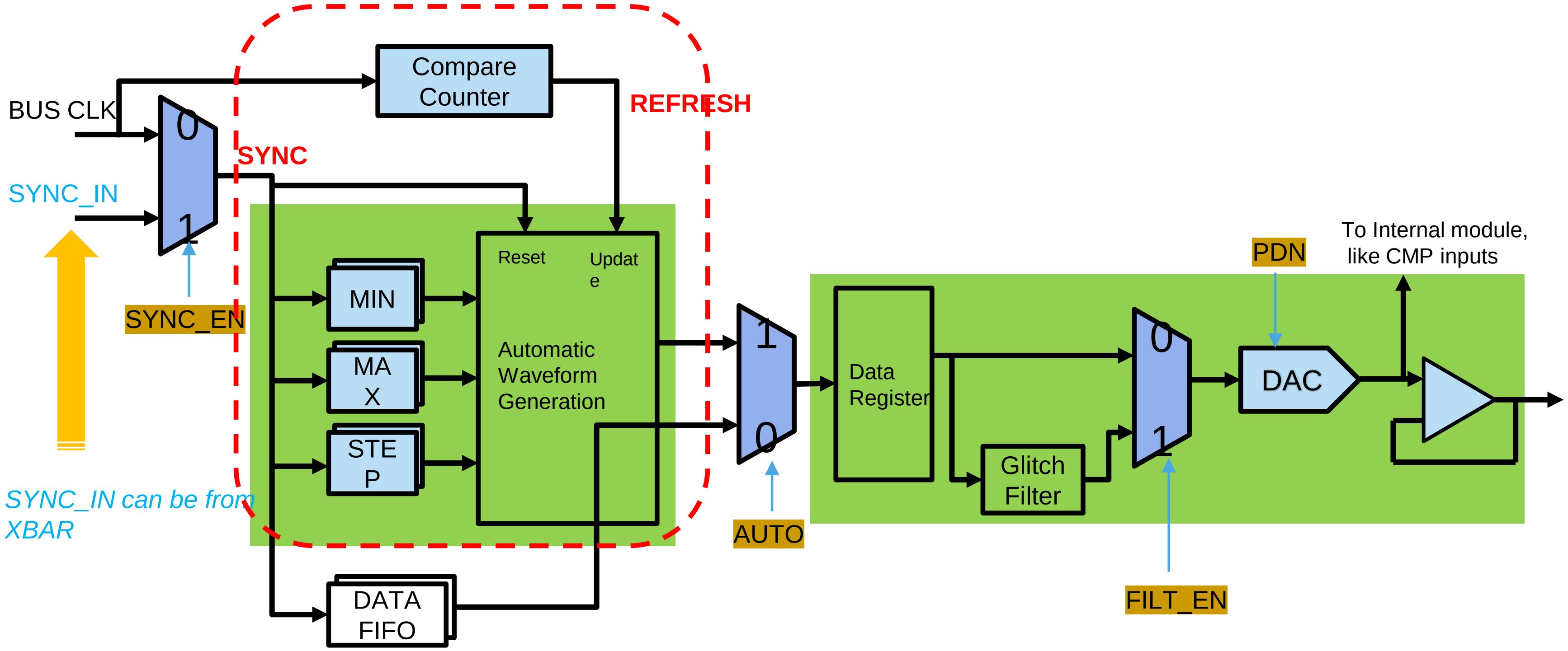


HSCMP /W 6/8-BIT REFERENCE DAC

- Multiple analog comparators with integrated programmable DAC references
- selectable internal hysteresis levels
- Full rail-to-rail comparison range
- Selectable input source includes external pins and internal 8-bit or 12-bit DACs and OPAMP out
- Comparator output may be:
  - Sampled
  - Windowed (ideal for certain PWM zero-crossing-detection applications)
  - Digitally Filtered
- External hysteresis can be used
- Integrated DAC is powered down to conserve power when it isn't used



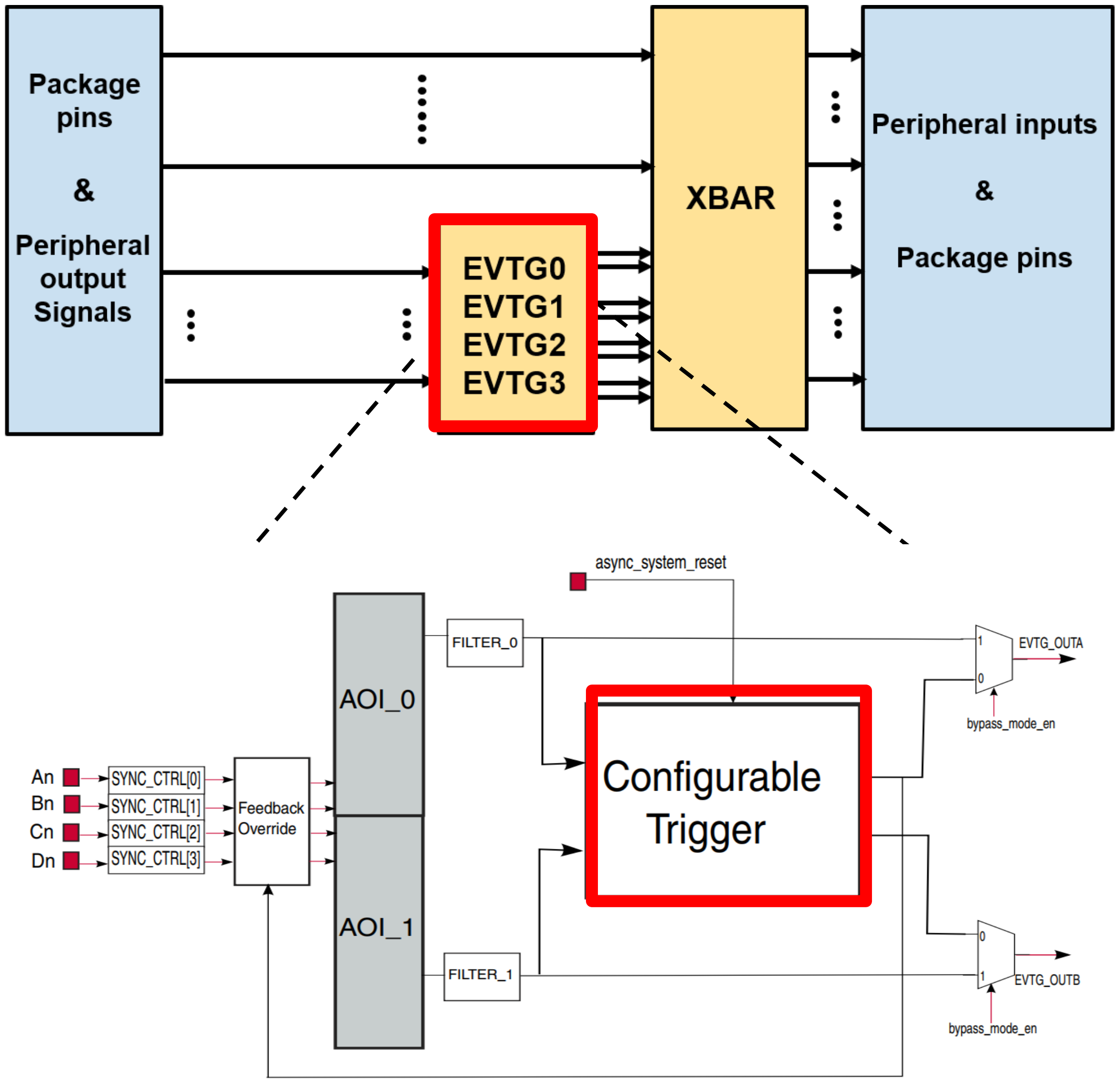
12-BIT DAC



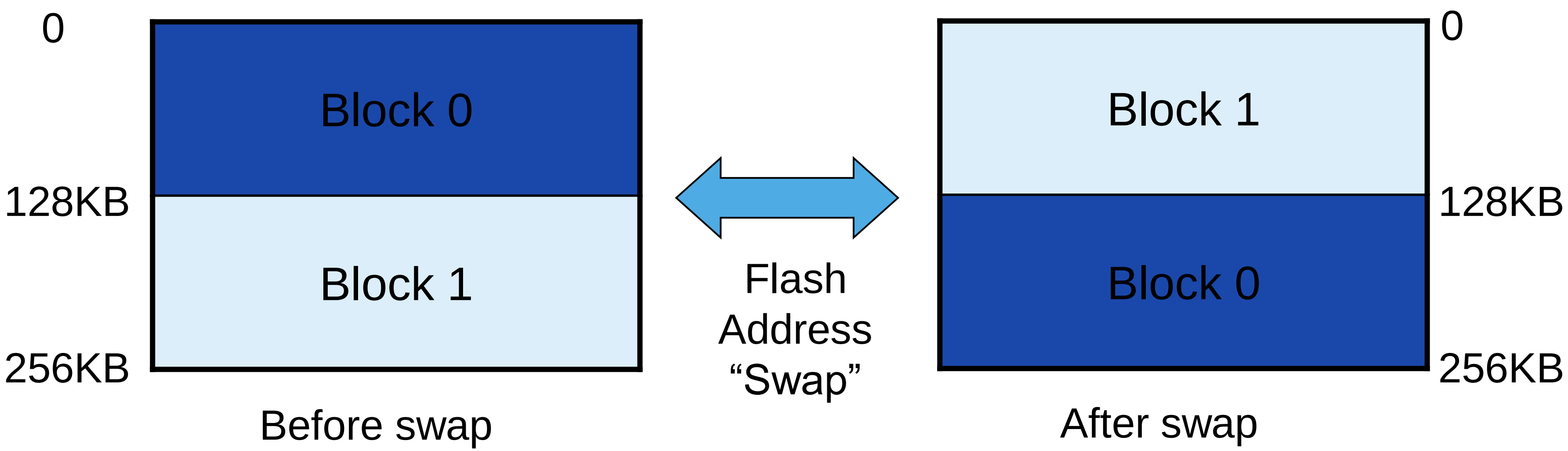
- Automatic waveform generation:
  - MAX/MIN/STEP are buffered and updated with sync signal
  - Sync signal reset the automatic waveform to its new start point defined by new MAX/MIN
  - Configurable update rate
  - Automatic waveform can hold its last value until the next active edge of SYNC_IN

CONFIGURABLE LOGIC – XBAR + EVENT GENERATOR (EVTG)

- XBAR
  - A switch matrix with dozens of inputs and outputs
  - Each output can choose any input
  - The inputs and outputs are connected to peripherals or package pins
- EVTG
  - Each has four input A,B,C and D and two outputs
  - Each has two groups of AOI to generate two combinational expressions.
  - Each has one flexible flipflop that can be configured as RS, D-FF,T-FF, JK-FF and Latch, etc.



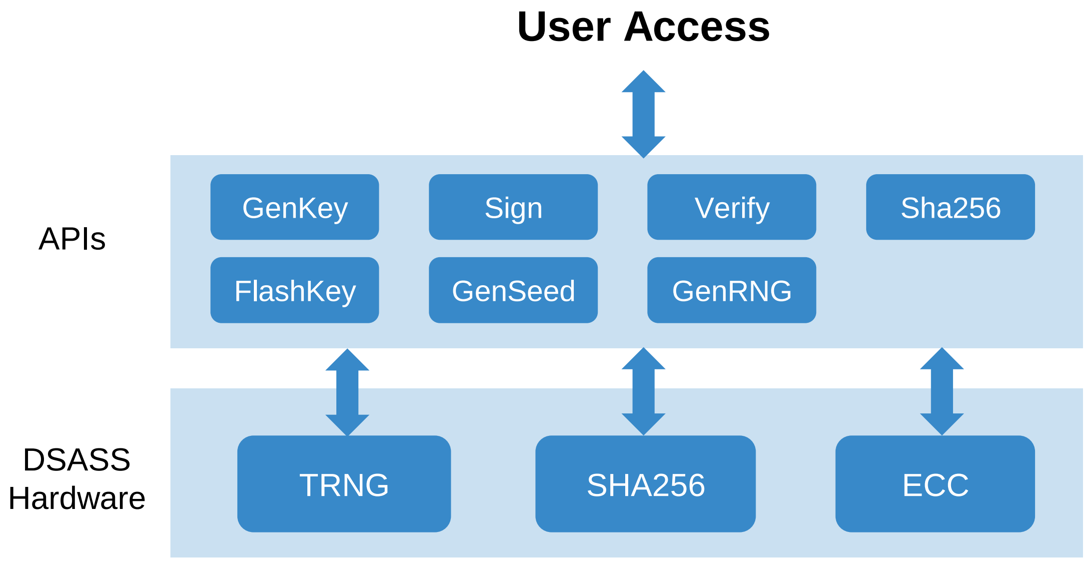
FLASH SWAP



- Two Flash blocks
- User can execute from block 0 while re-programming block 1
- When block 1 is ready for execution, user completes the swap process by executing a SWAP command and a reset
- The addresses of block 0 and block 1 exchanges after reset. Program now executes in block 1 because it is mapped to address range which starts from 0

CRYPTO ENGINE – DSASS

- **DSASS** = **D**igital **S**ignature **A**lgorithm **S**ecurity **S**ubsystem
- DSASS contains HW realization of below algorithms:
  - Elliptical Curve Cryptography (ECC) based digital signature authentication
  - SHA256
  - True random number generator (TRNG)
- Complete APIs and example codes to utilize the crypto capability



Typical Digital Power Use Cases Introduction

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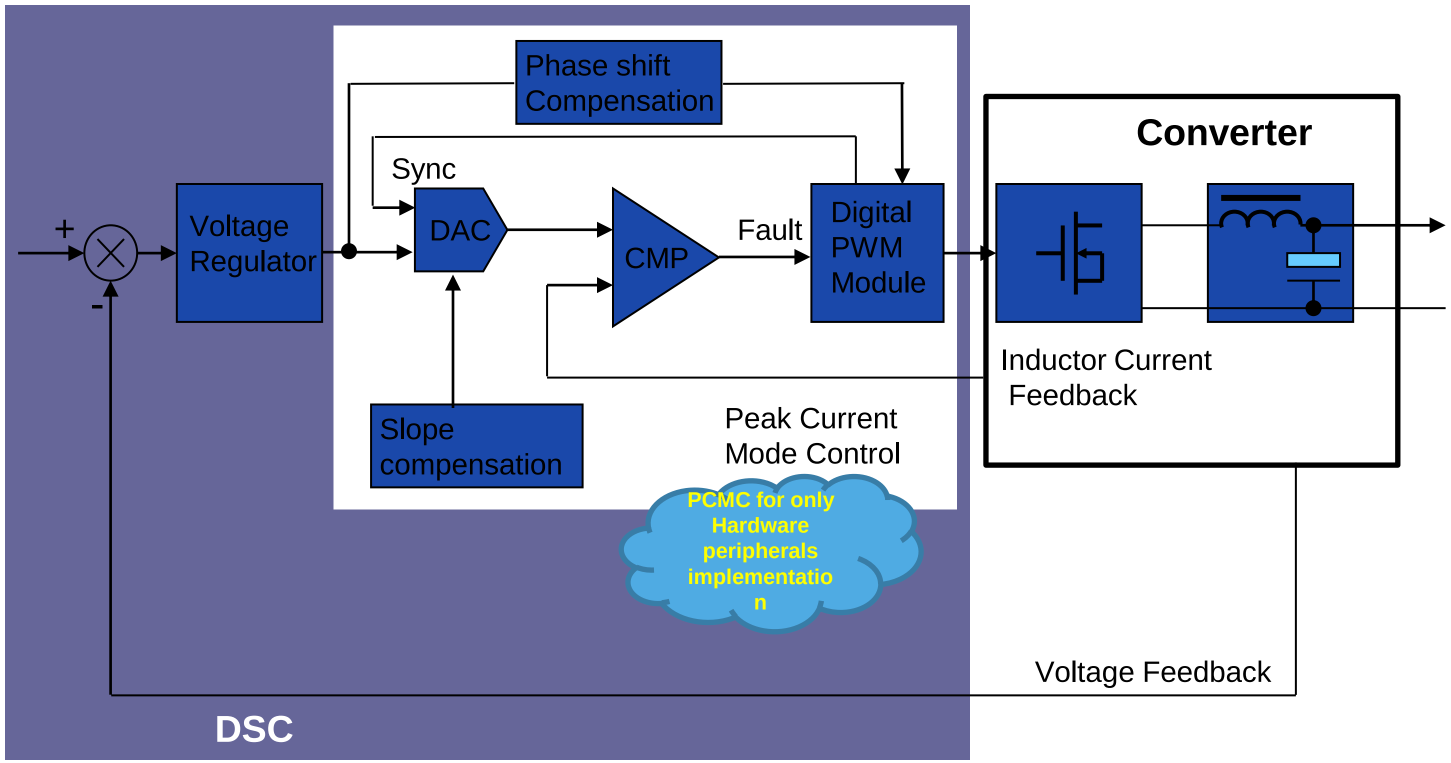
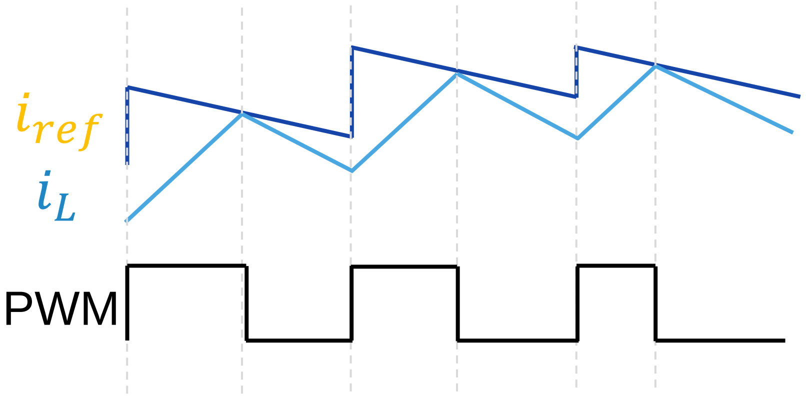
PEAK CURRENT CONTROL





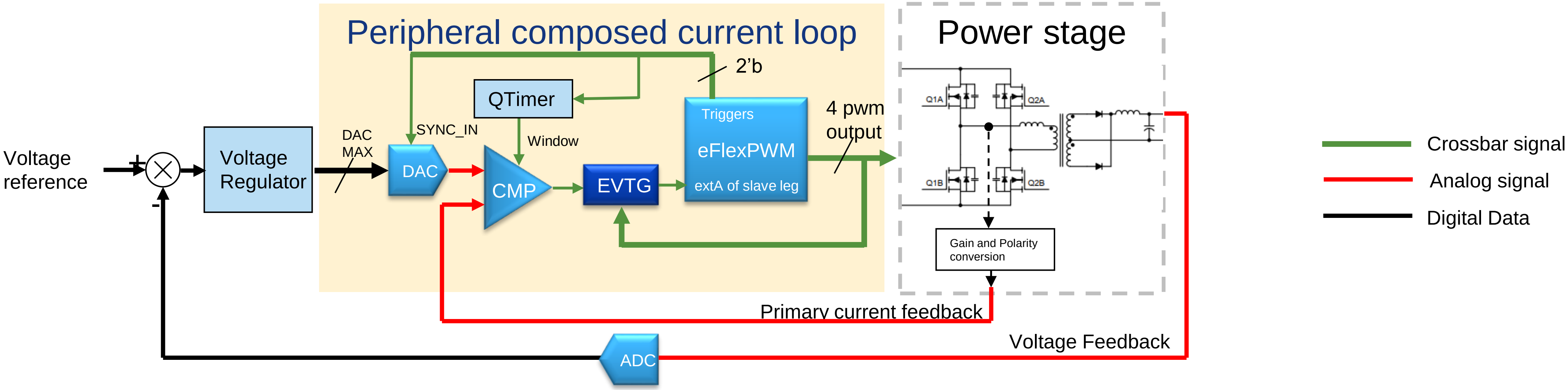
Window Mode Comparator → Only take effect when PWM is on for more reliable

12 Bit High Resolution DAC → Slop compensation with adjustable slow rate

PWM Signal Synchronization → CBC Peak Value control (cooperate with AOI to achieve minimum duty cycle control)

Fully hardware realization solution, which brings larger bandwidth and elimination of CPU overhead. Now CPU can focus on voltage loop and other staffs, like housekeeping.

PEAK CURRENT CONTROL MODE(PCCM) PSFB

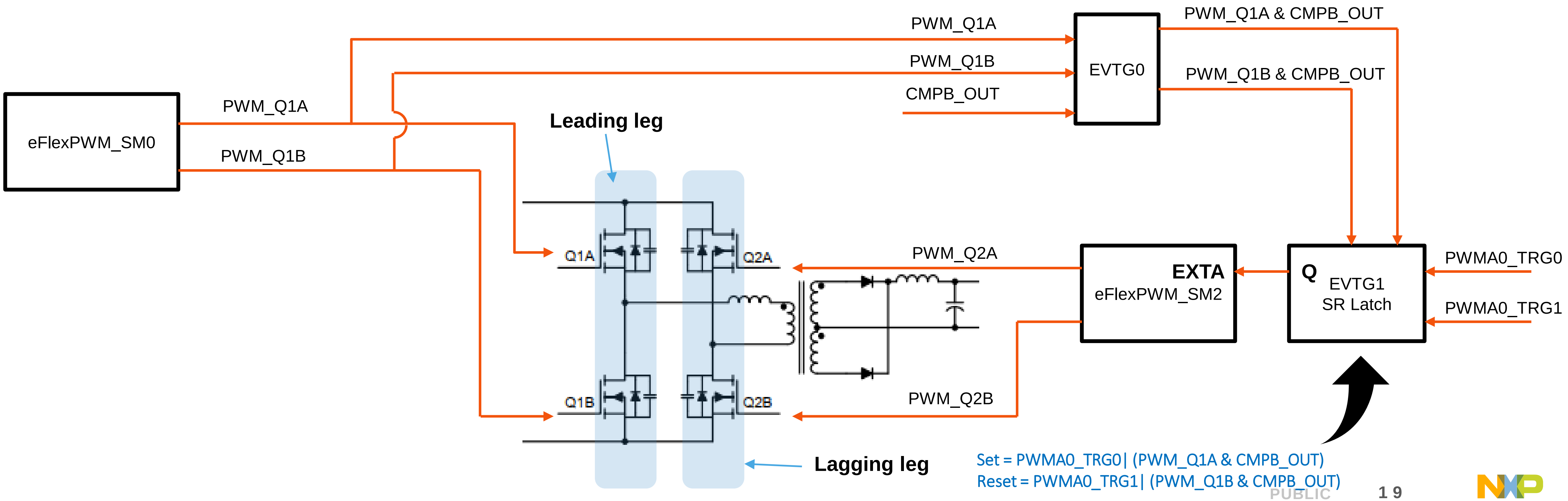


With the presence of EVTG and XBAR, the status and phase of the bridge legs can be monitored to avoid maloperation (e.g. multiple switches of slave leg within half of the PWM period).

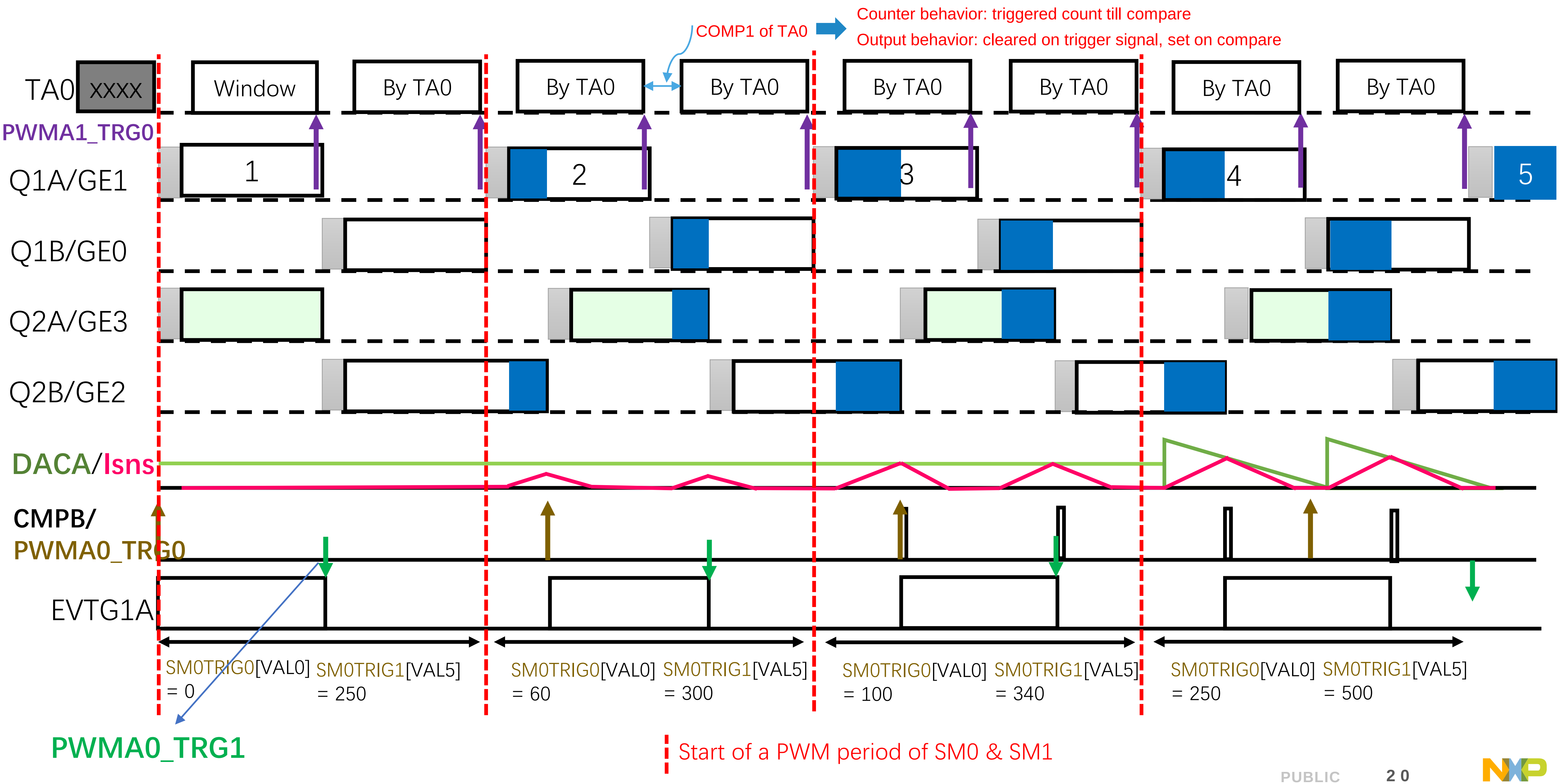
PWM GENERATION FOR LEADING AND LAGGING LEGS CONTROL

EVTG flip flop works at Set/Reset mode. Master leg (Q1A&Q1B) is controlled by SM0 of eFlexPWMA, where fixed 50% duty complementary waveforms are applied. Slave leg(Q2A&Q2B) is controlled by SM1 of eFlexPWMA, the SM1 outputs are from its EXTA input, which is fed by EVTG output. With the convenience that both PWMA output signals and its trigger signals can be routed to XBAR inputs simultaneously, the Reset and Set input signals of EVTG can be realized so that slave leg is fully synchronized with master leg and also controlled by coil current.

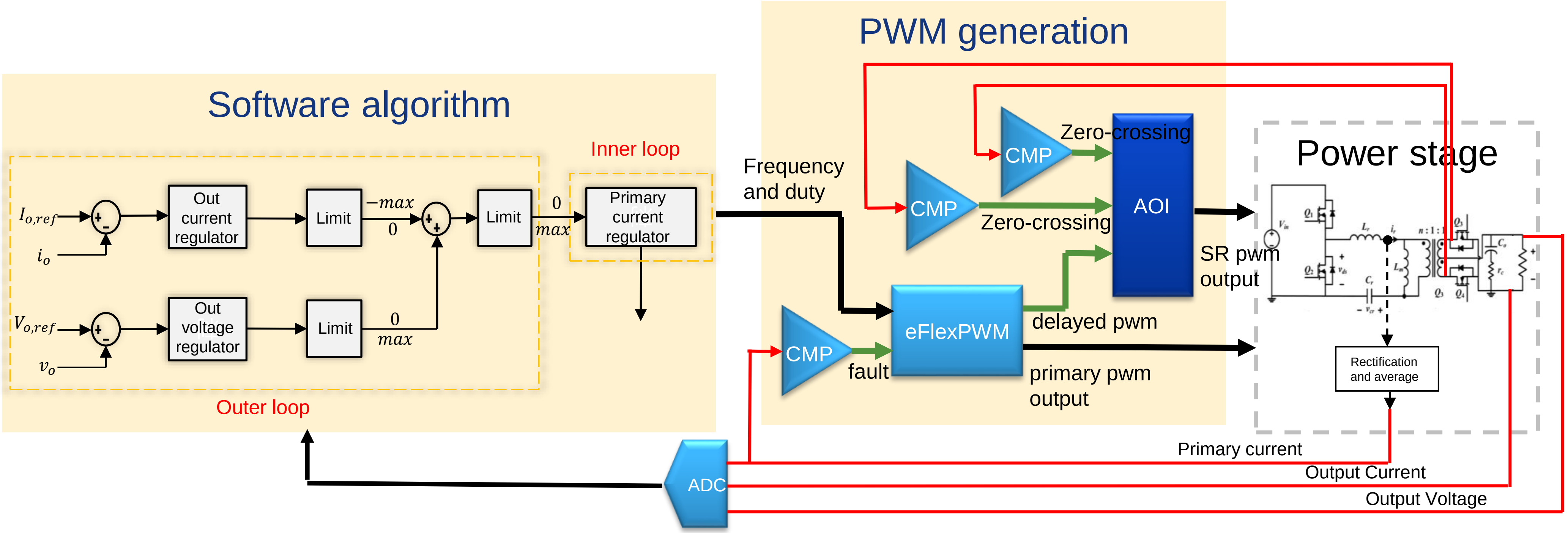
The control loop of primary coil current is realized without CPU overhead at all, which means high dynamic response can be achieved. Meanwhile, the outer voltage loop and other house keeping tasks are flexibly realized by firmware. This control method combines the advantages of pure analog control loop and digital MCU control, where EVTG plays an important role.



SOFT-START PROCESS EXAMPLE

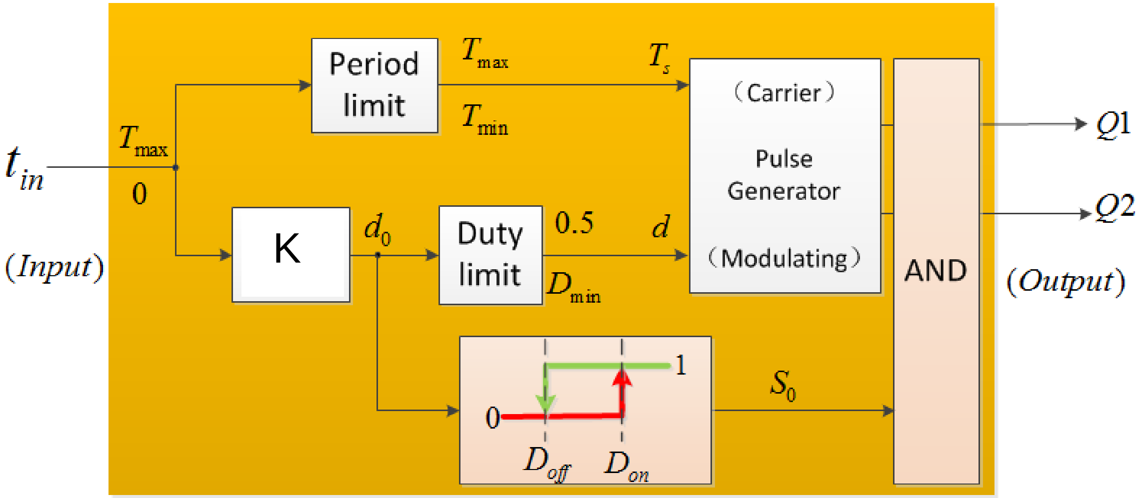


AVERAGE CURRENT CONTROLLED LLC

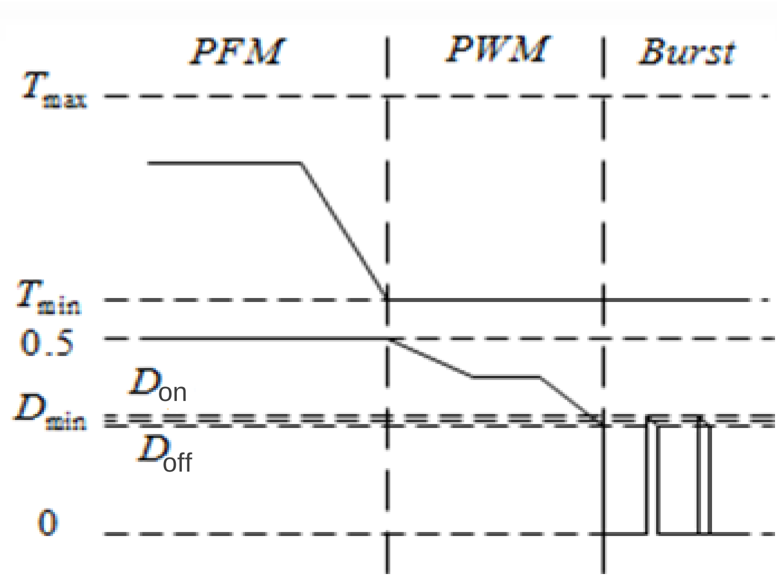


- Flexible software algorithm: concurrent output loop smooth transition to achieve constant output voltage and overload current limiting, smooth transition between PFM, PWM and burst mode
- Precise SR control
- Hardware fault protection

AUTOMATIC MODULATION MODES SWITCH



Drive signal generator block diagram



- Mode 1: PFM

$$T_{\min} \le t_{in} \le T_{\max} \Rightarrow T_s = t_{in}, d = 0.5$$

- Mode 2: PWM

$$KD_{off} < t_{in} < T_{min} \Rightarrow T_s = T_{\min}, D_{\min} < d < 0.5$$

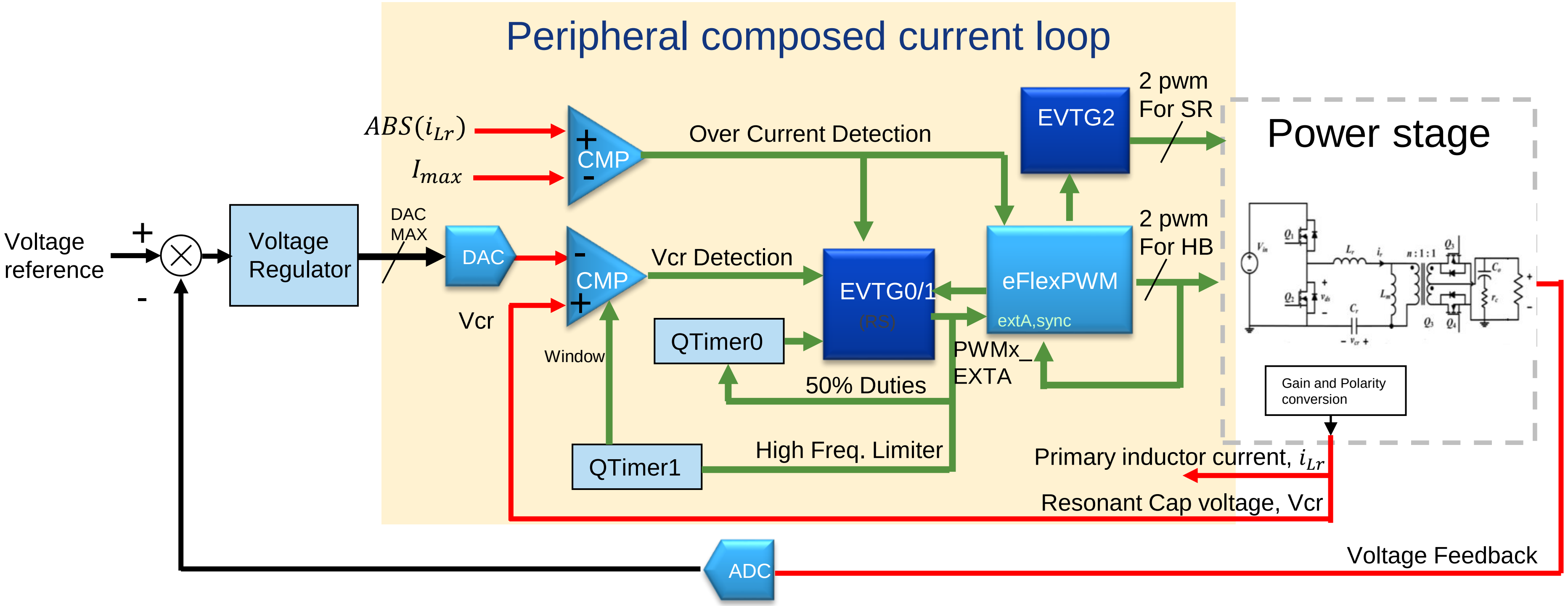
- Mode 3: Burst mode

$$t_{in} < KD_{off} \Leftrightarrow d_0 < d_{off}$$

$d_0 > D_{on} \Rightarrow S_0 = 1$ Burst on

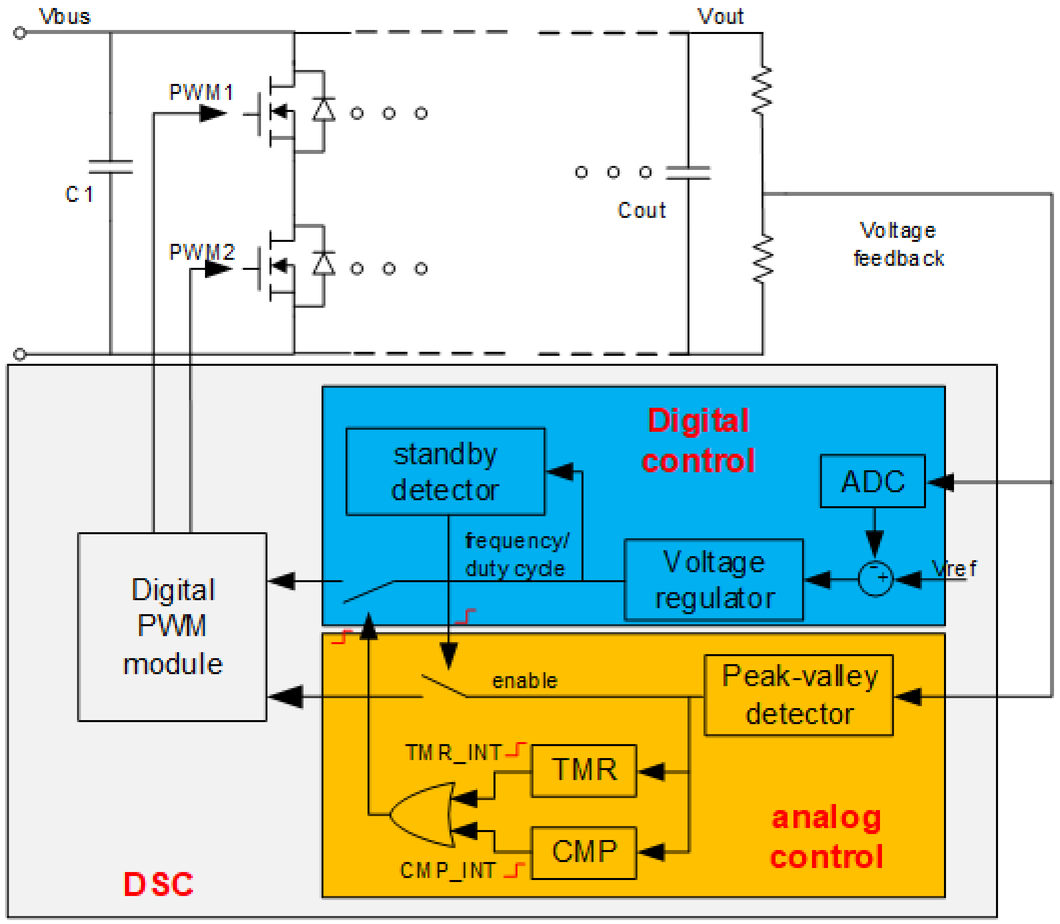
$d_0 < D_{off} \Rightarrow S_0 = 0$ Burst off

CHARGE CURRENT CONTROLLED LLC



- Rich and flexible peripherals and flexible signal interconnection promise the complex control requirements:
  - Maximum current limit
  - 50% duty cycle
  - High/low frequency limit
  - Ramp compensation

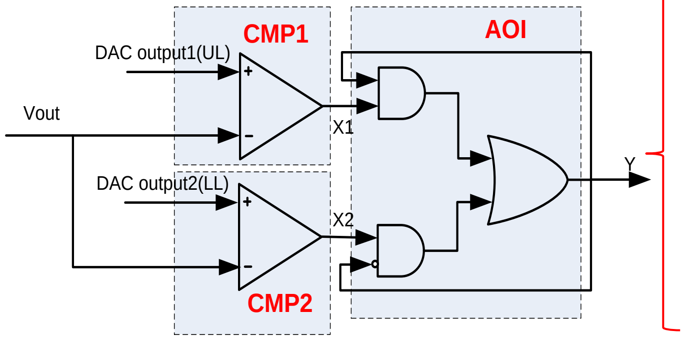
INNOVATIVE METHOD FOR STANDBY EFFICIENCY IMPROVEMENT

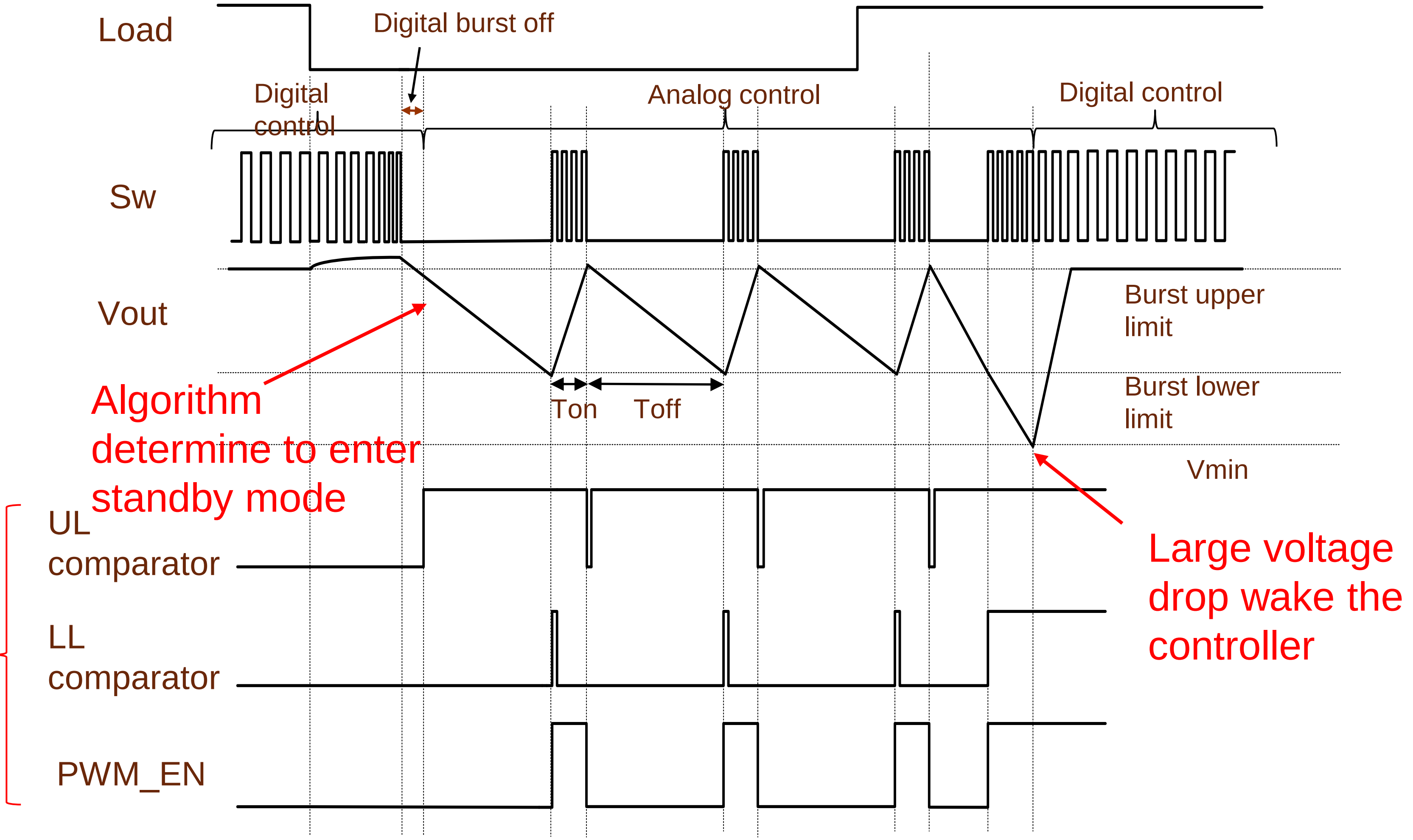


Hybrid control in one DSC to minimize the controller power consumption during system standby mode.

- In digital control mode: core and memory of the controller are powered up, the PWM signal are adjusted according to software algorithm
- In analog control mode: core and memory of the controller are powered off, the controller built-in peripherals constitute the controller
- Smooth and automatic switch between two mode
  - In digital control mode, the algorithm can judge whether to enter the analog mode
  - In analog mode, specific event can be configured to wake the controller

INNOVATIVE METHOD FOR STANDBY EFFICIENCY IMPROVEMENT – EXAMPLE





WRAP-UP

Through this session, you already learned:

- Benefits of digital controlled power conversion system
- DSC highlighted features designed for digital power applications:
  - 56800EX core
  - eFlexPWM
  - Analog peripherals: High speed cyclic ADC, multi-mode OPAMP, 12-bit DAC with automatic waveform generation, HSCMP with reference DAC
  - XBAR and EVTG
  - Flash swap
  - Crypto engine
- Typical digital power use cases:
  - PCCM PSFB DC/DC converter
  - Average current controlled LLC DC/DC converter
  - Charge current controlled LLC DC/DC converter
  - Standby system efficiency improvement

Q&A

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