NXP 20G LINEAR RE-DRIVER PTN38007/PTN38003A/PTN3944 /PTN3816

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SECURE CONNECTIONS
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Agenda

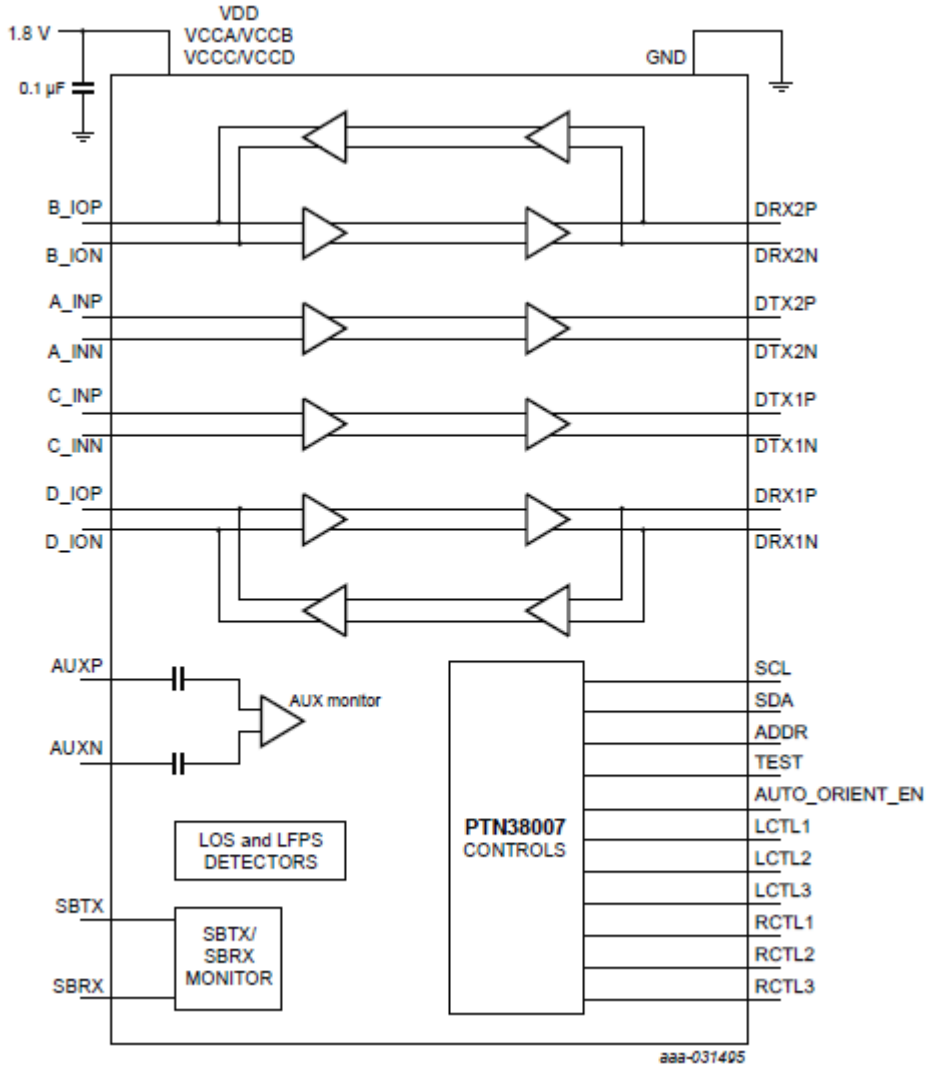
- **NXP Linear Re-driver Family Overview**
- **Design Block Diagram Examples**
- **Programming Overview**
- **EVM Overview**

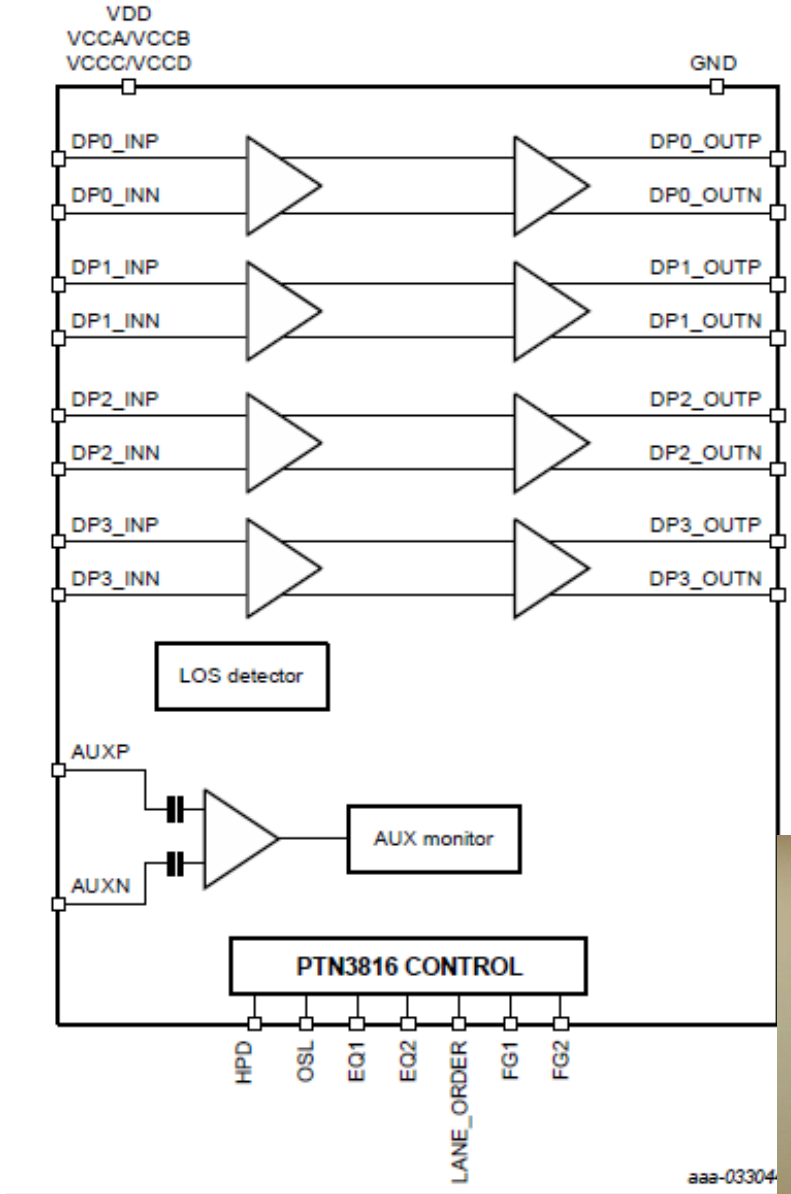
NXP 20Gbps Linear Re-driver Family Overview

PTN38007/PTN38003A/PTN3944/PTN3816 Overview

	PTN38007	PTN38003A	PTN3816	PTN3944
Order Number	PTN38007EWY	PTN38003AEWY	PTN3816EWY	PTN3944EWY
Host Interface	I²C (4 possible addresses) Strapping Options @ POR	I²C (4 possible addresses) Strapping Options @ POR	Strapping Options only	I²C (32 possible addresses) Strapping Options @ POR
Chip ID (Reg[0x00])	0x09	0x0B	----	0x0F
Target application interfaces	Type-C Port with USB3.x/ DisplayPort 2.0/ Thunderbolt 3/ USB4/	Type-C Port with USB3.x/ DisplayPort 2.0	DisplayPort 2.0	PCIe Gen 4 @ 16Gbps
Power on default mode of operation	Deep power saving	Deep power saving	DisplayPort 4 Lane	PCIe 4 Lane Single Direction
AUX Snooping	Yes	Yes	Yes	No
LS(Tx/Rx) Snooping	Yes	No	No	No
Gain Control	I2C or LCTRL/RCTRL	I2C or LCTRL/RCTRL	LCTRL/RCTRL	I2C or LCTRL/RCTRL
FG Control	I2C	I2C	FG1/FG2 pins	FG1/FG2 pins
HPD input	No	No	Yes	No

PTN38007/PTN38003A/PTN3944/PTN3816 Overview

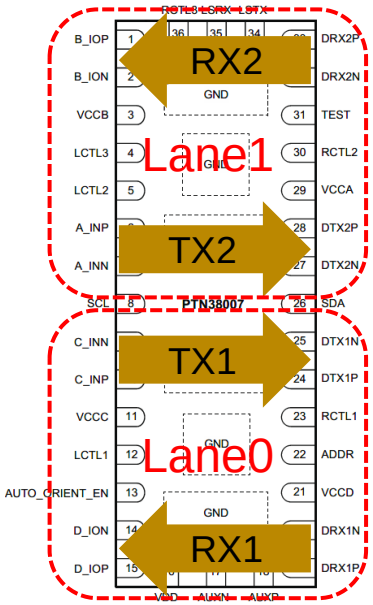




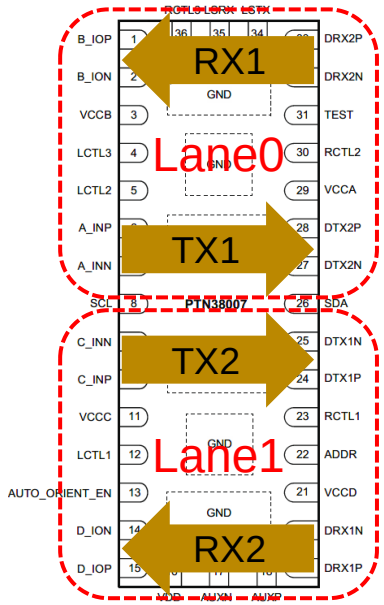
Different Operating Modes (All 4 Lanes Active)

PTN38007	PTN38007	PTN3816
		PTN3944
		PTN38007
PTN38003A	PTN38003A	PTN38003A

USB3/USB4/TBT3

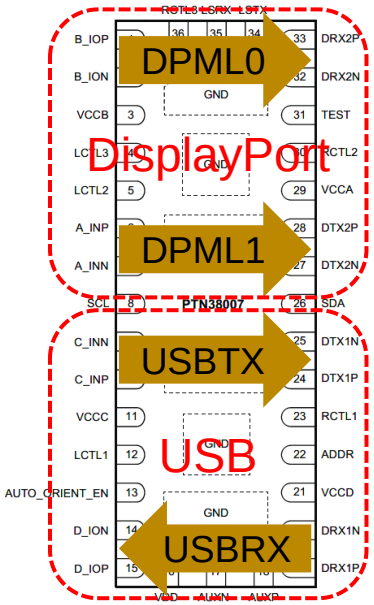


Normal Orientation

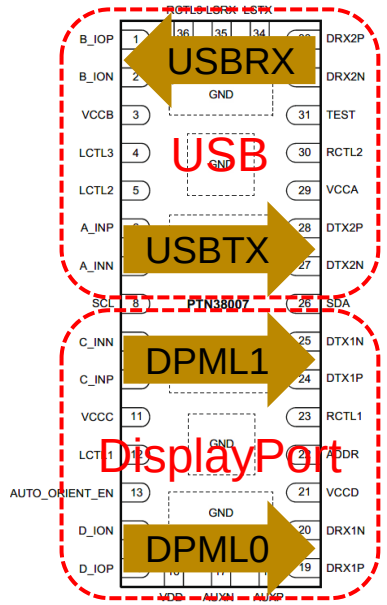


Reversed Orientation

USB3+DP2Lane

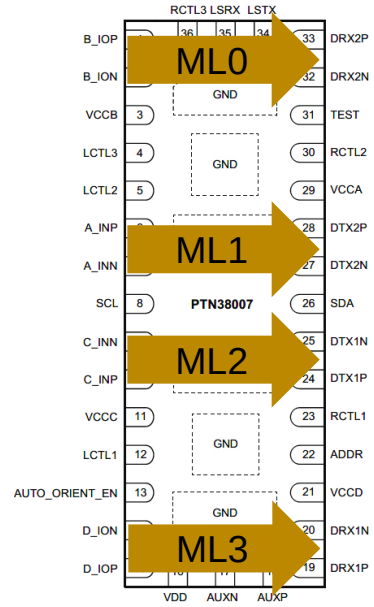


Normal Orientation



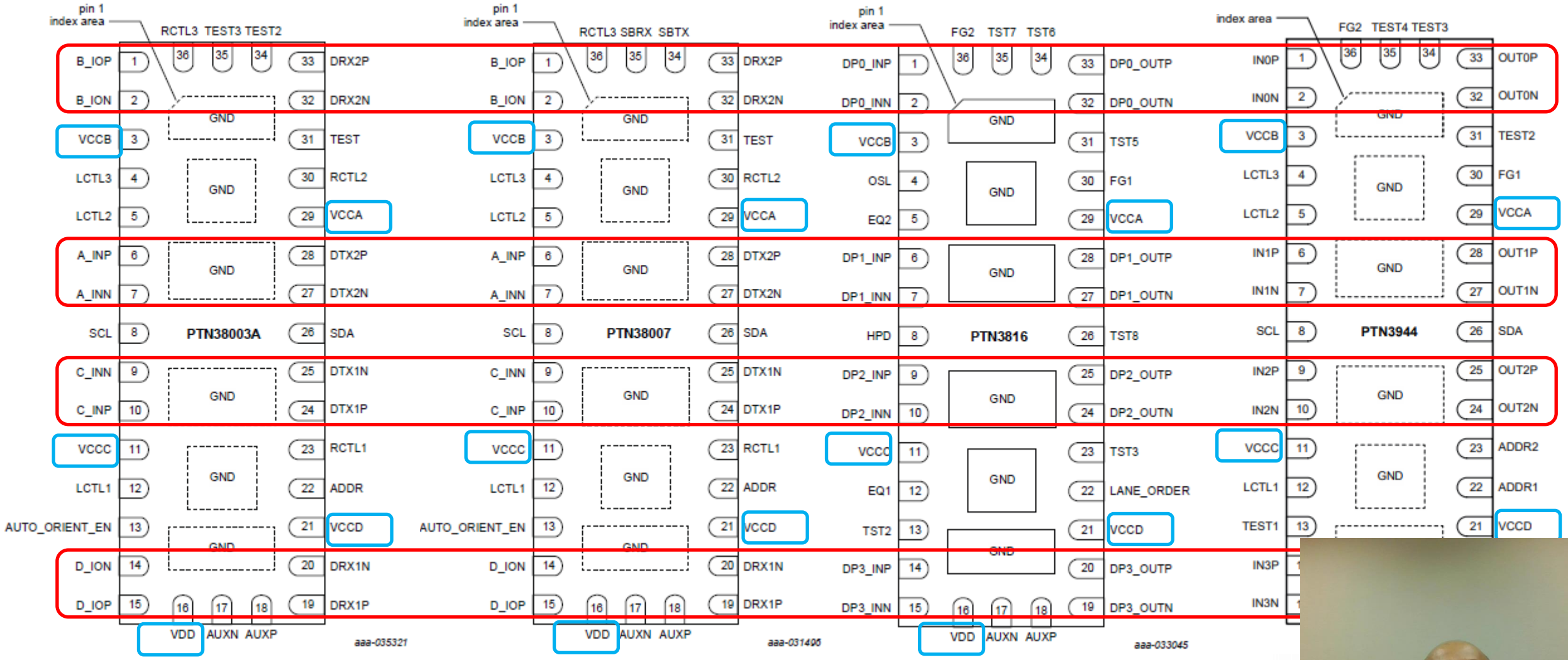
Reversed Orientation

DP4Lane/PCIe



Normal Orientation

PTN38007/PTN38003A/PTN3944/PTN3816 Overview



Pin Out overview

PTN3816				FG2	TST7	TST6				
	PTN3944			FG2	TEST4	TEST3				
		PTN38003A/7		RCTL3	LSRX	LSTX				
			Fixed Definition		GND	GND				
			IN0P	1	36 35 34	33	OUT0P			
			IN0N	2	GND	32	OUT0N			
			VCCB	3	GND	31	TEST			TST5
OSL	LCTL3	LCTL3		4	GND	30		RCTL2	FG1	FG1
EQ2	LCTL2	LCTL2		5		29	VCCA			
			IN1P	6	GND	28	OUT1P			
			IN1N	7		27	OUT1N			
HPD	SCL	SCL		8		26		SDA	SDA	TST8
			IN2P	9	GND	25	OUT2P			
			IN2N	10		24	OUT2N			
			VCCC	11	GND	23		RCTL1	ADDR2	TST3
EQ1	LCTL1	LCTL1		12		22		ADDR	ADDR1	LANE_ORDER
TST2	TEST1	AUTO_ORIENT_EN		13	GND	21	VCCD			
			IN3P	14		20	OUT3P			
			IN3N	15 16 17 18		19	OUT3N			
				VDD						
					AUXN	AUXP				
					ADDR3	ADDR4				
					AUXN	AUXP				

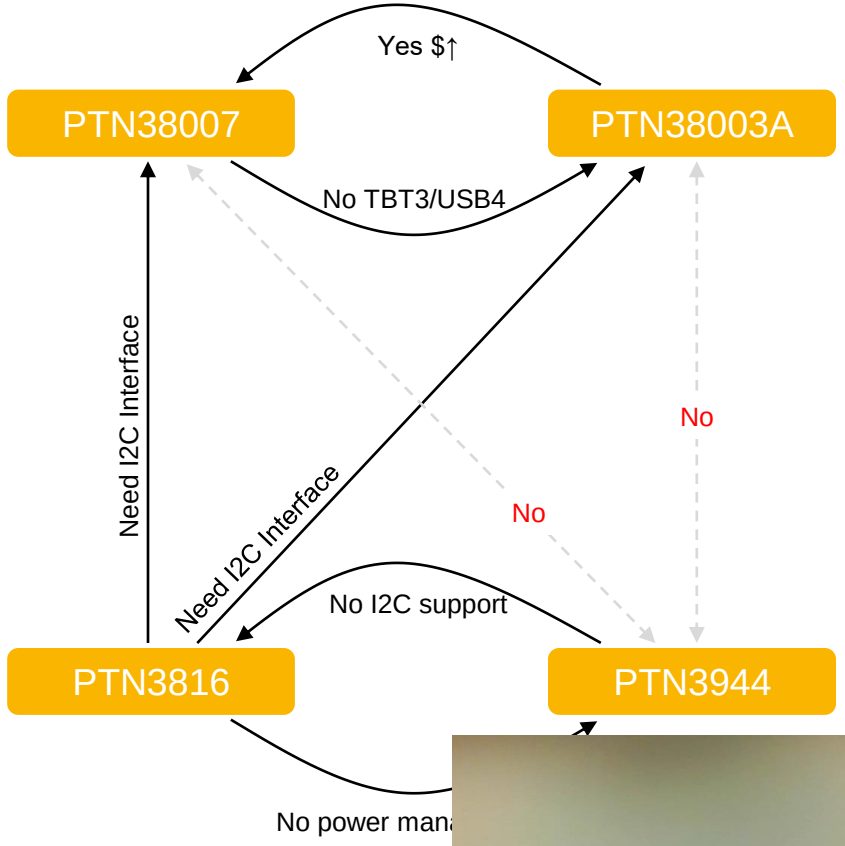
- Fixed pins
  - High speed path $In_{[0..3]}$←→$Out_{[0..3]}$
  - Power and GND
- Multi-purpose pins
  - I2C←→HPD
  - LCTL/RCTL←→FG OS EQ ADDR
  - AUX←→ADDR[3:4]
  - ADDR←→ADDR1←→LANE_ORDER

PTN38003A/PTN38007/PTN3816/PTN3944 Share Pin Out

Pin #	PTN38007	PTN38003A	PTN3816	PTN3944
4	LCTL3	LCTL3	OSL	LCTL3
5	LCTL2	LCTL2	EQ2	LCTL2
8	SCL	SCL	HPD	SCL
12	LCTL1	LCTL1	EQ1	LCTL1
13	AUTO_ORIENT_EN	AUTO_ORIENT_EN	TST2	TEST1
17	AUXN	AUXN	AUXN	ADDR3
18	AUXP	AUXP	AUXP	ADDR4
22	ADDR	ADDR	LANE_ORDER	ADDR1
23	RCTL1	RCTL1	TST3	ADDR2
26	SDA	SDA	TST8	SDA
30	RCTL2	RCTL2	FG1	FG1
34	LSTX	TEST2	TST6	TE
35	LSRX	TEST3	TST7	TE
36	RCTL3	RCTL3	FG2	FG

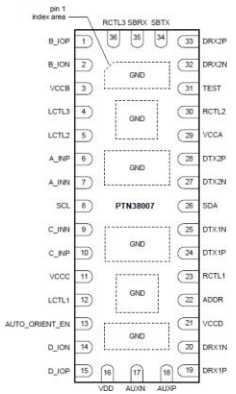
Are they inter-changeable?

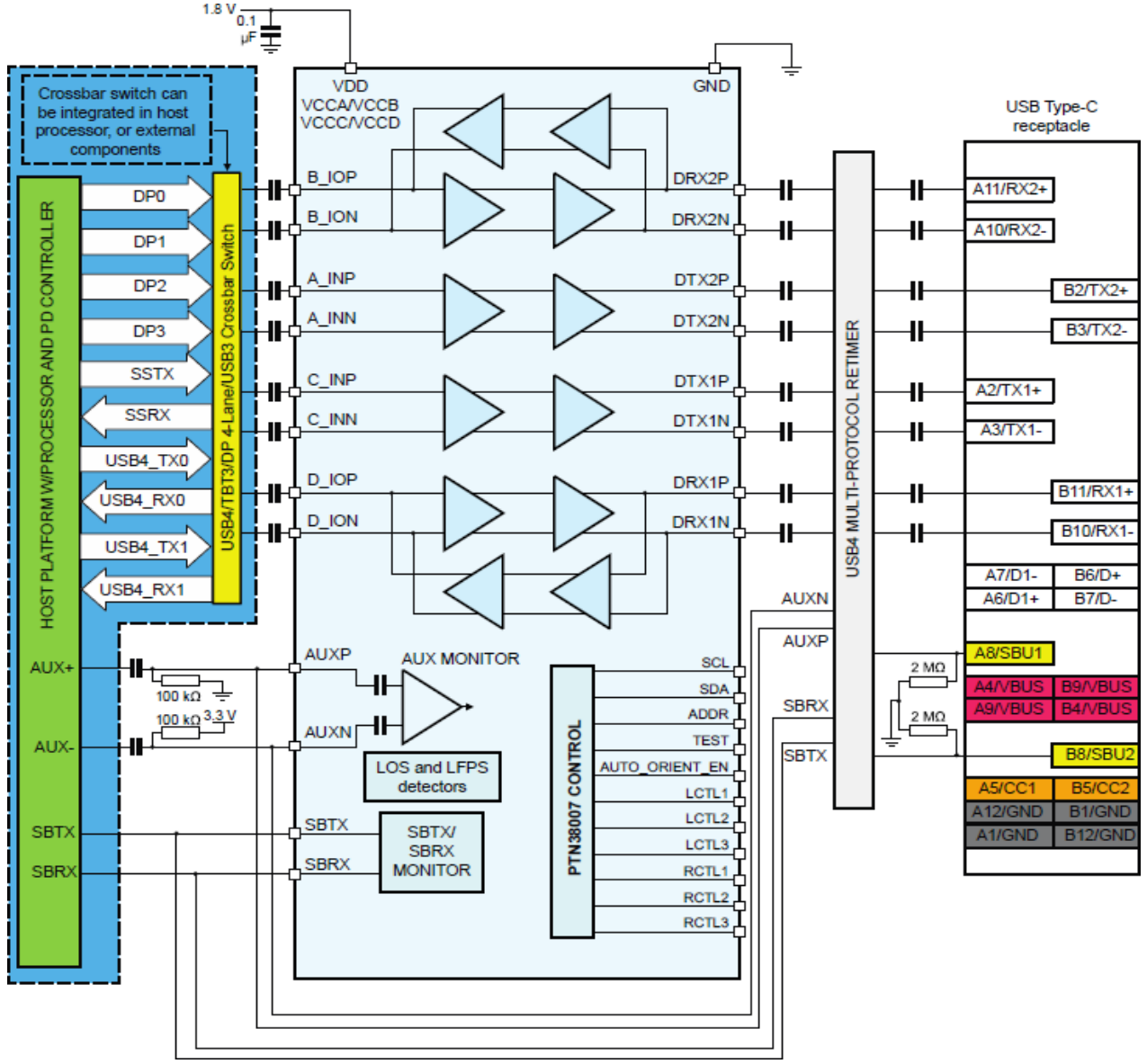
- Can I change PTN38007 to PTN38003A
  - Only if you don't need the TBT3/USB4 functions
- Can I change PTN38003A to PTN38007
  - Yes, but the price will be different ($\$_{PTN38007} > \$_{PTN38003A}$)
- Can I change PTN3816 to PTN38007/PTN38003A
  - Only if you have I2C master to configure PTN38007/PTN38003A. No HPD support.
- Can I change PTN3944 to PTN38007/PTN38003A
  - No. PTN3800x will need to have special programming to enable 4 channels pass through mode. This programming is NXP proprietary, and not for customer to use.
- Can I change PTN3816 to PTN3944
  - Yes, but will lose power management function
- Can I change PTN3944 to PTN3816
  - Yes, pull up HPD pin, no I2C support



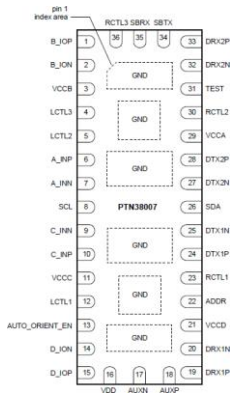
Design Block Diagram Examples

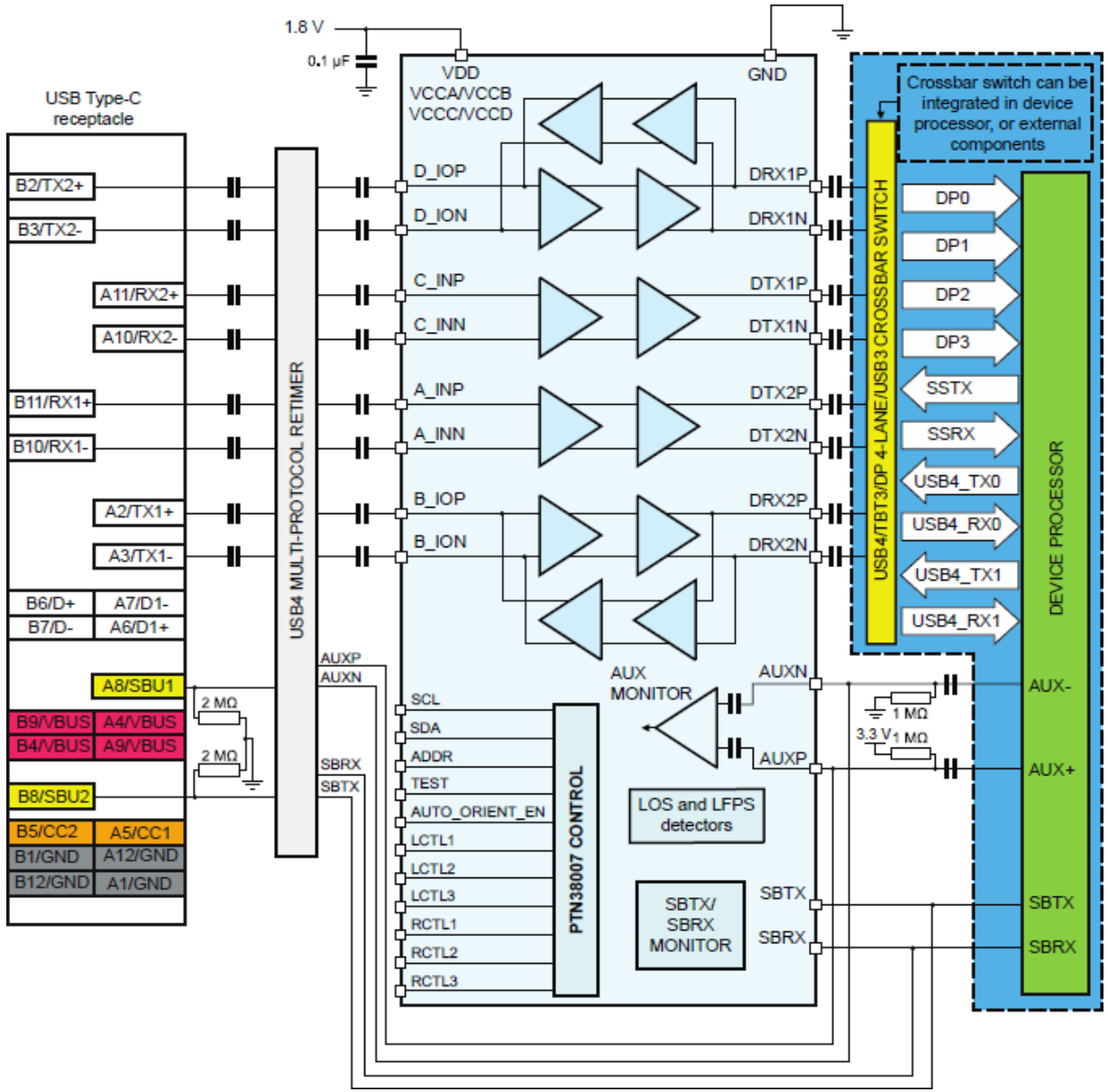
PTN38007/PTN38003A DFP Application





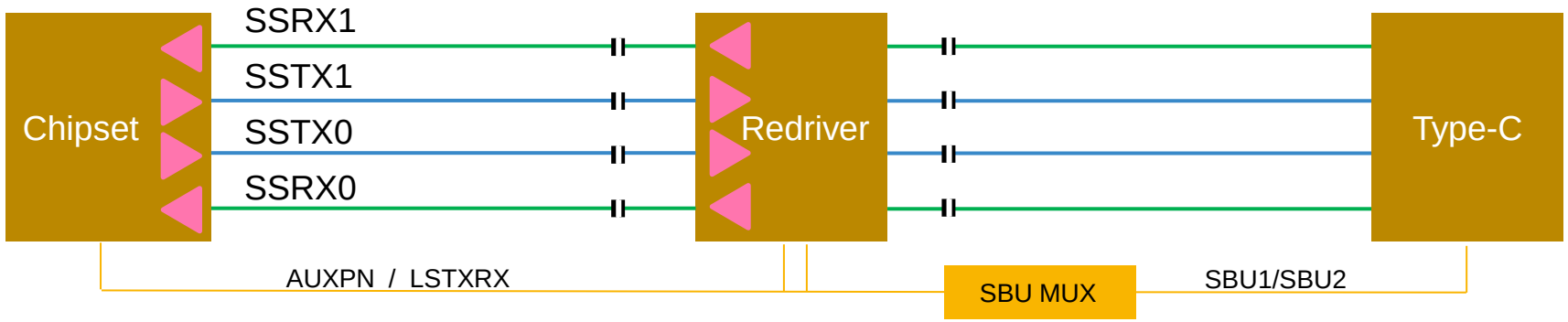
PTN38007/PTN38003A UFP Application



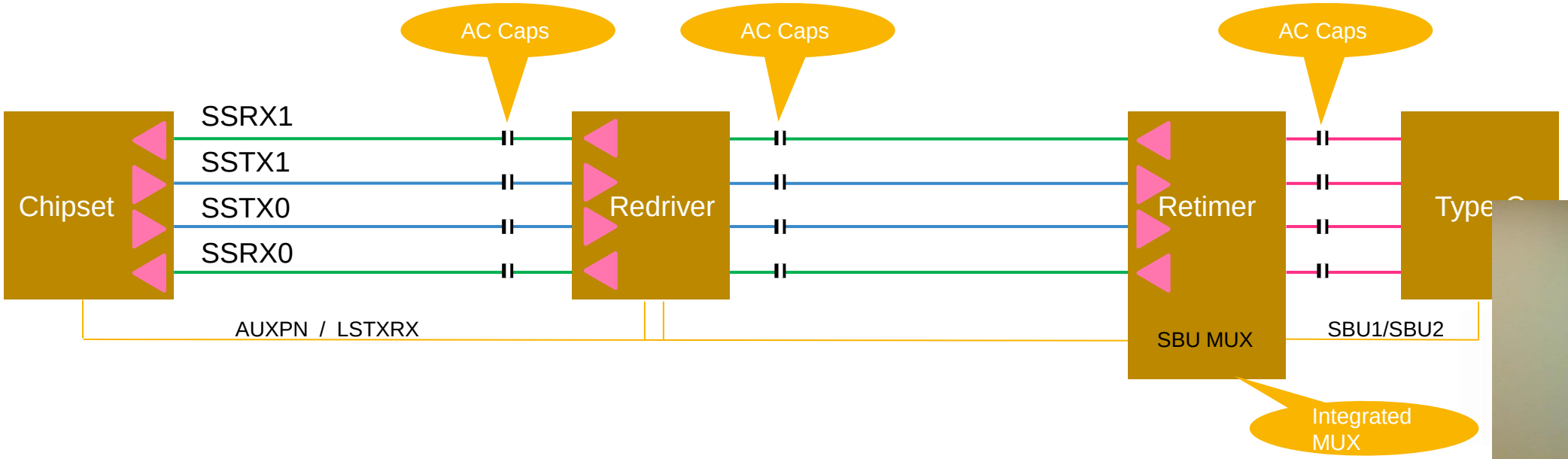


PTN38007/PTN38003A Typical Applications

- Chipset → Redriver → Type-C Connector

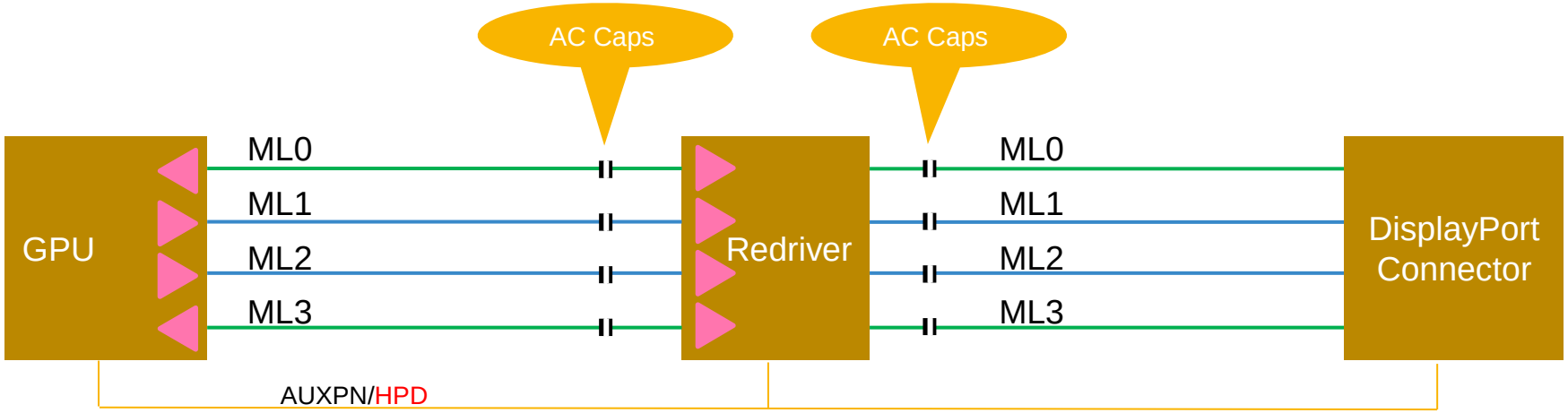


- Chipset → Redriver → Retimer → Type-C Connector

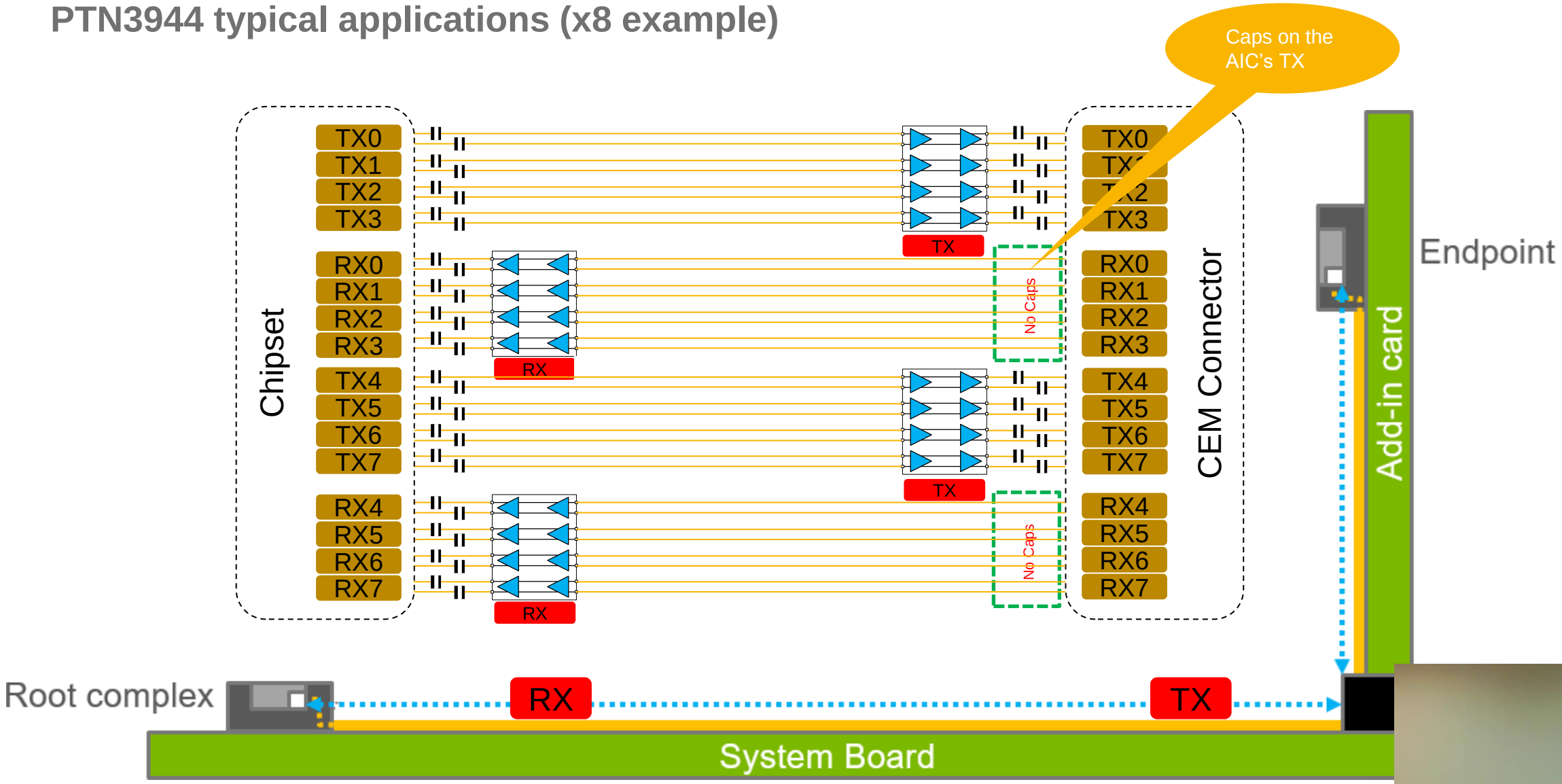


PTN3816 Typical Applications

- GPU → Redriver → DisplayPort Connector (full size or miniDP)

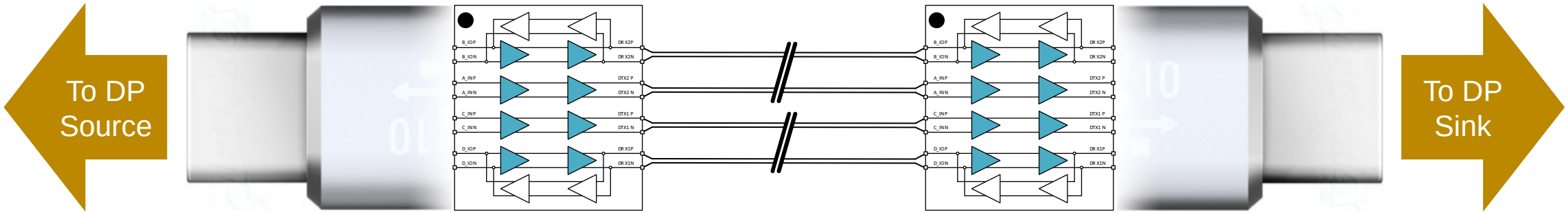


PTN3944 typical applications (x8 example)



Using PTN38007/PTN38003A on an Active Cable Design

- PTN38007 or PTN38003A redriver has 2 out of 4 paths that are unidirectional. Placement of these redrivers need to be aligned with DisplayPort signal flow. Plugs to source side and sink side are not reversible.



- Other consideration:
  - Need 1.8V power for redriver. Need a buck converter to convert from VCONN (5V) to 1.8V
  - Need to have I2C master to configure the redriver (usually an e-marker can work just fine)
  - If bi-directional cable is required, more components (such as muxes) needs to be added to design

Programming Overview

Programming PTN38007/PTN38003A

- PTN38007/PTN38003A require I2C programming to configure to different operating modes. When POR, the chip is in deep power saving state (non-working state).
  - Operating mode can't be changed via GPIO strapping options.
- PTN3944 programming is optional
  - EQ/FG settings can be done through GPIO strapping options or I2C.
- Who should be programming redriver's registers?
  - Usually, a PD controller has I2C bus to control redriver/retimer
  - If there is no PD controller, then an EC (embedded controller) can program redriver/retimer
- When does redriver need to be programmed?
  - (1) Power up initialization (to setup EQ/FG @ different operating mode)
  - (2) Entering different operating modes (DPS, USB3.2, DisplayPort Alternate Mode, Thunderbolt3 Mode, USB4 Mode), with respective orientation

Power-on initialization

```
// PTN38007 Initialization for Safe State
// USB3 Initialization
Reg[0x0f] = 0x00              // Enable LOS Detector
Reg[0x10] = 0x0e              // Downstream RCTL[2:1] = 10dB, should adapt to different PCB design if necessary
Reg[0x12] = 0x0e              // Upstream   LCTL[2:1] = 10dB, should adapt to different PCB design if necessary
Reg[0x11] = 0x03              // Upstream   RCTL[3] = 950mVppd, should adapt to different PCB design if necessary
Reg[0x13] = 0x03              // Downstream LCTL[3] = 950mVppd, should adapt to different PCB design if necessary
//Reg[0x0f] = 0x00 0x0e 0x03 0x0e 0x03
// DisplayPort Initialization
Reg[0x07] = 0x0e              // Lane 0 LCTL[2:1] = 8.3dB, should adapt to different PCB design if necessary
Reg[0x09] = 0x0e              // Lane 1 LCTL[2:1] = 8.3dB, should adapt to different PCB design if necessary
Reg[0x0b] = 0x0e              // Lane 2 LCTL[2:1] = 8.3dB, should adapt to different PCB design if necessary
Reg[0x0d] = 0x0e              // Lane 3 LCTL[2:1] = 8.3dB, should adapt to different PCB design if necessary
Reg[0x08] = 0x03              // Lane 0 LCTL[3] = 950mVppd, should adapt to different PCB design if necessary
Reg[0x0a] = 0x03              // Lane 1 LCTL[3] = 950mVppd, should adapt to different PCB design if necessary
Reg[0x0c] = 0x03              // Lane 2 LCTL[3] = 950mVppd, should adapt to different PCB design if necessary
Reg[0x0e] = 0x03              // Lane 3 LCTL[3] = 950mVppd, should adapt to different PCB design if necessary
//Reg[0x07] = 0x0e 0x03 0x0e 0x03 0x0e 0x03 0x0e 0x03
// Thunderbolt Initialization
Reg[0x15] = 0x09              // Downstream RCTL[2:1] = 12.7dB, should adapt to different PCB design if necessary
Reg[0x17] = 0x09              // Upstream   LCTL[2:1] = 12.7dB, should adapt to different PCB design if necessary
Reg[0x16] = 0x03              // Upstream   RCTL[3] = 950mVppd, should adapt to different PCB design if necessary
Reg[0x18] = 0x03              // Downstream LCTL[3] = 950mVppd, should adapt to different PCB design if necessary
//Reg[0x15] = 0x09 0x03 0x09 0x03
// DFP SafeState Initialization
Reg[0x04] = 0x00              // Default Safe State, With Normal Orientation
```

Used for PCIe programming

Consolidate:

```
Reg[0x07] =
 0x0e 0x03 0x0e 0x03
 0x0e 0x03 0x0e 0x03
 0x00 0x0e 0x03 0x0e
 0x03 0x00 0x09 0x03
 0x09 0x03
```

Reg[0x14] = Read Only Status

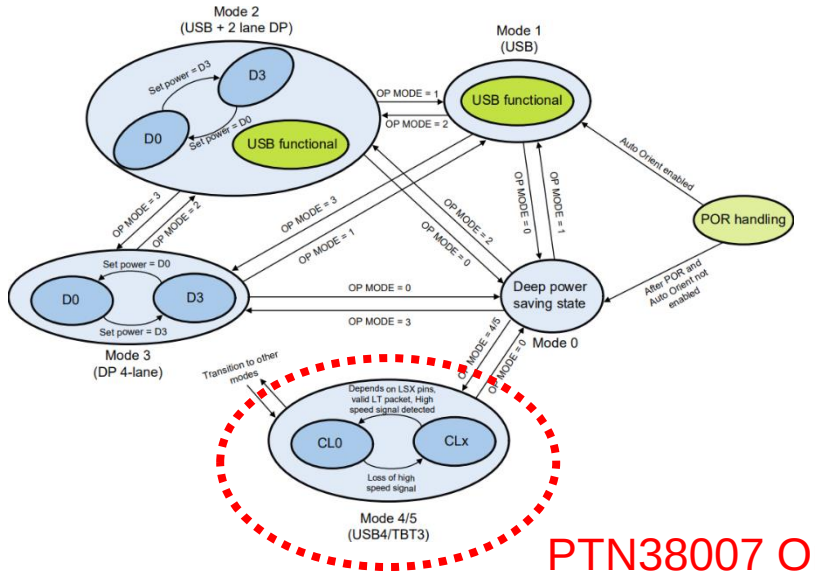
Operating Mode Programming

- DFP

Orientation / DFP Modes	Normal	Reversed
Safe State (Mode = 0)	Reg[0x04] = 0x00	Reg[0x04] = 0x10
USB3 Only (Mode = 1)	Reg[0x04] = 0x01	Reg[0x04] = 0x11
USB3+DP2Lane (Mode = 2)	Reg[0x04] = 0x02	Reg[0x04] = 0x12
DP4Lane (Mode = 3)	Reg[0x04] = 0x03	Reg[0x04] = 0x13
Thunderbolt (Mode = 4)	Reg[0x04] = 0x04	Reg[0x04] = 0x14
USB4 (Mode = 5)	Reg[0x04] = 0x05	Reg[0x04] = 0x15

- UFP

Orientation / DFP Modes	Normal	Reversed
Safe State (Mode = 0)	Reg[0x04] = 0x20	Reg[0x04] = 0x30
USB3 Only (Mode = 1)	Reg[0x04] = 0x21	Reg[0x04] = 0x31
USB3+DP2Lane (Mode = 2)	Reg[0x04] = 0x22	Reg[0x04] = 0x32
DP4Lane (Mode = 3)	Reg[0x04] = 0x23	Reg[0x04] = 0x33
Thunderbolt (Mode = 4)	Reg[0x04] = 0x24	Reg[0x04] = 0x34
USB4 (Mode = 5)	Reg[0x04] = 0x25	Reg[0x04] = 0x35



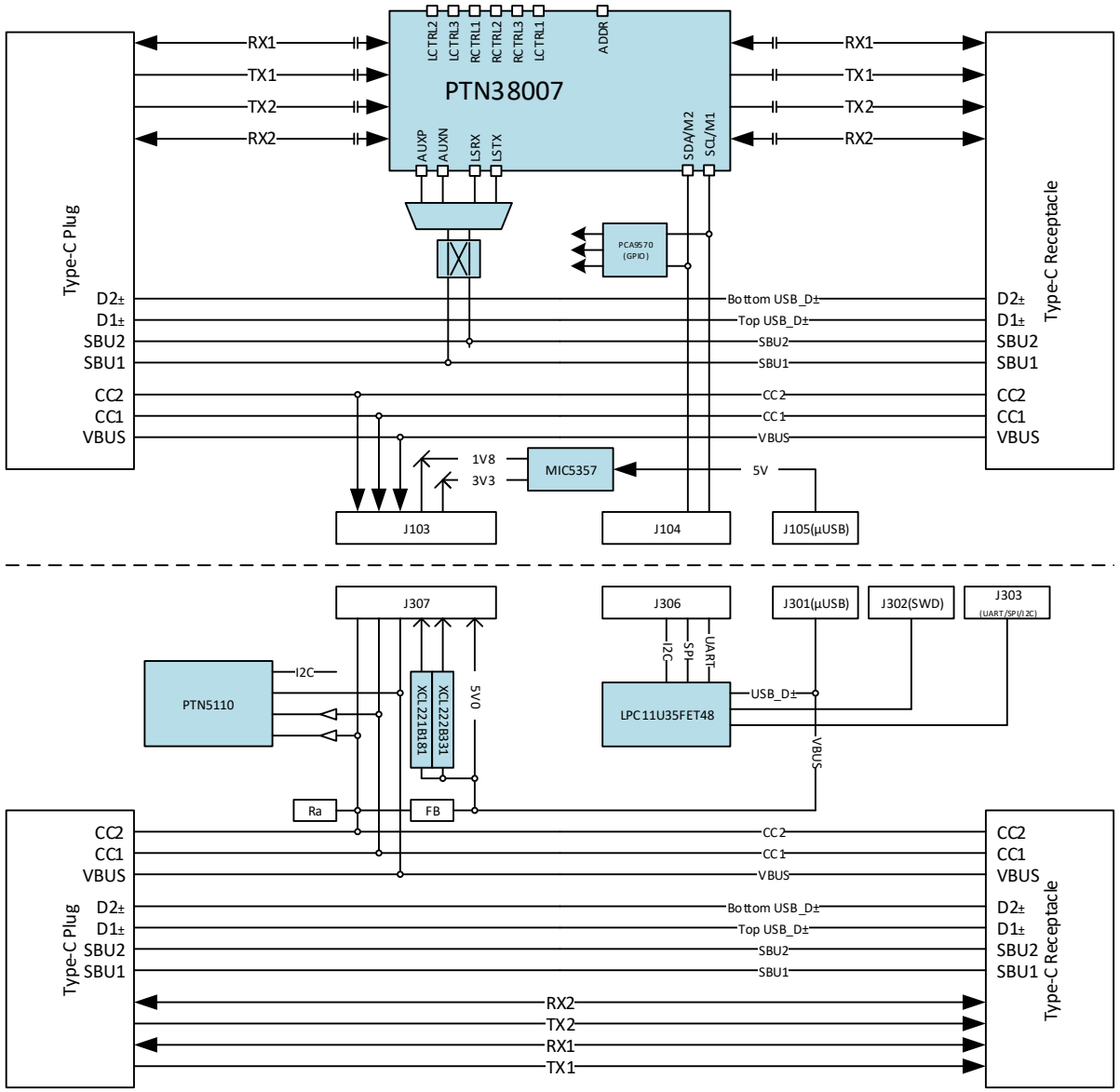
PTN38007 Only

EVM Overview

NXP Linear Re-driver EVMs

Product	EVM Types	I2C Interface Adapter	Evaluation Location	Interface Connector/Cable
PTN38007 PTN38003A	DFP (H2) Board	LPC11U35 Baseboard	Host Side (notebook ports)	Type-C Plug to Receptacle
	UFP (D2) Board	LPC11U35 Baseboard	Device/Dock Side (device/dock ports)	Type-C Plug to Receptacle
PTN3944	PCIe Add-In-Card	LPC11U35 Baseboard	PCIe Slots between motherboard and add-in-card	PCIe gold fingers/CEM connector
PTN3816	DP Adapter		Between DP source & sink	Full Size DisplayPorts

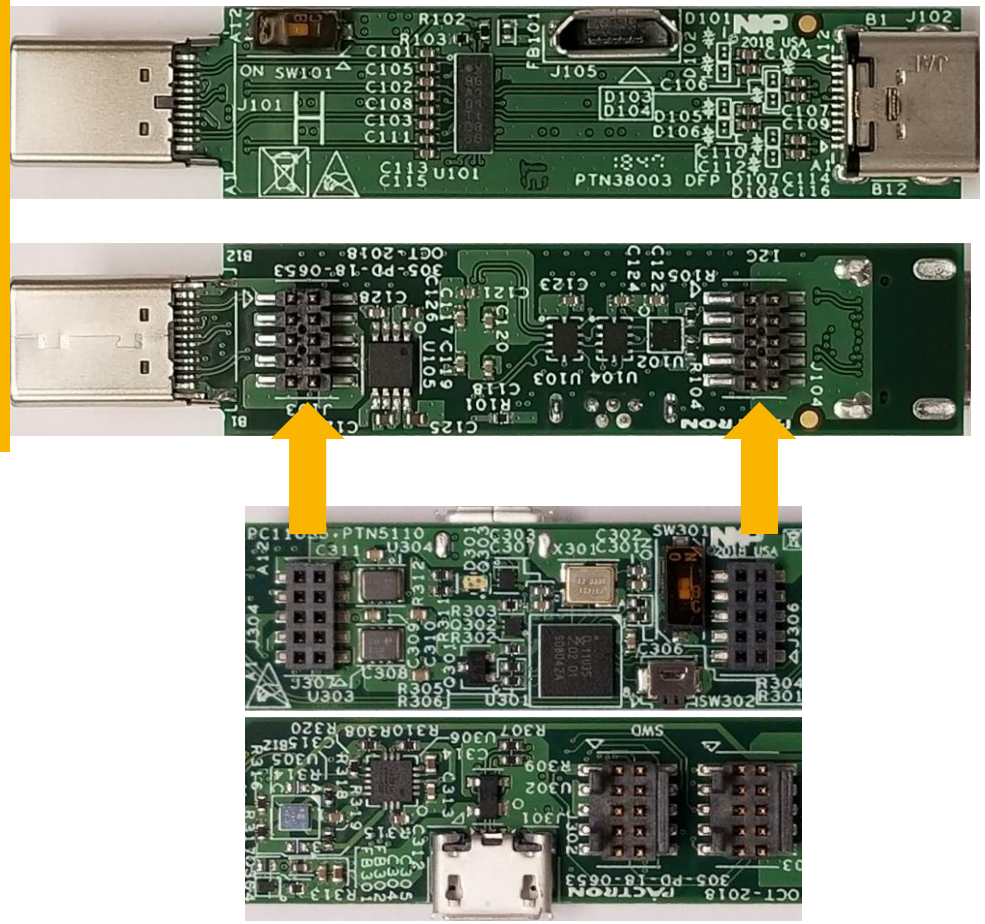
PTN38007/PTN38003A EVM Block Diagram



PTN38007/PTN38003A EVMs

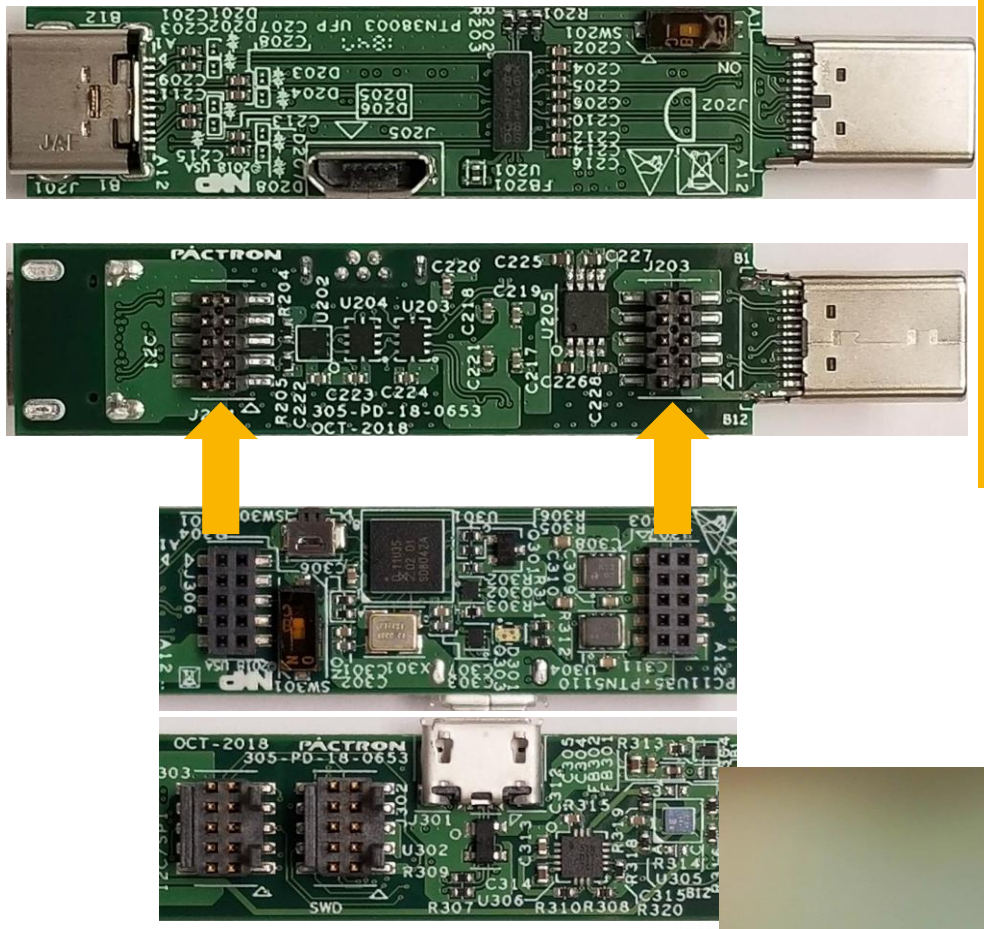
- H2 Board (DFP)

Host PC



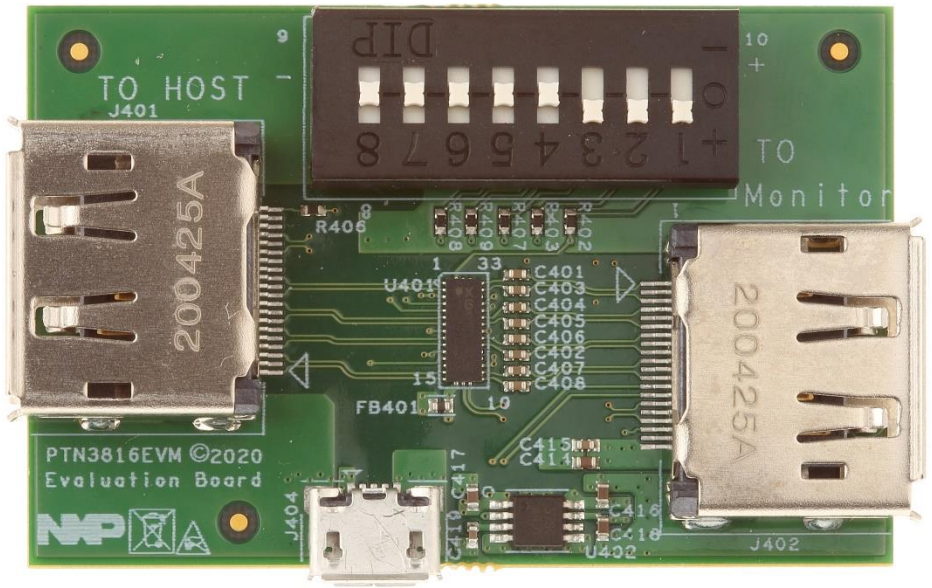
- D2 Board (UFP)

Device/Dock/Monitor



PTN3816 EVM

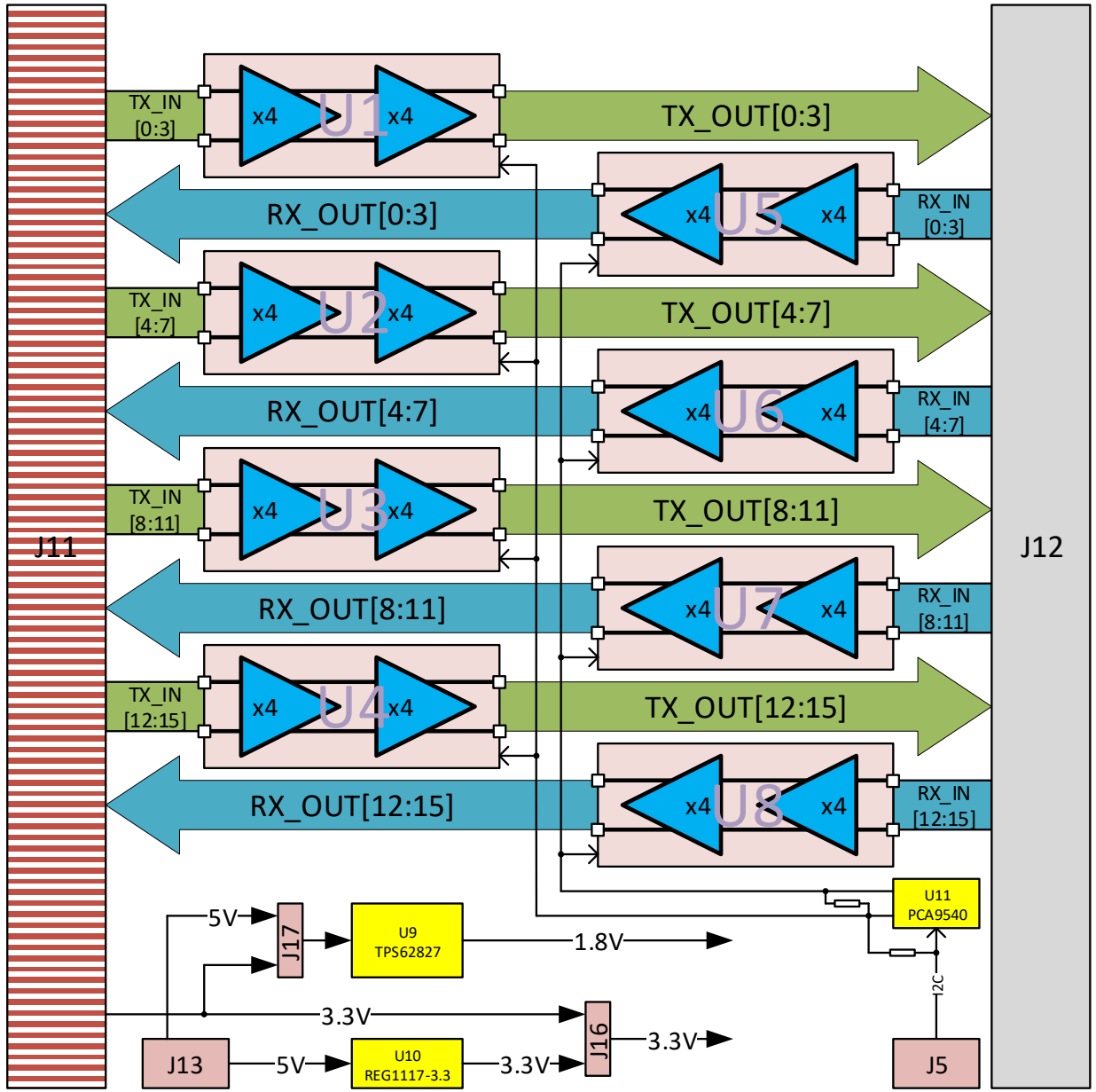
From Host's DP Output



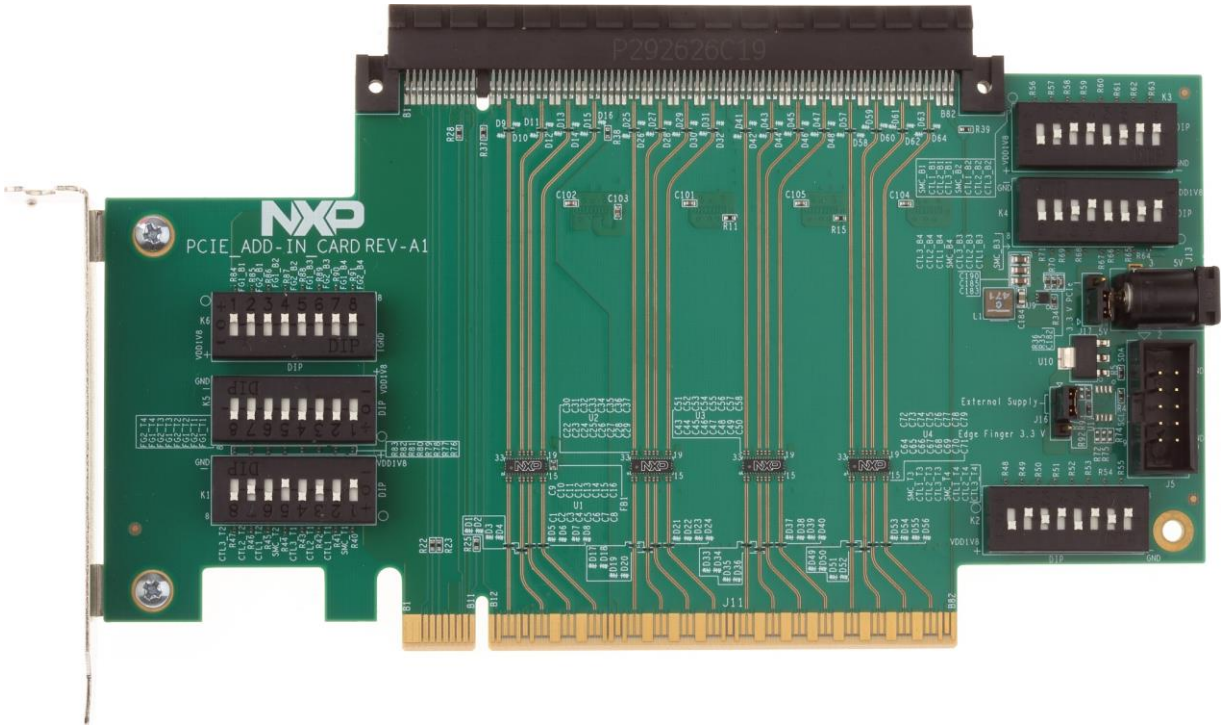
To DP Monitor

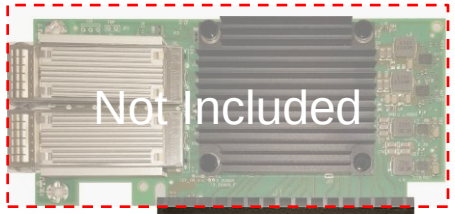
5V

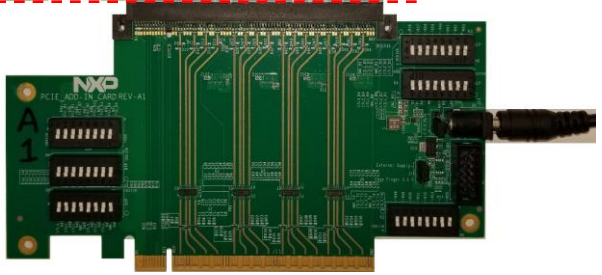
PTN3944 EVM Block Diagram

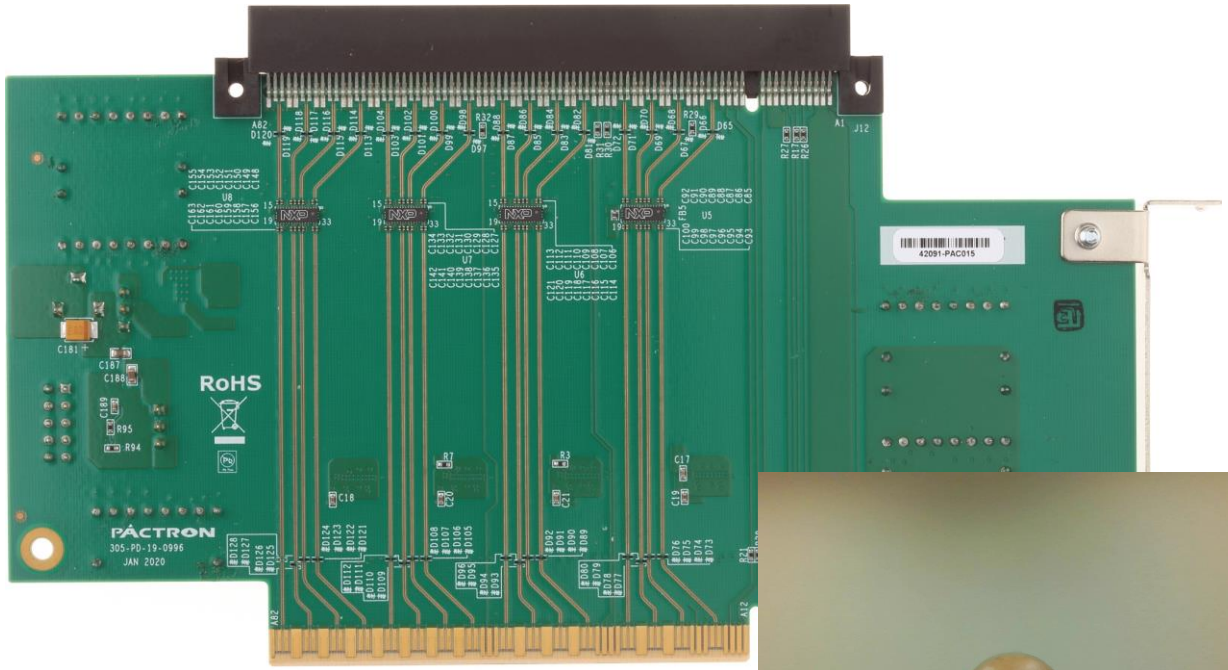


PTN3944 EVM


PCIE_ADD-IN_CARD REV-A1


Not Included




RoHS
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305-PD-19-0996
JAN 2020

EVM – Website link

PTN38003A
https://www.nxp.com/products/interfaces/signal-conditioners/type-c-usb-3-2-and-displayport-v-1-4-combination-linear-redriver:PTN38003A?tab=Design_Tools_Tab
PTN38007
https://www.nxp.com/products/interfaces/signal-conditioners/multiprotocol-usb-4-20-gbps-linear-redriver:PTN38007?tab=Design_Tools_Tab
PTN3816
https://www.nxp.com/products/interfaces/signal-conditioners/20-gbps-per-lane-4-lane-displayport-linear-redriver:PTN3816?tab=Design_Tools_Tab
PTN3944
https://www.nxp.com/products/interfaces/signal-conditioners/multi-channel-pcie-gen-4-linear-equalizer:PTN3944?tab=Design_Tools_Tab

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