PMSM FOC WITH INTERLEAVED BOOST PFC ON SINGLE CHIP

NXP SE Team

MAY 2022

SECURE CONNECTIONS FOR A SMARTER WORLD

AGENDA

- Introduction
- System Timing and Key Configurations
- PMSM FOC Scheme
- Interleaved Boost PFC Converter Scheme
- Test Results
- Development Tools
- Summary
- Q & A

Introduction

SECURE CONNECTIONS
FOR A SMARTER WORLD

SYSTEM FEATURES

- Interleaved PFC and one PMSM control implemented on HVP-56F83783(daughter card) and HVP-MC3PH(power stage) – Single control chip solution.
  - ✓ Sensorless PMSM FOC with 16 kHz PWM and control frequency
  - ✓ Interleaved 2-phase boost PFC with 32 kHz control frequency and 96 kHz PWM frequency
  - ✓ Remote SCI control through FreeMaster
  - ✓ Software and hardware protections including OCP/OVP/UVP/OFP/UFP
- Input voltage 85–265 VAC, 47–63 Hz.
- Multiple optimization strategies to improve PF and THDI.
- Peak efficiency of the PFC stage above 96% under high line input.
- Power factor above 0.99 over a wide range of the loading.

HARDWARE SETUP

HVP-56F83783

UART
- USB bridge

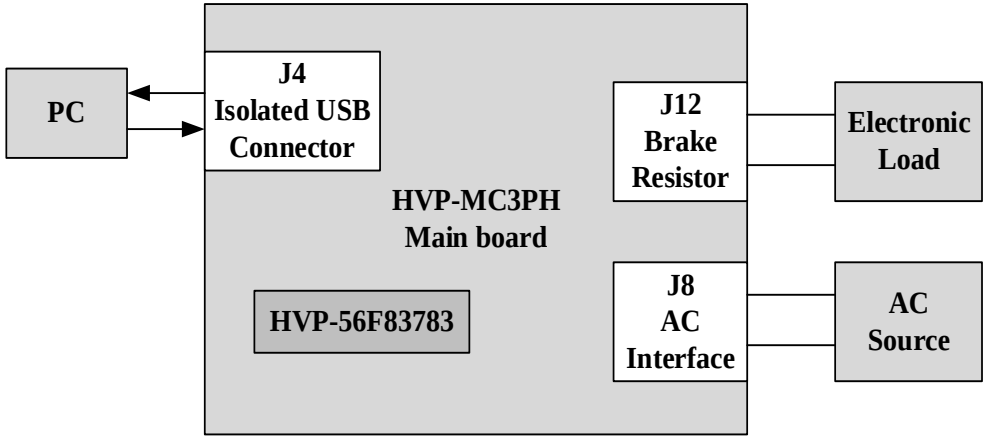
HVP system

www.nxp.com/hvp

AC input connector

Brake resistor connector

3ph motor connector

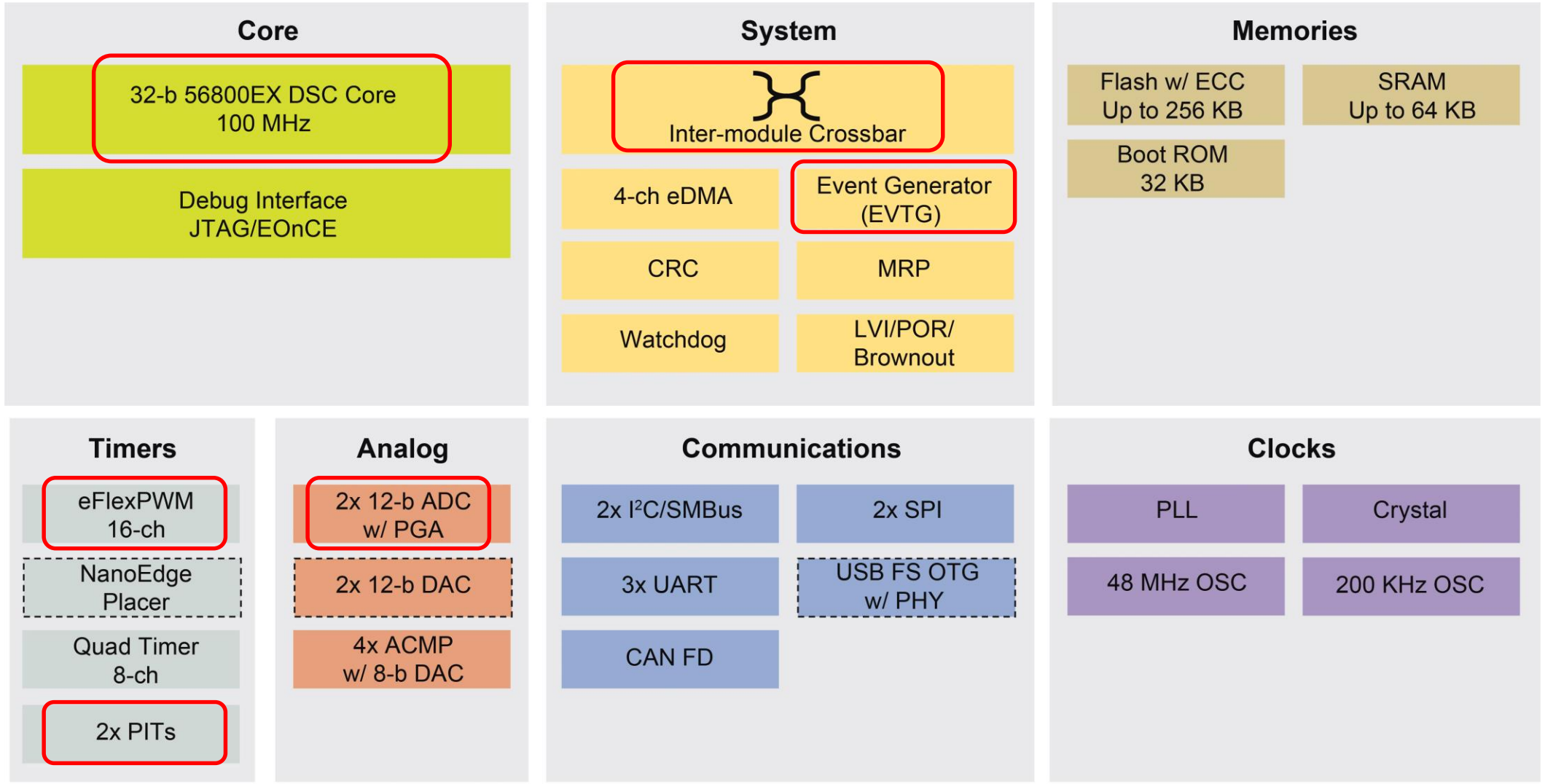


Hardware setup

ITEM	PARAMETER
Input voltage	85–265 VAC, 47–63 Hz
Output voltage	400V
Output power	800/400W
phase	2

Boost PFC specifications

DSC 56F83783 FEATURES



System Timing and Key Configurations

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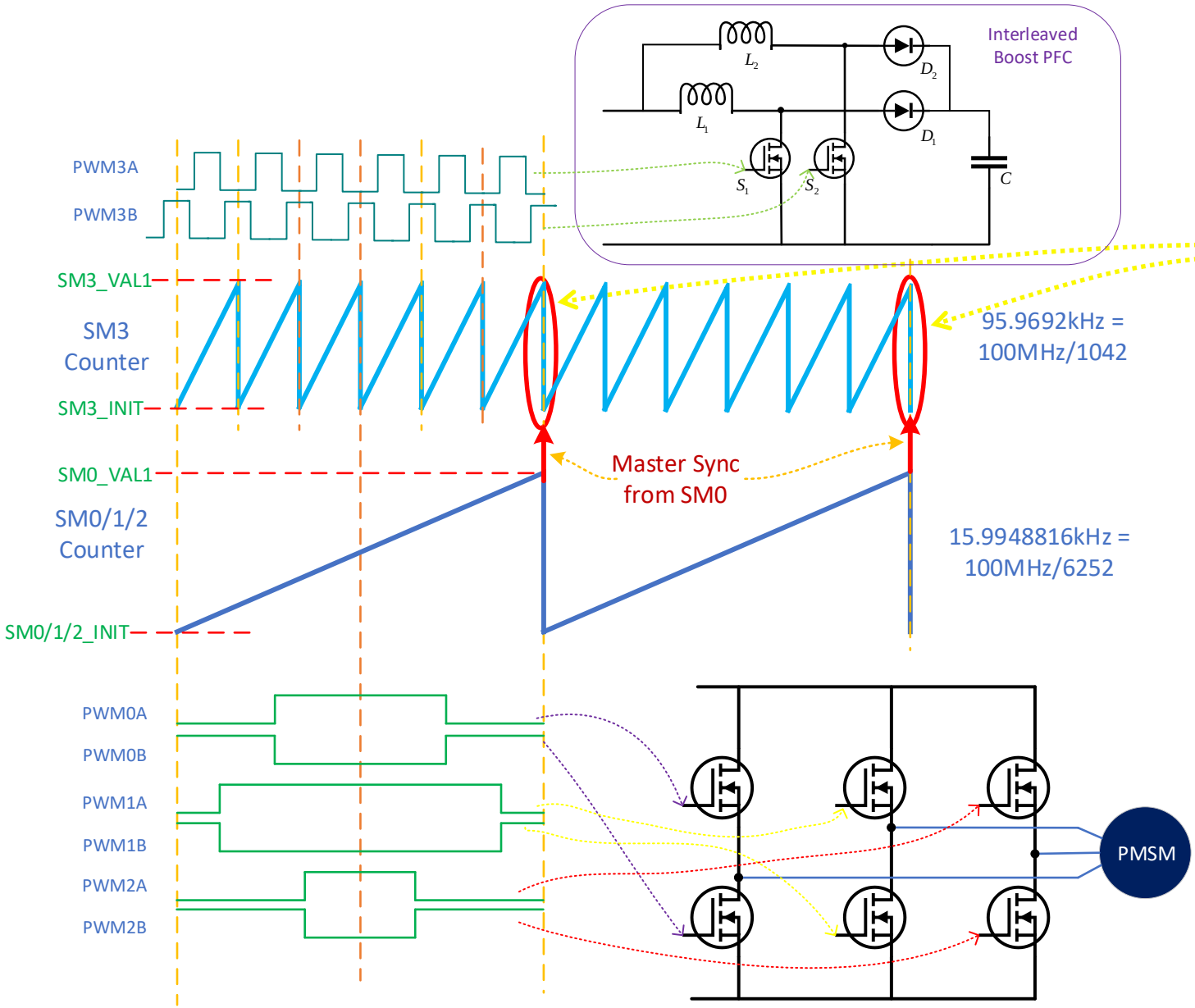
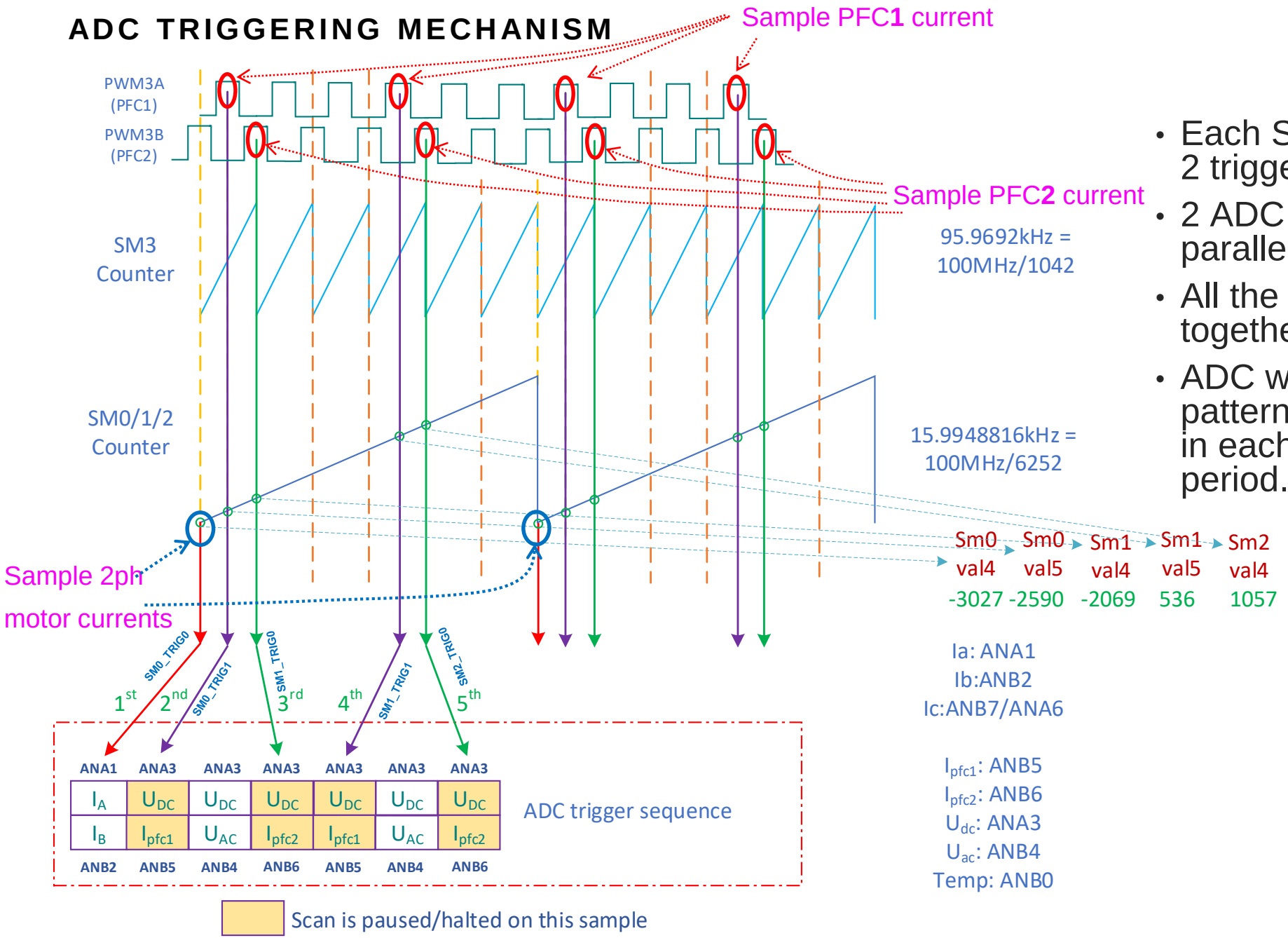
PWM SYNCHRONIZATION BETWEEN PFC AND MOTOR



SM3 counter is forced to INIT value by master sync signal from SM0.

- One eFlexPWM module has 4 sub-modules(SM0~3), each SM has an independent counter and 2 PWM outputs(PWMnA & PWMnB).
- SM3 outputs are used to control PFC.
- SM0~2 outputs are used to control motor.

ADC TRIGGERING MECHANISM

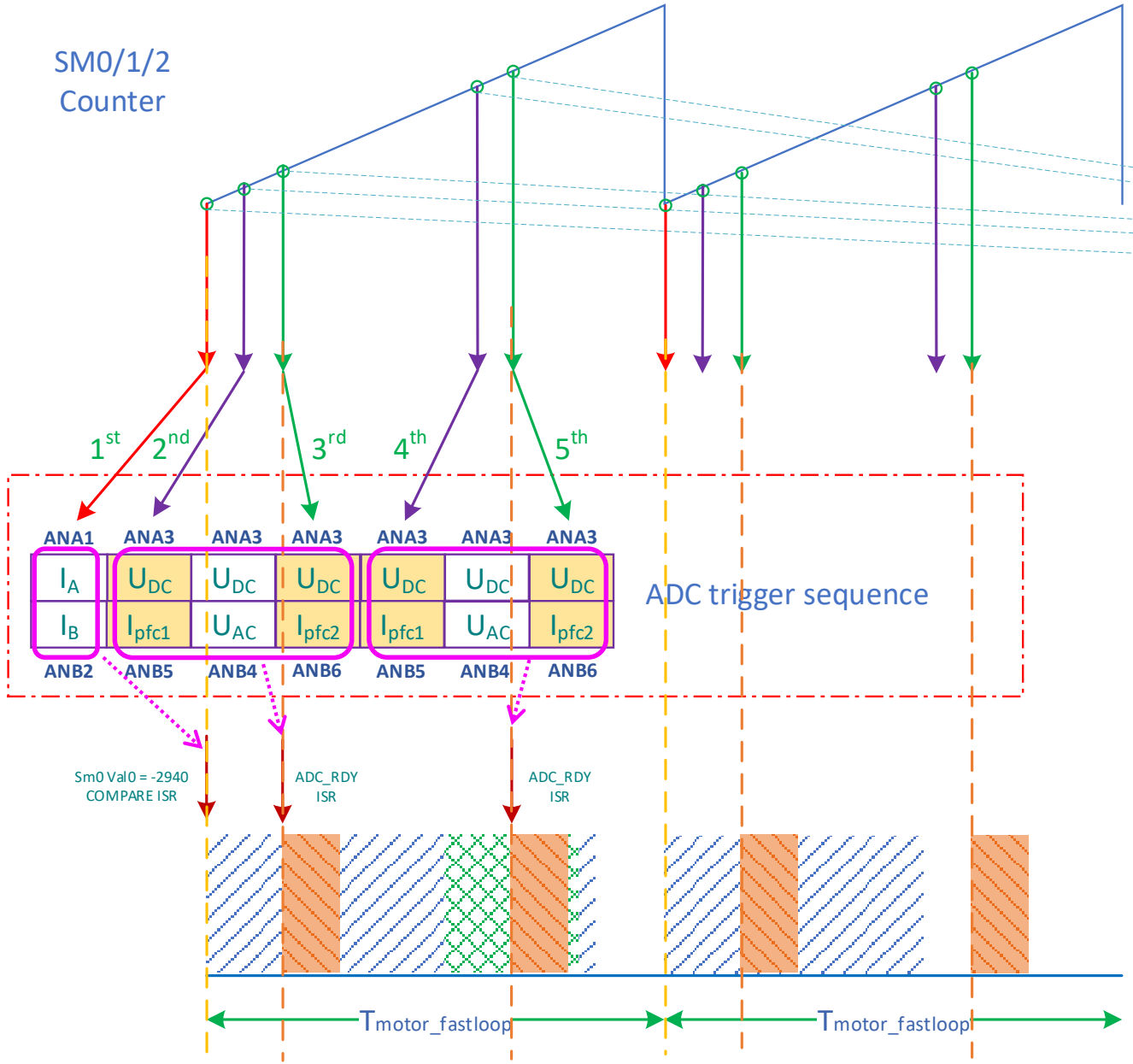


- Each SM is capable of generating 2 trigger signals.
- 2 ADC modules can work in parallel.
- All the trigger signals are OR'ed together to ADC.
- ADC works under a sequence pattern. This pattern is repeated in each motor control PWM period.

Ia: ANA1
Ib:ANB2
Ic:ANB7/ANA6

I_{pfc1}: ANB5
I_{pfc2}: ANB6
U_{dc}: ANA3
U_{ac}: ANB4
Temp: ANB0

MOTOR CONTROL FAST LOOP AND PFC CURRENT LOOPS ARRANGEMENT



PFC fast loop – priority 2(highest)

PFC slow loop – priority 1

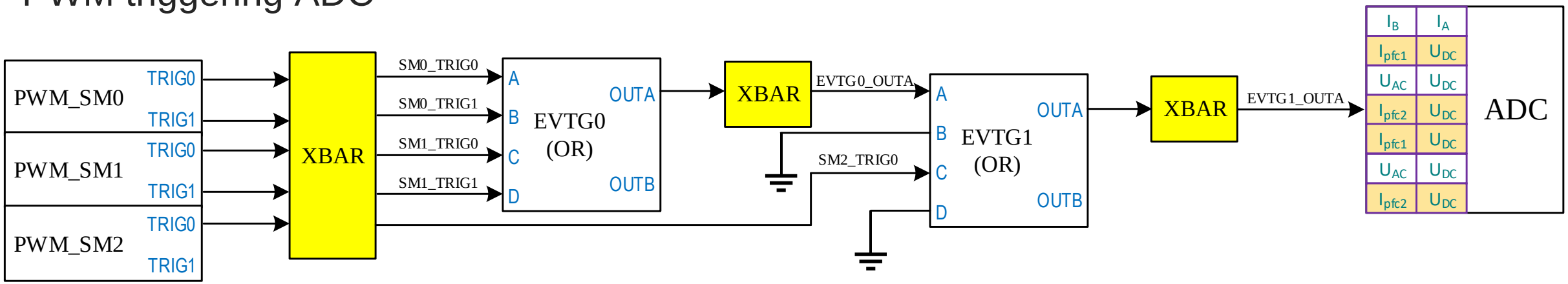
Motor control fast loop – priority 0 (lowest)

Scan is paused/halted on this sample

PWM AND CONTROL FREQUENCY

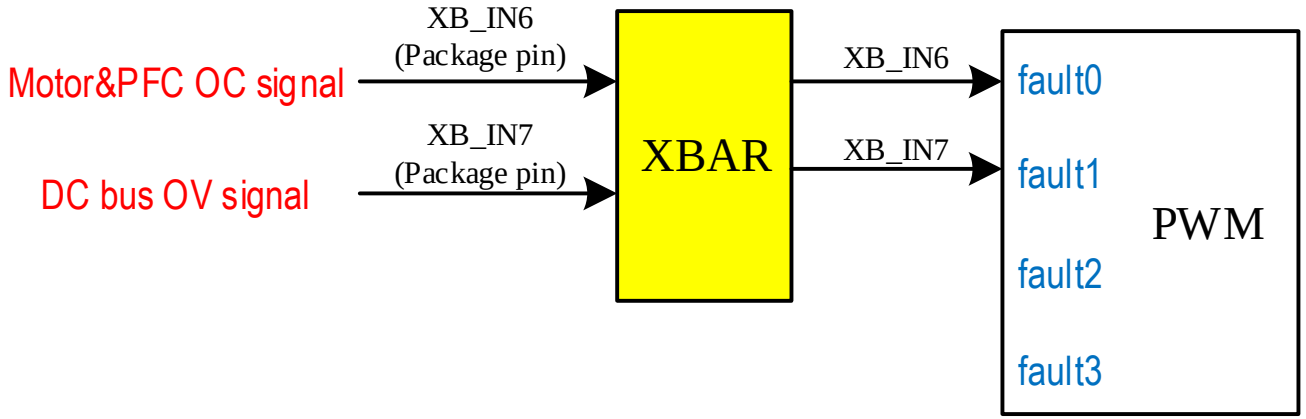
Item	Interrupt Function	Priority	Frequency
PFC power switch			96kHz
PFC fast loop	ADC_A_IRQHANDLER	Priority 2 (highest)	32kHz
PFC slow loop	PIT0_IRQHANDLER	Priority 1	10kHz
Motor control PWM			16kHz
Motor control loop	PWMA_COMPARE_0_IRQHANDLER	Priority 0 (lowest)	16kHz

- PWM triggering ADC



ADC_TRIG = SM0_TRIG0|SM0_TRIG1|SM1_TRIG0|SM1_TRIG1|SM2_TRIG0

- OC and OV signals disabling PWM outputs



PROTECTIONS

- **Hardware protection**
  - PFC/MOTOR current
  - DC bus voltage

- **Software protection**
  - DC bus voltage(over voltage / under voltage)
  - PFC/MOTOR current
  - Grid voltage (over voltage / under voltage)
  - Grid frequency (over frequency / under frequency)

PMSM FOC Scheme

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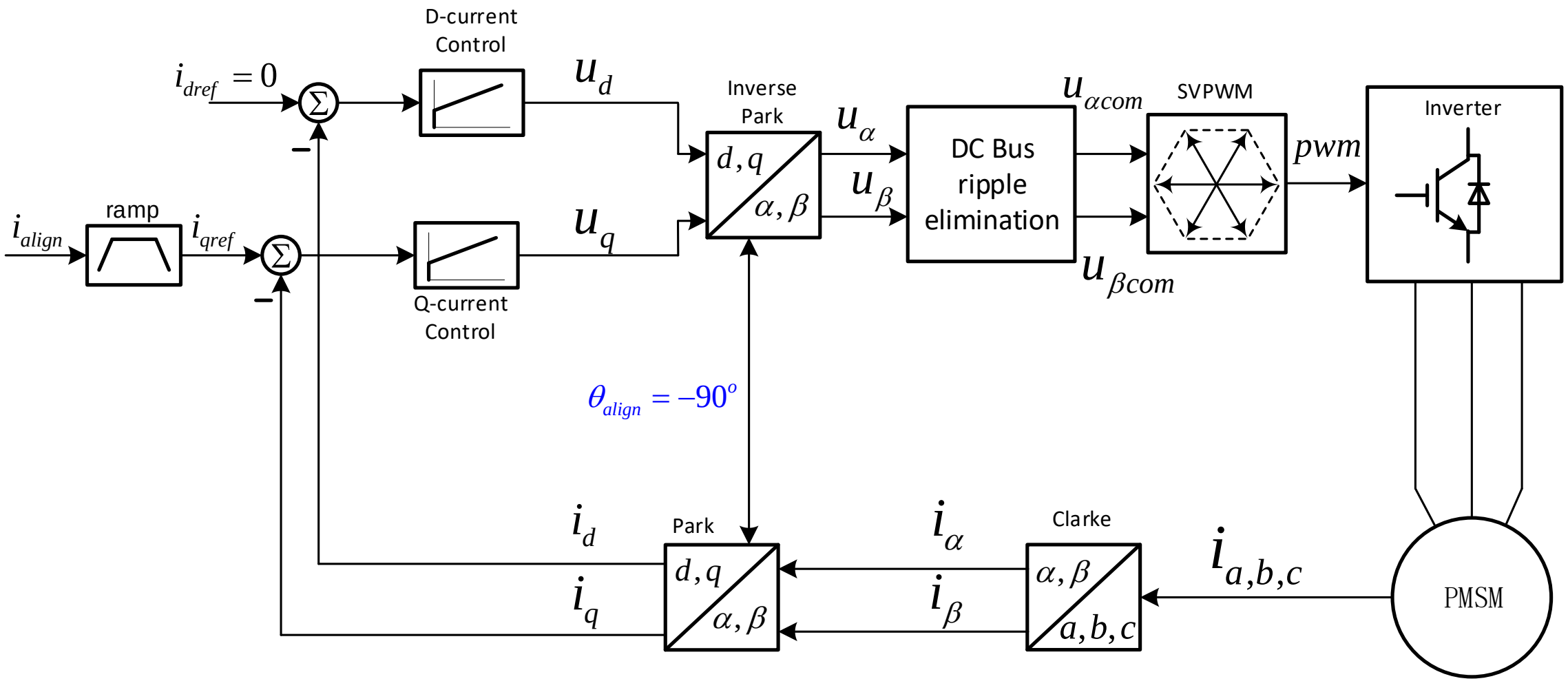
PMSM SENSORLESS FOC

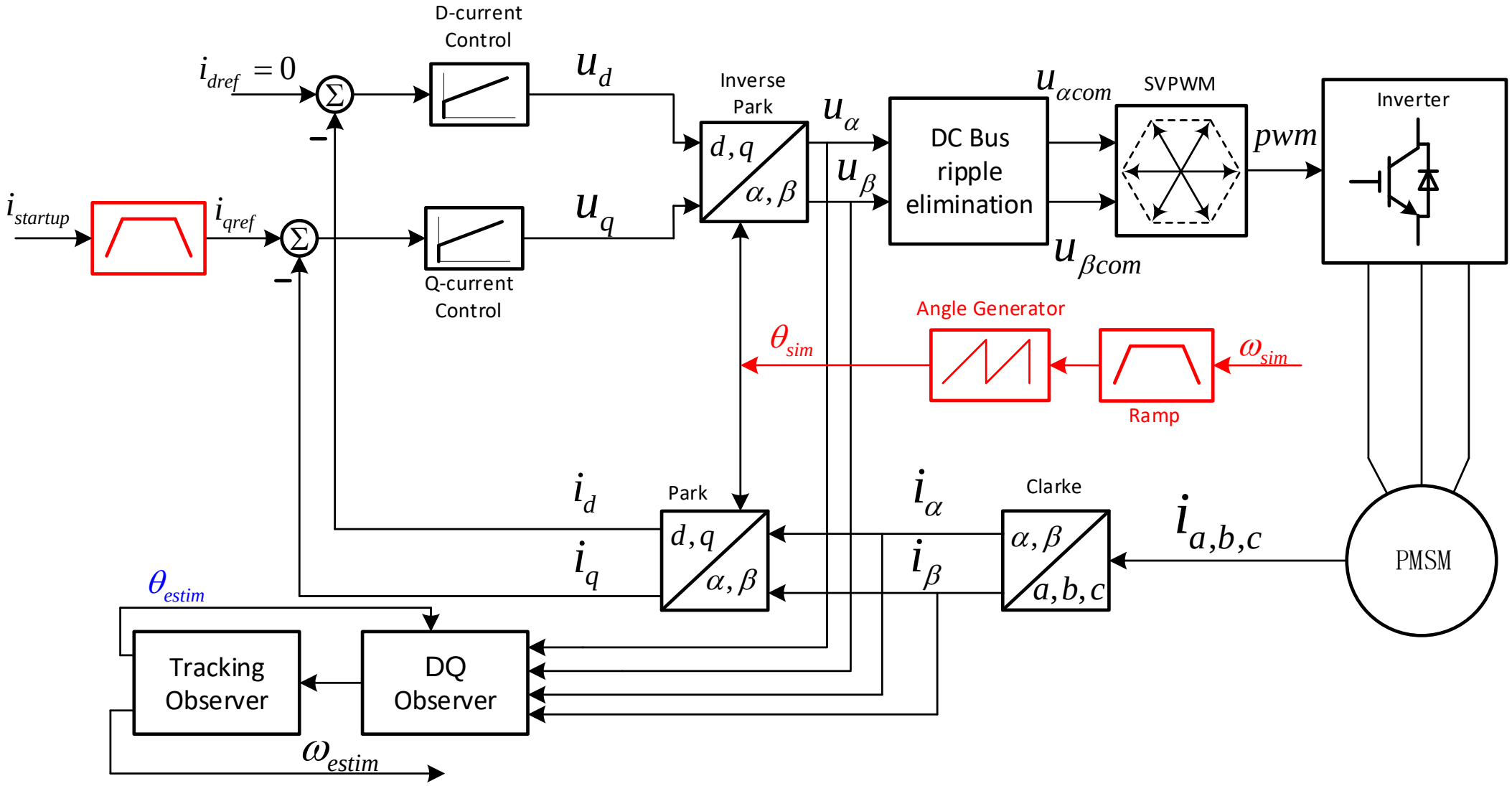
- It needs four major stages to run the motor:
  - Alignment
  - Speed open-loop startup
  - Position merge
  - Speed closed-loop spin

- Most FOC components and the observer are from RTCESL (Real Time Control Embedded Software Library) is used for rotor position estimation. More RTCESL information: www.nxp.com/rtcesl

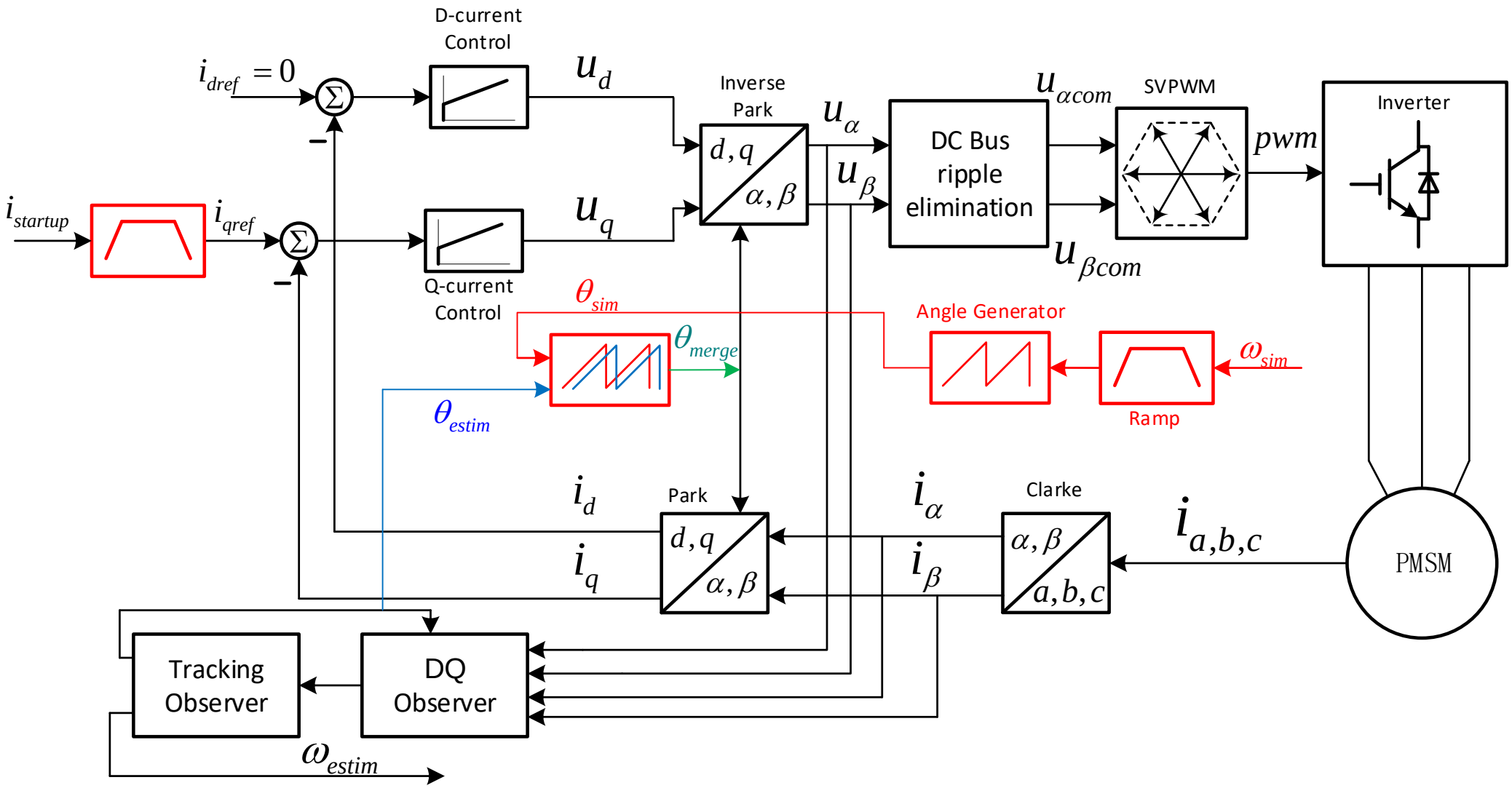
ALIGNMENT


D-current
Control
$i_{dref} = 0$
u_d
Inverse
Park
u_α
u_β
DC Bus
ripple
elimination
$u_{\alpha com}$
$u_{\beta com}$
SVPWM
pwm
Inverter
ramp
i_{align}
i_{qref}
u_q
Q-current
Control
$\theta_{align} = -90^o$
i_d
i_q
Park
i_α
i_β
Clarke
$i_{a,b,c}$
PMSM

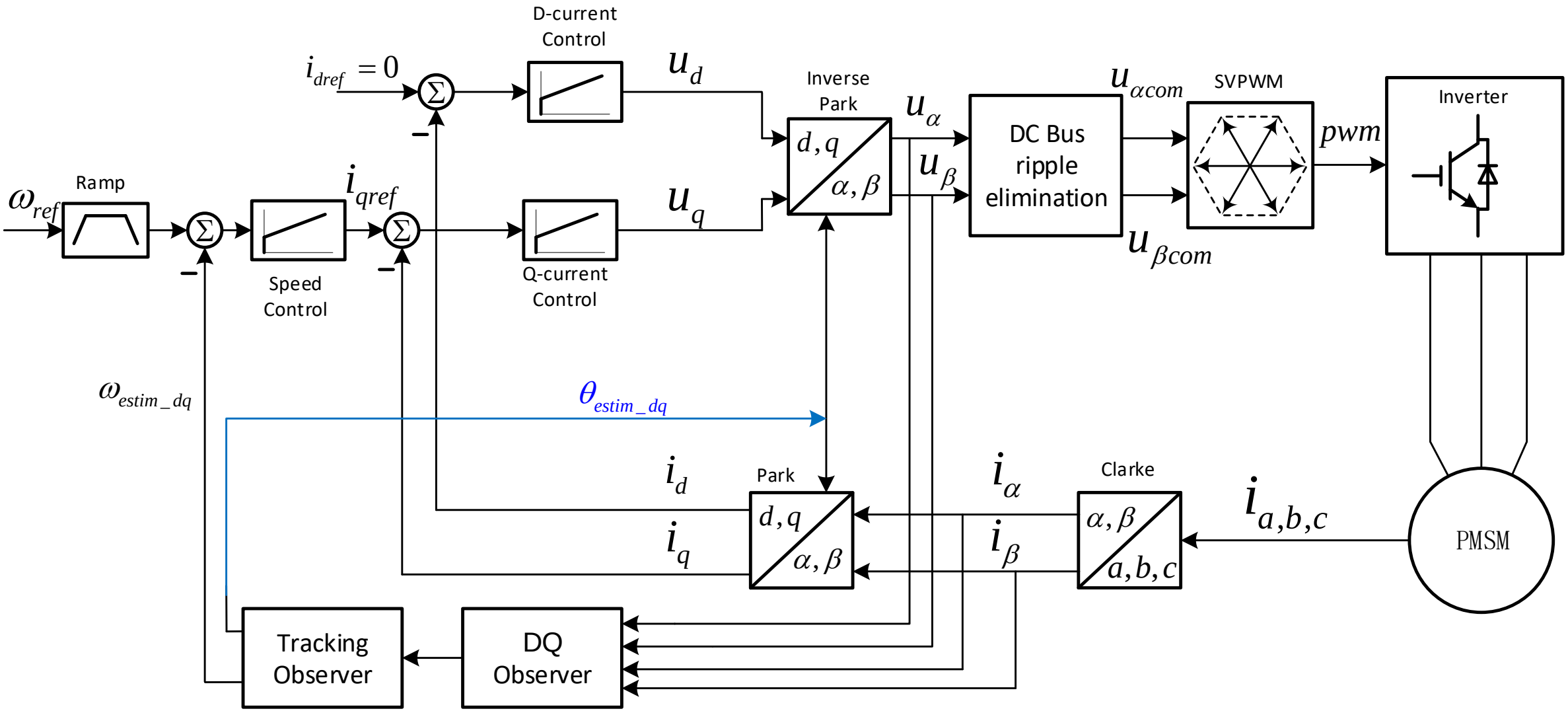
OPEN-LOOP STARTUP



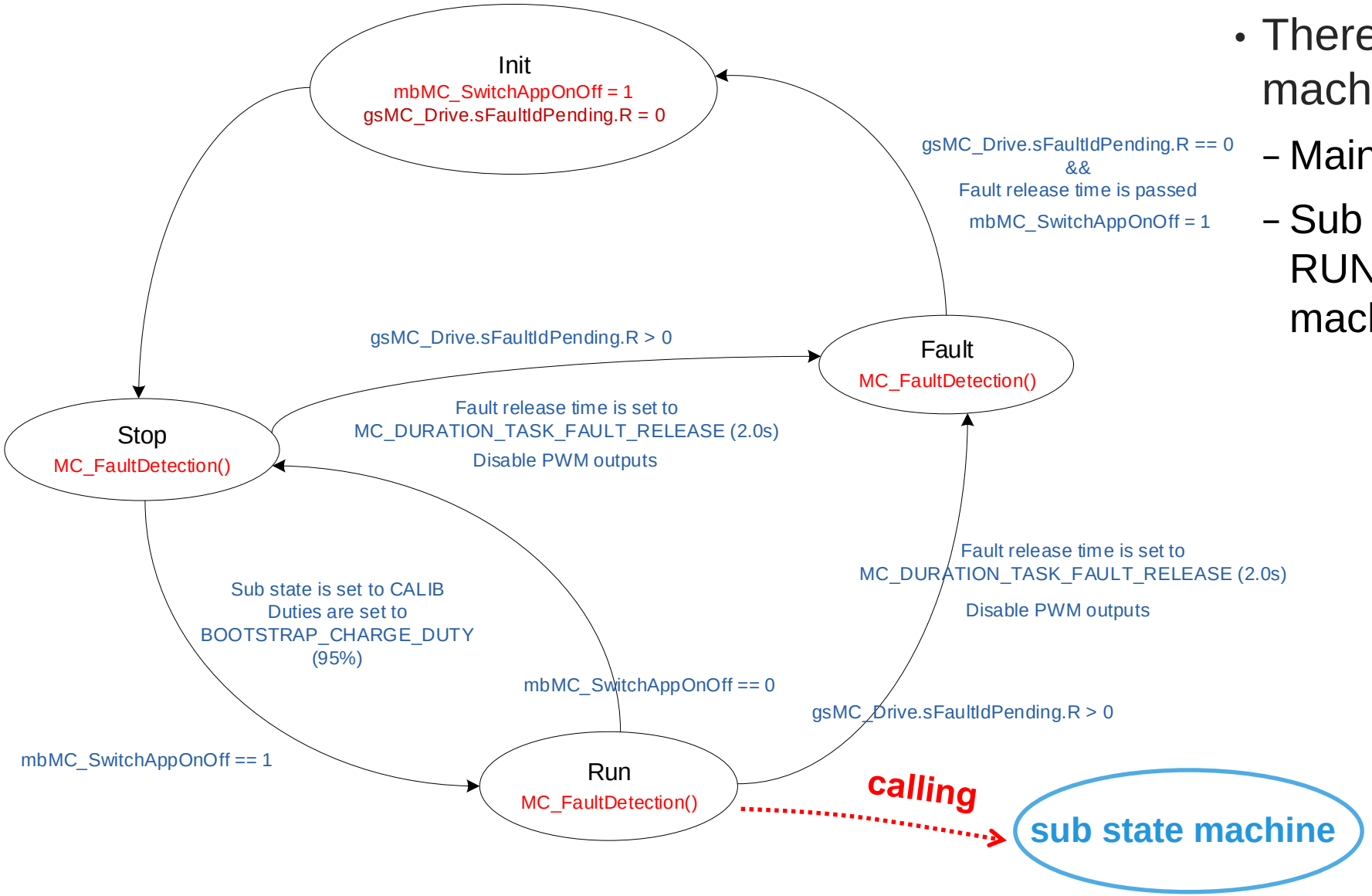
MERGE


D-current Control
$i_{dref} = 0$
u_d
Inverse Park
u_α
u_β
DC Bus ripple elimination
$u_{\alpha com}$
SVPWM
pwm
Inverter
$u_{\beta com}$
$i_{startup}$
i_{qref}
u_q
Q-current Control
θ_{sim}
Angle Generator
θ_{merge}
ω_{sim}
θ_{estim}
Ramp
i_d
Park
i_α
Clarke
$i_{a,b,c}$
i_q
i_β
PMSM
Tracking Observer
DQ Observer
ω_{estim}

CLOSED-LOOP SPIN

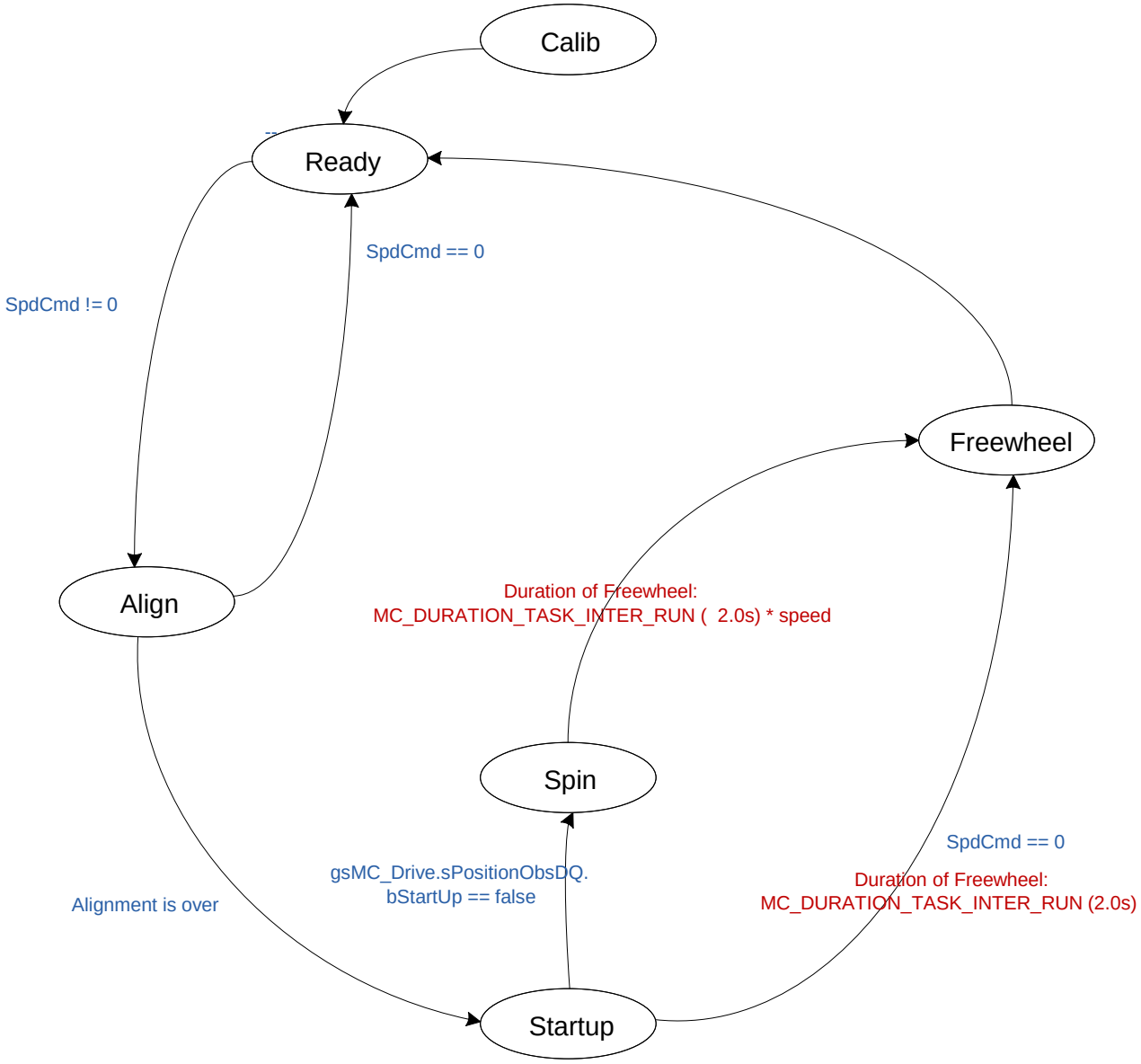


MAIN STATE MACHINE FOR MOTOR CONTROL



- There are 2 sets of state machines for motor control
  - Main state machine
  - Sub state machine residing in RUN state of the main state machine

SUB STATE MACHINE FOR MOTOR CONTROL



Interleaved Boost PFC Converter Scheme

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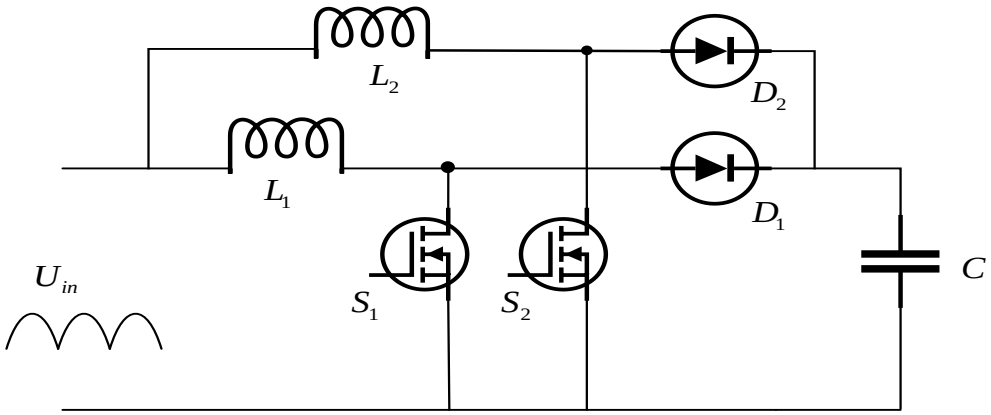
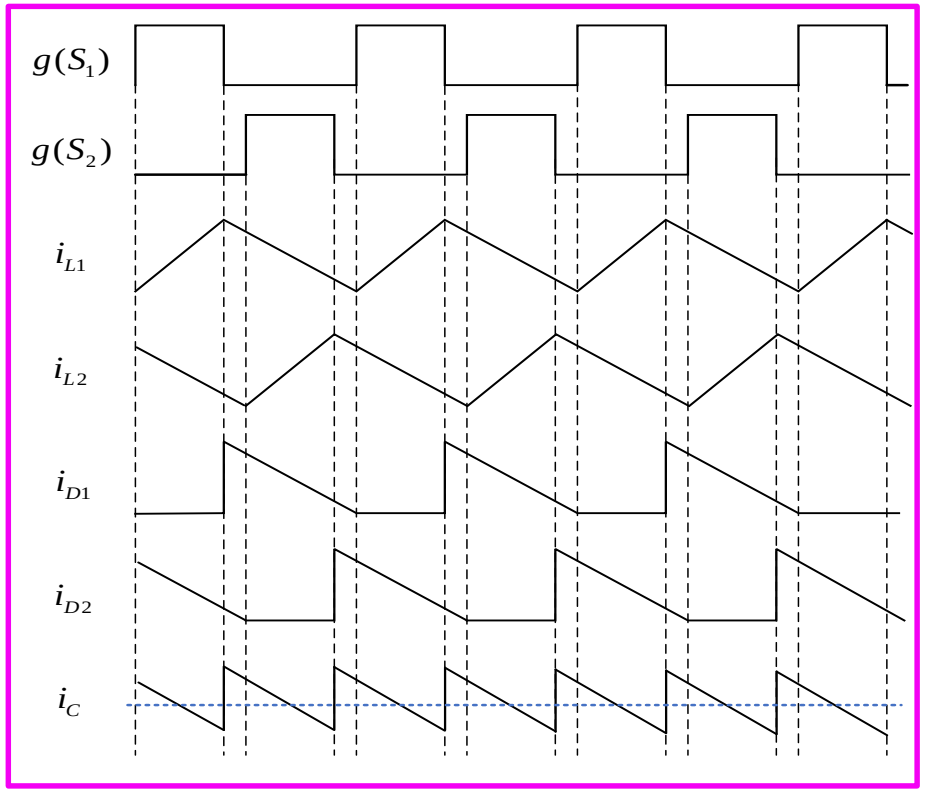
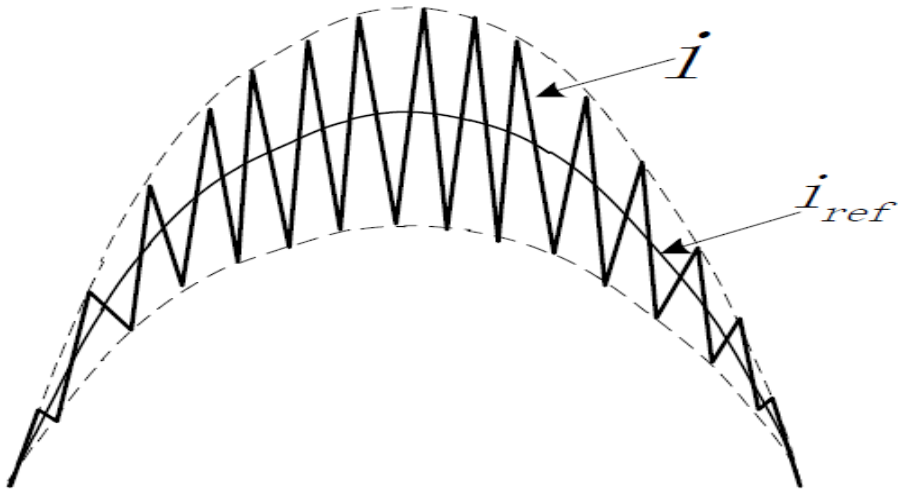
FOR A SMARTER WORLD

INTERLEAVED BOOST PFC CONVERTER



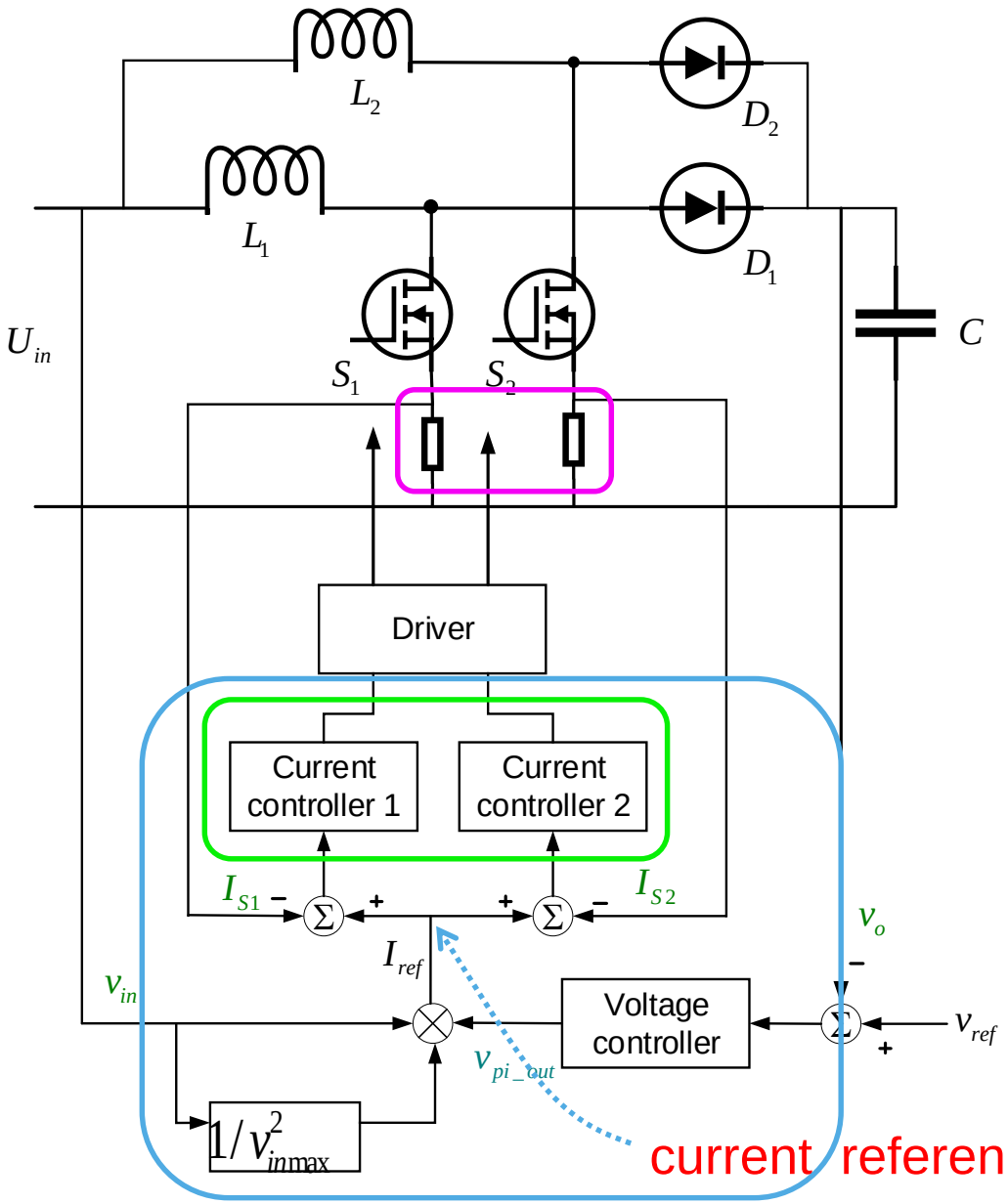


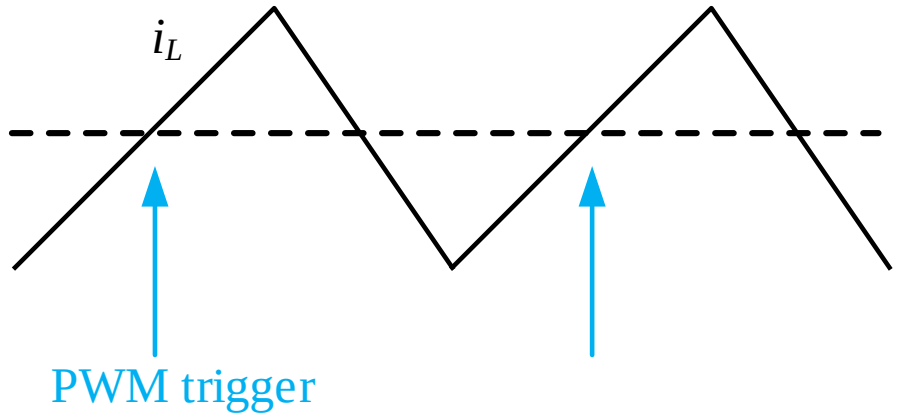
- Reduce the filter size with the **interleaving** technology
- Designed working at **CCM mode** for high power application
- Implemented with the **average current control** mode



Average current control / CCM mode

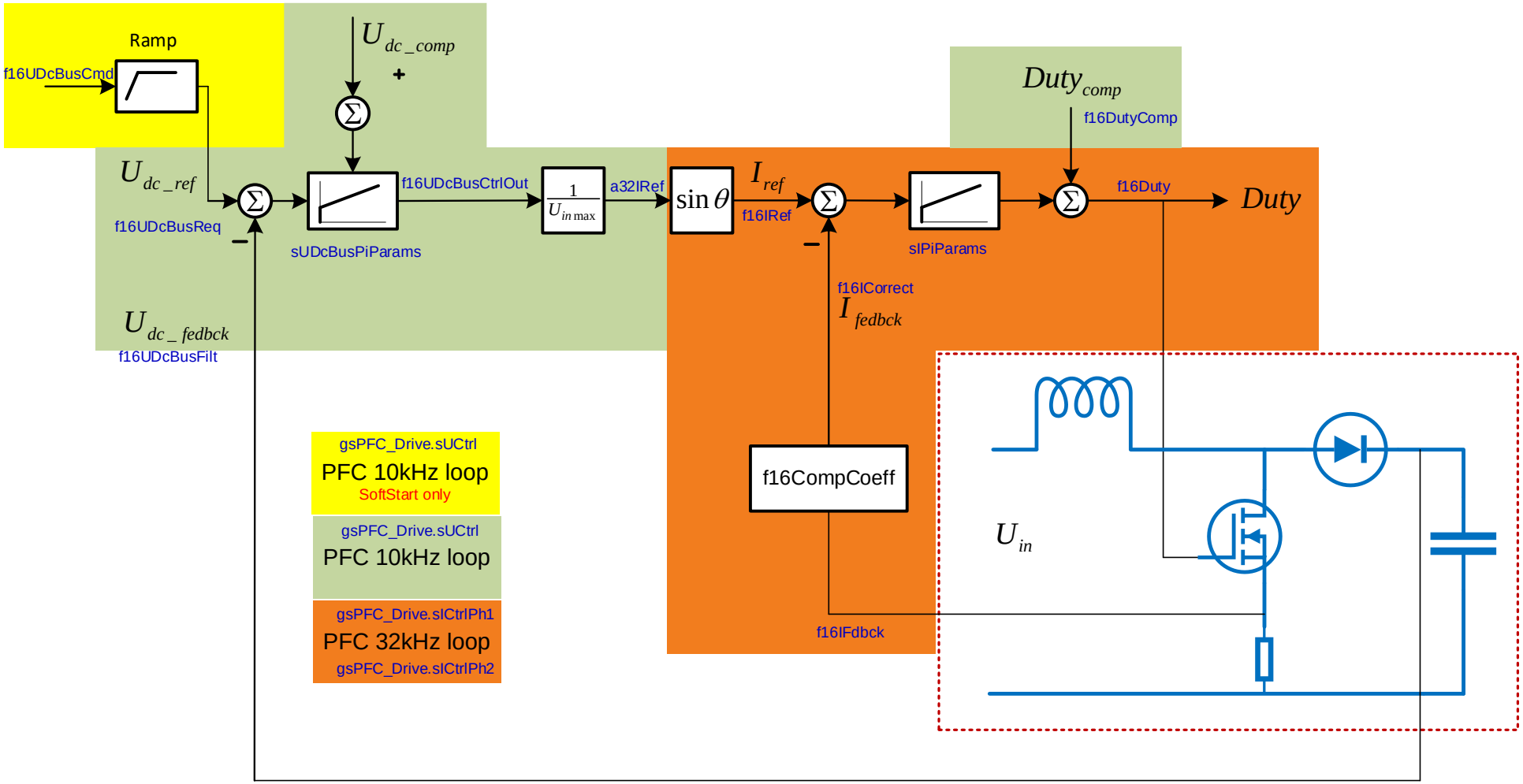
BASIC CONTROL STRATEGY





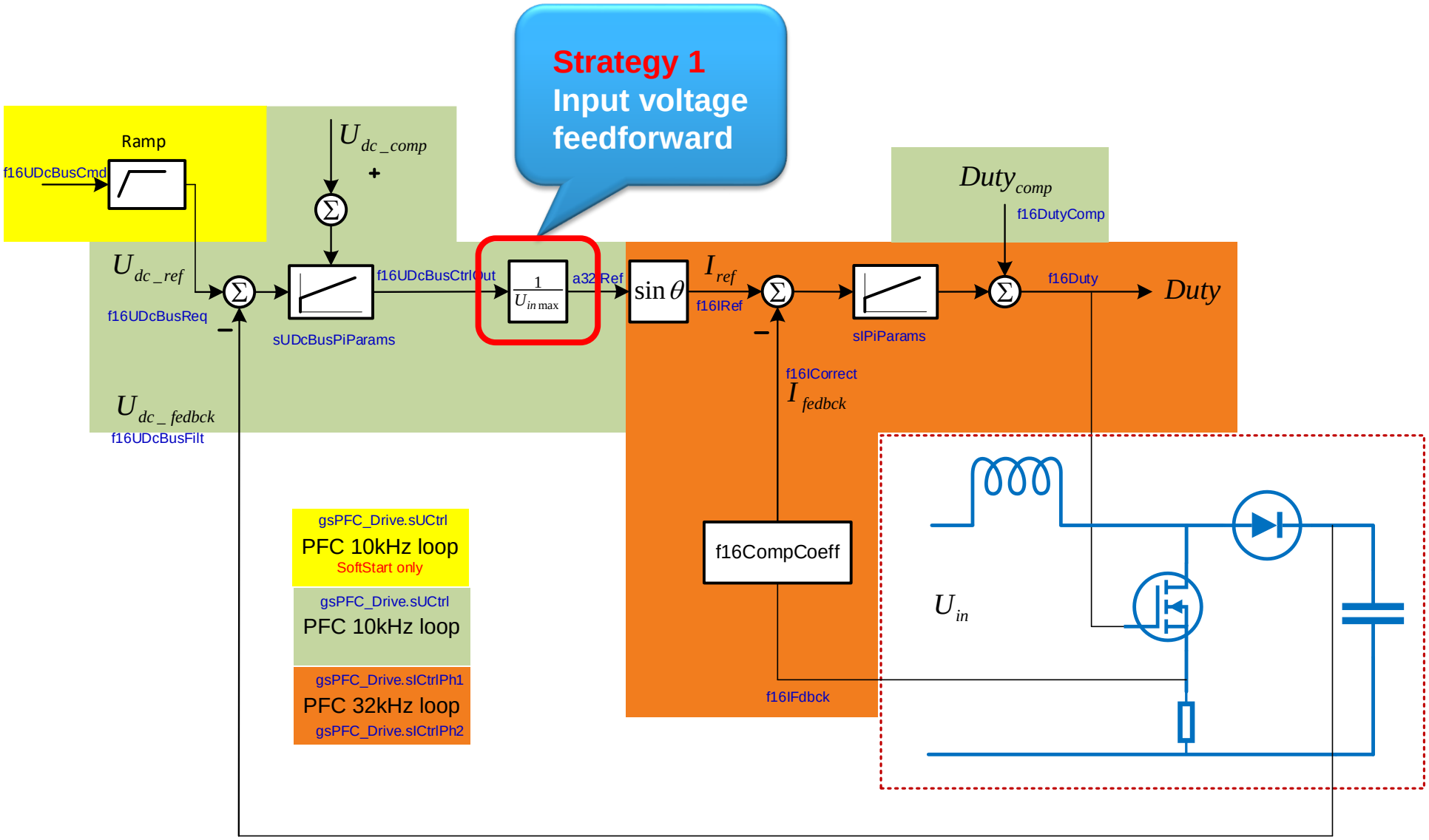
- Dual loop control with the outer voltage loop and inner current loop
- The average current sensed by shunt resistors at the center of the switching on/off time
- Two dedicated current loops for each phase to realize the current sharing with the **shared current reference**

CONTROL LOOP



Optimized control strategies…

STRATEGY 1 : INPUT VOLTAGE FEEDFORWARD



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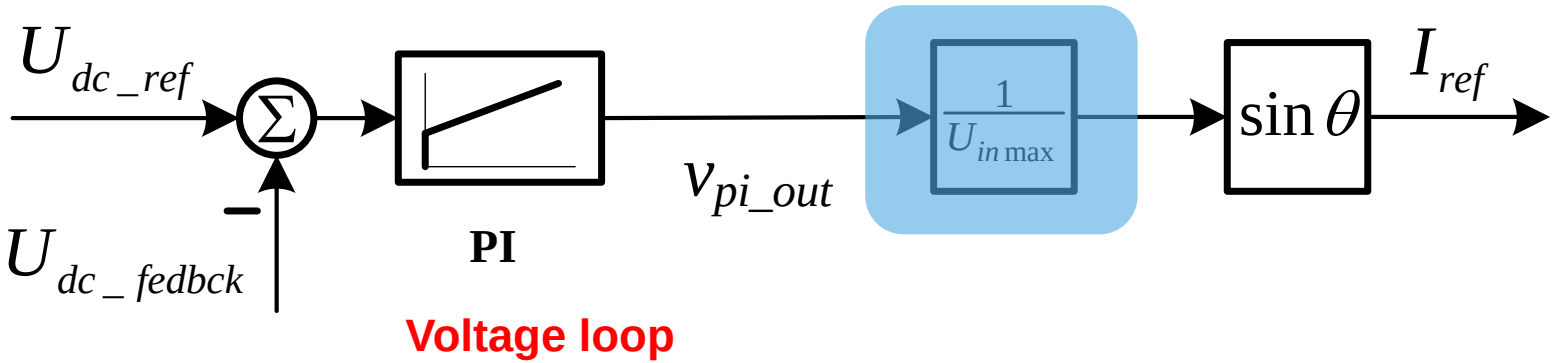


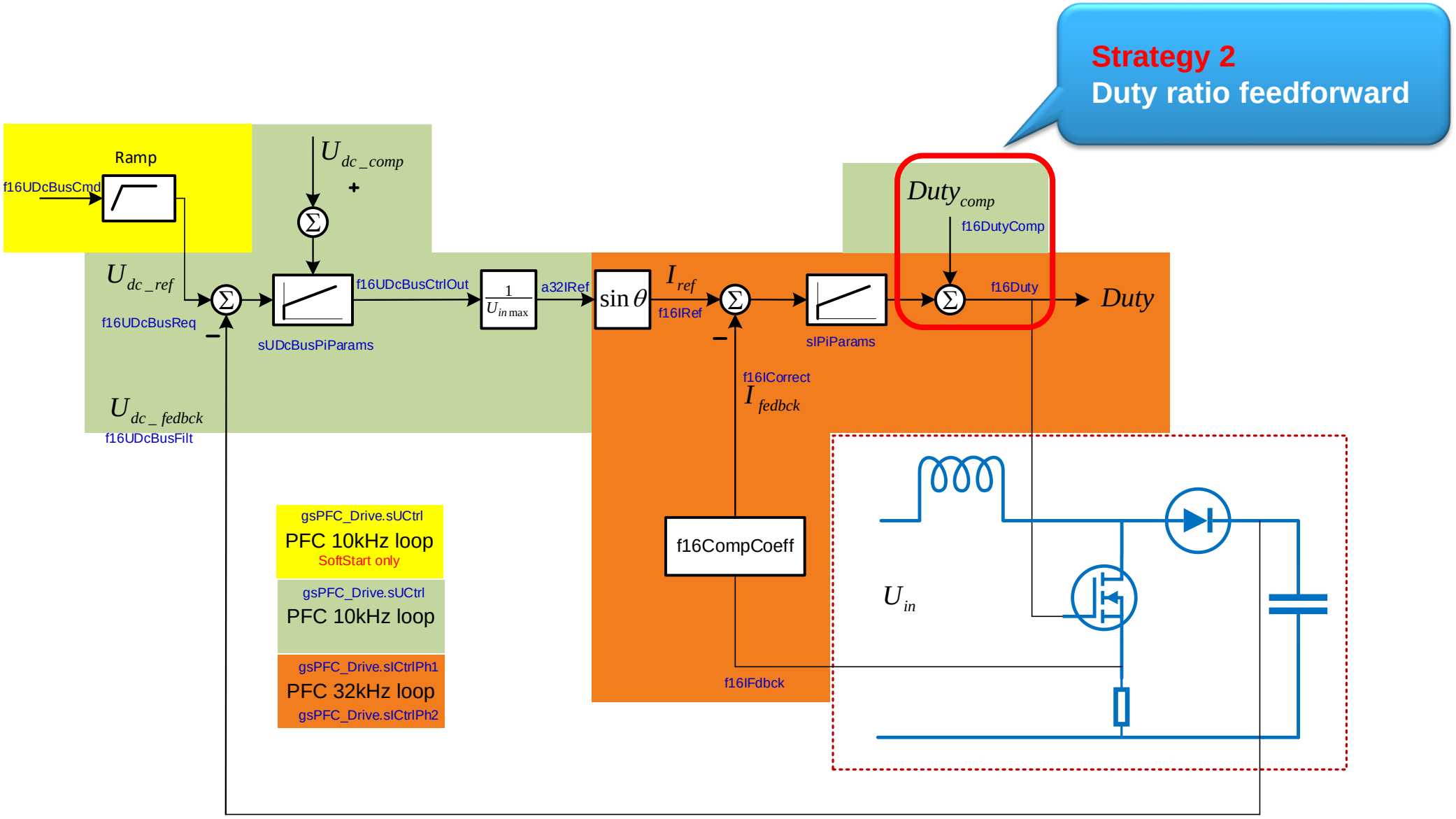
$$I_{ref} = \frac{v_{pi\_out}}{U_{in\,max}} \sin\theta$$

$$u_{in} = U_{in\,max} \sin\theta$$

$$p_{in} = u_{in} i_{in} = u_{in} I_{ref} = v_{pi\_out} \sin^2\theta$$

- The **input power will not change with the input voltage**
- Eliminate the influence of the grid voltage fluctuation

STRATEGY 2 : DUTY RATIO FEEDFORWARD



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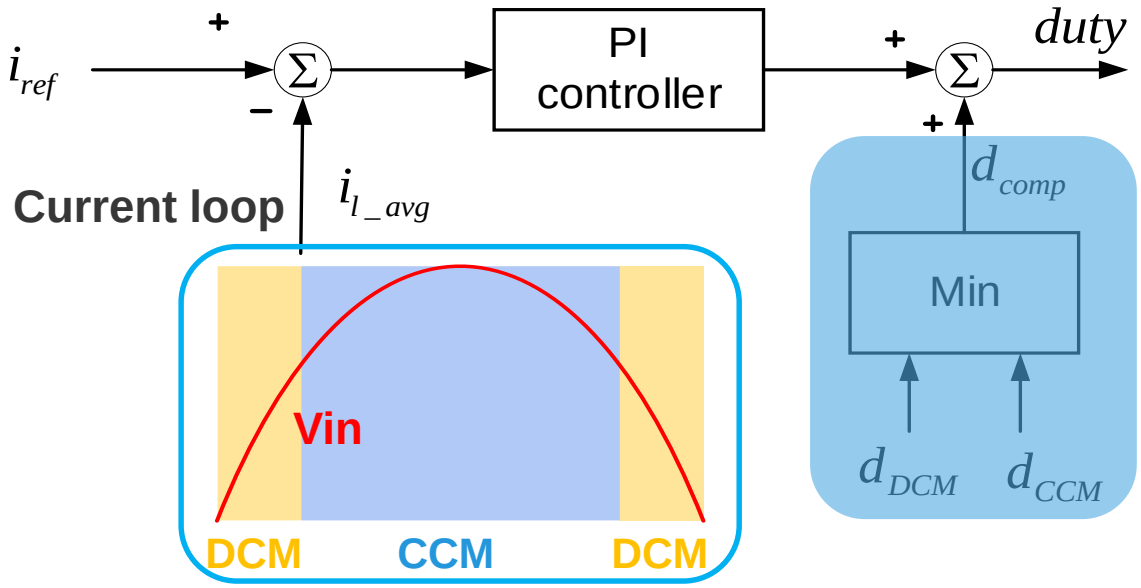
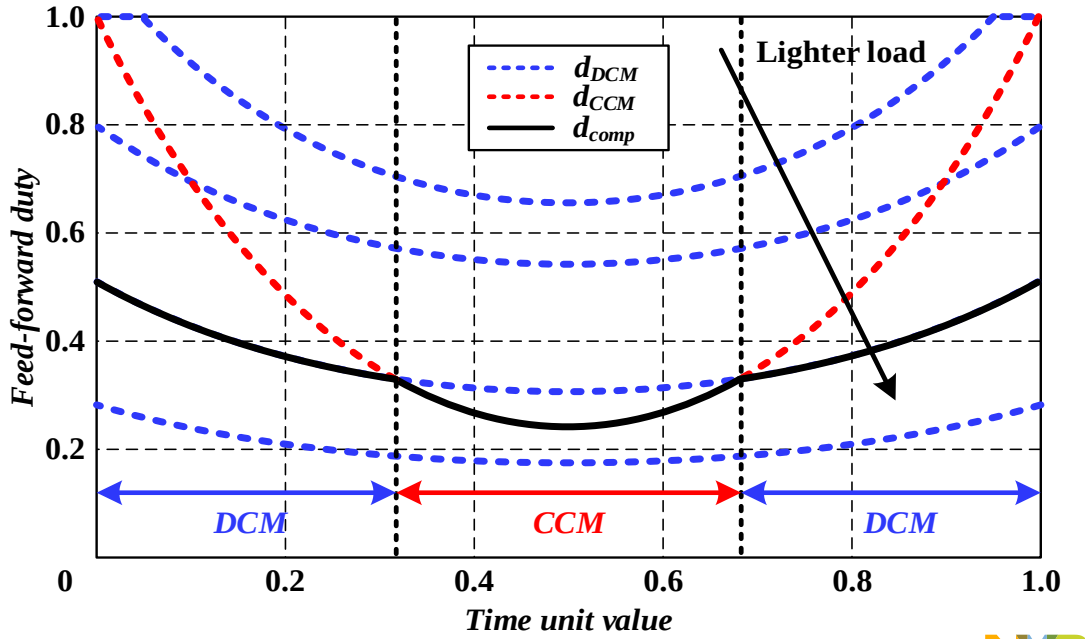


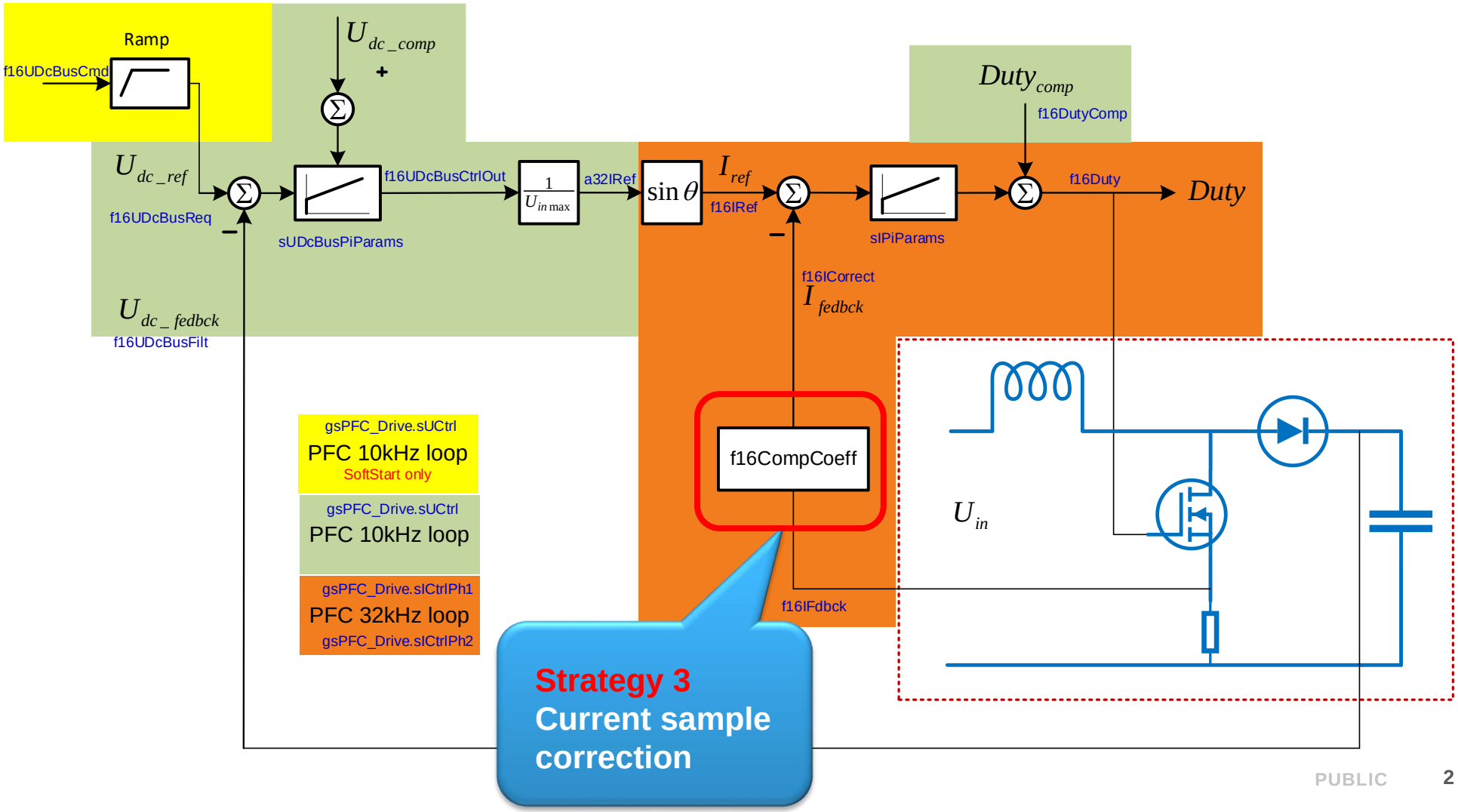
$$d_{comp}=min(d_{CCM},d_{DCM})$$

$$\begin{cases} d_{DCM} = \sqrt{\dfrac{2L}{T_S}\dfrac{v_{pi\_out}}{v_{in\max}^2}\,d_{CCM}} \\ d_{CCM} = 1-\dfrac{v_{in}}{v_o} \end{cases}$$

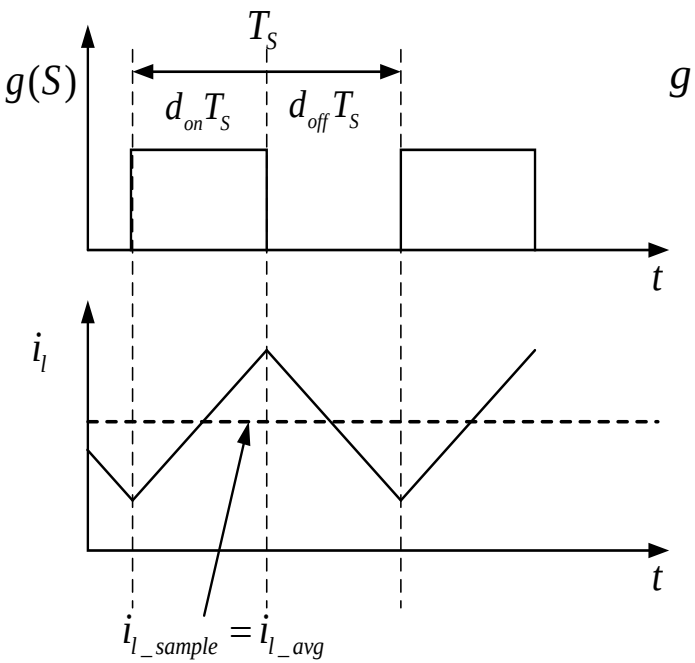


- Obtain the theoretical duty based on known quantities
- Compensate the dynamics model difference between CCM and DCM mode
- Only small error need be compensated, **high current loop gain isn't required**

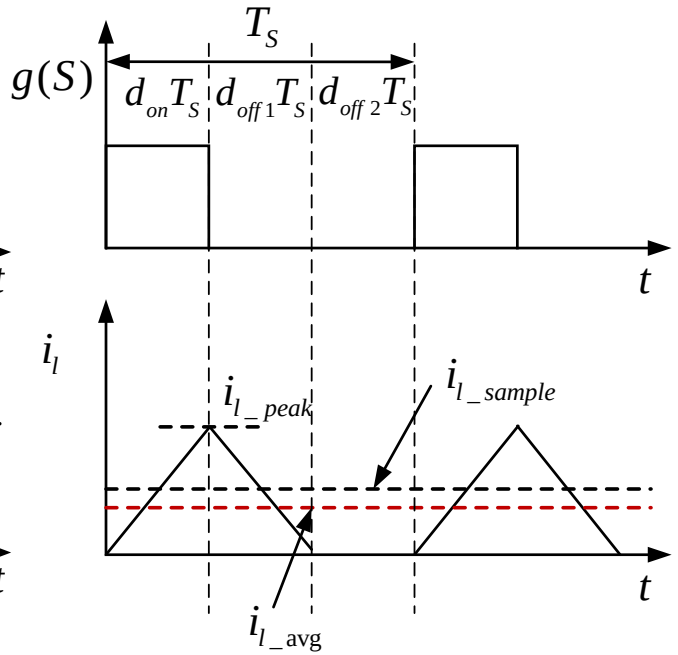
STRATEGY 3 : CURRENT SAMPLE CORRECTION



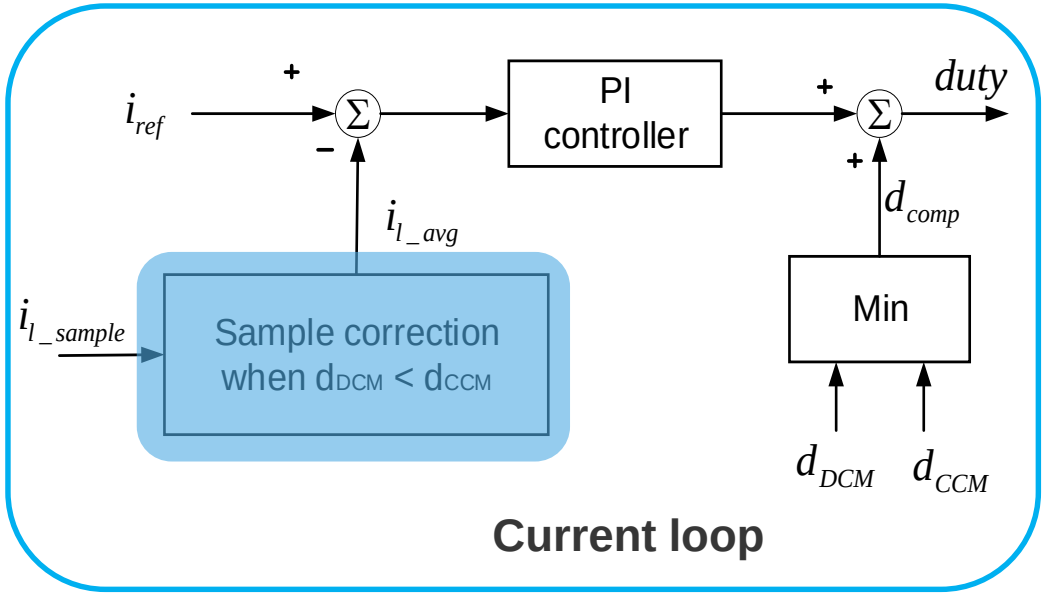
STRATEGY 3 : CURRENT SAMPLE CORRECTION



CCM mode



DCM mode

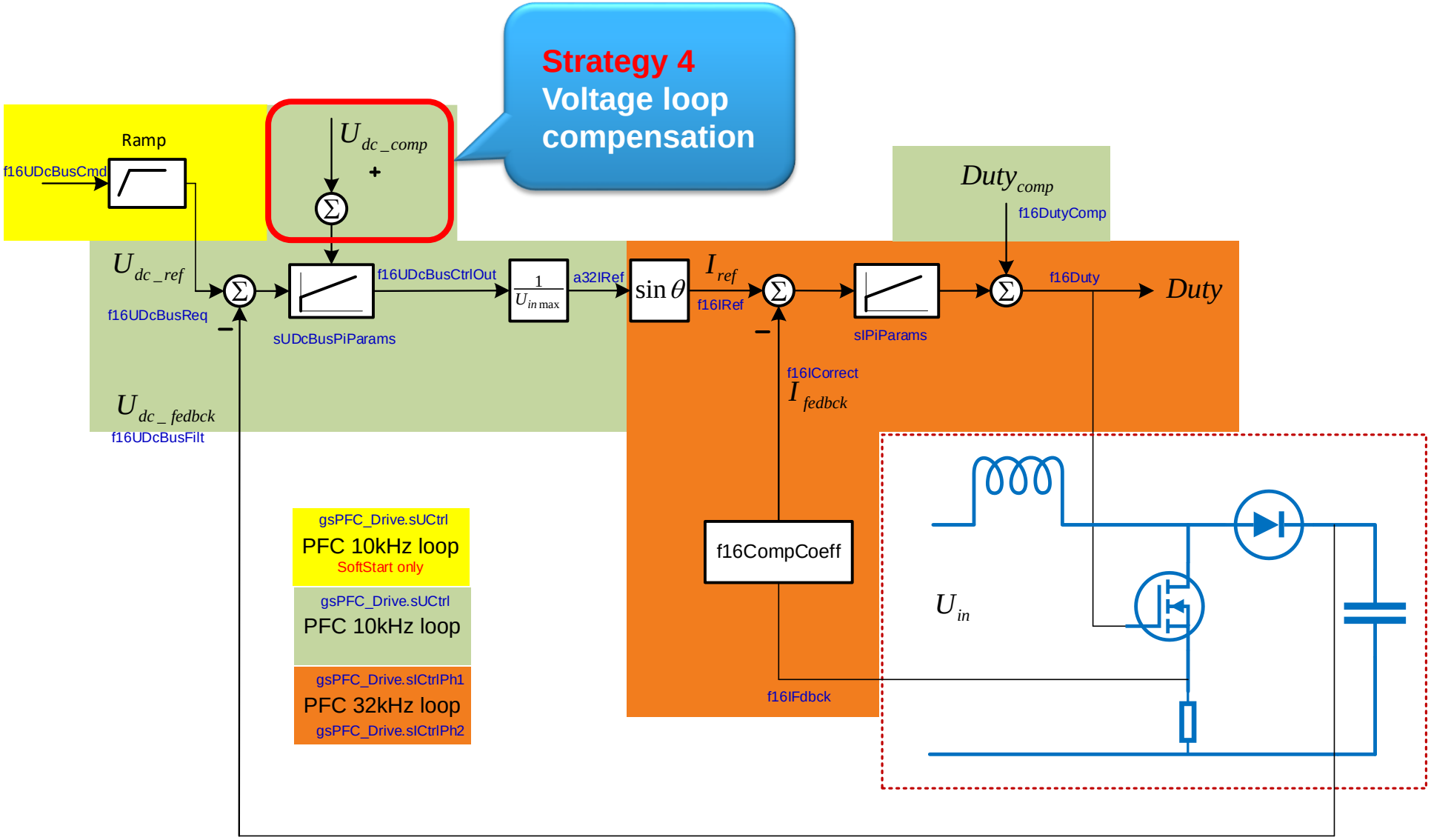


$$i_{l\_avg} = i_{l\_sample}$$

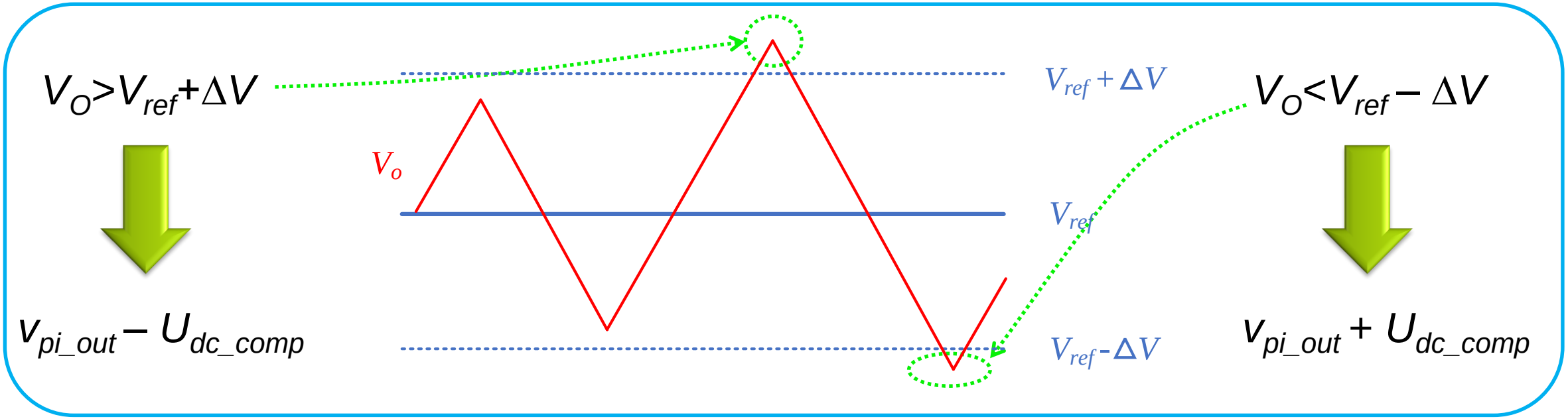
$$i_{l\_avg} = i_{l\_sample} \frac{v_o d_{on}}{v_o - v_{in}}$$

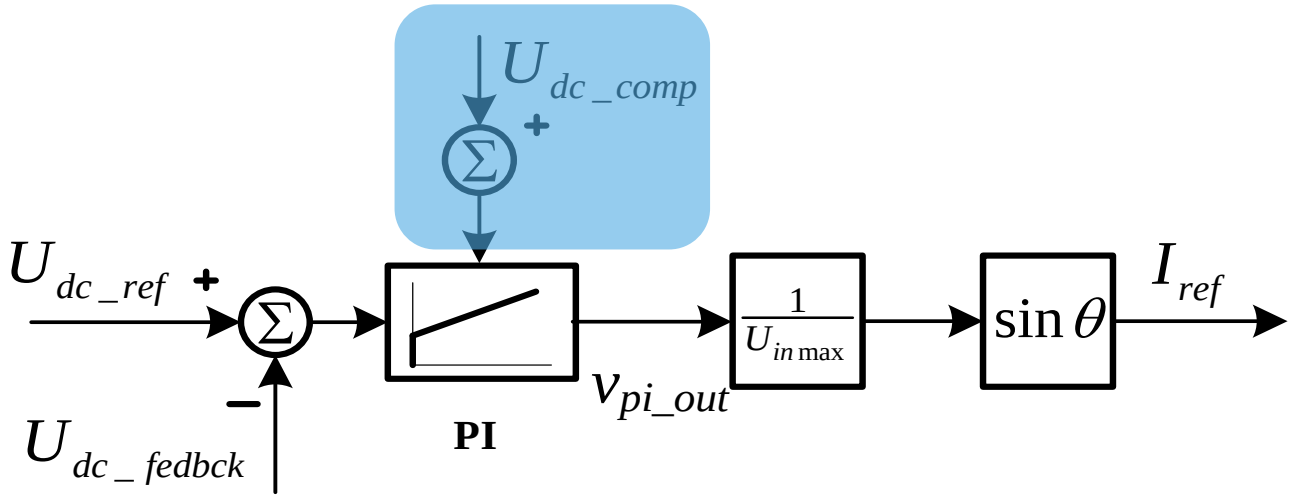
Correction coefficient

STRATEGY 4 : VOLTAGE LOOP COMPENSATION



STRATEGY 4 : VOLTAGE LOOP COMPENSATION





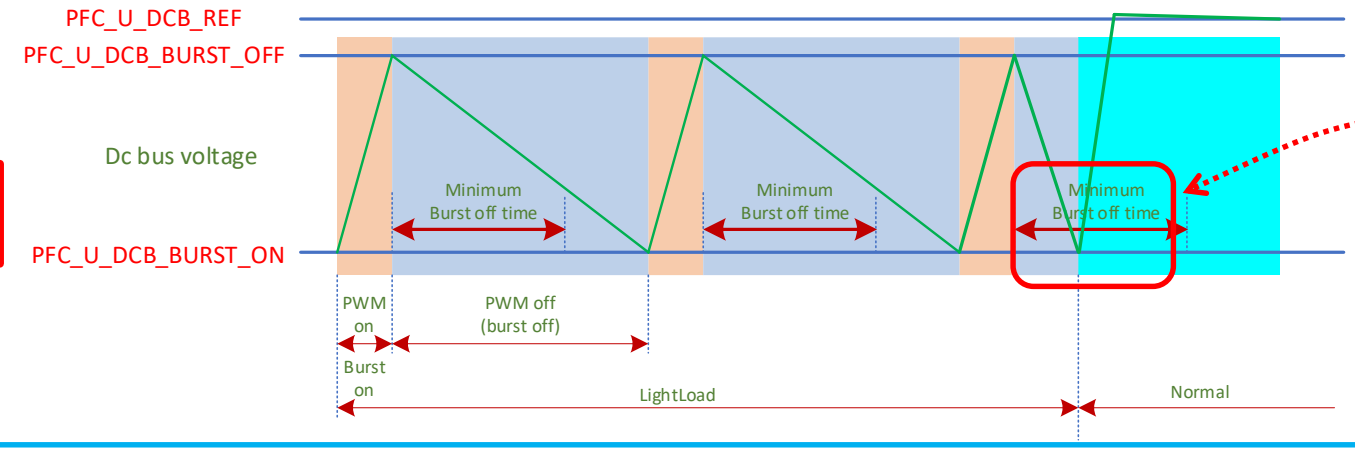
Improve the dynamic performance of the PFC

STRATEGY 5 : LIGHT LOAD EFFICIENCY OPTIMIZATION

Burst mode

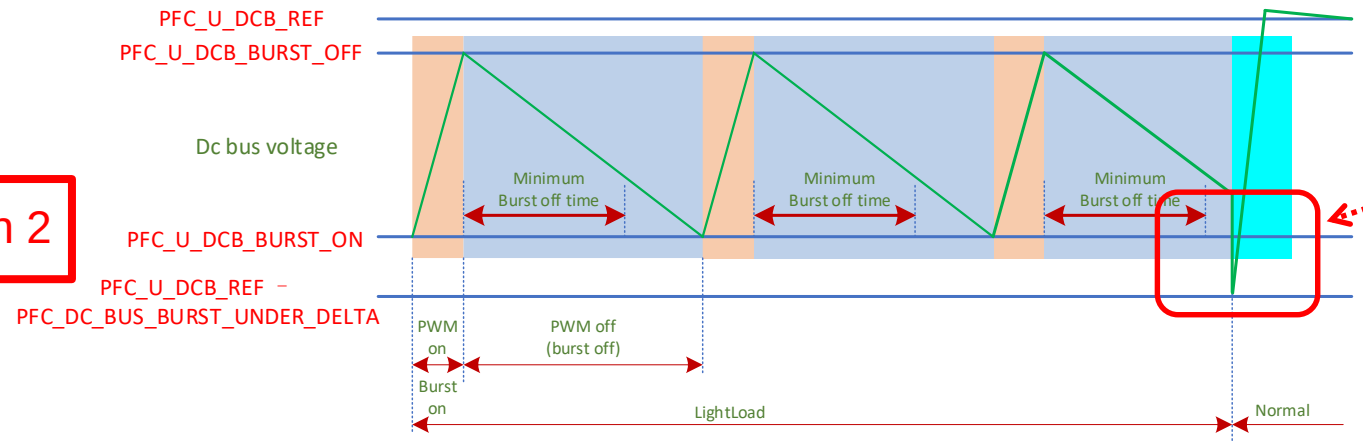
- Block switch driving signal periodically. When switch on, the RMS value of the reference current is fixed
- Equivalent switching frequency is reduced, **so the driving and switching loss is reduced**

Condition 1



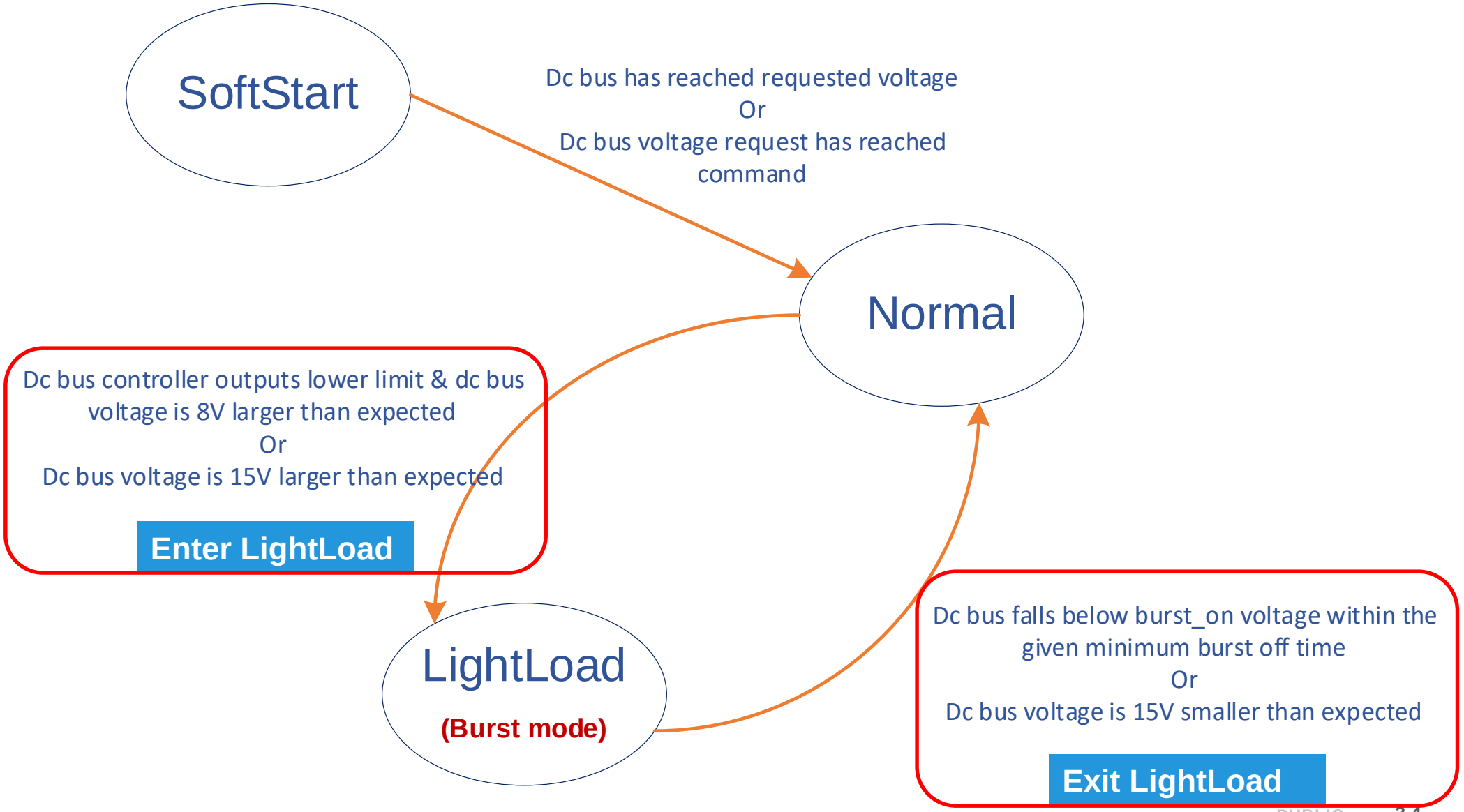
DC bus voltage falls below burst_on voltage within given minimum burst off time

Condition 2

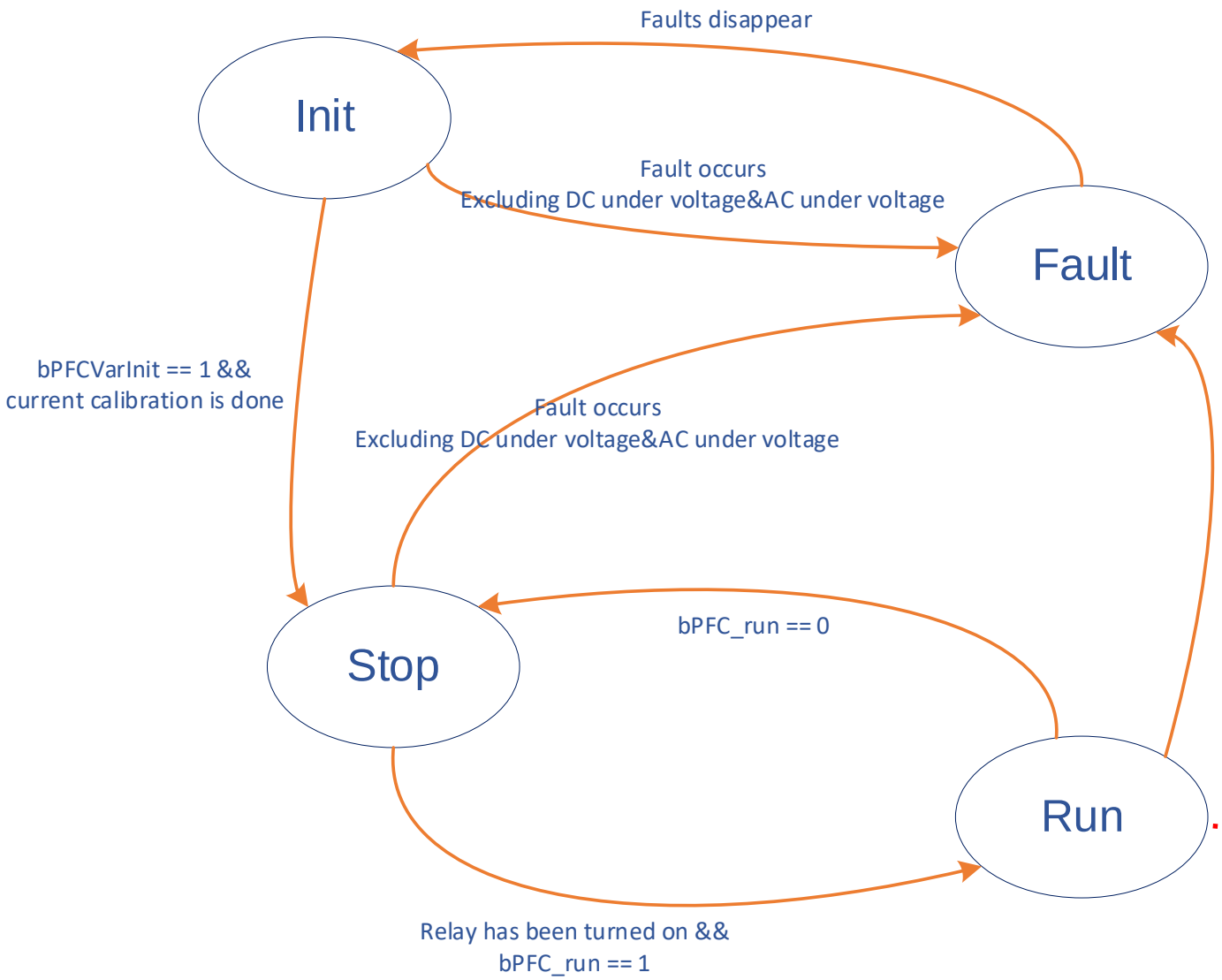


DC bus voltage is 15V smaller than expected

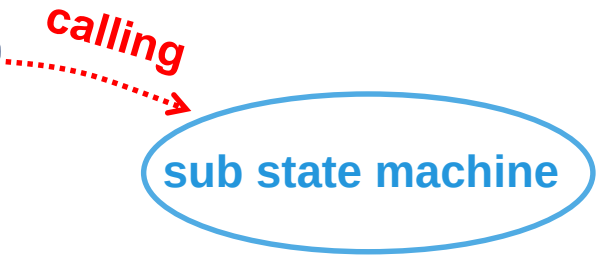
STRATEGY 5 : LIGHT LOAD EFFICIENCY OPTIMIZATION



STATE MACHINE



INIT	All variables are initialized, and the current offsets are calibrated within 200 ms
STOP	AC input voltage and DC bus voltage are monitored to determine if DC bus relay should be turned on or off
RUN	System is running. Run sub-state is called. PWM output is enabled
FAULT	System is at a fault condition, PWM output is disabled



Test Results

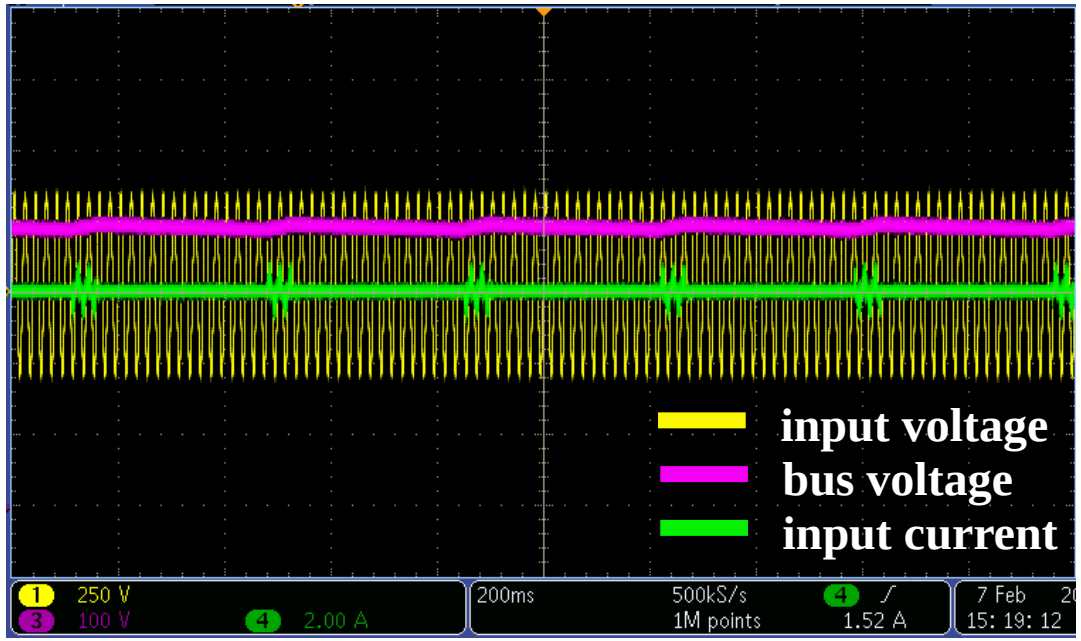
SECURE CONNECTIONS
FOR A SMARTER WORLD

POWER FACTOR

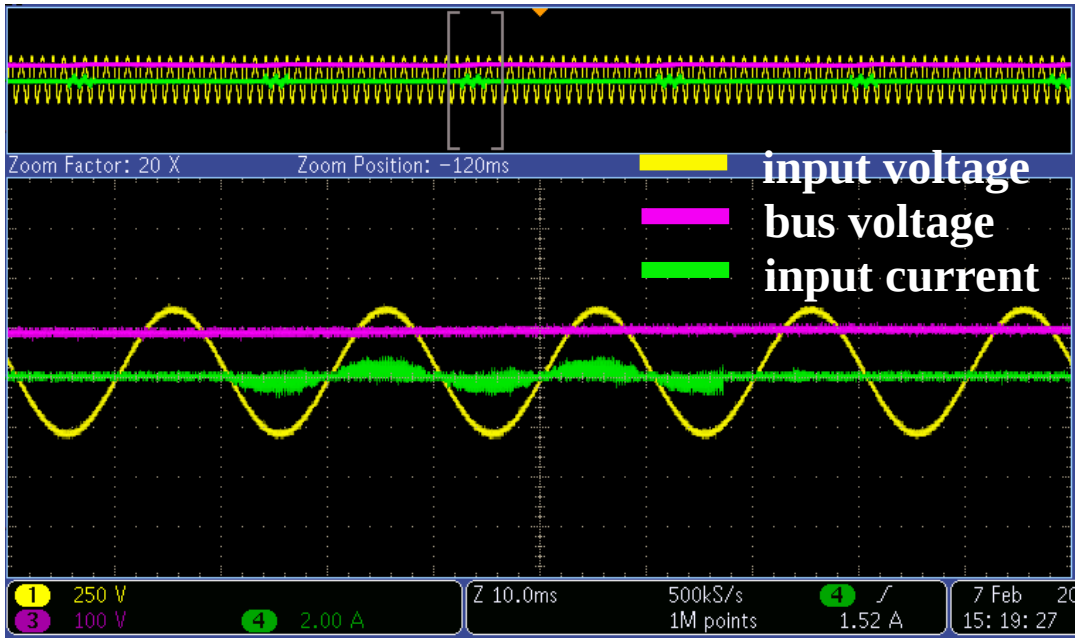
Input AC voltage	Output power (W)	Power factor
110V/60Hz	100	0.99
	200	0.996
	300	0.998
	400	0.998

Input AC voltage	Output power (W)	Power factor
220V/50Hz	200	0.987
	400	0.992
	600	0.997
	800	0.997

NO LOAD WAVEFORMS



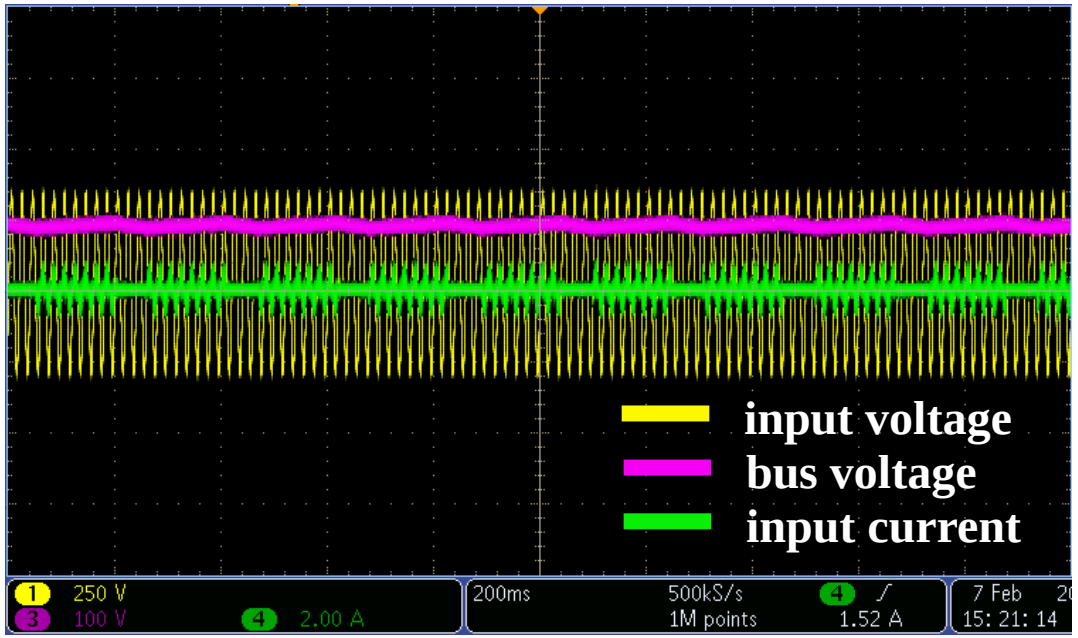
zoom in



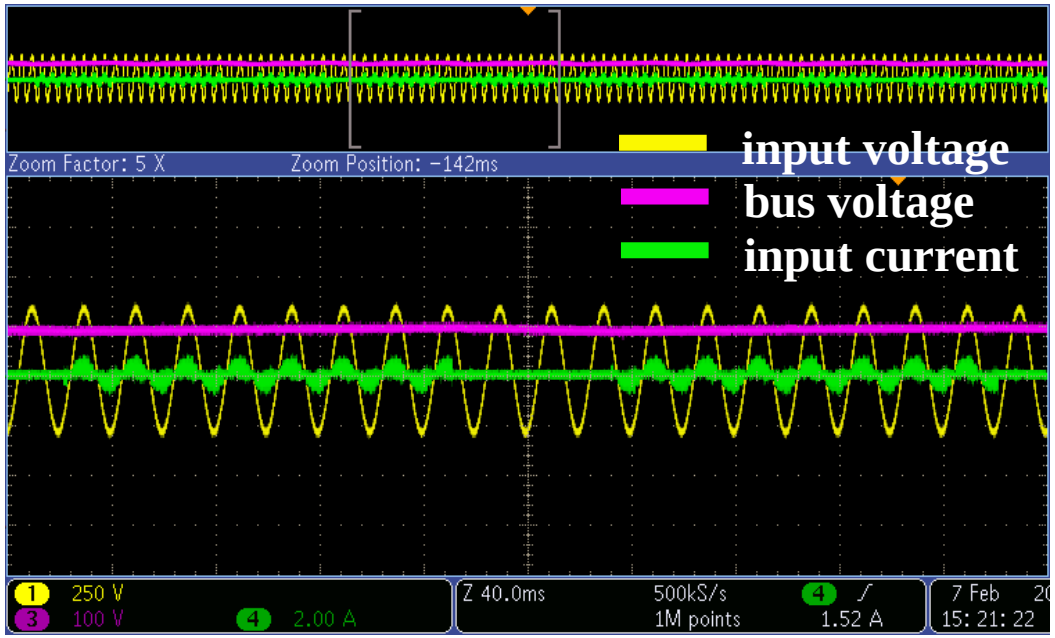
Vin=220VAC/50Hz, Po=0W

Operate at the burst mode to improve the light load efficiency

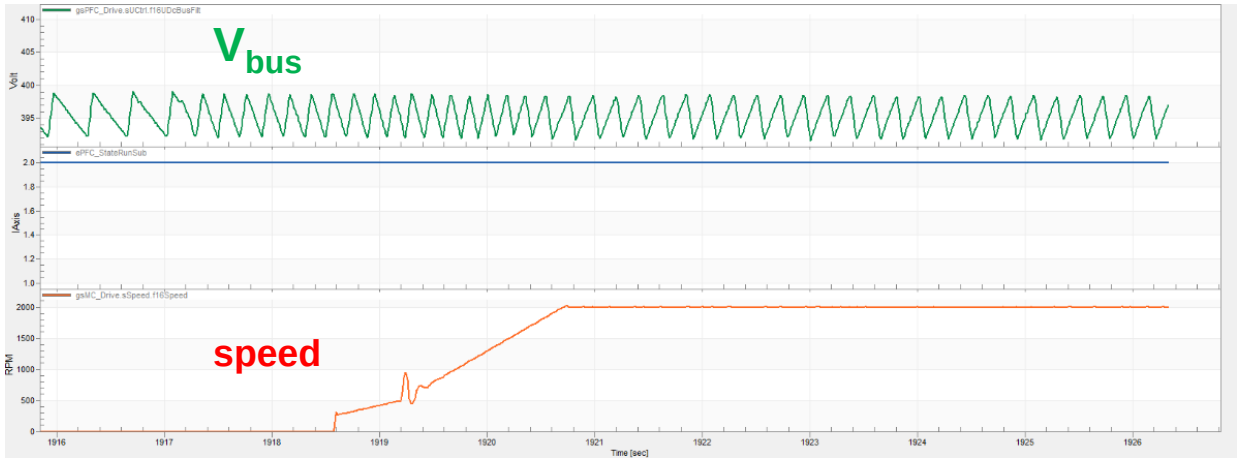
MOTOR LOAD WAVEFORMS



zoom in

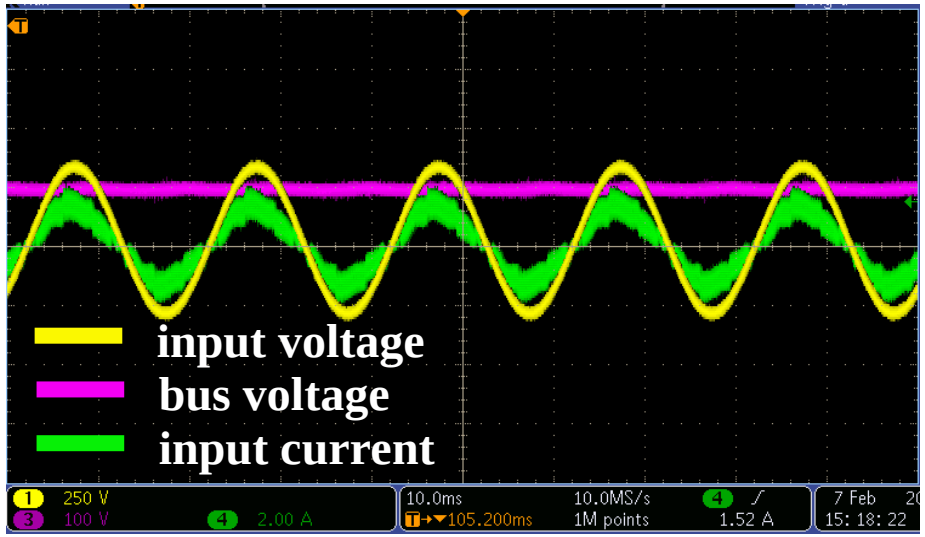


Vin=220VAC/50Hz, motor load

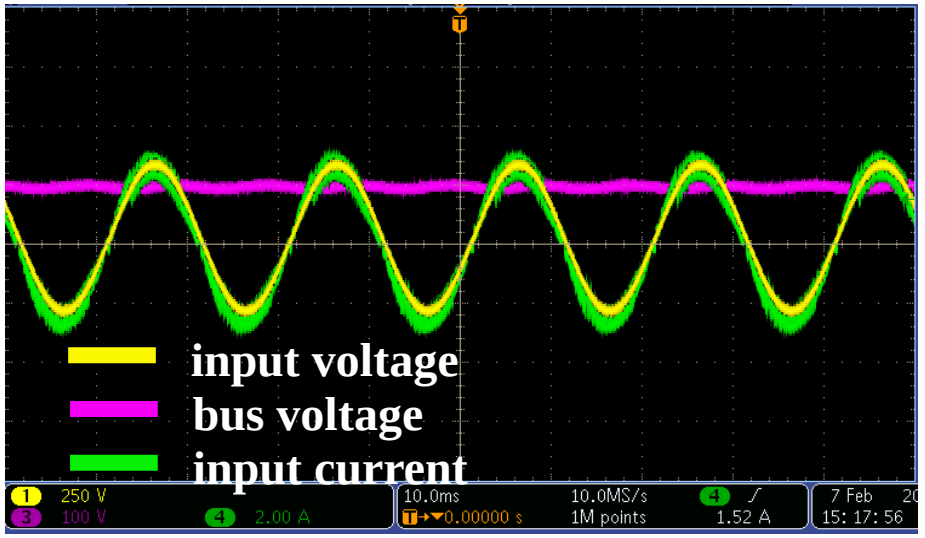


Motor start-up waveform in FreeMaster

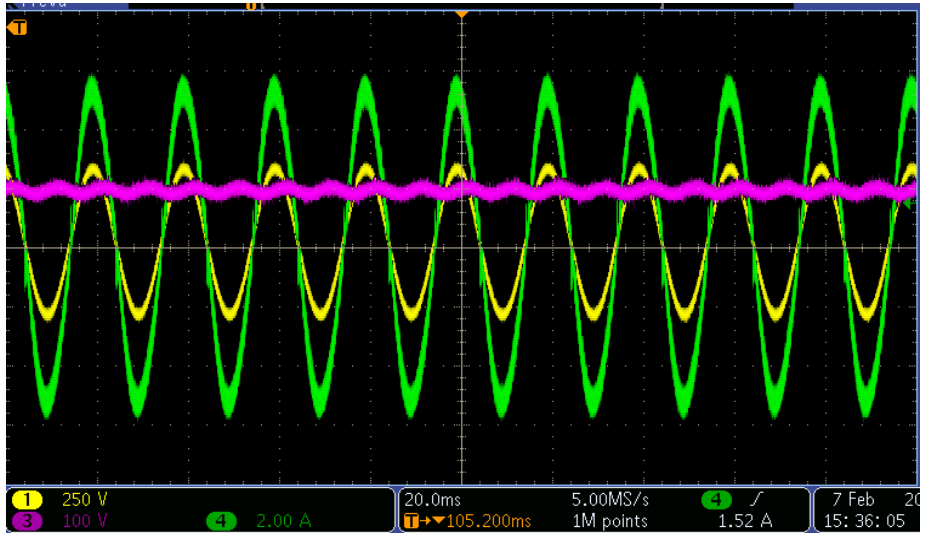
PFC STEADY STATE WAVEFORMS



V_{in}=220VAC/50Hz, P_o=200W



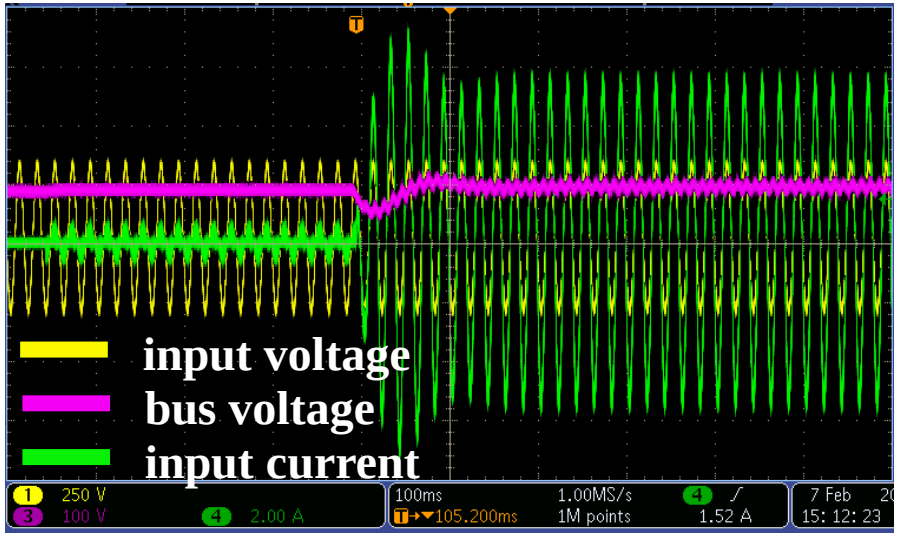
V_{in}=220VAC/50Hz, P_o=400W



V_{in}=220VAC/50Hz, P_o=800W

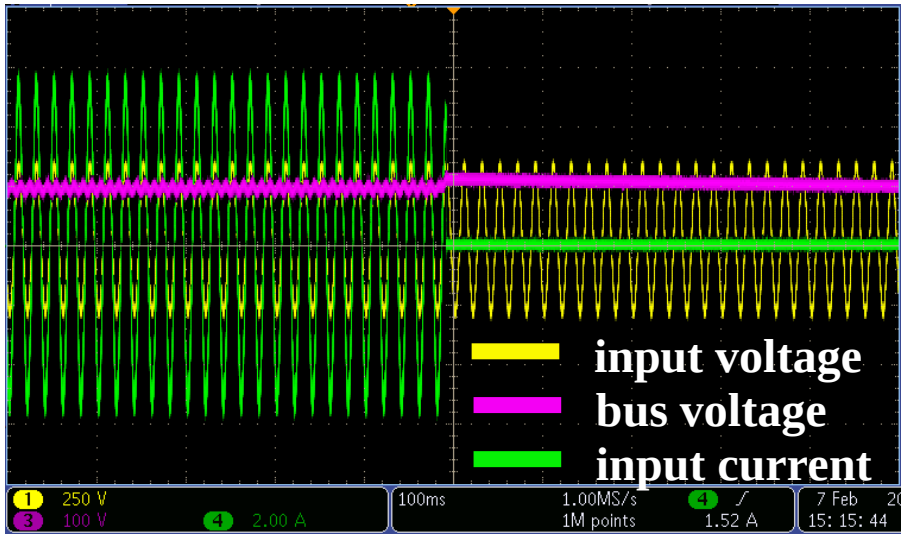
- The input current is a sine wave and in phase with the input voltage
- With the load increasing, the performance of the current controller becomes better

PFC DYNAMIC STATE WAVEFORMS

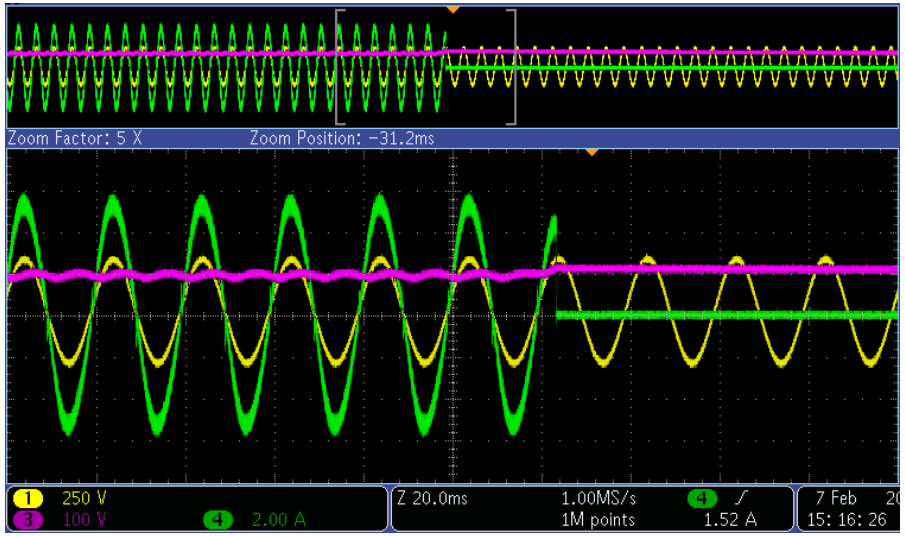


- The dynamic response is fast and the voltage surge is acceptable
- The input current is in phase with the input current under the dynamic state

Vin=220VAC/50Hz, 0W to 800W load transition



zoom in



Vin=110VAC/60Hz, 400W to 0W load transition

Development Tools

SECURE CONNECTIONS
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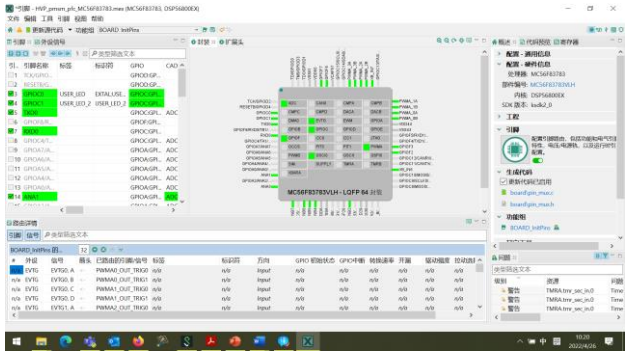
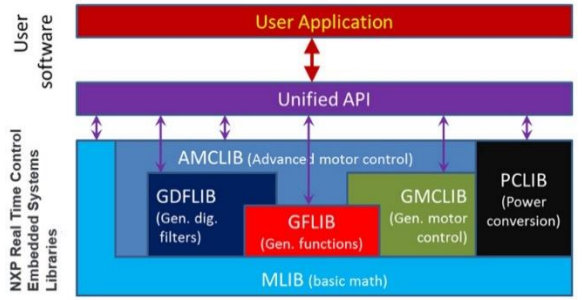
TOOLS – ALL FREE FOR 32-BIT DSC!

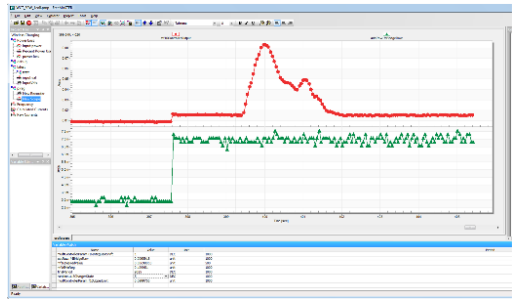
- **IDE - CodeWarrior Development Studio for DSC v11.x** (Compiler optimization ongoing!)
  - **License Free!**
  - Eclipse Front End for industry standard interface
- **Config GUI – MCUXpresso Config Tool - Pins, Clocks, Peripherals**
  - Includes pins, clocks and peripheral tools to speed up the development
- **MCUXpresso SDK**
  - A comprehensive software enablement package designed to simplify and accelerate application development
- **Library – RTCESL** (**Real Time Control Embedded Software Library**)
  - For motor control and power conversion common APIs
  - Include Math / General Function / General Motor Control / General Digital Filter / Advanced Motor Control / Power Control library
- **Run-time Debugging Tool – FreeMASTER**
  - Non-intrusive monitoring of variables on a running system
  - Oscilloscope-like display



Config Tool GUI

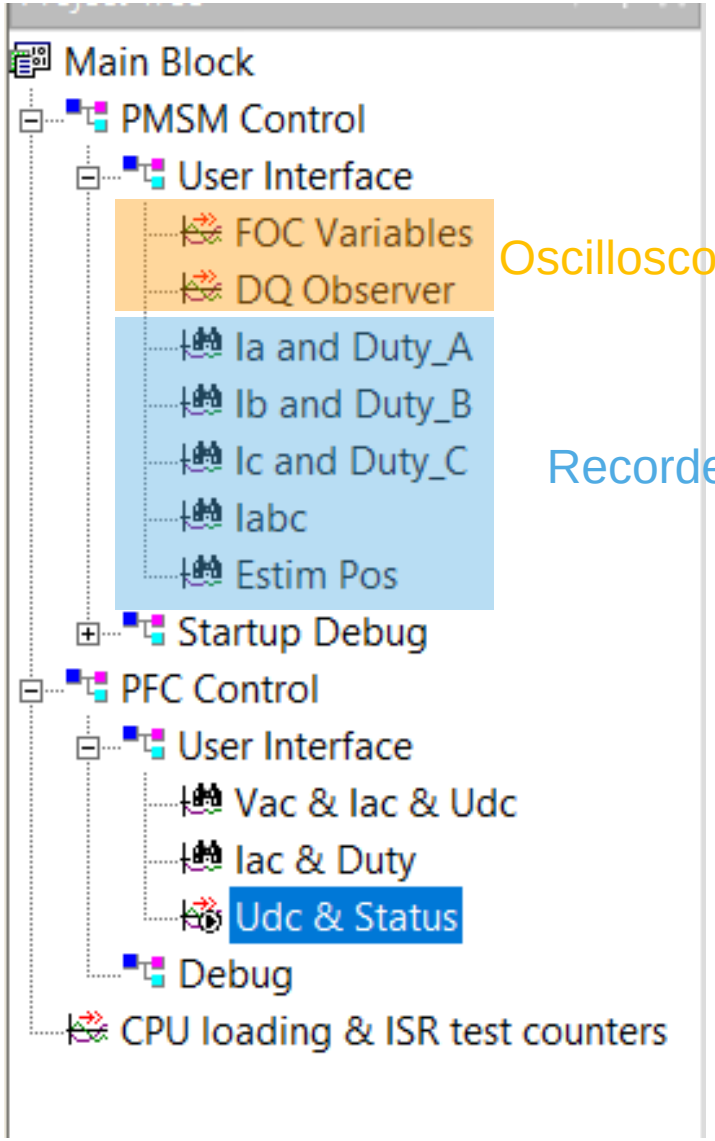


RTCESL



FreeMASTER

FREEMASTER USAGE



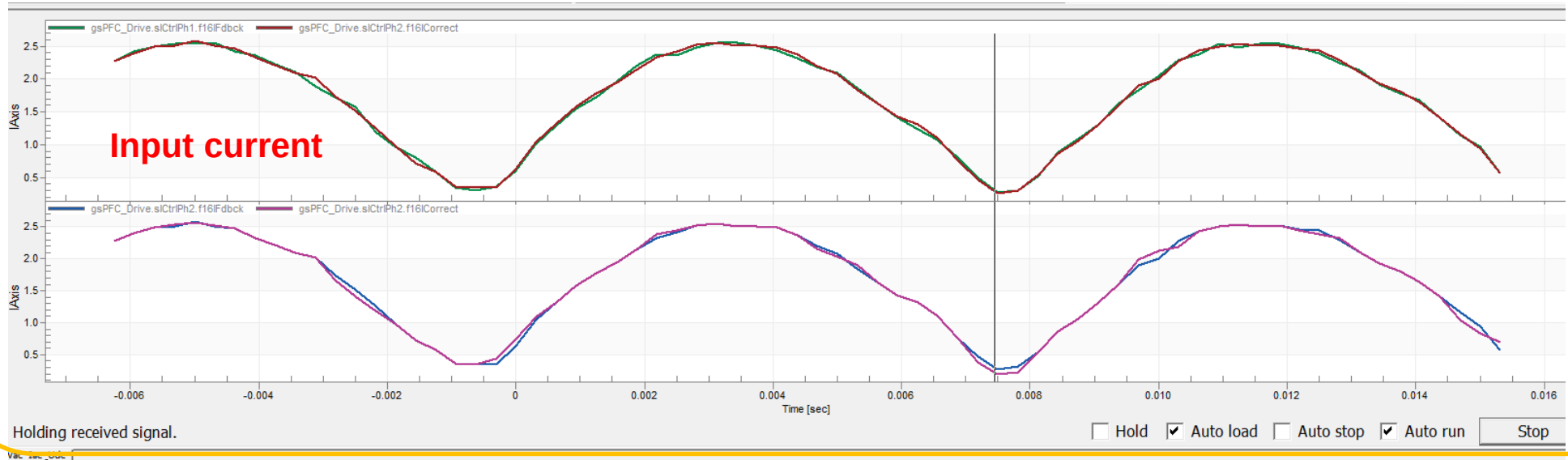
Variable Watch

Name	Value	Unit	
bPFC_RUN	1	DEC	1000
gsPFC_Drive.FaultId.R	NORMAL	ENUM	1000
gsPFC_Ctrl.eState	Run	ENUM	1000
ePFC_StateRunSub	LightLoad	ENUM	1000
gsPFC_Drive.sUCtrl.f16UDcBusCmd	399.991	Volt	1000
gsPFC_Drive.sUCtrl.f16UDcBusFilt	395.683	Volt	1000
mbMC_SwitchAppOnOff	ON	ENUM	1000
gsMC_Drive.sSpeed.f16SpeedCmd	2000	RPM	1000
Motor+PFC loading	2493, 236, 3959	(VAL, MIN, MAX)	0
PFC fast loop loading	394, 263, 762	(VAL, MIN, MAX)	0
w16ExeTimePfc_slowloop	337, 100, 1585	(VAL, MIN, MAX)	0

Variable watch

- **Oscilloscope** and **recorder** could be used to display the waveform of the variable
- Oscilloscope is suitable for low frequency signal and recorder is suitable for high frequency signal
- Through **variable watch** window, users could observe and modify the value of the variable in real time

FREEMASTER USAGE



Recorder window

Variable Watch

Name	Value	Unit	Period [ms]
gsPFC_Ctrl.eState	Run	ENUM	1000
ePFC_StateRunSub	Normal	ENUM	1000
gsPFC_Drive.sUCtrl.f16UDcBusCmd	399.991	Volt	1000
gsPFC_Drive.sUCtrl.f16UDcBusFilt	397.917	Volt	1000
mbMC_SwitchAppOnOff	OFF	ENUM	1000
gsMC_Drive.sSpeed.f16SpeedCmd	0	RPM	1000
Motor+PFC loading	879. 208. 2961	(VAL. MIN. MAX)	0
PFC fast loop loading	344. 246. 469	(VAL. MIN. MAX)	0
w16ExeTimePfc_slowloop	814. 63. 938	(VAL. MIN. MAX)	0
gsPFC_Drive.sPFCalculate.f16UInRMS	107.735	unit	1000
gsPFC_Drive.sPFCalculate.f16IInRMS	3.62207	unit	1000
gsPFC_Drive.sPFCalculate.f32ActivePowerAver	388.108	unit	1000
gsPFC_Drive.sPFCalculate.f32ApparentPower	388.243	unit	1000
gsPFC_Drive.sPFCalculate.f16PowerFactor	0.999207	unit	1000

Variable watch

FreeMaster window

SUMMARY

- The digital control of the PMSM FOC and the interleaved Boost PFC converter can be realized with one DSC chip to reduce the volume and cost of the system.
- The complex control timing is implemented with the flexible DSC peripherals.
- High light-load efficiency and low THDI is ensured by the optimized digital algorithm.
- The development cycle of the customers can be reduced by the powerful DSC enablement.

Visit www.nxp.com for more information

Q&A

TECHNOLOGY SHOWROOM

JOURNEYS BY DESIRED ENGAGEMENT

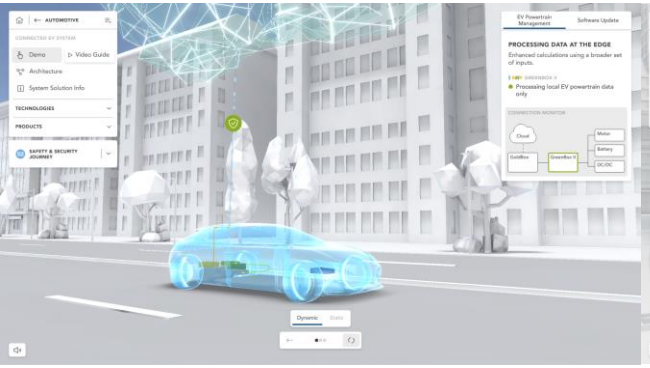
Self-guided tour
Live-streaming at set times
Guided tours

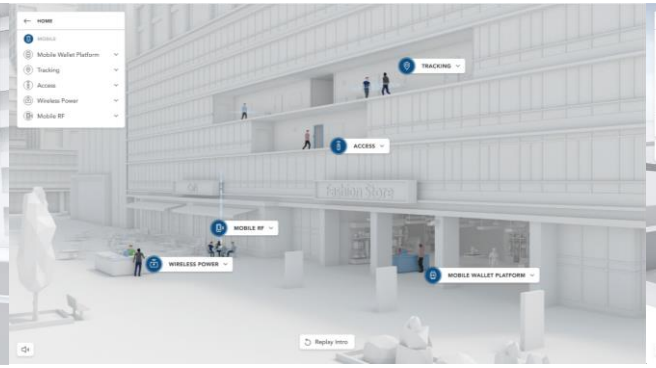
60+ VIRTUAL DEMOS

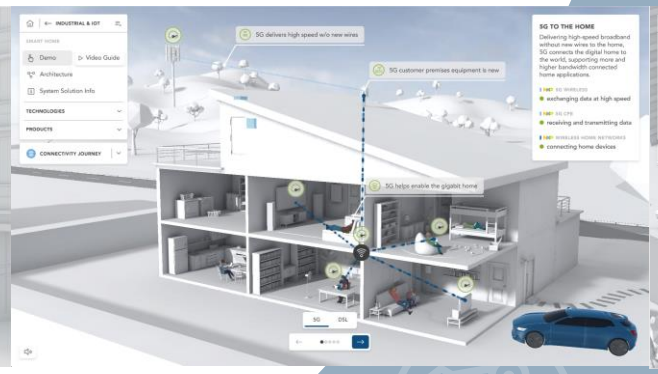
Focus on system solutions
Set up along NXP verticals

JOURNEYS BY DESIRED FOCUS

Low Power Innovations
Advanced Analog
Connectivity
Edge & AI/ML
Safety & Security







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