

AN14284

FlexIO模拟接口的时序参数调整

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应用笔记

文档信息

信息	内容
关键词	AN14284、FlexIO、SPI
摘要	本应用笔记介绍了如何使用附加定时器来调整RT1170-EVK中SPI主设备的建立时间。



1 介绍

FlexIO是Kinetis、S32K、RT和MCX微控制器系列中配备的一个片上外设。它具有高度可配置性，能够模拟UART、I²C、SPI、I²S和LIN等各种通信协议以及J1850、I3C、Manchester等其他协议。¹

这个单独的外设模块FlexIO可用作微控制器的一个额外的外设模块，并不是要替代任何通信外设。

FlexIO的主要特点是灵活性强，让用户甚至可以自定义时序参数。

本应用笔记介绍了如何使用附加定时器调整RT1170-EVK中SPI主设备的建立时间。

2 模拟SPI主设备

2.1 概述

要用FlexIO模拟SPI主设备，请使用以下资源：

- 两个移位器：一个是发送器，另一个是接收器。
- 两个定时器：一个用于生成片选，另一个用于生成时钟以控制两个移位器。
- 四个引脚：CS、SCK、MOSI和MISO。

2.2 在高波特率下的接收错误

模拟SPI主设备的驱动程序通常包含在MCUXpresso SDK中。下面是

evkmimxrt1170_flexio_spi_edma_lpspi_transfer_master_cm7以20MHz频率运行时的结果。SPI主设备接收到移位了一位的数据，发生了某种错误，如下图所示。

```
FLEXIO Master edma - LPSPI Slave edma example start.
This example use one flexio spi as master and one lpspi instance as slave on oneboard.
Master uses edma and slave uses edma way.
Please make sure you make the correct line connection. Basically, the connection is:
FLEXIO_SPI_master -- LPSPI_slave
    CLK      --    CLK
    PCS      --    PCS
    SOUT     --    SIN
    SIN      --    SOUT
This is LPSPI slave call back.

Master receives:
    FF  FF  FE  FE  FD  FD  FC  FC  FB  FB  FA  FA  F9  F9  F8  F8
    F7  F7  F6  F6  F5  F5  F4  F4  F3  F3  F2  F2  F1  F1  F0  F0
Slave transmits:
    FF  FE  FD  FC  FB  FA  F9  F8  F7  F6  F5  F4  F3  F2  F1  F0
    EF  EE  ED  EC  EB  EA  E9  E8  E7  E6  E5  E4  E3  E2  E1  E0

Error occurred in FLEXIO SPI master <-> LPSPI slave transfer!

End of example.
```

¹ 使用FlexIO模拟四线SPI主设备（文件[AN14175](#)）

使用FlexIO模拟通信和定时外设（文件[AN12174](#)）

图1所示为逻辑分析仪测量到的信号。

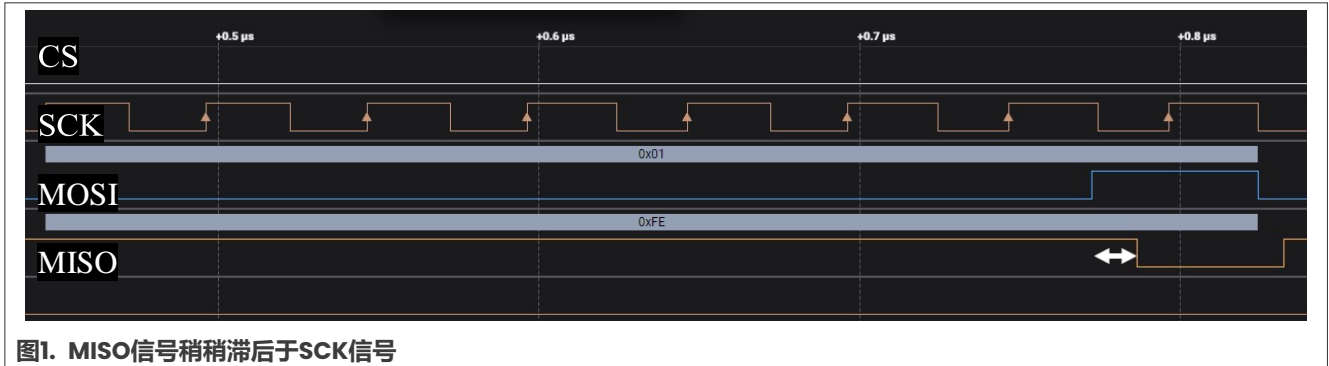


图1. MISO信号稍稍滞后于SCK信号

MISO信号稍稍滞后于SCK信号，因为从设备是由主设备驱动的，而MISO是由SCK的上升沿采样的。所以会导致一位的数据移位。

这就是所谓的建立时间。延迟时间取决于所连接的从设备的速度。

3 通过延迟时钟调整建立时间

3.1 延迟时钟是什么

在单纯的实现方案中，接收器在SCK的上升沿移位，当MOSI信号稍稍滞后于SCK信号时，就会导致一位的移位。通过使用接收器的内部延迟时钟，即使MOSI信号滞后于SCK信号，主设备也能接收到正确的数据。

3.2 配置移位器和定时器

要实现延迟时钟，还需要四个定时器。虽然发送移位器仍由SCK控制，但接收移位器由Delayed SCK（延迟SCK）控制。每个定时器的输出必须遵循此时序图，如图2所示。

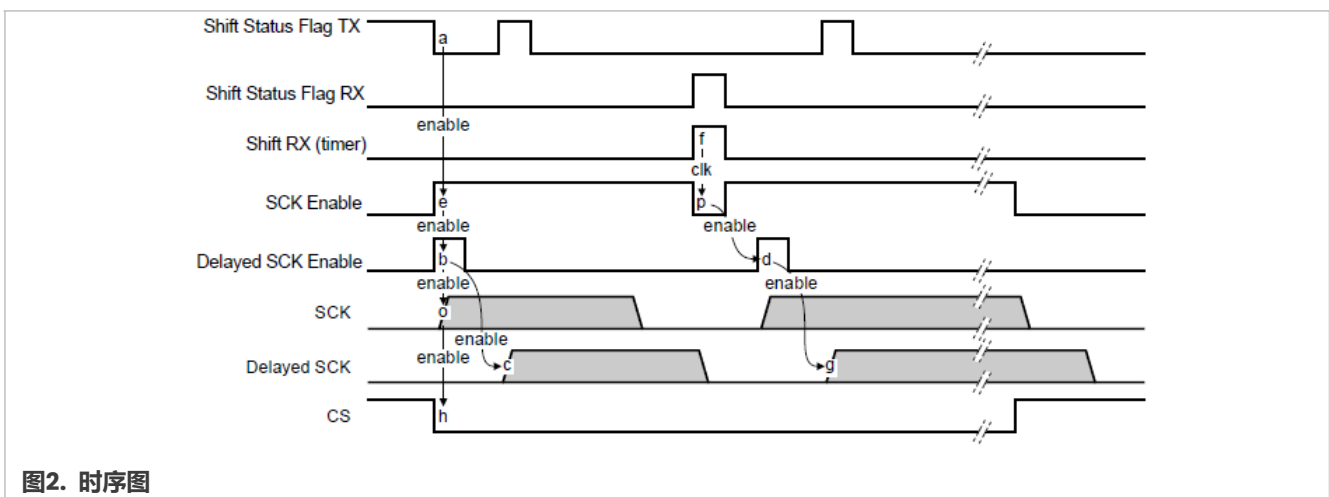


图2. 时序图

- 添加移位器RX以便将移位器状态标志位（SSF）转换为定时器输出。它用于SCK Enable（SCK启用）。
- 当SCK Enabled信号发出时，SCK被启用。当SSF TX为低电平且SSF RX处于下降沿时，SCK Enable信号被发出。

- Delayed SCK Enable信号发出时，Delayed SCK（延迟SCK）启用。Delayed SCK Enable会计算Delayed SCK需要多长的延迟时间。一个单位为一个FlexIO周期。在此演示中，Delayed SCK被配置为延迟两个周期，但它是可定制的。

具体来说，定时器的配置如下。

表1. 定时器配置

定时器	名称	触发器选择	引脚选择	启用条件	关闭条件	递减源
0	Shifter RX	SSF RX	输出(ShifterRxFPin)	触发器上升沿	定时器比较	触发器
1	SCK Enable	SSF TX	输入(ShifterRxFPin)	触发器低电平	定时器比较	引脚
2	Delayed SCK Enable	SCK启用	未使用	触发器上升沿	定时器比较	FlexIO时钟
3	SCK	SCK启用	输出(SCKPin)	触发器上升沿	定时器比较	FlexIO时钟
4	Delayed SCK	Delayed SCK启用	输出(DelayedSCKPin)	触发器上升沿	定时器比较	FlexIO时钟
5	CS	SCK启用	输出(CSxFPin)	触发器上升沿	定时器比较	触发器

3.3 运行演示

要运行示例，请按表2所示进行连接。

表2. 引脚连接

信号	从设备	主设备
MOSI	J10-10	J26-6
MISO	J10-8	J26-4
SCK	J10-12	J26-2
延迟SCK (测试点)	—	J26-10
CS	J10-6	J26-8

1. 移除R200、R406、R408和R404的0Ω电阻。
2. 在PC主机和电路板上的OpenSDA USB端口之间连接一条mini USB线。
3. 在计算机上打开一个OpenSDA串行设备的串行终端，设置如下：
 - 115200波特率
 - 8个数据位
 - 无奇偶校验
 - 1个停止位
 - 无流量控制
4. 将程序下载到目标板。
5. 按下板上的复位按钮或启动IDE中的调试器，开始运行演示程序。

如果示例运行成功，您将在终端上看到以下信息。

```

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  SIN      --      SOUT
This is LPSPI slave call back.

Master receives:
  FF  FE  FD  FC  FB  FA  F9  F8  F7  F6  F5  F4  F3  F2  F1  F0
  EF  EE  ED  EC  EB  EA  E9  E8  E7  E6  E5  E4  E3  E2  E1  E0
Slave transmits:
  FF  FE  FD  FC  FB  FA  F9  F8  F7  F6  F5  F4  F3  F2  F1  F0
  EF  EE  ED  EC  EB  EA  E9  E8  E7  E6  E5  E4  E3  E2  E1  E0
FLEXIO SPI master <-> LPSPI slave transfer all data matched!

End of example.

```

图3所示为Delayed SCK按配置延迟了两个FlexIO周期。

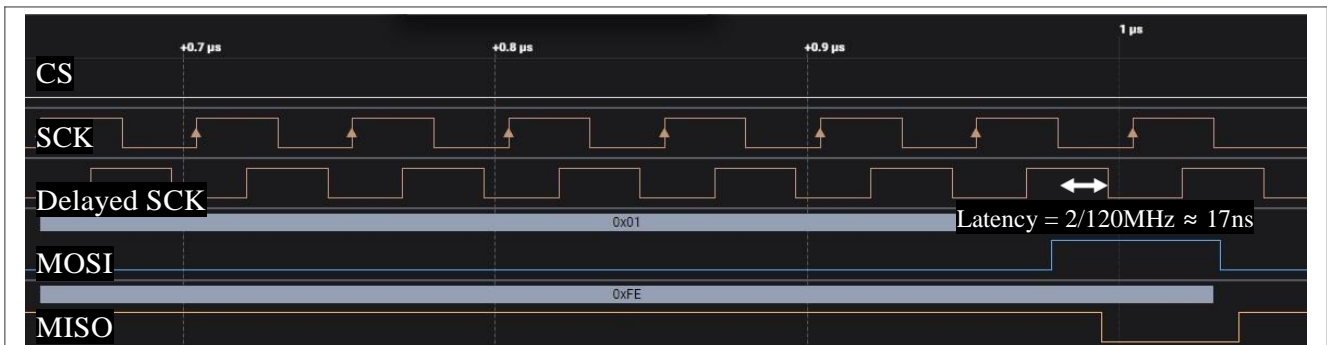


图3. Delayed SCK延迟了两个FlexIO周期

4 结语

通过使用额外的定时器，在FlexIO模拟接口上，甚至能自定义时序参数。

5 关于本文中源代码的说明

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6 修订历史

[表3](#)总结了本文档的修订情况。

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文档ID	发布日期	说明
AN14284 v.1	2024年4月12日	首次公开发布

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