White Paper

Small Cells Call for Scalable Architecture

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Introduction

If 2011 was the year of the heterogeneous network (HetNet) concept[1], Mobile World Congress 2012 in Barcelona was characterized by the emergence of "small cells" as a solution to help operators optimize their network architecture and face the rapidly growing demand for coverage and capacity: currently there are close to 5.3 billion mobile subscribers texting, talking and downloading. By 2015, mobile subscriptions are expected to reach 6.4 billion and mobile data will exceed 30 times that of current levels.

Reducing distance between the user and the base station and reducing the number of instantaneous users seeks to improve the signal quality and allow a higher data rate in both up and down links. The names "femto," "pico" and "micro" are now complementary to the well-known "macrocell" terminology and define a wide range of options for network deployment[2]. They have been considered recently by the standardization bodies under the names "home base station," "local area base station," "medium range base station" and "wide area base station" respectively[3,4]. Additionally, we have the term "metrocell," which defines high capacity, compact equipment deployed in urban areas. Depending on the deployment scenario, metrocell equipment can be a picocell or microcell.

Future networks must offer the best service using the most advanced communication standards while maintaining 2G (GSM) service whose legacy will be continued for some time. How both types of communications are managed simultaneously by the network poses an interesting question. One scenario is that 2G communications are managed by the macro base stations while the small cells focus on providing the most advanced standards (W-CDMA and LTE). This approach means that small cell equipment should be optimized for the fastest data rate to avoid the tight requirements of signal integrity linked to the multi-carrier GSM protocol. A second scenario takes into consideration countries with a solid 2G legacy. Many of these countries will transition directly to 4G without having deployed 3G networks. Moving from 2G to 4G requires equipment designed to manage 2G and 4G standards simultaneously. Based on those considerations, it seems reasonable to think that when pico and femto cells are focusing on 3G and 4G, a high-end portion of small cell equipment will evolve toward broader capabilities (2G, 3G and 4G). For example, microcell equipment may be a downscale version of the multi-standard macrocell base station supporting all types of transmission.

Small cell deployment is expected to follow a similar trend with first applications in the spectrum commonly allocated to 3G (2.1 GHz) and 4G (2.6 GHz). These spectrums are particularly well adapted to short coverage in urban environments where the greatest need exists for high capacity. However, leveraging the new spectrum freed by the digital TV broadcast at 0.7 GHz, we may see small cell deployment in this frequency as well. Considering further extension into the GSM bands, this means that the RF transmitter will target wideband operations in the near future. However, due to the limited number of subscribers that small cells must support, the instantaneous signal bandwidth is significantly smaller than macro base station transmissions.

Along with the complex modulation schemes used by 3G and 4G, advanced antenna schemes are a key technology employed to achieve the high data throughput required by mobile subscribers. The multi input, multi output (MIMO) antenna scheme is now part of the specifications[3,4], and more sophisticated active antenna systems are considered also to further improve network performances[6]. On the other hand, most of the small cells consider only one or two sectors.

All of the above considerations are summarized in table 1.

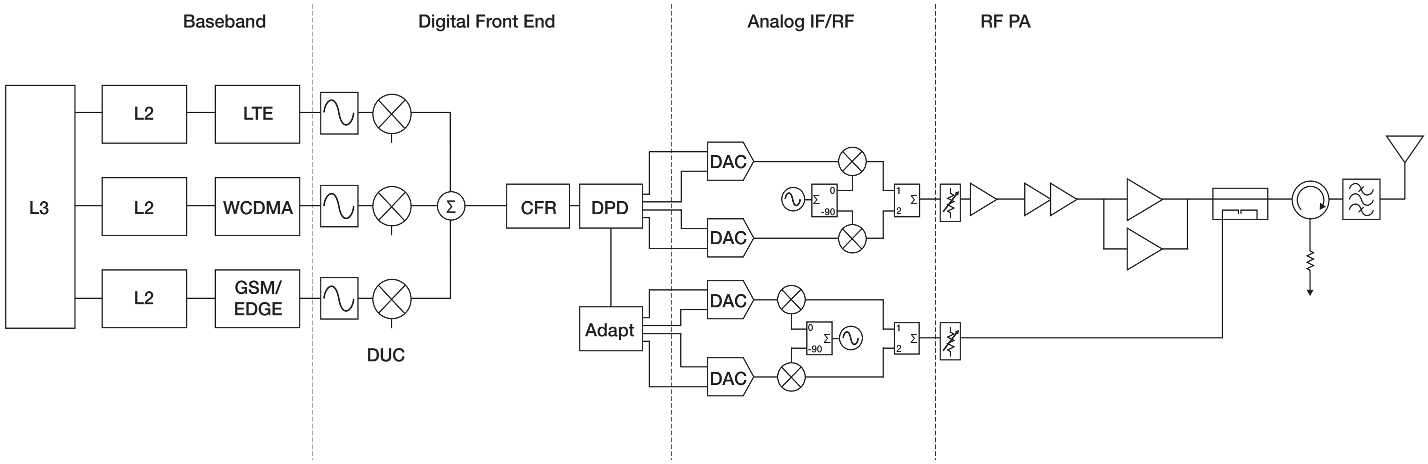
Small cells seem to have a bright future because they are considered the most cost-effective solution to add capacity to existing networks. However, some important challenges remain in order to transform this promise into reality. First, the backhaul. There are solutions, such as fixed fiber, line-of-sight point-to-point radio links at 60 GHz or non-line-of-sight radio below 6 GHz, each of them being particularly well adapted to a different scenario, but there is no one-size-fits-all solution, and this lack of consistency is an issue for operators. The second challenge is managing a network with a significantly larger number of cells. The self organizing network (SON) concept defines the capability of equipment to self-optimize its settings for efficient and consistent transmission, but here again the exact translation in technical specifications depends on the equipment vendor. Finally, small cell equipment must be compact for acceptance in the commercial market and by regulating authorities for positive public opinion. A base station with MIMO 2 x 2 should fit in a volume lower than 10 liters for a weight lower than 10 Kg, including backhaul solutions.

Based on these considerations, this paper analyzes the challenges and opportunities created by new small cell equipment and shows how careful system analysis enables new types of semiconductor solutions for efficient and scalable designs.

Table 1: Small Cell Family, in Contrast with Macrocell Application

Cell		Subscribers	Max Cell Radius (Km)	Max RF Power (dBm)	Standard	Signal Bandwidth (MHz)	RF Spectrum Band	Sector	MMO
Femto	Indoor	4–16	0.01	20	3G/4G/Wi-Fi®	10	1, 3, 7, 34, 38, 40...	1	2 x 2
Pico	In/outdoor	32–100	0.2	24	3G/4G	20	1, 3, 7, 34, 38, 40...	1	2 x 2
Micro/Metro	Outdoor	200	2	38	2G/3G/4G	20,40	1, 2, 3, 5, 6, 8, 7, 13...	1–2	4 x 4
Macro	Outdoor	200–1000	10	50	2G/3G/4G	60–75	1, 2, 3, 5, 6, 8, 7, 13...	3	4 x 4

Figure 1: Single-Sector Multi-Standard Downlink Architecture



System Architecture

The level of performance required for a femtocell is not the same as the requirements for a macrocell; neither are the constraints on cost and manufacturing volume. Femtocell equipment can be plugged into a domestic AC power supply or Ethernet cable, with dedicated constraints on DC power consumption, whereas macrocell equipment must be able to work on a battery, justifying an architecture optimized for power efficiency. Together with the criteria we listed in the first section (channel bandwidth, number of sectors), these examples help define the best architecture for each cell type.

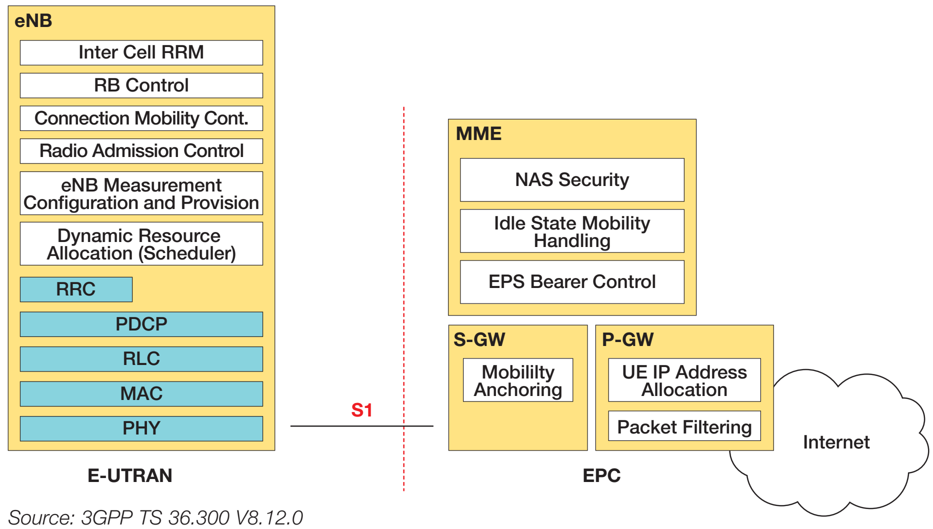
A typical one-sector transmission link is depicted in figure 1 with the important interfaces identified.

Digital baseband processing in an LTE base station (eNB) is divided into several layers (figure 2). L2 and L3 layers can be decomposed in three sub layers: medium access control (MAC), radio link control (RLC) and packet data convergence protocol (PDCP). Typically, these are implemented by a general-purpose processor (GPP) device.

The charts in figure 3 depict the chain of functions building the PHY (L1) layer in an LTE base station. Typically, PHY functions are implemented in the digital signal processing (DSP) device by the DSP cores and baseband accelerators.

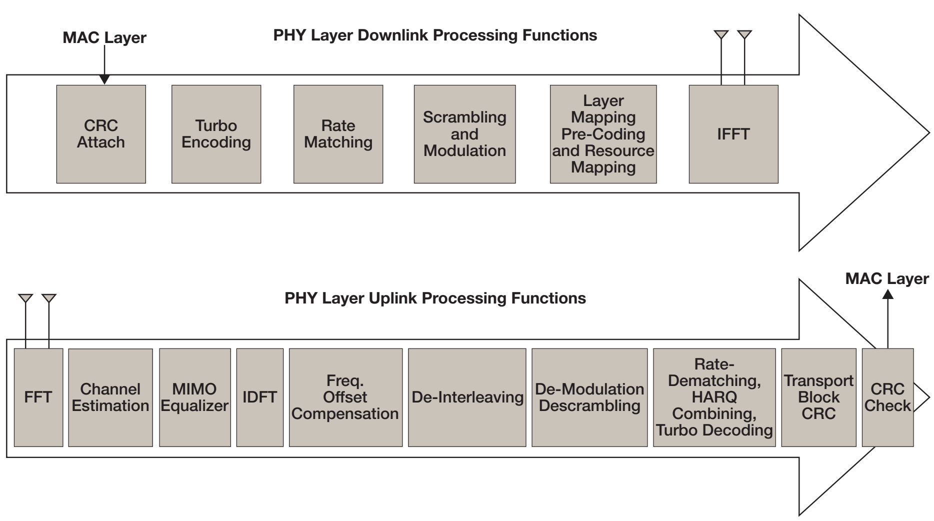
Finally, digital radio front end logic typically in an ASIC, FPGA or off-the-shelf transceiver prepares the signal to be sent to the RF amplifier.

Figure 2: LTE Processing in eNodeB/eNB (LTE Base Station)



Source: 3GPP TS 36.300 V8.12.0

Figure 3: PHY Layer 1 Functions



Digital Baseband Processing Elements in LTE eNodeB (eNB) Base Station

As wireless networks evolve, support for LTE and WCDMA standards and multimode operation with both technologies running simultaneously are becoming requisite. Given the inherent differences between these wireless standards, a number of technical challenges have to be solved on various levels of the processing stacks.

On the L1 physical layer, the 3GPP standards for third-generation WCDMA and next-generation LTE have taken different approaches to modulate and map the data onto the physical medium. As the name indicates, WCDMA is based on code division multiple access and typically requires processing resources to efficiently perform spreading/despreading, scrambling/descrambling and combining operations. These are the main functions needed in the RAKE receiver approach typically used in WCDMA. The L1 operations in WCDMA are a mix of streaming and batch type operations, which the baseband architecture must process efficiently.

In contrast, LTE uses a mix of OFDMA for downlink and SC-FDMA modulation for uplink. This multicarrier approach follows the principle of modulation for orthogonal subcarriers to maximize the spectrum density. The predominant operations in OFDMA/SC-FDMA are the discrete Fourier transforms (DFT) in the form of FFT or DFT and multiply-accumulate operations.

The nature of data organization and subframe structure in LTE allows the L1 processing steps to be scheduled sequentially according to the available subframe user and allocation information. The key challenge is meeting the tight latency budgets of the physical layer processing to maximize the available time budget in the MAC layer scheduler.

Baseband Acceleration and Addressing the Multimode Challenges

With Freescale devices, the physical layer (PHY) on the DSP is implemented using a mix of StarCore SC3850 or SC3900FP high-performance DSP cores and a baseband accelerator platform called MAPLE (multi accelerators platform). The MAPLE accelerators provide highly efficient hardware implementation of the standardized building blocks for each of the air interface standards in single mode and in multimode operations, handling:

- **Fourier transform processing element:** Used primarily in LTE for FFT and DFT Fourier transforms operations as well as RACH operations. It also can be used in WCDMA for frequency domain search and RACH operations. The ability to perform additional vector post and pre-multiplier operations makes this unit also very suitable for correlation and filtering operations.
- **Turbo/Viterbi decoding processing element:** Used for forward error correction (FEC) deploying turbo and Viterbi decoding algorithms in both in LTE/LTE-A and WCDMA. Other functions like CRC calculation, rate de-matching operations and HARQ combining are also covered.
- **Downlink encoding processing element:** Used for FEC deploying turbo encoding algorithms for both LTE/LTE-A and WCDMA and rate matching operations.
- **Chip rate processing element:** Used to accelerate downlink (DL) and uplink (UL) spreading/despreading and scrambling/descrambling operations for both data and control channels. This block is used exclusively for WCDMA and CDMA2K/EV-DO standards.
- **Equalization processing element:** Performs the MIMO equalization operations based on minimum mean square error (MMSE), interference rejection combining (IRC), successive interference cancellation (SIC) or maximum likelihood (ML) approaches, with internal algorithms and outputs done and generated in floating point mathematics. A number of configurable operation modes allow adaptation of the equalization process to the user characteristics and channel conditions. These equalization algorithms are quite complex, requiring substantial computation resources. Hence, Freescale selected to implement the algorithms in hardware acceleration, which is adaptable to different nuances and frees them from the DSP cores, leaving these for other tasks in the processing chain.
- **Physical downlink processing element:** Performs an encoding of the physical downlink shared channel (PDSCH) starting from the user information bits up to the cyclic prefix (CP) insertion and antenna interface handshake. Including DL-MIMO precoding and layer mapping operation.
- **Physical uplink processing element:** Performs decoding of physical uplink shared channel (PUSCH) resulting in decoded information bits.

As mentioned previously, there is a need to support multiple standards concurrently as users slowly migrate to LTE. It is especially important that small cells covering a given, relatively limited cell radius and number of users continue to support multimode while providing an upgrade path for handling more advanced technologies. In order to handle multimode operation, the DSP cores are fully programmable and can implement any standard. The MAPLE hardware block was designed to enable multimode operation such as turbo and Viterbi decoding; turbo encoding and FFT/DFT can operate concurrently on both standards in terms of the algorithms' processing and capacity.

The layer 2 and layer 3 algorithms use a mix of Power Architecture® general-purpose, high-performance cores and security acceleration. Most of this processing is done on programmable cores where any standard including multimode operation can be implemented efficiently. The commonality between WCDMA and LTE is the requirement for secure backhaul processing. The bulk of this is Ethernet, QoS, IPSec and WCDMA frame protocol processing, which is offloaded to hardware acceleration and leaves software flexibility for the actual L2 stacks of both standards.

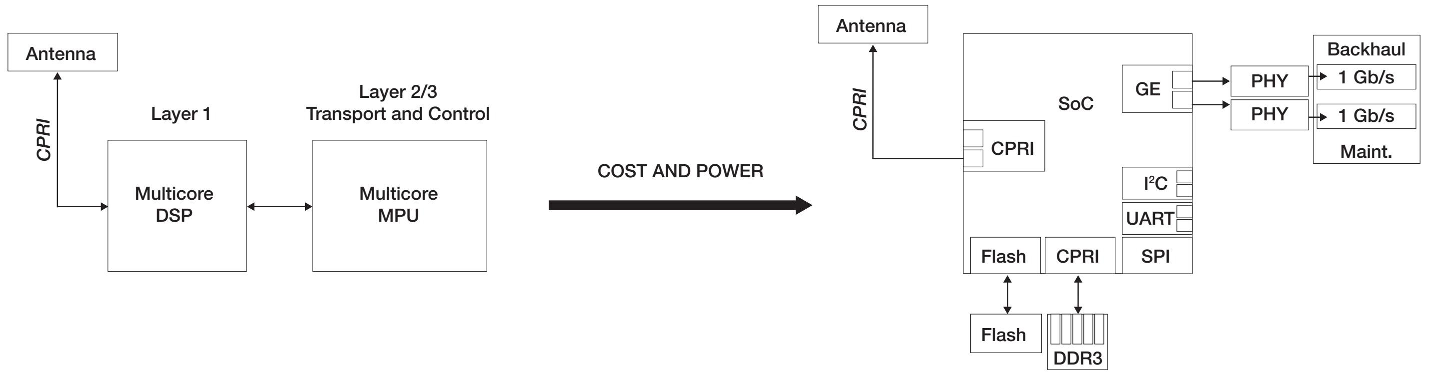
Meeting the Latency Budget

To ensure continued competitiveness to 3G technology, the 3GPP standards body based LTE on orthogonal frequency division multiplexing (OFDM) and MIMO antenna techniques. The major performance goals are significantly increased data rates, reduced latencies and improved spectrum efficiencies.

Latency is a key network metric and has a major influence on a user's experience both in voice calls and data transactions such as video and Internet applications. The key challenge is meeting the tight latency budgets of the PHY processing to maximize the available time budget for the rest of the PHY processing and MAC layer scheduler tasks. The LTE standard defines the end-user roundtrip latency at less than 5 ms, which requires the latency within the base station to be significantly lower (less than 0.5 ms in DL and less than 1 ms in UL).

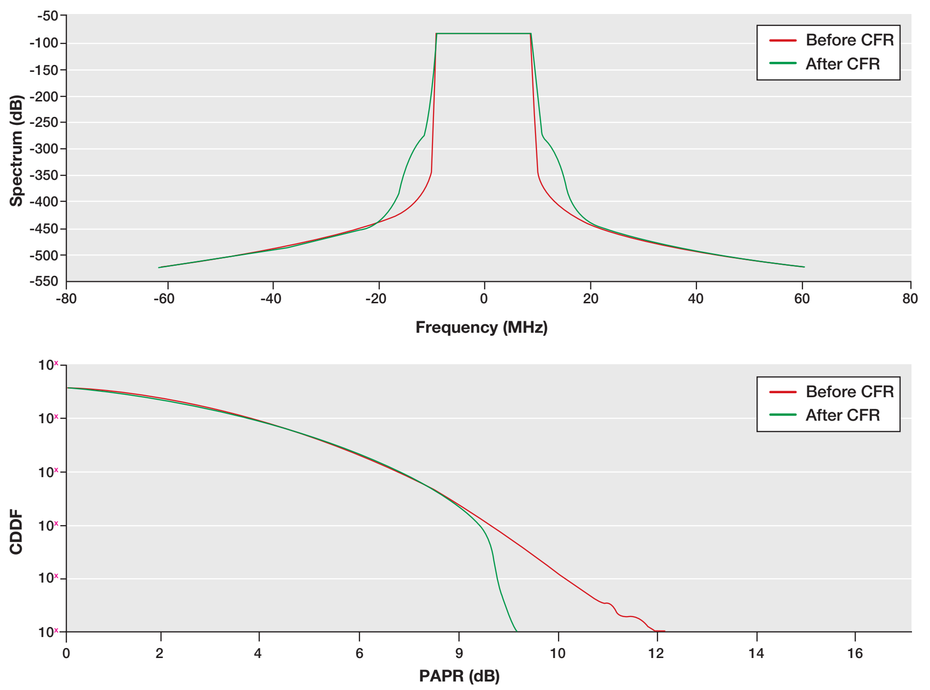
MIMO equalization/detection and FEC are heavily used in newer, high bit-rate wireless communication standards such as LTE and WiMAX. The MIMO equalizer and turbo coding error correction algorithms both in UL and DL are the major influencers on base station throughput and latency.

Figure 4: Baseband Integration



In typical macro and micro base stations, the baseband channel card is composed of a single GPP device and multiple DSP devices to handle scalable and variable numbers of sectors, the number of users and throughputs based on the specific deployment requirements. Alternately, femto, pico and metrocell base stations typically handle a single sector and a given number of users and data throughputs. The traditional single GPP device and single DSP discrete device paradigm is evolving into a single unified system-on-chip (SoC) solution (see figure 4).

Figure 5: LTE 20 MHz Spectrum and CCDF



Digital Front End (DFE)

The DFE receives the different signals created by the baseband processing board and prepares them to be physically transmitted to the RF transmitter. In a standard 3G radio lineup, its first function is multiplexing and combining the different carriers, the second is peak-to-average power ratio (PAPR) limiting (i.e. crest factor reduction) and the third is RF hardware linearization (i.e. digital predistortion).

Digital Up Converter (DUC): Receives the different carriers created by layer 1, which can be of different natures (for example: one carrier LTE + one carrier WCDMA), pulse shapes and sums them according to the carrier specified pattern. This operation involves oversampling and filtering functions.

In a macro base station, the RF power amplifier contributes the most to the overall power consumption and it is imperative to allocate baseband processing resource to increase the RF power amplifier efficiency. In small cell equipment, it makes sense to carefully investigate the overall digital and RF front-end architecture, as the power consumed in the baseband processing and transceiver chips may offset the gain obtained in the RF power amplifier. The main features involved to increase RF lineup efficiency are crest factor reduction (CFR) and digital pre-distortion (DPD).

Crest Factor Reduction: Complex modulated signals vary in both amplitude and phase. When they can be described in the frequency domain by their power spectrum, we can characterize the amplitude in the time domain by its statistical distribution (figure 5). This analysis extracts the PAPR, which is used to size the RF power amplifier devices; if one needs to transmit 30 dBm average with a signal PAPR=10 dB, the RF PA saturated power (Psat) should be in excess of 30+10=40 dBm. Then, the PAPR dictates the minimum back-off from Psat (OBO) at which the PA operates most of the time. This has a direct consequence on the amplifier efficiency as this parameter lowers when OBO increases (figure 6). Consequently, reducing the PAPR helps to reduce both the RF PA device size (as well as cost) and its power consumption. Due to its impact on the equipment performance, CFR is a clear differentiator among competitive solutions[7].

Digital Pre-Distortion: Amplitude modulated signals create challenges for the amplifier as its non-linear behavior creates in-band (EVM impacting) and out-of-band (spectral regrowth) distortion. To meet linearity specifications and increasing RF PA efficiency requirements, the PA must be linearized and DPD is the most popular linearizer scheme in wireless cellular infrastructure applications today (see figure 7).

A key step in DPD consists in approximating the PA behavior by a behavioral model. The level of the correction depends on the model accuracy and its capacity to follow the PA behavior variations. Such variations can be "slow" compared to the signal envelope variations. For example, this is the case of temperature, carrier frequency or output power variations. PA behavior variation can also be fast (comparable to the envelope speed) and can depend on the previous PA state. This dependency to the past is called "memory effects." The lower the contribution of memory effects, the easier the correction.

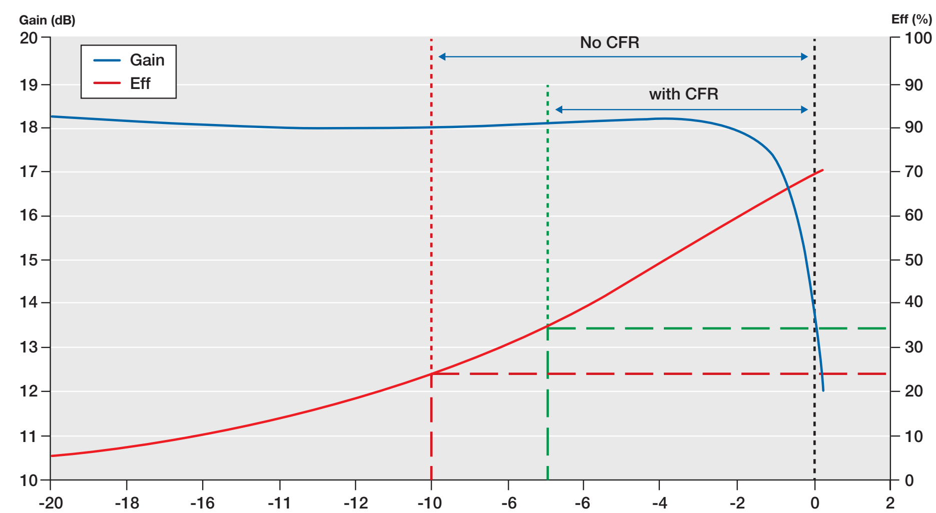
Memory effect content depends on the PA architecture: when Class A or Class AB PA show low memory effect (but low efficiency), Doherty amplifiers exhibit significantly larger memory effects (and higher efficiency). Then, the burden put on DPD to meet linearity specifications depends on the PA architecture.

The simplest DPD scheme is an open-loop correction without memory effects compensation, based on the static AM/AM and AM/PM PA behavior. The more complex DPD architecture is closed loop with memory correction (based, for example, on Volterra series) and requires a demodulation path to sample the output signal and compare it to the desired transmitted one.

On the Rx path, the DFE gets the multi-carrier uplink signal, extracts and filters each carrier to be transferred to the PHY layer. The functional blocks described above typically fall under the umbrella of the DFE. Depending on the transmitter architecture, some of those can be eliminated or others can be added. For example, in the case of an envelope tracking PA, which is a competitive architecture with Doherty to increase average efficiency, the DFE also includes the drain envelope signal generation together with its synchronization with the RF path.

There are different possibilities to implement the DFE functionalities in practical hardware: FPGA, ASIC and DSP. Each has its strength and weakness in terms of flexibility, cost and power consumption and those aspects have to be taken into consideration when defining the overall system architecture.

Figure 6: Single-Stage Class AB PA Gain and Efficiency



RF/IF Transceiver

The RF/IF transceiver design depends upon the transmitted signal; GSM or LTE require a different resolution and dynamic range for the DAC and ADC. Also, CFR and/or DPD may impact this resolution marginally.

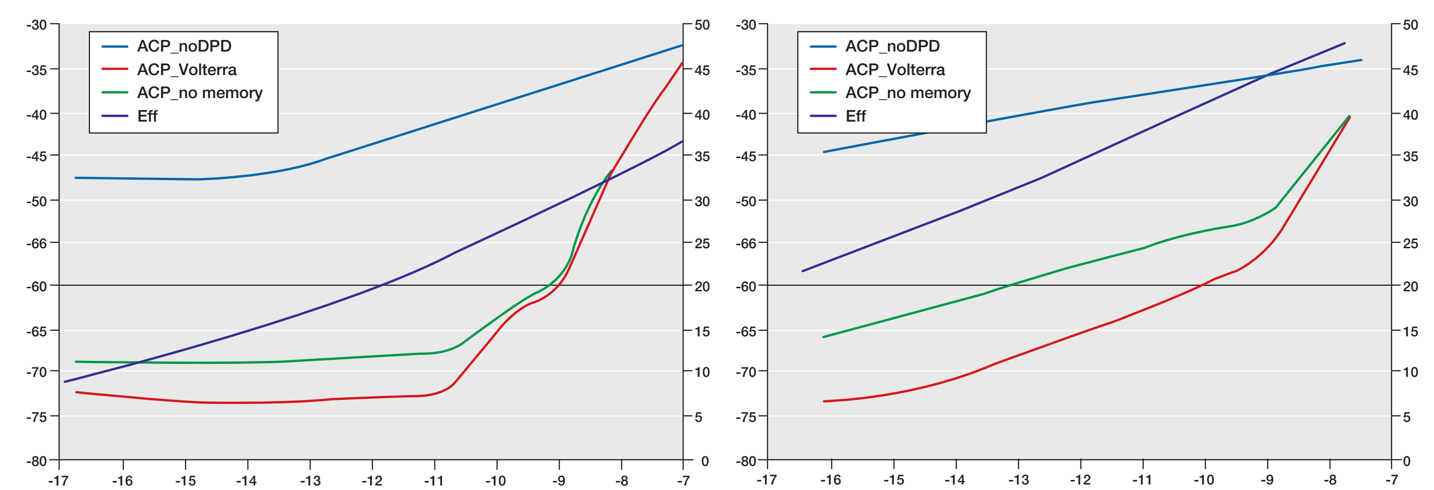
Conversion speed depends not only on the signal bandwidth, but also on the presence or absence of DPD, because the pre-distorted signal should be able to include up to fifth order intermodulation products to allow good correction.

DPD may also require an additional return path to sample the output signal back to the DFE for adapting the pre-distorted signal. This added complexity has a cost, which should be justified or offset by the system performance improvements.

RF PA Transmitter

We have shown how DFE features are linked with the RF front end architecture and both should be optimized together for optimum system performances. Compared to macrocells, small cells present an additional

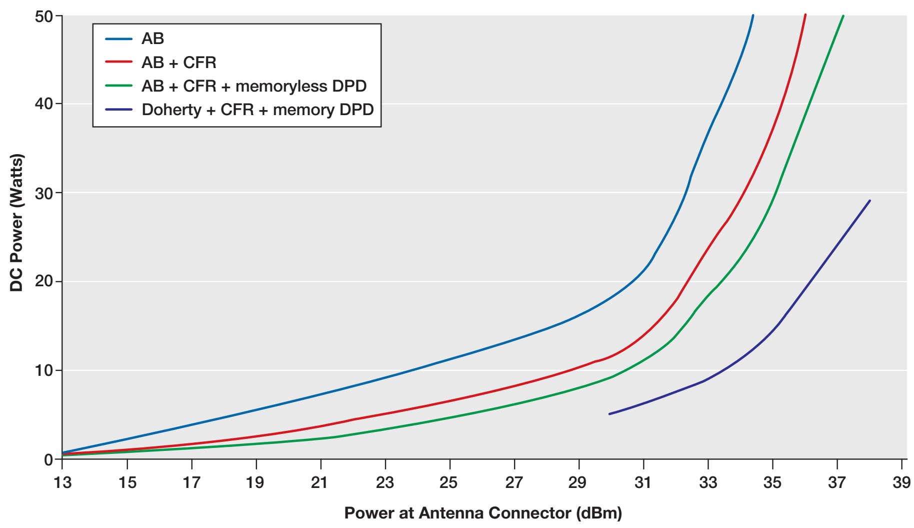
Figure 7: Final Stage PA, Simulated ACP with and without DPD



Class AB PA: ACP vs. OBO, LTE 20 MHz, PAR=9 dB

Doherty PA: ACP vs. OBO, LTE 20 MHz, PAR=9 dB

Figure 8: DC Power Budget for the RF Amplifier



challenge in that the DC power consumed by the baseband signal processing is no longer negligible compared to the power consumed by the RF power amplifier and a careful analysis should be done to define the best system architecture.

Based on realistic performances of RF power transistors (5 V GaAs, 28 V LDMOS) and RF power amplifier architectures (class AB, Doherty), an analysis has been performed to estimate a budget for the DC power required by the RF power amplifier for the different small cell types and frequencies. Figure 8 compares the performances for the different scenarios. These figures apply for >50 dB gain lineup, and signals showing PAR=10 dB without CFR, PAR=7 dB with CFR (@0.01 percent probability). Depending on the power amplifier architecture and DPD scheme, margin for linearity varies from 4 to 1 dB. The figures consider 3 dB losses between the output of the power amplifier and the antenna connector to account for the isolator and filters blocks.

From figure 8, we can extract the following assessments: for low-power transmitters (<15 dBm), there is no need for CFR or DPD. For medium power (15<pout<24 dBm), CFR brings an interesting improvement for a modest increase of system complexity and cost. For larger power (>24 dBm), linearization helps to maintain the RF transmitter consumption at a reasonable level and Doherty architecture is required above 31 dBm.

This analysis highlights how system performance can be improved with CFR and DPD, together with an optimized RF amplifier architecture, but equivalent analysis measuring DC power consumption and estimating the cost associated with the signal processing features implemented by the DFE is needed to achieve optimum system definition, keeping in mind that figure 8 is based on a single RF transmitter, when usual equipment includes at least two, sometimes four, RF power amplifiers for enabling MIMO transmission.

Still, there are side effects that need to be considered to get the full picture: improving power amplifier efficiency is not only "green" from a pure power point of view, but also dictates the need for managing the dissipated power. For example, it impacts the RF device mounting (bolt down, PCB with copper coin, true SMD mounting on PCB with via holes) and the cooling principle chosen (forced convection with fan, free air convection). Consequently, equipment size and cost are directly impacted by the DFE and RF front end choices.

Freescale Solutions

Baseband Processing Solutions

Unlike some competitors, Freescale's ownership of the key intellectual property (IP), coupled with deep engagement with leading original equipment manufacturers (OEMs) in the wireless access market, puts the company in a unique position to define architectures and drive integration that provides performance, power and cost benefits. Being relatively independent from external IP provider's next-generation technologies and timelines enables Freescale to drive a roadmap of devices that helps OEMs meet targets for performance and timelines for their next-generation wireless technologies.

The key processing elements in any device for mobile wireless infrastructures are the programmable cores, hardware accelerators, internal interconnects and high-speed interfaces. Freescale has long been an embedded processing leader. The market-proven Power Architecture core is at the heart of our strength and has been used by leading wireless OEMs worldwide for many years. Significantly enhanced from generation to generation, it comes with a rich ecosystem to provide customers with a seamless migration from their current products to higher performance products.

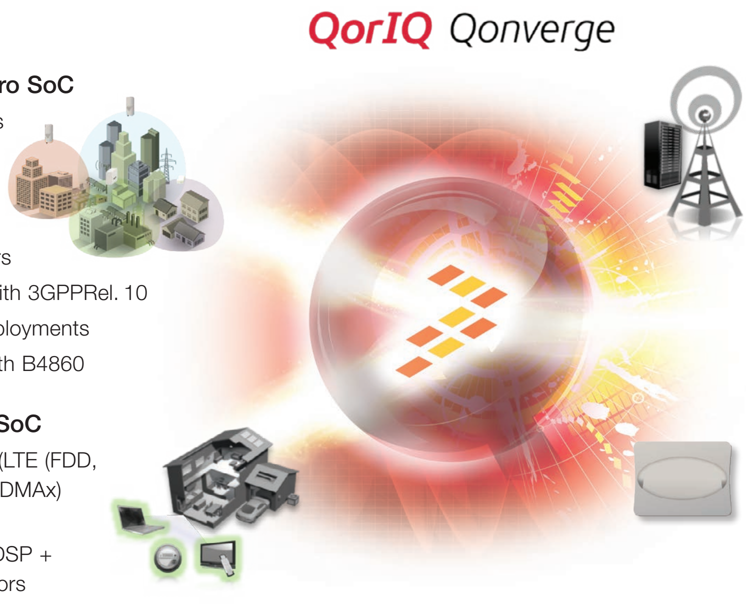
The StarCore DSP core has been enhanced by Freescale from generation to generation for more than a decade and is known for its high performance and programmability. The SC3850 is used today in DSP devices deployed by many of the wireless manufacturers in LTE, WCDMA and WiMAX deployments and has earned leading results from top benchmarking firms.

Other important components are the internal fabric, accelerator throughputs and standards compliance. The internal fabric is a component that connects all processing elements and memories within the device; it must enable high throughputs and low latencies for data movement throughout the SoC as well as preventing stalling of any of the elements attached to it for processing data. Both the internal fabric and the accelerators are proven to be highly efficient and were field deployed by Freescale customers.

Device Architectures and Capacities

Leveraging the StarCore and Power Architecture legacies, Freescale has developed a family of software-compatible devices that scale from femtocells to macrocells: the BSC9130/31 targets femtocell applications (16 users) embedding 1xe500 power amplifier core and 1xSC3850 DSP core, the BSC9132 is optimized for pico base station, addressing up to 100 users with 2xe500 power amplifier cores and 2xSC3850 DSP cores.

Figure 9: Freescale QorIQ Qonverge SoC for Base Stations



B4420 Micro/Metro SoC

- Hundreds of users
- High throughputs
- Multistandard and multimode
- One to two sectors
- Full compliance with 3GPPRel. 10
- Ready HetNet deployments
- Pin compatible with B4860

BSC9131 Femto SoC

- Eight to 16 users (LTE (FDD, TDD), WCDMA, CDMAx) and multimode
- One MPU + one DSP + wireless accelerators

B4860 Macro SoC

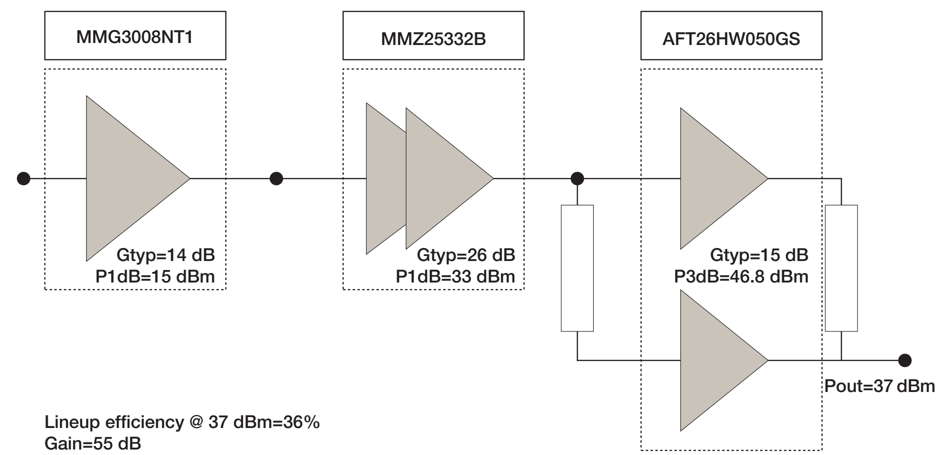
- Very high throughputs
- Thousands of users
- Multisector
- Multistandard and multimode
- Full compliance to 3GPPRel. 10
- New advanced cores and acceleration technologies
- Ready for cloud and HetNet deployments

BSC9132 Pico SoC

- 32 to 100 users (LTE (FDD, TDD), WCDMA) and multimode
- Two MPU + two DSP + wireless accelerators

To address the high-end portion of the wireless infrastructure market, Freescale introduced the B4420 for microcells and the B4860 for macrocells in 2012, both built around the latest DSP and Power Architecture cores (SC3900FP and e6500 respectively) (see figure 9).

Figure 10: Freescale RF Lineup for 5 W @ 2.6 GHz

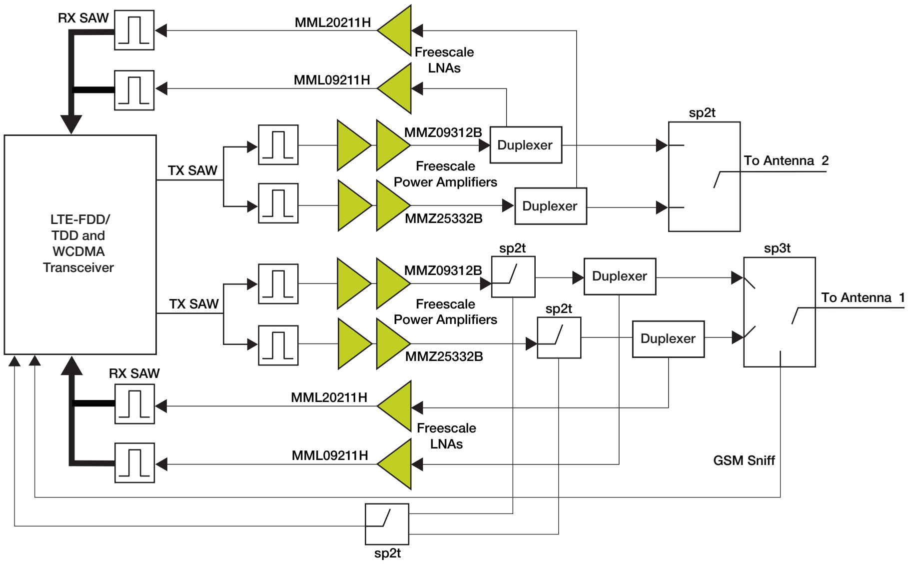


RF Front End

Freescale is a clear leader in RF power products for cellular infrastructure applications and holds a solid number one market share position with the broadest product portfolio in the industry from femto to macro cells[8]. Under our new Airfast brand, Freescale offers innovative RF solutions integrating the latest developments in die technologies, package concepts and system architecture expertise.

Leveraging these advantages, Freescale provides optimized solutions for small cells. Recently, the company released the AFT26HW050GS, an in-package single-stage Doherty for 2.6 GHz LTE applications based on the latest 28 V LDMOS generation. The AFT26HW050GS is designed specifically for wide instantaneous bandwidth micro/metro cell LTE applications between 2500–2700 MHz and exhibits 48 percent drain efficiency at 8 dB output backoff from its saturated power, the highest reported in the industry at the 2.6 GHz. To drive the final stage, Freescale offers the MMZ25332, two-stage class AB 5 V InGaP HBT MMIC, exhibiting 25 dB linear gain and 33 dBm output power at 1 dB compression over 1.8–2.7 GHz. To complement the lineup, Freescale provides the MMG3008, a broadband general-purpose amplifier in the SOT89 SMD low-cost package (see figure 11 on next page).

Figure 11: Dual-Band RF Front End for Femto Base Station



The MMZ25332 is not only an excellent driver, it can be used in a pico base station as final stage with an output power up to 24 dBm, where its embedded output power detector opens the door for power control and alarm information. On the receive path, Freescale offers a state-of-the-art, single-stage, low-noise amplifier built on E-Phemt 5 V GaAs technologies.

As an example illustrating the effectiveness of a clever system approach, the block diagram in figure 11 describes the RF front end of a femto dual-band reference board designed to work with the BSC913X SOC.

Conclusion

This paper analyzes the new requirements relating to the emergence of small cells and identifies paths for system optimization. Particularly, it demonstrates how the baseband processing features and the RF transmitter architecture should be considered together to achieve optimum cost and performances.

Freescale is approaching this market by providing scalable baseband signal processors and RF solutions. Associated with a very broad device portfolio, a set of design tools completes the ecosystem allowing customers to design in a consistent and stable environment with reduced time to market.

How to Reach Us:

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