

UM12624

FRDMGD3130HB2EVM half-bridge evaluation board

Rev. 1.0 — 15 September 2026

User manual

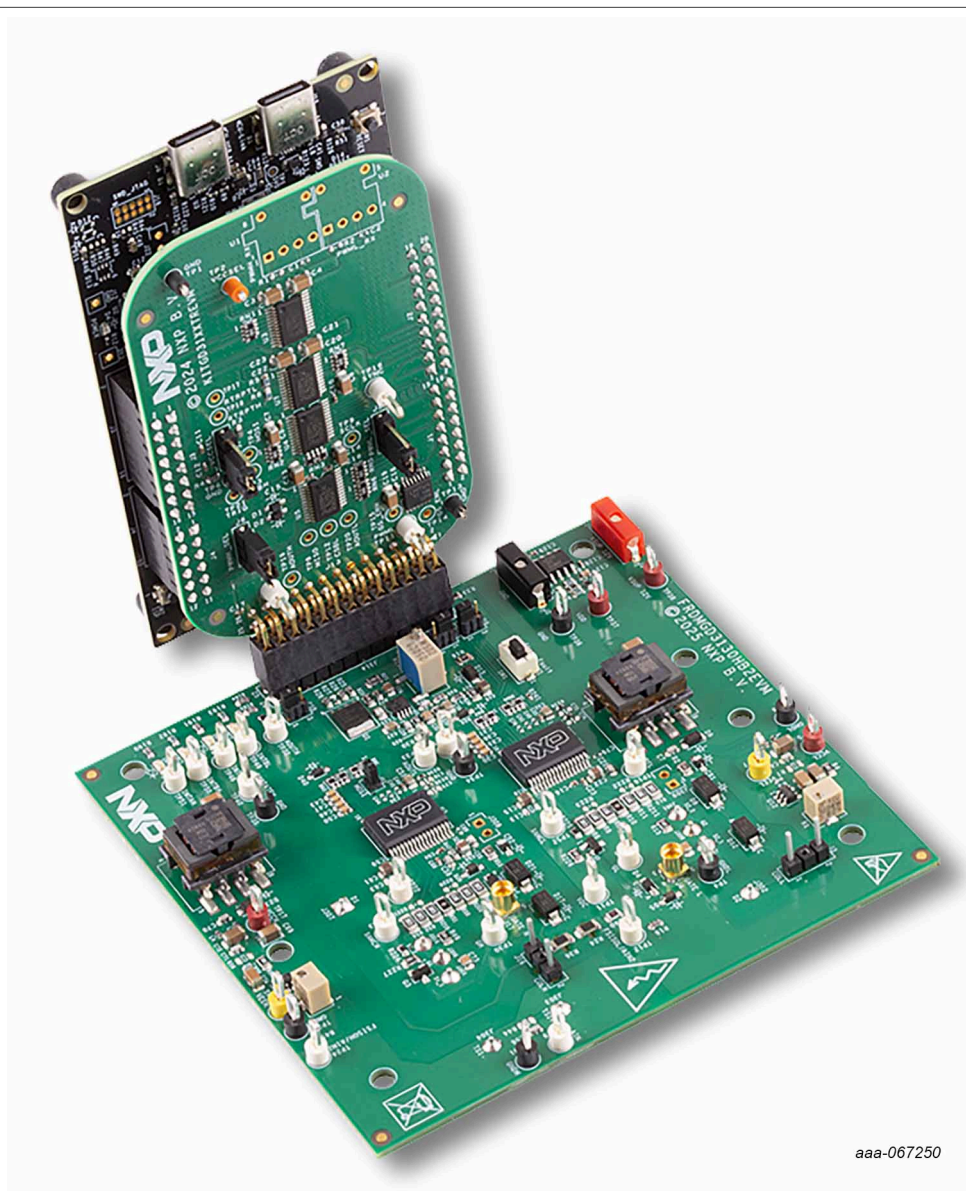
Document information

Information	Content
Keywords	Gate driver, half bridge, GD3130
Abstract	This user manual guides the reader through the features of the GD3130 and FRDMGD3130HB2EVM evaluation kit.



1 Introduction

[Figure 1](#) shows the FRDMGD3130HB2EVM half-bridge evaluation board connected to the KITGD31XXTREVM (translator + MCU) board to use with the FlexGUI 2 software.



aaa-067250

Figure 1. FRDMGD3130HB2EVM evaluation kit

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Evaluation kits or reference designs are intended solely for technically qualified professionals, specifically for use in research and development environments to facilitate evaluation purposes.

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The evaluation kit or reference design is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation kit or reference design may be used with any development system or other source of I/O signals by connecting it to the host MCU or computer board via off-the-shelf cables. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality. This evaluation kit or reference design provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end device incorporating the evaluation product. Due to the open construction of the evaluation product, it is the responsibility of the user to take all appropriate precautions for electric discharge. To minimize risks associated with the customers' applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

2 Finding the kit resources and information on the NXP web site

The NXP analog product development boards provide a platform for evaluating NXP products. The boards support a range of analog, mixed-signal, and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology.

The information page for FRDMGD3130HB2EVM evaluation kit is at <https://www.nxp.com/FRDMGD3130HB2EVM>. The overview tab provides an overview of the device, product features, a description of the kit contents, a list of (and links to) supported devices, a list of (and links to) any related products, and a Get Started section.

The Get Started section provides links to everything needed to start using the device and contains the most relevant, current information applicable to the FRDMGD3130HB2EVM.

1. Go to <https://www.nxp.com/FRDMGD3130HB2EVM>.
2. On the Overview tab, locate the Jump To navigation feature on the left side of the window.
3. Select the Get Started link, review each entry, and download an entry by clicking the title.
4. After reviewing the Overview tab, visit the other product-related tabs for additional information:
 - **Documentation:** download current documentation
 - **Software and tools:** download current hardware and software tools
 - **Buy/Parametrics:** purchase the product and view the product parametrics

After downloading files, review each file, including the user guide, which includes setup instructions. If applicable, the bill of materials (BOM) and supporting schematics are also available for download in the Get Started section of the Overview tab.

3 Getting ready

Working with the FRDMGD3130HB2EVM evaluation board requires the kit contents, additional hardware, and a Windows PC workstation with installed software.

3.1 Kit contents

The FRDMGD3130HB2EVM kit includes:

- Assembled and tested FRDMGD3130HB2EVM board in an anti-static bag
- 3.3 V to 5.0 V translator board (KITGD31XXTREVB) connected to the FRDM-MCXA153
- USB cable, type A male/type C male
- Quick start guide

3.2 Required hardware

- Compatible HybridPACK Drive G2 SiC MOSFET module
- DC-link capacitor compatible with the HybridPACK Drive G2 module
- 1.27 mm jumpers for configuration (included with kit)
- 30 μ H to 50 μ H, high current air core inductor for double pulse testing
- HV power supply with protection shield and hearing protection
- 12 V, 1.0 A DC power supply
- 500 MHz 2.5 GS/s 4-channel oscilloscope
- Rogowski coil, PEM Model CWT Mini HF60R, or CTW MiniHF30 (smaller diameter)
- Isolated high-voltage probes
- Digital voltmeter

3.3 Minimum system requirements

The evaluation kit requires the following to function properly with the software:

- Windows 11 or higher operating system

4 Getting to know the hardware

4.1 Kit overview

The FRDMGD3130HB2EVM is a half-bridge evaluation kit populated with two GD3130 single-channel gate drive devices. The kit includes the Freedom MCXA153 microcontroller hardware for interfacing with a PC installed with the FlexGUI 2 software for communication to the serial peripheral interface (SPI) registers on the GD3130 gate-drive devices in either daisy chain or standalone configuration.

The KITGD31XXTREVB translator board is used to translate 3.3 V signals to 5.0 V signals between the MCXA153 MCU and the GD3130 gate drivers. The evaluation kit can be connected to a compatible insulated gate bipolar transistor (IGBT) or SiC module for half-bridge evaluations and applications development.

4.2 Board features

- Able to connect to the HybridPACK Drive G2 module for half-bridge evaluations
- Adjustable negative VEE gate low-drive level (0 V to -10 V DC)
- Adjustable VCC gate high-drive level (10 V to 25 V DC)
- Configurable jumper for disabling dead-time fault protection when short-circuit testing
- Accessible power, ground, and signal test points
- Install and use FlexGUI 2 to interface via SPI through PC; software includes double-pulse and short-circuit testing capabilities
- DC-link bus voltage monitor on low-side driver via AIN and AOUT
- Temperature-sense connection and configurable for monitoring power-module temperature

4.3 Device features

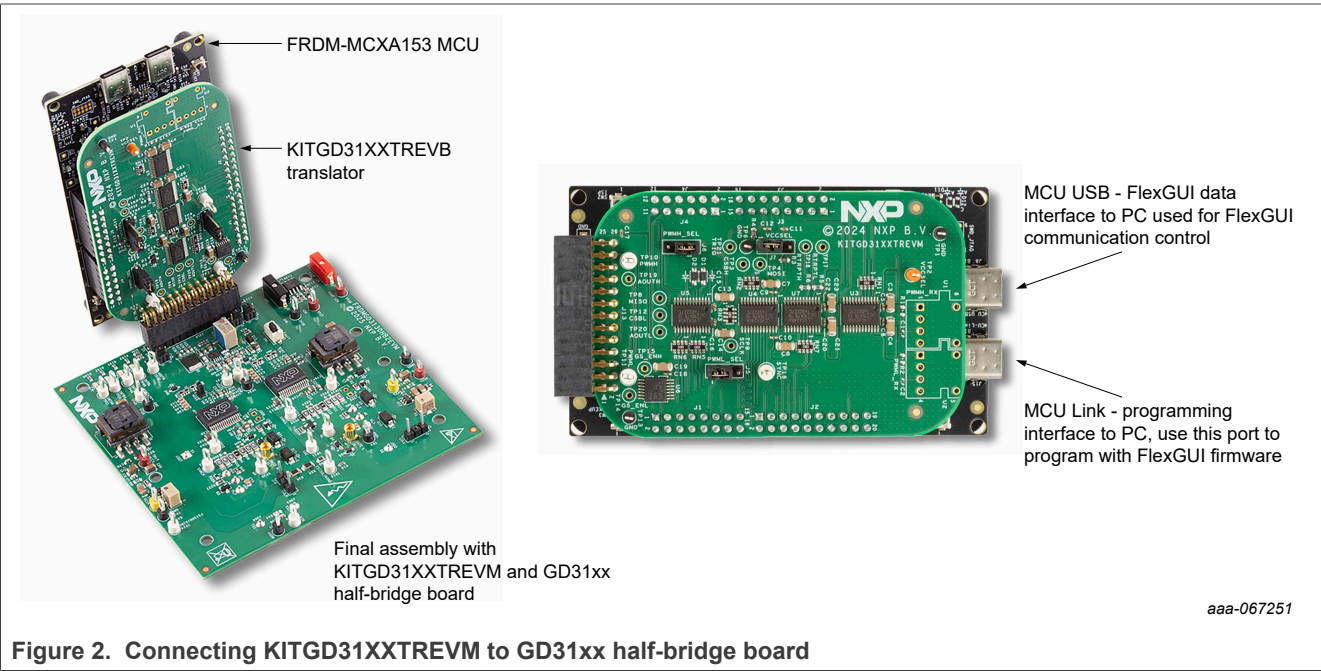
Table 1. Device features

Device	Description	Features
GD3130	The GD3130 is an advanced, single-channel gate driver for IGBT and SiC with dynamic gate strength adjust.	• DESAT detection capability for detecting V_{CE} desaturation condition • Fast short-circuit protection for IGBT and SiC MOSFETs • Compliant with ASIL C and ASIL D ISO 26262 functional safety requirements • SPI for safety monitoring, programmability, and flexibility • Integrated galvanic signal isolation up to 8 kV • Integrated boost capability for increased drive strength • Interrupt pins for fast response to faults and real-time reporting capability • Compatible with negative gate supply • Active bus discharge functionality • XAMC predriver output to drive external logic level FET for higher AMC current

4.4 Board description

The FRDMGD3130HB2EVM is a half-bridge evaluation board populated with two GD3130 single-channel IGBT or SiC gate-drive devices. The board supports connection to an MCXA153 microcontroller for SPI communication configuration, programming, and monitoring. The board includes DESAT circuitry for short-circuit detection and implementation of GD3130 shutdown protection capabilities.

The evaluation board is designed to connect to a HybridPACK Drive G2 module for evaluation of the GD3130 performance and capabilities.



4.4.1 Low-voltage logic and control connector

Low-voltage domain is 5 V VDD domain that interfaces with the MCU and GD3130 control registers through a 26-pin connector interface.

Low-side driver and high-side driver domains are driver-control interfaces to HybridPACK Drive G2 module single-phase connections and test points.

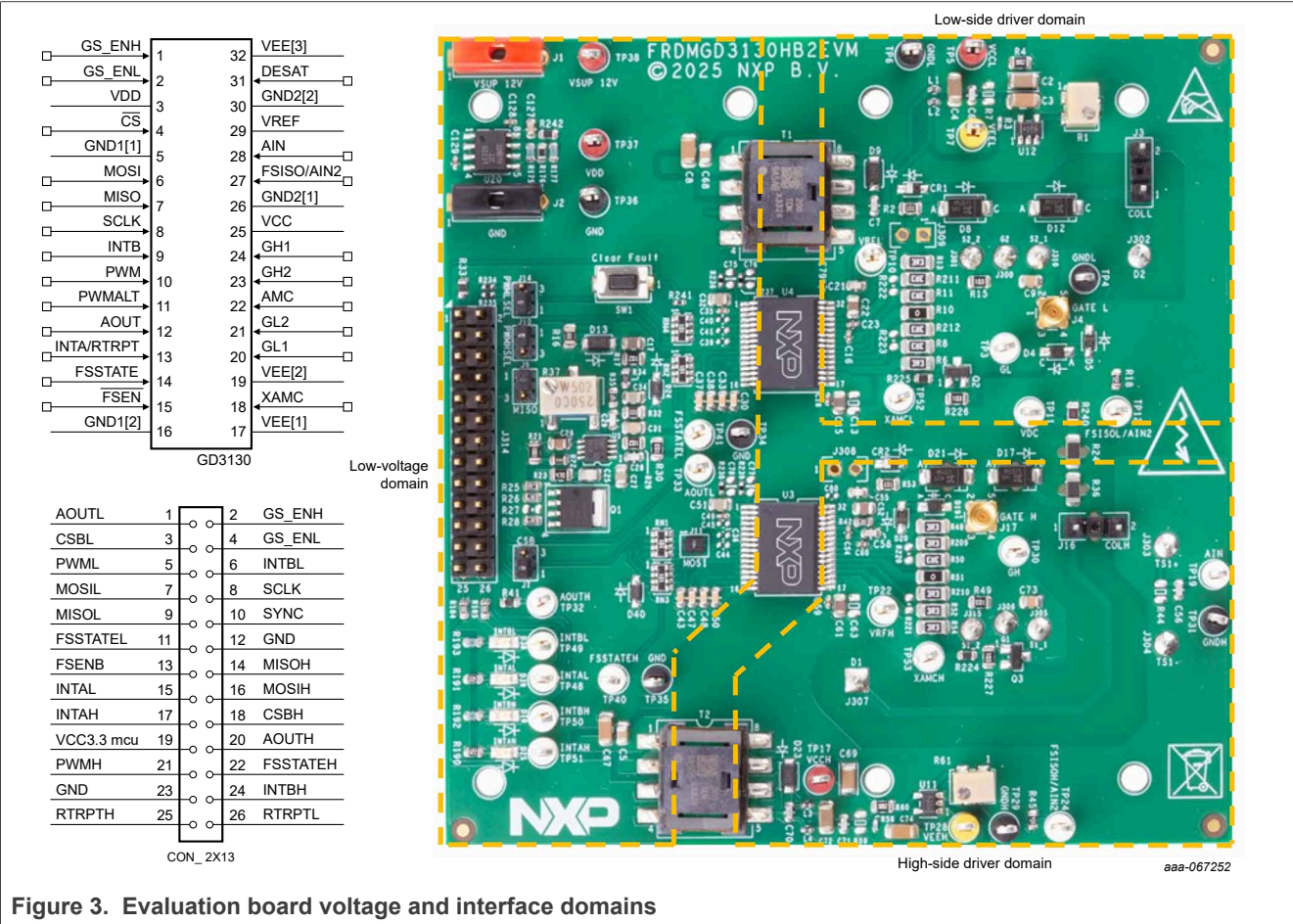


Figure 3. Evaluation board voltage and interface domains

Table 2. Low-voltage domain 26-pin connector definitions

Pin	Name	Function
1	AOUTL	Analog output, duty-cycle encoded signal (low side) for reading temperature via AIN and voltage via AIN2
2	GS_ENH	Gate strength enable high – gate-drive pullup strength control logic
3	CSBL	Chip select bar (low side)
4	GS_ENL	Gate strength enable low – gate-drive pulldown strength control logic
5	PWML	Pulse width modulation (PWM) input (low side)
6	INTBL	Interrupt bar (low side)
7	MOSIL	SPI input (low side)
8	SCLK	Serial clock input
9	MISOL	SPI output (low side)
10	SYNC	No connect
11	FSSTATEL	Fail-Safe state (low side)
12	GND	Ground
13	FSENB	Fail-safe enable (high side and low side)
14	MISOH	SPI output (high side)
15	INTAL	Fault reporting and real time V_{CE} and V_{GE} monitoring (low side)
16	MOSIH	SPI input (high side)
17	INTAH	Fault reporting and real time V_{CE} and V_{GE} monitoring (high side)
18	CSBH	Chip select bar (high side)
19	NC	No connect
20	AOUTH	Analog output, duty-cycle encoded signal (high side) for reading temperature via AIN and voltage via AIN2
21	PWMH	PWM input (high side)
22	FSSTATEH	Fail-safe state (high side)
23	GND	Ground
24	INTBH	Interrupt bar (high side)
25	RTRPTH	Real-time reporting pin VGEMON or VCEMON (high side)
26	RTRPTL	Real-time reporting pin VGEMON or VCEMON (low side)

4.4.2 Test-point definitions

All test points are clearly marked on the evaluation board. [Figure 4](#) shows the location of various test points.

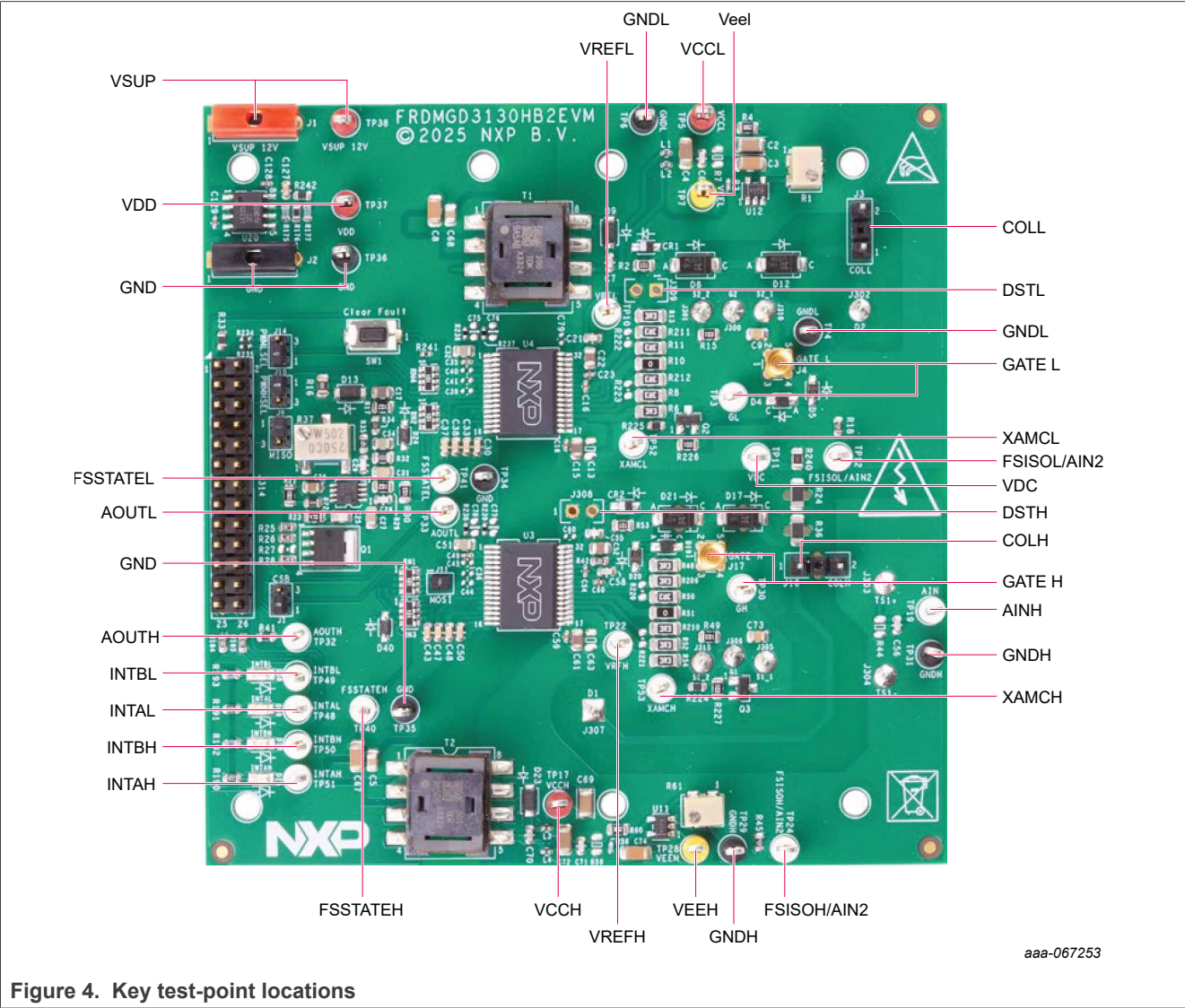
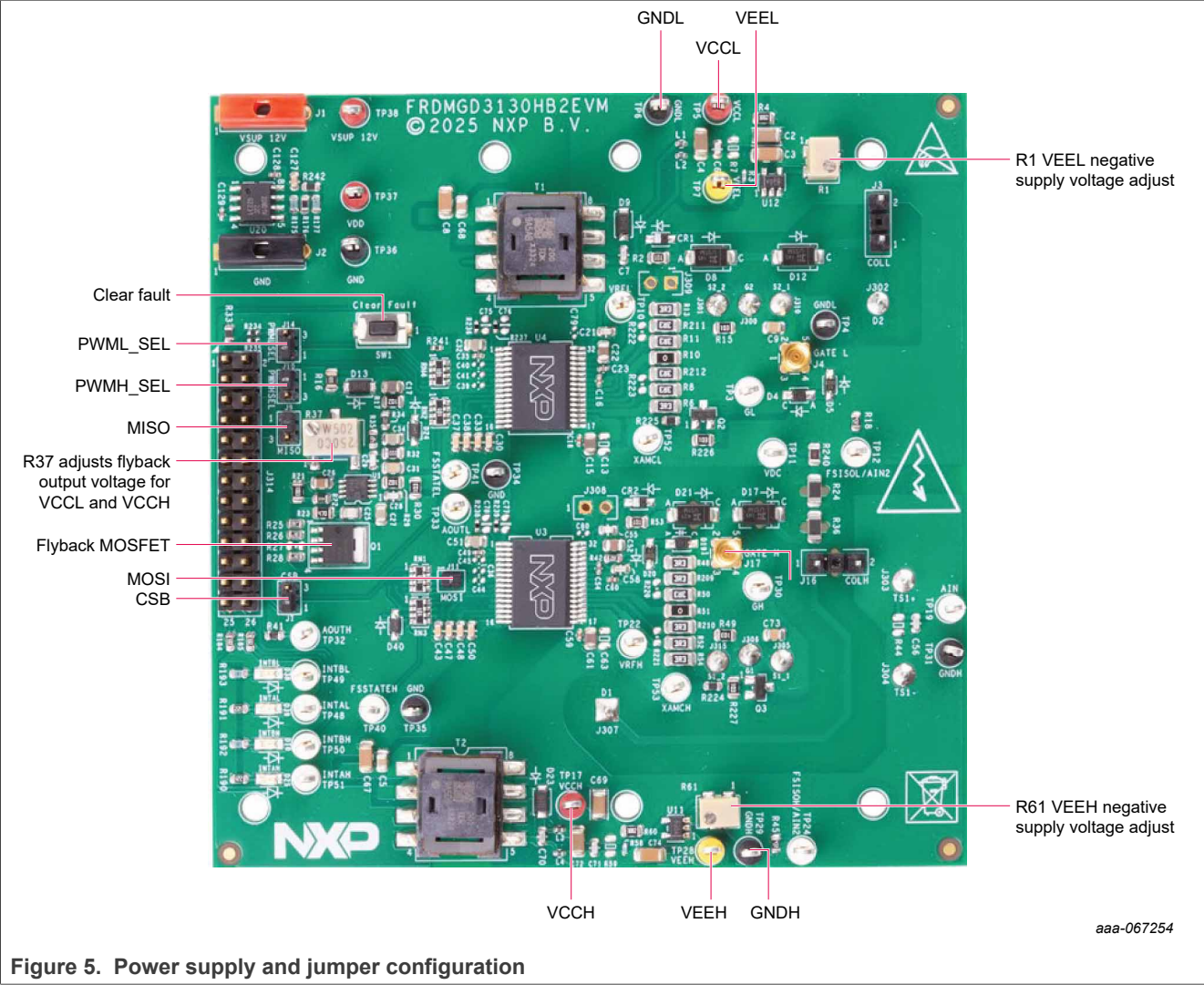


Table 3. Test-point definitions

Test point	Definition
Low-voltage domain	
VSUP	12 V DC external power supply input connection for flyback power supply and 5 V LDO
VDD	VDD power test point of GD313x devices. Derived from VSUP 12 V supply via 5 V LDO
GND	Grounding points for low-voltage domain
INTAH	Fault monitor and VCE/VGE real-time report monitor high-side test point
INTBL	Interrupt bar low-side test point
INTAL	Fault monitor and VCE/VGE real-time report monitor low-side test point
INTBH	Interrupt bar high-side test point
FSSTATEL	Fail-Safe state input test point low side
AOUTL	Analog output test point low side
FSSTATEH	Fail-Safe state input test point high side
AOUTH	Analog output test point high side
Low-side driver domain	
GNDL	Low-side domain ground point
VCCL	Positive flyback voltage supply test point for isolated circuitry and low-side driver domain
VREFL	5.0 V reference test point for isolated analog circuitry on low-side driver
XAMCL	External active Miller clamp test point low side
GATE L	Module gate test point on low-side driver domain, which is the charging pin of the gate; including MMCX probe connection
FSISOL/AIN2	High-voltage domain fail-safe low-side test point or analog input AIN2
DSTL	V_{CE} desaturation test-point header 100 mil connection to low-side driver DESAT pin and circuitry
VEEL	Negative voltage supply test point for low-side driver gate of IGBT or SiC module
VDC	DC-link voltage test point at voltage divider
COLL	Collector test point/connection terminal on low side (200 mil probe connection)
High-side driver domain	
VCCH	Positive voltage supply test point for isolated circuitry and high-side driver domain
GNDH	High-side domain ground point
COLH	Collector test point/connection high side (200 mil probe connection)
VRFH	5.0 V reference test point for isolated analog circuitry on high-side driver
FSISOH/AIN2	High-voltage domain fail-safe high-side test point or analog input AIN2
AINH	Analog input test point high-side
GATE H	Module gate test point on high-side driver domain, which is the charging pin of gate; including MMCX probe connection
DSTH	V_{CE} desaturation test-point header 100 mil connection to high-side driver DESAT pin and circuitry
VEEH	Negative voltage supply test point for high-side driver gate of IGBT or SiC module
XAMCH	External active Miller clamp test point high side



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Figure 5. Power supply and jumper configuration

4.4.3 Power supply and jumper configuration

Table 4. Jumper and resistor definitions

Jumper	Position	Function
PWMHSEL (J10)	1-2	Dead-time fault protection enabled (high side)
	2-3	Dead-time fault protection disabled (use for short-circuit testing)
PWMLSEL (J14)	1-2	Dead-time fault protection enabled (low side)
	2-3	Dead-time fault protection disabled (use for short-circuit testing)
CSB (J7)	1-2	Chip select for normal operation
	2-3	Chip select for daisy-chain operation
MOSI (J11)	Closed	Normal operation
	Open	Daisy chain operation
MISO (J9)	1-2	Normal operation
	2-3	Daisy chain operation
Clear fault (SW1)	Push button	Clear fault switch utilized for non-SPI GD313x
R37	Variable	Potentiometer for adjusting flyback VCCL and VCCH voltage level
R1	Variable	Potentiometer for adjusting VEEL low-side negative supply-voltage level
R61	Variable	Potentiometer for adjusting VEEH high-side negative supply-voltage level

4.4.4 Bottom view

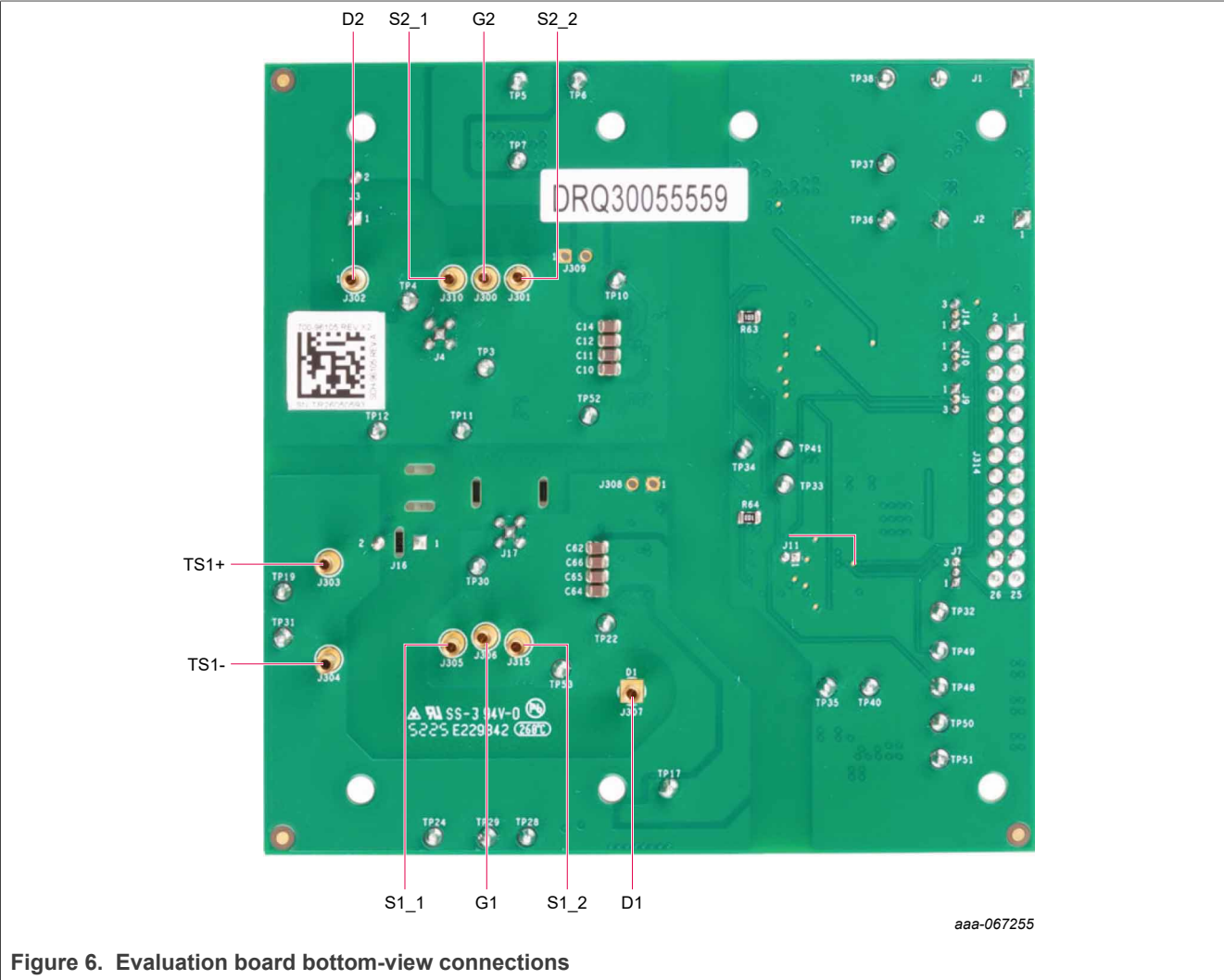


Figure 6. Evaluation board bottom-view connections

Table 5. Bottom connections to power module

Connection	Function
D2	Drain connection of low-side SiC MOSFET
S2_1	Source connection 1 of low-side SiC MOSFET
G2	Gate connection of low-side SiC MOSFET
S2_2	Source connection 2 of low-side SiC MOSFET
TS1+	Anode connection of temperature sensing diode
TS1-	Cathode connection of temperature sensing diode
S1_1	Source connection 1 of high-side SiC MOSFET
G1	Gate connection of high-side SiC MOSFET
S1_2	Source connection 2 of high-side SiC MOSFET
D1	Drain connection of high-side SiC MOSFET

4.4.5 Gate-drive resistors

- Gate-high resistors (RGH) in series with GH_1 (strong gate charge/turn-on pin) and GH_2 (weak gate charge/turn-off pin) and HybridPACK Drive module gate. These gate-drive output pins control the turn on of the SiC MOSFET gate and are enabled when PWM is logic HIGH and setting match GS_ENH.
- Gate-low resistors (RGL) in series with GL_1 (strong gate discharge/turn-off pin) and GL_2 (weak gate discharge/turn-off pin) and HybridPACK Drive module gate. These gate-drive output pins control the turn off of the SiC MOSFET gate and are enabled when PWM is logic LOW and setting match GS_ENL.
- Series resistor between HybridPACK Drive module gate and AMC input pin (RAMC) of the GD3130 driver for gate sensing and active Miller clamping.
- External active Miller clamping (XAMC) FET for higher AMC current.

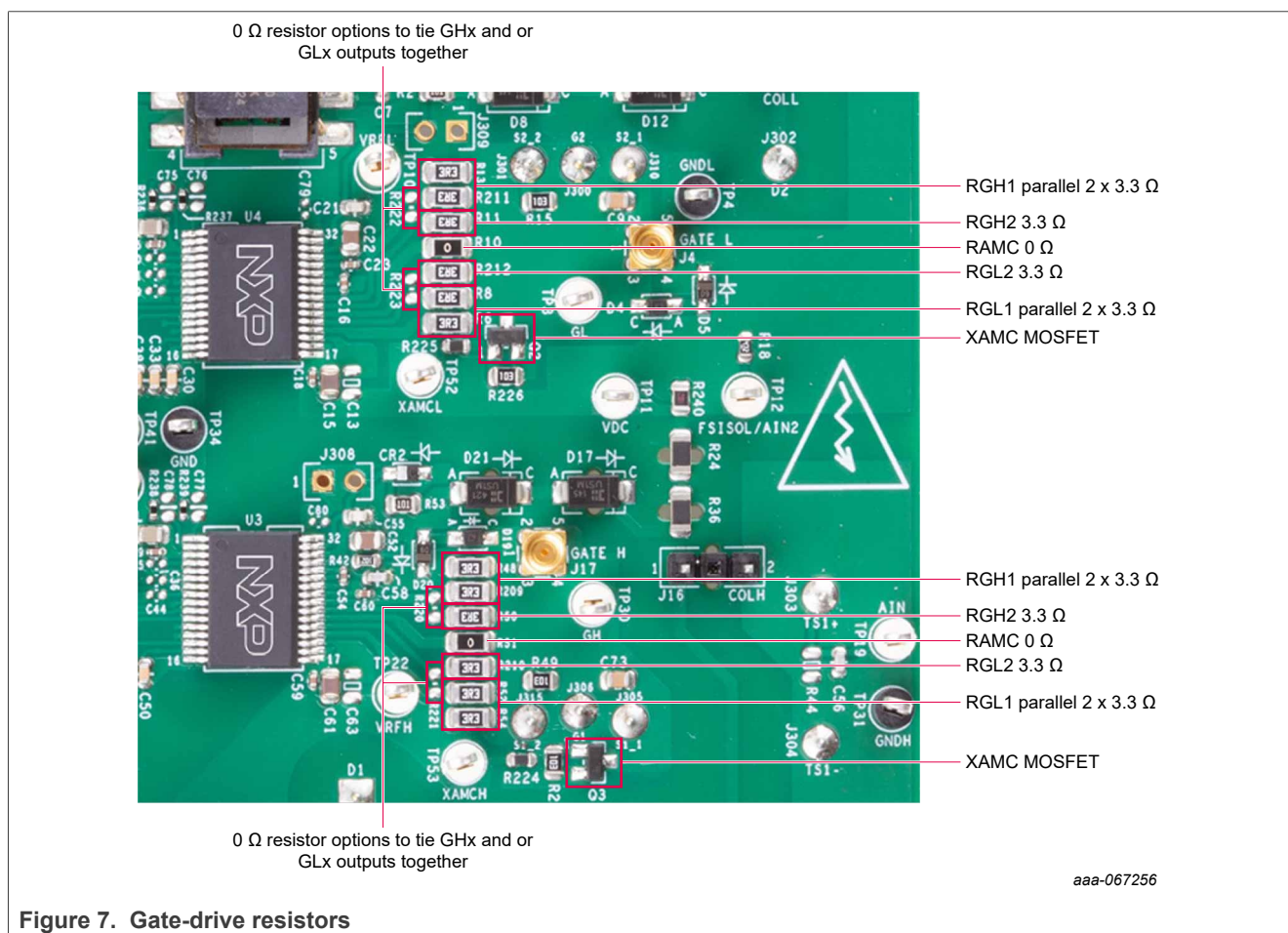


Figure 7. Gate-drive resistors

4.4.6 LED interrupt indicators

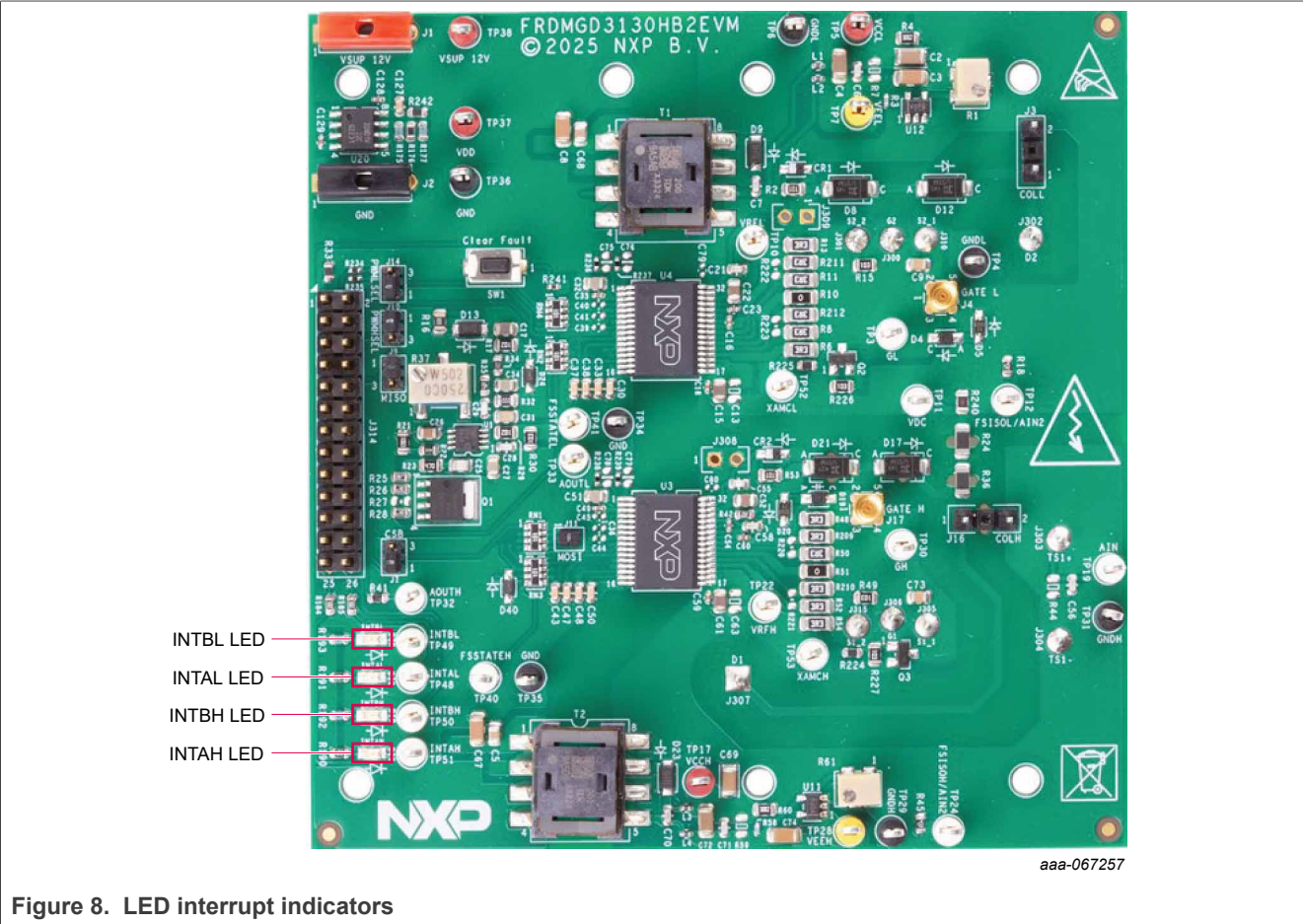


Table 6. LED interrupt indicators

LED	Description
INTBL	Connected to the INTB output pin of low-side driver indicating reported fault status when on (active LOW)
INTAL	Connected to the INTA output pin of low-side driver indicating reported fault status when on (active LOW)
INTBH	Connected to the INTB interrupt output pin of high-side driver indicating reported fault status when on (active LOW)
INTAH	Connected to the INTA interrupt output pin of high-side driver indicating reported fault status when on (active LOW)

4.5 MCXA153 Freedom board

The FRDM-MCXA153 board is a design and evaluation platform based on the NXP MCXA1xx MCU. The MCXA1xx MCU is a low-power microcontroller for industrial and consumer Internet of Things (IoT) applications. It has one Arm Cortex-M33 core running at speeds of up to 96 MHz. It supports industrial communication protocol, brushless direct current (BLDC) motor/permanent magnet synchronous motor (PMSM) control, and integrated sensor interfaces (MIPI-I3C, I²C, and SPI).



Figure 9. FRDM-MCXA153 development board

4.6 3.3 V to 5.0 V translator board

The KITGD31XXTREVM translator enables level shifting of signals from MCU 3.3 V to 5.0 V SPI communication.

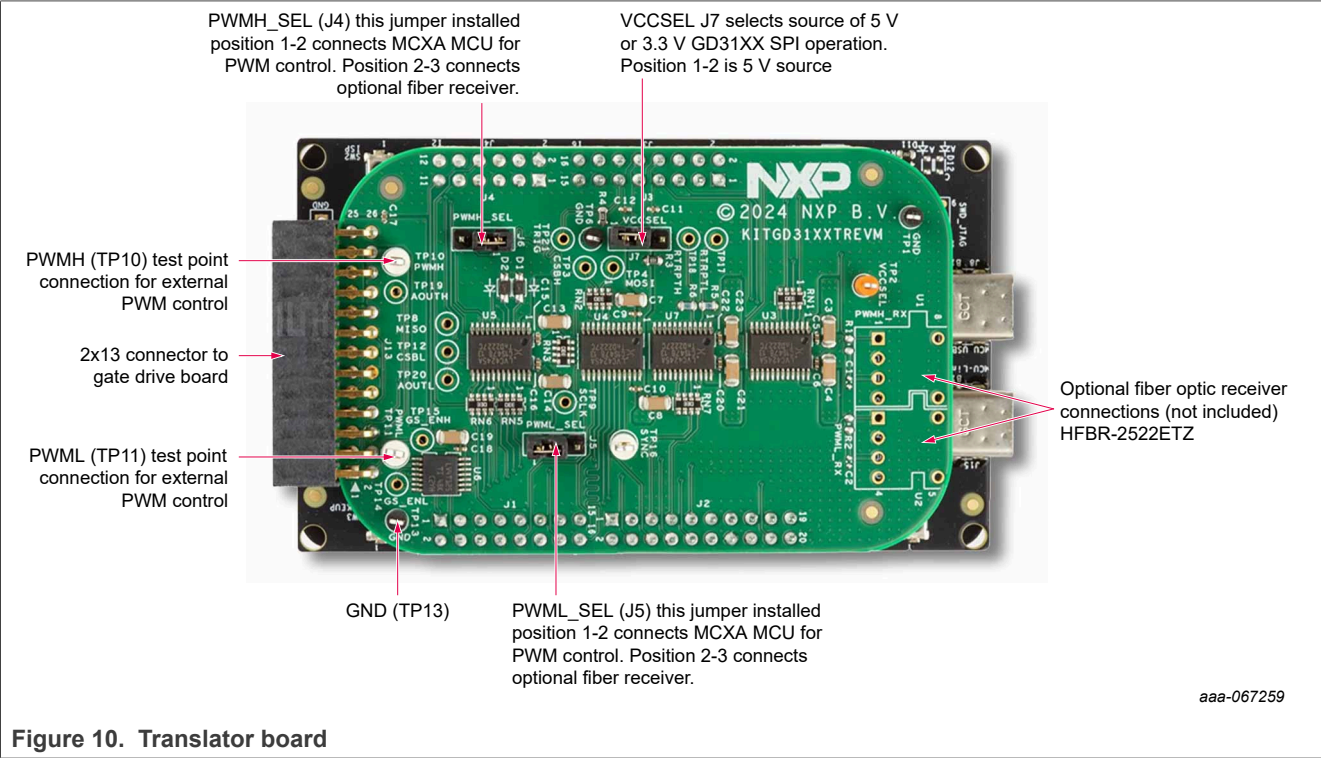


Figure 10. Translator board

Table 7. Translator board jumper definitions

Jumper	Position	Function
VCCSEL (J7)	1-2	Selects 5.0 V for 5.0 V compatible gate drive
	2-3	Selects 3.3 V for 3.3 V compatible gate drive
PWMH_SEL (J4)	1-2	Selects PWM high-side control from MCXA153 MCU
	2-3	Selects PWM high-side control from fiber-optic receiver inputs
PWML_SEL (J5)	1-2	Selects PWM low-side control from MCXA153 MCU
	2-3	Selects PWM low-side control from fiber-optic receiver inputs

5 Configuring the hardware

The FRDMGD3130HB2EVM is designed to be connected to a compatible SiC MOSFET HybridPACK Drive G2 module with a DC-link capacitor, [Figure 11](#). Double-pulse and short-circuit testing can be conducted using a Windows-based PC with FlexGUI software.

Suggested equipment needed for test:

- Rogowski coil high-current probe
- High-voltage differential voltage probe for measuring voltage drain to source
- High sample-rate, digital oscilloscope with probes
- DC-link capacitor compatible with HybridPACK Drive power module
- HybridPACK Drive G2 power module
- Windows-based PC
- High-voltage DC power supply for DC-link voltage
- Low-voltage DC power supply for VSUP
 - +12 V DC gate-drive board low-voltage domain
- Voltmeter for monitoring high-voltage DC-link supply
- Load coil for double-pulse testing

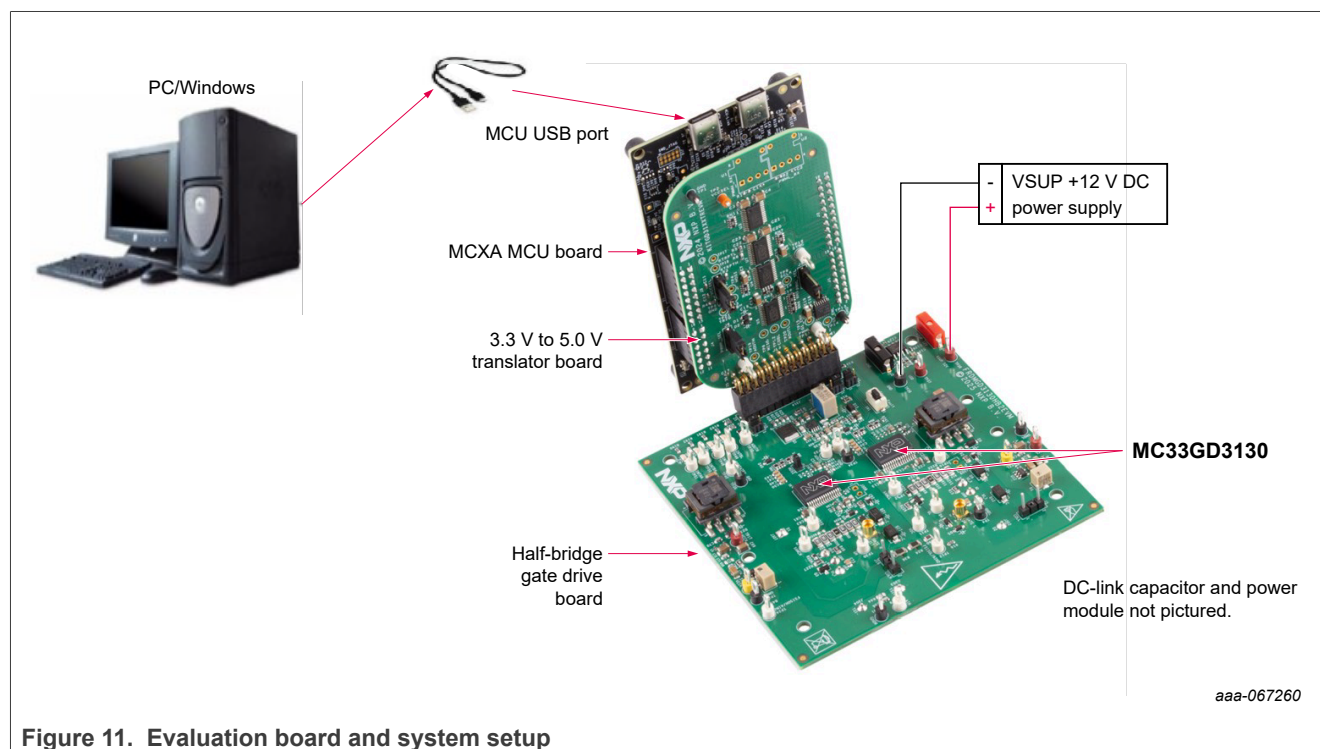


Figure 11. Evaluation board and system setup

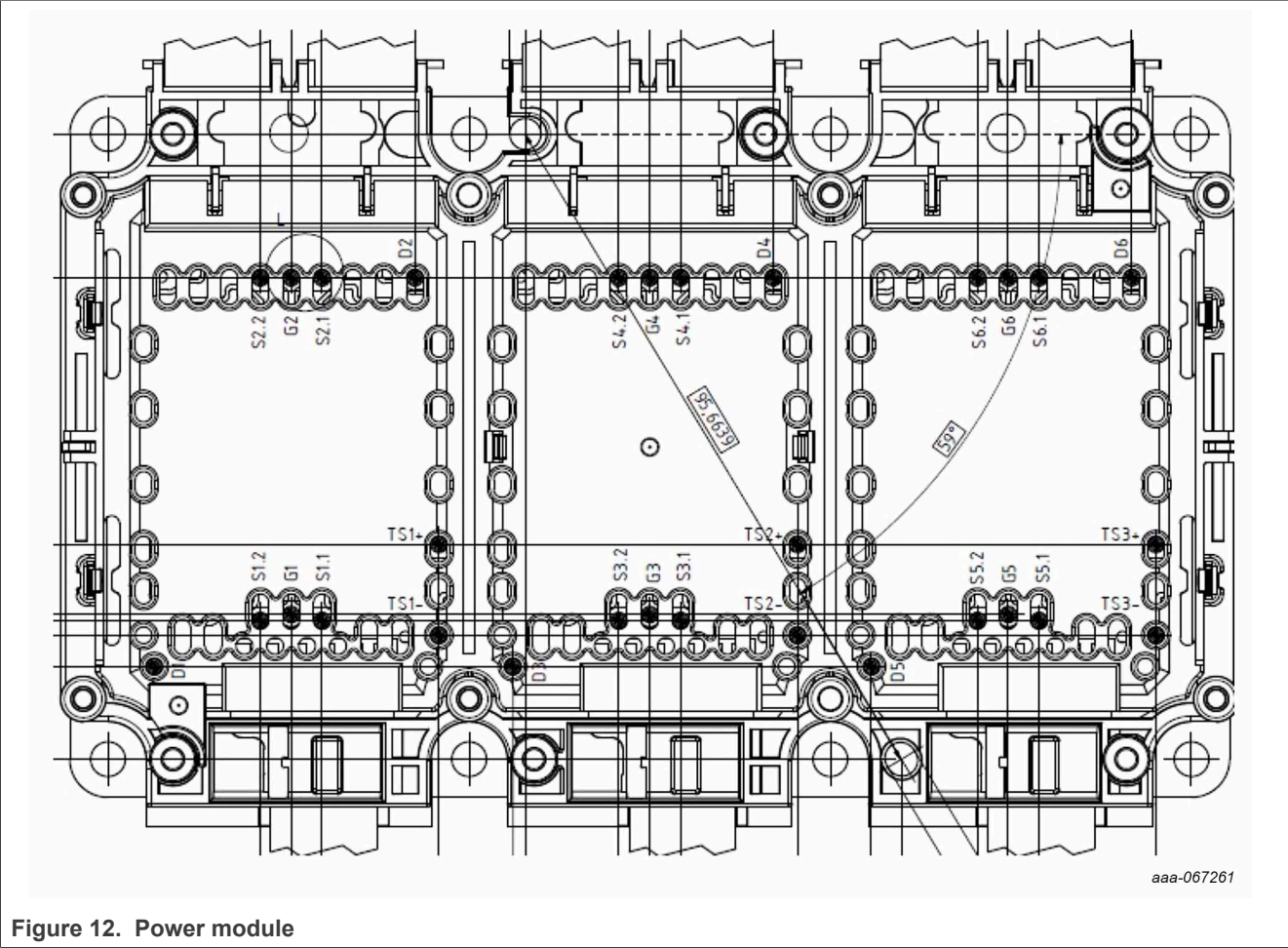


Figure 12. Power module

6 Installation and use of software tools

Software for the FRDMGD3130HB2EVM is distributed with the FlexGUI tool (available on <https://www.nxp.com>). Necessary firmware can be installed onto the FRDM-MCXA153 MCU.

It is recommended to install this software as a backup or to help debugging, even if the user intends to test with other software or PWM input.

6.1 Installing FlexGUI 2

The latest version of the FlexGUI 2 supports all GD3100, GD3160, GD3162, and GD313x. It is designed to run on any Windows 11-based operating system. To install the software, do the following:

1. Go to <https://www.nxp.com/FlexGUI> and click **Download FlexGUI 2 for GD31xx Advanced Gate Driver Evaluation Software**.
2. Clicking **Download** will download the flexgui-app zip file to the Downloads folder
3. Extract/unzip the file and go to GUI folder to install on the PC
4. **NXP_GD31xx_GUI_public-x.x.x.msi**: Installing the device driver overwrites any previous FlexGUI installation and replaces it with a current version containing the GD31xx drivers. However, configuration files (.spi) from the previous version, if any, remain intact.
5. Follow the installation steps. The FlexGUI 2 shortcut icon will appear on the desktop as NXP_GD31xx_GUI_public.

6.2 Configuring the FRDM-MCXA153 firmware

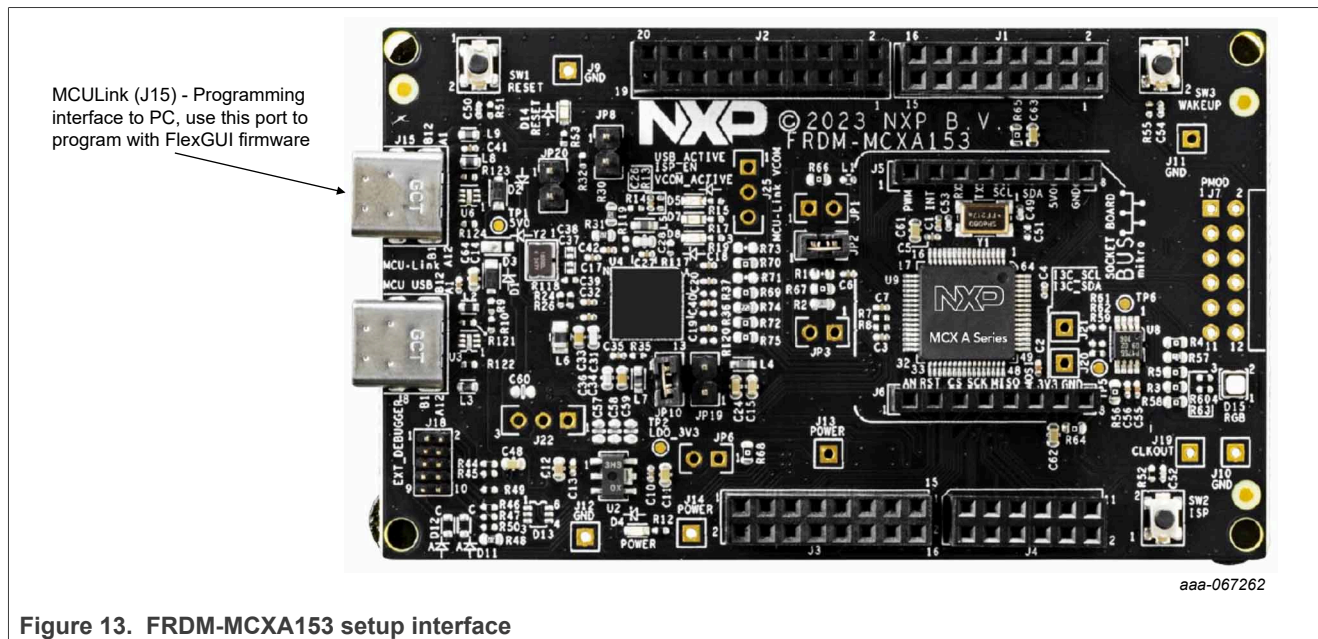


Figure 13. FRDM-MCXA153 setup interface

To install the latest firmware onto the MCXA153 MCU board, LINKSERVER for Windows is needed and can be downloaded from <https://www.nxp.com> using [LinkServer for Microcontrollers | NXP Semiconductors](#) Download (LinkServer installer for Windows).

1. Install the application, a LinkFlash shortcut icon will appear on PC desktop.
2. Bring up the LinkFlash GUI menu.
3. Plug a USB-Type C cable from a Windows PC to MCU Link (J15) on the MCXA153 MCU board.
4. Click **Refresh** on the LinkFlash GUI. MCU-LINK FRDM-MCXA153 will be displayed beside "Probe" and "Device". See [Figure 14](#).
5. In the File menu, browse to the FlexGUI 2 downloaded flexgui-app folder and go to the MCU folder. Select the MCXA153 folder and select the firmware file to be programmed (flexgui2_fw_mcxa153_gd31xx_public_vx.x.x.bin)
6. Start address = 0
7. Click **Program** to begin the flash firmware process. Once finished, "Operation completed successfully" will appear at bottom of GUI. See [Figure 14](#).

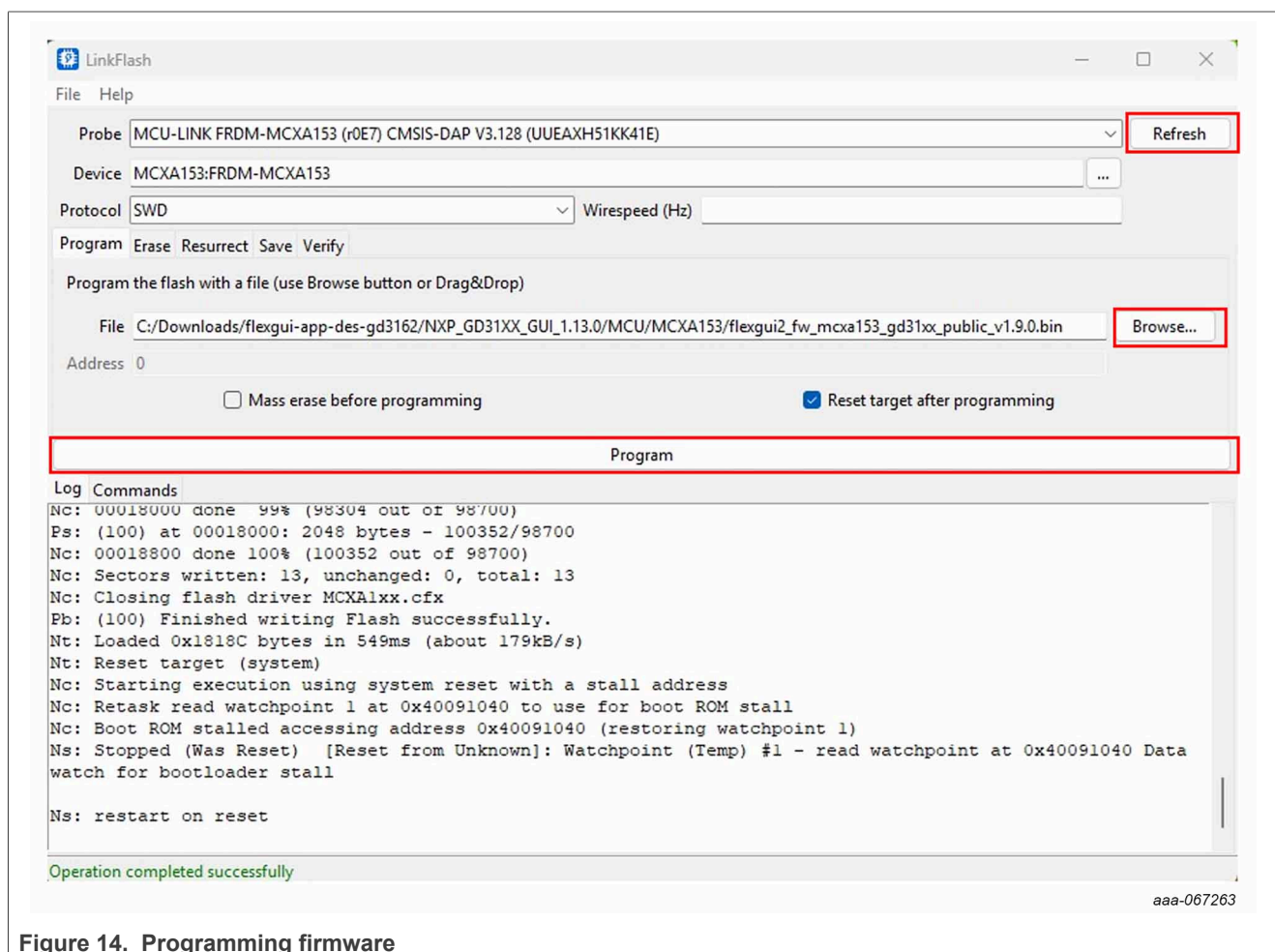


Figure 14. Programming firmware

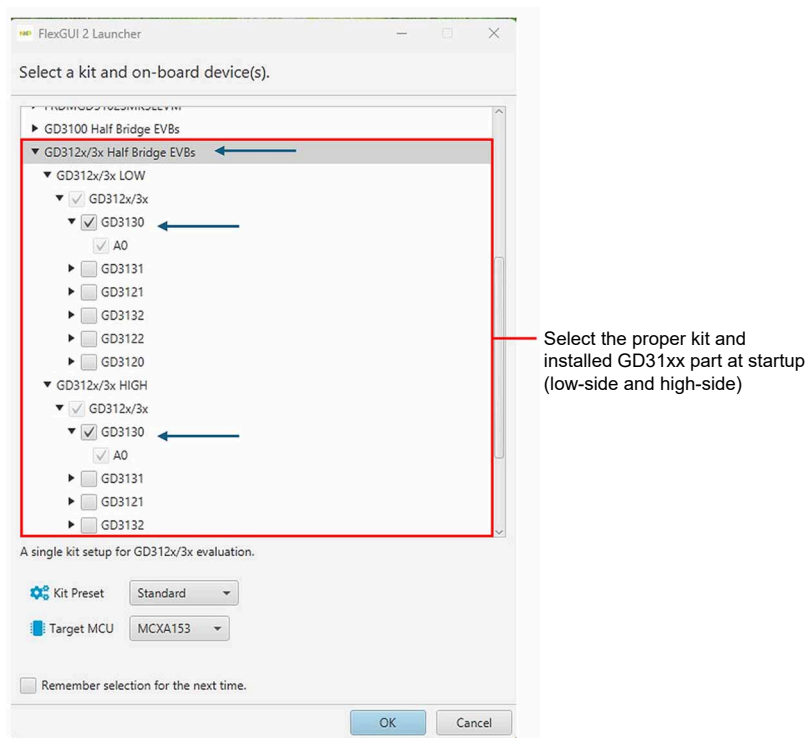
6.3 Using FlexGUI 2

FlexGUI 2 is available from <https://www.nxp.com/FlexGUI> as an evaluation tool demonstrating GD31xx-specific functionality, configuration, and fault reporting. FlexGUI 2 also includes basic capacity for the FRDMGD3130HB2EVM to control an IGBT or SiC module, enabling double-pulse and short-circuit testing.

SPI messages can be realized graphically or in hexadecimal format. CSB is selectable to address one or both GD3130 on the board via daisy chain.

Starting FlexGUI 2 for GD31xx

1. Download FlexGUI 2 and run the install program on the PC (if not already installed)
 - FlexGUI 2 install program (NXP_GD31xx_GUI_public-x.x.x.msi)
2. When the application starts, [Figure 15](#) shows where to select the target application board, half-bridge EVB, or three-phase inverter (x3 - 2 channel) or (x6 - 1 channel), kit preset (standard or daisy chain), and target MCU



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Figure 15. Kit selection

FlexGUI 2 connection

- Select **FRDM-MCXA153 COM** port from the drop-down menu and select **Connect** to establish USB connection
 - If a connection is not established, check the USB cable connection between PC and MCXA153 port (MCU_USB) and scan again
 - If a connection is not established, ensure that the proper firmware is installed on the FRDM-MCXA153 MCU for FlexGUI 2 (see step 6 in [Section 6.2](#))

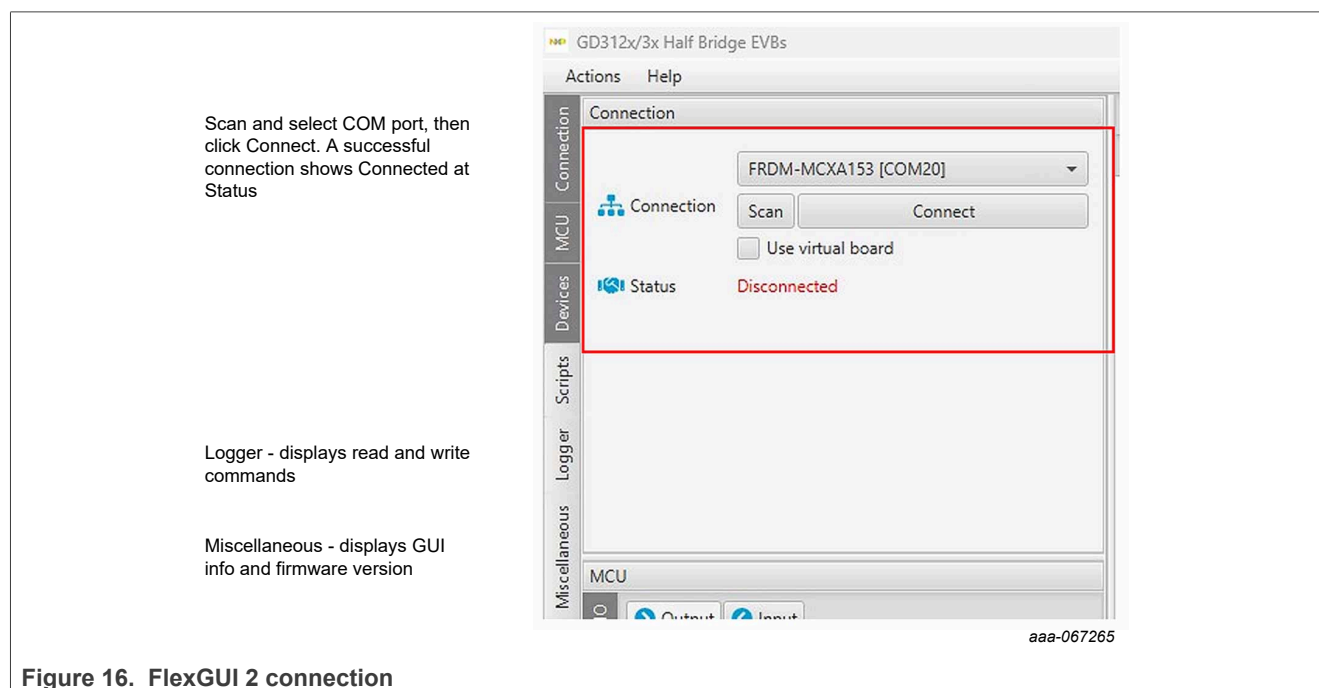


Figure 16. FlexGUI 2 connection

Set GUI actions and preferences

- Access Preferences from the actions menu at top left of the GUI

Preferences

General

Devices

Register Map

Group Operations

Enable synchronized read

☐

Enable synchronized write

☐

OK

Cancel

Apply

Enable synchronized read and write to set both HS and LS devices simultaneously with same settings if desired

Preferences

General

Devices

Register Map

Behavior

Use register init value

☒

Enable read after write

☒

Enable to set read value to write value.

☒

UI

Adaptive bit field width

☐

Fixed bit field width [px]

100

OK

Cancel

Apply

Enable Use register init value and Enable read after write and Enable to set read value to write value if desired (recommended)

aaa-055040

Figure 17. Actions and preferences settings

MCU

GPIO

Output

Input

INTAL

Low

High

☒

☐

INTAH

Low

High

☐

☒

INTBL

Low

High

☐

☒

INTBH

Low

High

☐

☒

Read

Poll

1000

Interrupt A low side

Interrupt A high side

Interrupt B low side

Interrupt B high side

INTA and INTB fault indicators - interrupt LOW means there is a fault latched

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Figure 18. MCU GPIO input

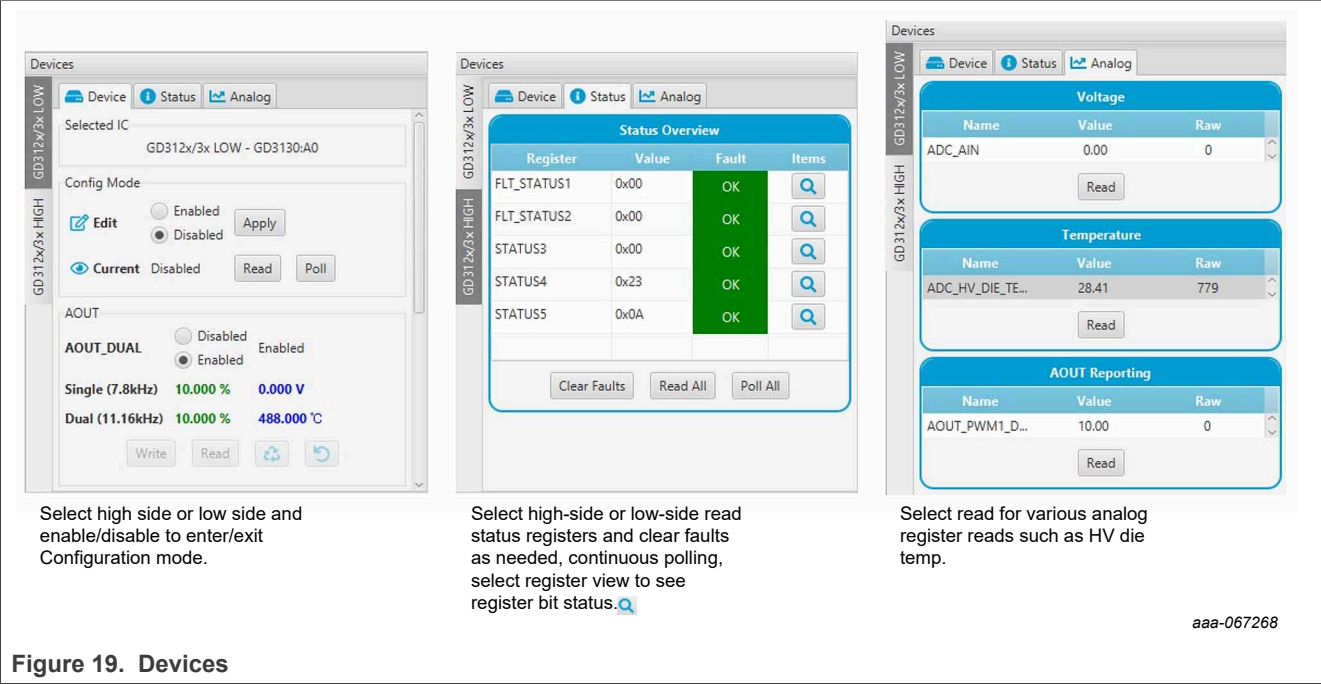


Figure 19. Devices



- Registers are grouped according to function; independent lines are used to read and write the registers
- Individual registers can be read by clicking the **R** button and can be written using the **W** button
- Click the **Copy** button to copy the read values to the write line; can be set to copy automatically
- Global register controls perform the selected command on all registers with the checkbox selected
- **Add to Script** adds current and selected register values to a script in the Script Editor window

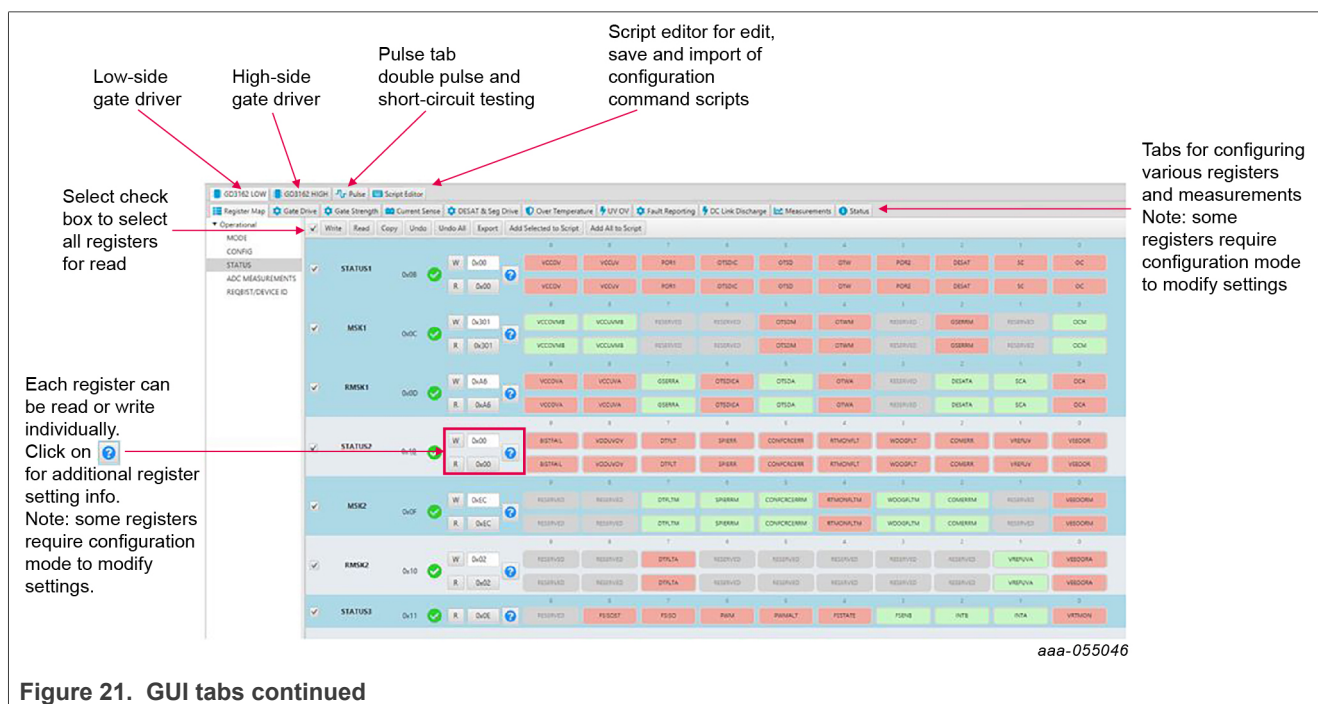


Figure 21. GUI tabs continued

Gate Drive tab

- Allows setting of parameters related to the gate drive; controls are disabled when not in Config mode
- Provides a visual way to set parameters
- Automatically synchronizes all settings with the register controls

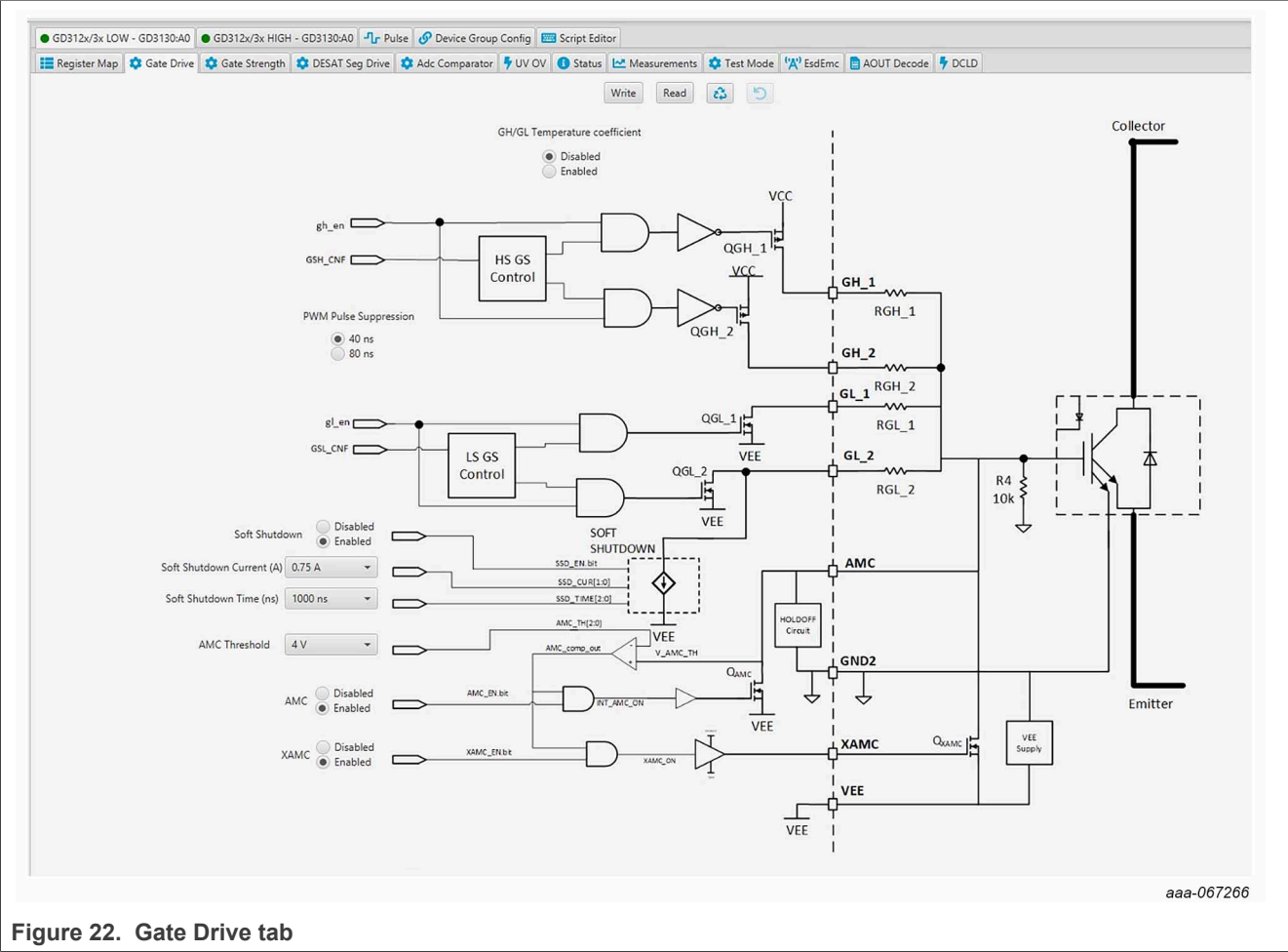


Figure 22. Gate Drive tab

- Allows setting of parameters related to DESAT
- Provides a more intuitive visual way to set parameters
- Automatically synchronizes all settings with the register controls

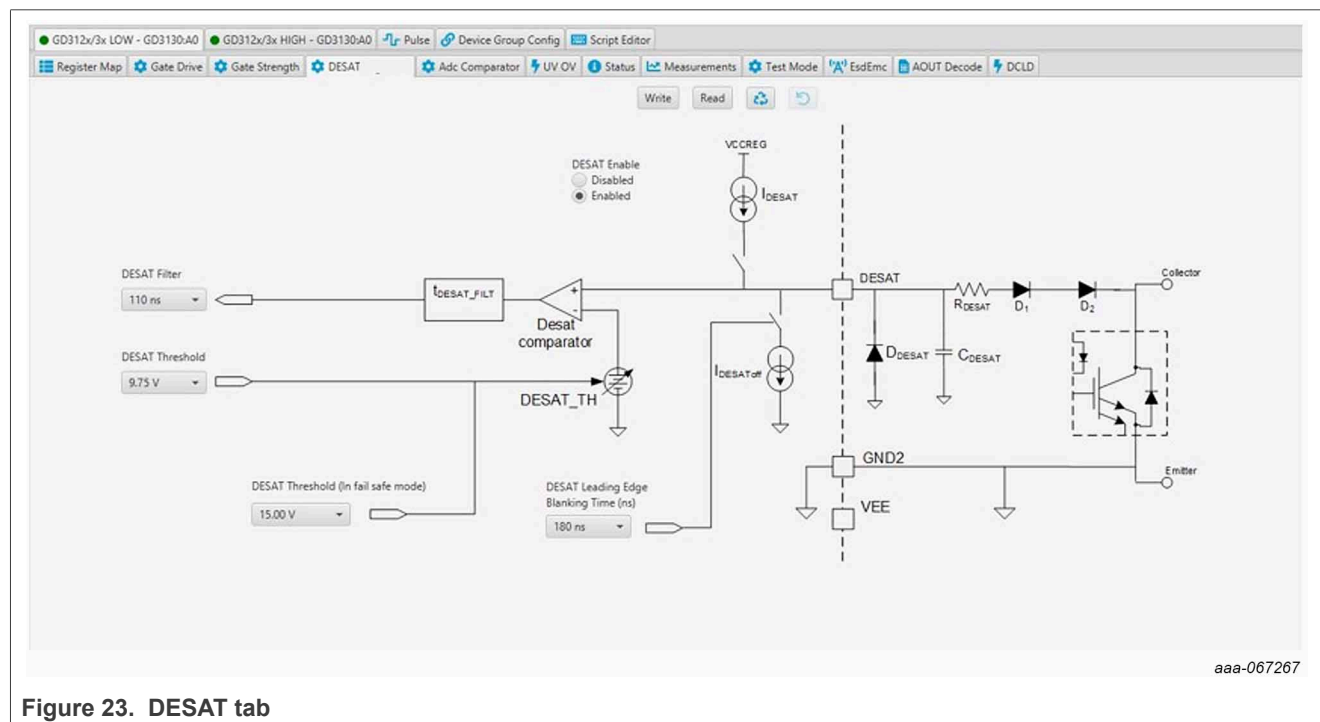


Figure 23. DESAT tab

Undervoltage and overvoltage threshold tab

- Allows setting of parameters related to undervoltage and overvoltage threshold
- Provides a visual way to set parameters
- Automatically synchronizes all settings with the register controls

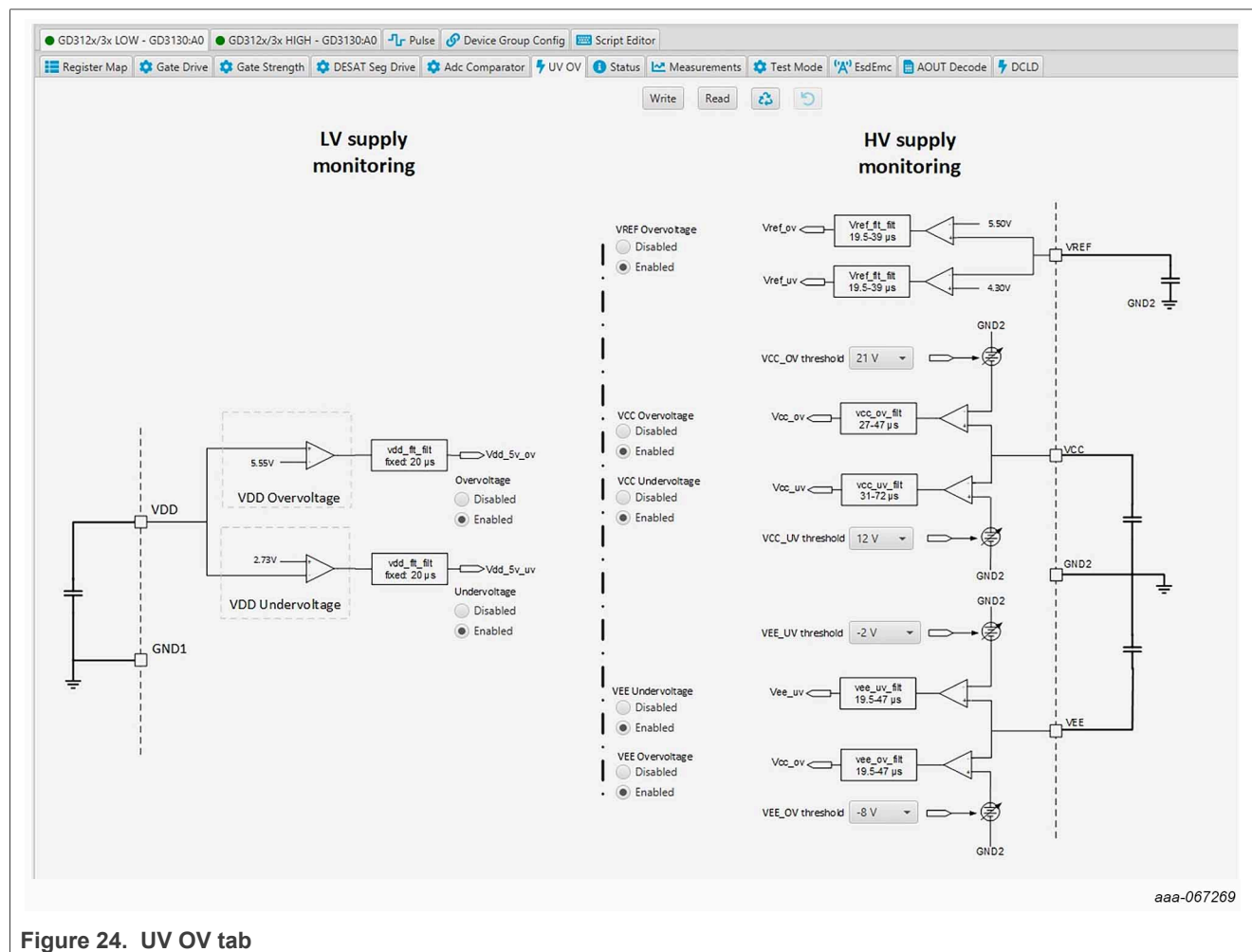


Figure 24. UV OV tab

Measurements tab

- Allows monitoring and graphing of ADC and temperature values (Check Configuration register CONFIG8 for ADC_DLY sampling)



Figure 25. Measurements tab

Pulse tab

- Used for double pulse, short-circuit testing
- Select desired t1, t2, and t3 timings for each test type; click **Enable**, then generate pulses

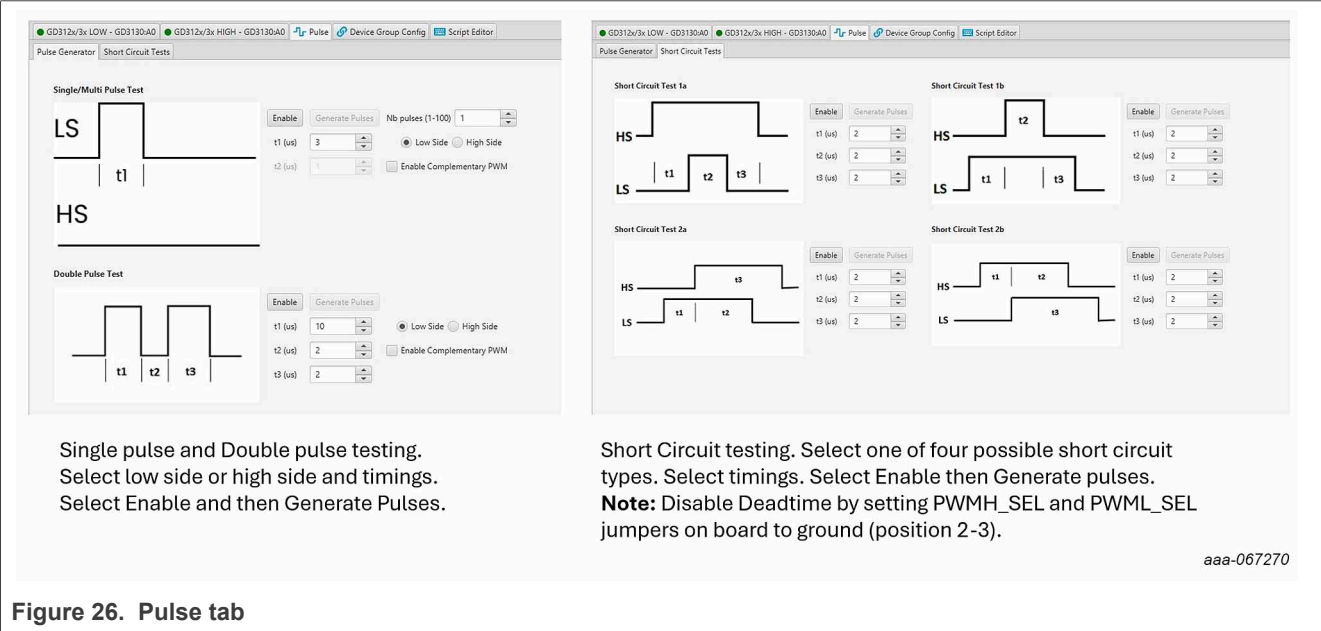


Figure 26. Pulse tab

6.4 Troubleshooting

Some common issues and troubleshooting procedures are detailed in [Table 8](#). This is not an exhaustive list by any means, and additional debug may be needed:

Table 8. Troubleshooting

Problem	Evaluation	Explanation	Corrective action(s)
Unable to establish COM port connection	Check that the USB cable is connected to the MCU USB port on the MCXA153 board	If the USB cable is not connected to the PC USB and the MCXA153 USB port, the GUI will not be able to establish connection	Plug the USB cable to the PC USB port and the MCXA153 USB port
	Incorrect firmware installed on MCXA153 MCU	If incorrect firmware is installed on the MCU board GUI will not be able to establish connection	Go to step 6 in the user guide for installing FlexGUI 2 on your computer and locate the firmware file in the GUI download package; go through steps to program/flash the MCXA153 MCU.
No PWM output (no fault reported)	Check the PWM jumper position on the translator board	Incorrect PWM jumpers obstruct the signal path, but do not report a fault	Set PWMH_SEL (J4) and PWML_SEL (J5) jumpers properly, for desired control method: 3.3 V to 5.0 V translator board reviewed in Section 4.6
	Check the PWM control signal	Ensure that proper PWM signal is reaching GD31XX	Monitor EXT_PWML (TP14) and EXT_PWMH (TP15) for commanded PWM state
	Check the FSENB status (see GD3130 pin 15, STATUS3)	PWM is disabled when FSENB = LOW	Set pin FSENB = HIGH (pin 15) to continue
	Check CONFIG_EN bit (MODE2)	PWM is disabled when CONFIG_EN is logic 1	Write CONFIG_EN = logic 0 to continue
No PWM output (fault reported)	Check VGE fault (VGE_FLT)	A short on IGBT or SiC module gate, or too low of VGEMON delay setting causes VGE fault, locking out PWM control of the gate	Clear VGE_FLT bit (STATUS2) to continue Increase VGEMON delay setting (CONFIG6) If safe operating condition can be guaranteed, set VGE_FLTM (MSK2) bit to logic 0, to mask fault
	Check for a short-circuit fault (SC) in STATUS1 register	SC is a severe fault that disables PWM. SC fault cannot be masked	Clear SC fault to continue; consider adjusting SC fault settings on GD3130: - Adjust short-circuit threshold setting (CONFIG2) - Adjust short-circuit filter setting (CONFIG2)
PWM output is good, but with persistent fault reported	Check for a dead-time fault (DTFLT) in STATUS2 register	Dead-time is enforced, but fault indicates that PWM controls signals are in violation	Clear DTFLT fault bit (STATUS2); check PWMHSEL (J10) and PWMLSEL (J9) are configured to bypass dead-time faults Consider adjusting dead-time settings on GD3130: - Change mandatory PWM dead-time setting (CONFIG5) - Mask dead-time fault (MSK2)
PWM or FSSTATE rising edge has longer delay than falling edge	Check the translator output voltage versus GD31xx VDD voltage	Low translator output voltage (compared with correct VDD at GD31xx) causes the high threshold at the GD31xx pin to be crossed later than commanded	Check that the translator output voltage selection (J7) is configured to the same level as the GD31xx VDD Check VCCSEL supply or translator outputs on the translator board for excessive loading or supply droop/pulldown

Table 8. Troubleshooting...continued

Problem	Evaluation	Explanation	Corrective action(s)
WDOG_FLT reported on startup	Check that VSUP and VCC are powered	On initialization, a watchdog fault is reported when one die is powered up before the other	Check that VSUP and VCC both have power applied Clear WDOG_FLT bit (STATUS2) to continue
SPIERR reported on startup	Check the MCXA153/translator connection	On initialization, SPIERR can occur when the SPI bus is open, or when GD31xx IC is powered up before the translator (which provides CSB)	Clear SPIERR fault to continue; reinitialize power to GD31xx after translator is powered (over USB)
SPIERR reported after SPI message	Check the bit length of the message sent	There is SPIERR if SCLK does not see a n*24 multiple of cycles	Use a 24-bit message length for SPI messages
	Check CRC	SPIERR faults if the CRC provided in a sent message is not good	Use the FlexGUI to generate commands with valid CRC; the command can be copied in binary or hexadecimal and sent from another program
	Check for sufficient dead-time between SPI messages	SPIERR fault bit is set when the time between SPI messages (txfer_delay) received is too short; minimum required delay time is 19 µs	Check that the time between the CSB rising edge (old message end) and the CSB falling edge (new message start) during normal SPI read, and ensure the transfer delay dead-time check SPIERR can also be cleared in BIST
VREFUV reported on startup	Check that the HV domain is powered correctly	Related to slow rise time of VCC supply on HV domain, or failed VREF regulator	Clear VREFUV bit (STATUS2) Reset the HV domain supply if the fault bit does not clear
	Check the VCC for undervoltage condition	Low VCC is visible indirectly through other HV domain faults	Tune VCC-GNDISO using R20 feedback
VCCOV fault reported on startup	Check the VEE level on suspect domain	If VEE level is not at desired negative voltage it could cause excessive VCC level	Check Zener diode in power supply circuit for proper value in setting VEE level Clear VCCOV bit (STATUS1) to continue
	Check VCC-GNDISO potential	PWM is disabled during a VCC overvoltage (20 V nom.)	Tune VCC-GNDISO potential to suitable level with power supply set resistor (R37) Clear VCCOV fault bit to continue
No PWM during short-circuit test	Check PWMxSEL jumpers	Incorrect configuration of PWMALT pins prevent a short-circuit test by enforcing dead-time	For the short-circuit test, set PWMLSEL (J9) and PWMHSEL (J10) to bypass dead-time; see Section 4.4.3 for details
Bad SPI data, appears to repeat previous response	Check VSUP/VDD for undervoltage condition	VDD_UV latches the SPI buffer contents, preventing updated fault reporting	Check the voltage provided at the VDD pin (pin 3) On each read, compare the address from the sent command and response (a difference indicates that the SPI response is latched due to inactive); read multiple addresses to ensure a good comparison
	Check VCC for undervoltage	Unpowered VCC prevents HV domain from updating data	Tune VCC-GNDISO using R37 feedback

7 Schematics, board layout, and bill of materials

The board schematics, board layout, and bill of materials are available at <https://www.nxp.com/FRDMGD3130HB2EVM> on the Overview tab under Get Started.

8 References

1. Tool summary page for FRDMGD3130HB2EVM <https://www.nxp.com/FRDMGD3130HB2EVM>
2. Product summary page for GD3130 device <https://www.nxp.com/GD3130>

9 Revision history

Table 9. Revision history

Document ID	Release date	Description
UM12624 v.1.0	15 September 2026	Initial version

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