UM12356

KITFS27-48VEVM evaluation board

Rev. 1.0 — 28 October 2025 **User manual**

Document information

Information	Content
Keywords	FS27, FS2700-B0, KITFS27-48VEVM, KITFS27-48VEVM-REVB, spf-93485, FRDM-KL25Z, SPI, I^2C, hardware, evaluation, power management, Flyback, 48 V, NXP GUI for Automotive PMIC Families
Abstract	The KITFS27-48VEVM provides a development platform to evaluate the flyback front-end regulator for 48 V compatible applications. The kit can be connected to the NXP GUI through an USB port. This document is intended for engineers involved in evaluation, design, implementation, and validation using the FS27 fail-safe system basis chip with multiple SMPS and LDO.

1 Introduction

This document is the user manual for the KITFS27-48VEVM evaluation board. This document is intended for engineers involved in evaluation, design, implementation, and validation using the FS27 12 V / 24 V / 48 V Safety System Basis Chip for ASIL D.

The scope of this document is to provide the user with information to evaluate the FS27. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The KITFS27-48VEVM evaluation board allows functional testing with flyback topology front-end regulator and programming of the soldered sample.

The NXP GUI for Automotive PMIC Families allows the user to play with registers, try configurations, and program the part.

1.1 KITFS27-48VEVM evaluation board

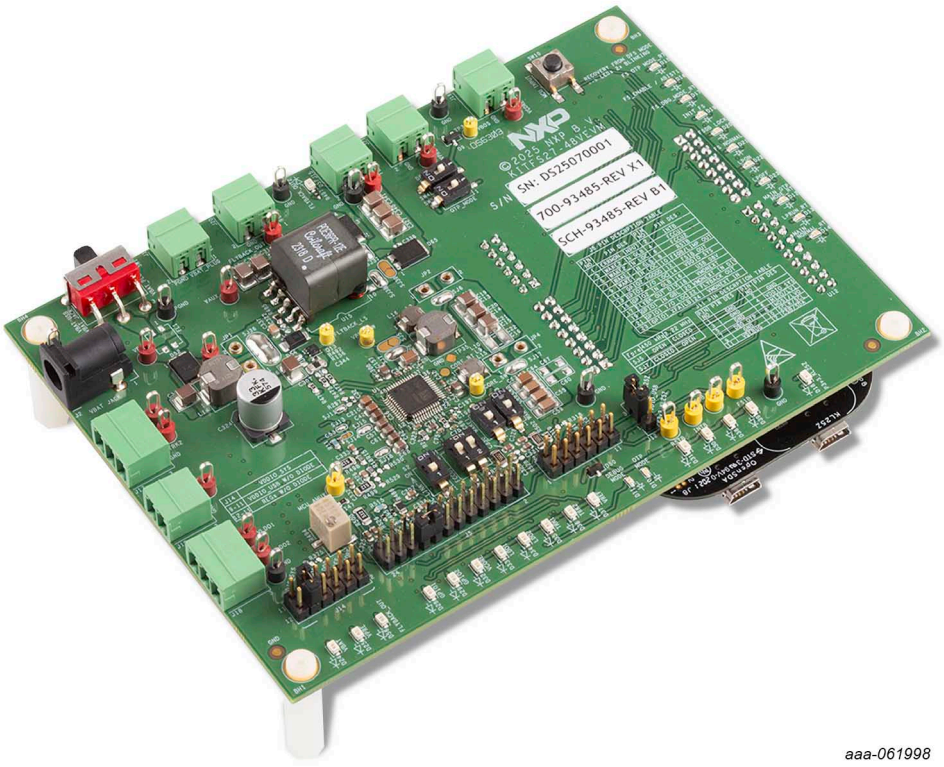


Figure 1. KITFS27-48VEVM evaluation board

IMPORTANT NOTICE

For engineering development or evaluation purposes only

NXP provides the product under the following conditions:

This evaluation kit is for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY.

It is provided as a sample IC pre-soldered to a printed-circuit board to make it easier to access inputs, outputs and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by connecting it to the host MCU computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application heavily depends on proper printed-circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The product provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end device incorporating the product. Due to the open construction of the product, it is the responsibility of the user to take all appropriate precautions for electric discharge. In order to minimize risks associated with the customers' applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

2 Finding kit resources and information on the NXP website

NXP Semiconductors provides online resources for this evaluation board and its supported devices on http://www.nxp.com.

The information page for KITFS27-48VEVM evaluation board is at http://www.nxp.com/KITFS27-48VEVM. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the KITFS27-48VEVM evaluation board, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community:

The NXP community is for sharing ideas and tips, asking and answering technical questions, and receiving input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

3 FS27: 12 V / 24 V / 48 V Safety System Basis Chip for ASIL D

3.1 General description

Devices in the FS27 automotive safety system basis chip (SBC) family are designed to support entry and midrange safety 28 nm microcontrollers. FS27 devices have multiple power supplies and the flexibility to work with other microcontrollers targeting automotive electrification. Possible FS27 applications include power train, chassis, safety, and low-end gateway technology.

This family of devices consists of several versions that are pin-to-pin and software compatible. These versions support a wide range of applications with Automotive Safety Integrity Levels (ASIL) B or D, offering choices in the number of output rails, output voltage settings, operating frequencies, power-up sequencing, and integrated system-level features.

The FS27 features multiple switch mode regulators and low dropout (LDO) voltage regulators to supply the microcontroller, sensors, peripheral ICs, and communication interfaces. FS27 offers a high-precision reference voltage supply for the system, and for two independent tracking regulators. The FS27 also offers various functionalities for system control and diagnostics, including an analog multiplexer (AMUX), General-Purpose Input/Outputs (GPIOs), and selectable wake-up events from I/O, Long-Duration Timer (LDT), Serial Peripheral Interface (SPI), or Inter-Integrated Circuit (I^2C) communications.

The FS27 is developed in compliance with the ISO 26262 standard, and includes enhanced safety features with multiple fail-safe outputs. FS27 disposes of the latest on-demand latent fault monitoring, and can be part of a safety-oriented system partitioning scheme covering both ASIL B and ASIL D safety integrity levels.

3.2 Features and benefits

Operating range

- 70 V DC maximum input voltage.
- Support operating voltage range down to battery 3.2 V with VBST in front-end.
- Support operating voltage range down to battery 4.5 V without VBST in front-end.
- Low Power *LPOFF mode* with 30 µA quiescent current.
- Low-Power *Standby mode* with 32 µA quiescent current with VPRE active. LDO1 or LDO2 activation is selectable via OTP configuration. GPIO1 or GPIO2 activation selectable via SPI/I^2C communication.
- Low-Power Run mode *LPRUN mode* with selectable power rails configurable by software.

Power supplies

- VPRE: Synchronous buck converter with integrated FETs. Configurable output voltage and switching frequency, output DC current capability up to 1.5 A or 2.5 A and PFM mode for Low-Power *Standby mode* operation.
- VCORE: Synchronous buck converter with integrated FETs. VCORE is dedicated for microcontroller core supply. Output DC current up to 2.5 A or 3.5 A, output voltage range set from 0.8 V to 5.0 V.
- VBST: Asynchronous low-side controller with external low-side switch, diode, and current sense resistor. VBST is configurable as a front-end supply to withstand low voltage cranking profiles, a back-end supply with configurable output voltage and scalable output DC current capability, SEPIC controller to withstand 24 V and 48 V applications and flyback controller to withstand 48 V applications.
- LDO1: LDO regulator for microcontroller I/O support with selectable output voltage between 1.0 V and 5.0 V and up to 400 mA current capability.
- LDO2: LDO regulator for system peripheral support with selectable output voltage between 1.0 V and 5.0 V and up to 400 mA current capability.
- VREF: High-precision reference voltage with 0.75 % accuracy for External ADC reference and internal tracking reference.

- TRK1 and TRK2: Voltage tracking regulators with selectable output voltage between VREF, LDO2, or Internal LDO reference. Support high-voltage protection for ECU off-board operation up to 40 V. Each tracker has a current capability up to 150 mA.

System support

- Two wake-up inputs with high-voltage support for system robustness.
- Two programmable GPIOs with wake-up capability or LS driver for GPIO1 and HS/LS driver for GPIO2.
- Programmable long duration timer (LDT) for system shutdown and wake-up control.
- Monitoring of system voltages (including battery voltage monitoring) through the analog multiplexer.
- Selectable wake-up sources from: WAKE/GPIO pins, LDT, or SPI/I^2C activity.
- Device control via 32-bit SPI or 40-bit I^2C interface with cyclic redundancy checks (CRC).
- Multi PMIC power-up/down synchronization.
- DCLINK capacitor discharge command with NXP GD31XX.

Compliance

- Electromagnetic compatibility (EMC) optimization techniques for switching regulators, including spread spectrum, slew rate control, and manual frequency tuning.
- Electromagnetic interference (EMI) robustness supporting various automotive EMI test standards.

Functional safety

- Scalable portfolio from Automotive Safety Integrity Levels (ASIL) B to D.
- Independent monitoring circuitry, dedicated interface for microcontroller monitoring, simple, or challenger watchdog function.
- Analog built-in self-test (ABIST1) and logical built-in self-test (LBIST) at startup.
- Analog built-in self-test (ABIST2) on demand.
- Safety outputs with latent fault detection mechanism (RSTB, FS0B/LIMP, FS1B). FS0B/LIMP upon part number.

Configuration and enablement

- LQFP48 pins with exposed pad for optimized thermal management.
- Permanent device customization via one-time programmable (OTP) fuse memory.
- OTP Emulation mode for hardware development and evaluation.
- *Debug mode* for software development, MCU programming, and debugging.

4 Getting ready

Working with the KITFS27-48VEVM requires the kit contents, additional hardware, and a Windows PC workstation with installed software.

4.1 Kit contents

- Assembled and tested evaluation board and preprogrammed FRDM-KL25Z board in an antistatic bag.
- 3.0 ft USB-STD A to USB-B-mini cable.
- Six connectors, terminal block plug, two positions, straight 3.81 mm.
- Two connectors, terminal block plug, three positions, straight 3.81 mm.
- Jumpers mounted on board.
- Quick start guide.

4.2 Additional hardware

No additional hardware is required for device evaluation. For an in-depth evaluation of power conversion capabilities (power delivery and stability), in addition to the kit contents, the following hardware is required when working with this kit:

- Power supply with a range of 20 V to 60 V and a current limit set initially to 1.0 A.

4.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- USB-enabled computer with Windows 7, 10 or 11.

4.4 Software

Software must be installed before working with this evaluation board.

- NXP GUI for Automotive PMIC Families.

All listed software is available on the NXP GUI for Automotive PMIC Families information page at http://www.nxp.com/NXP GUI for Automotive PMIC Families or from our “Secure Files” portal at https://www.nxp.com/mynxp/secure-files if device is not in production.

5 Getting to know the hardware

5.1 Kit overview

The KITFS27-48VEVM provides the flexibility needed to play with all the features of the device and to take measurements in the main sections of the application. The FRDM-KL25Z board connected to the kit, combined with the FS27 NXP GUI for Automotive PMIC Families software, allows full configuration and control of the FS27 SBC.

FS27 and KITFS27-48VEVM features:

- VBAT power supply connectors (jack and Phoenix).
- Flyback front-end regulator to support battery profiles for 48 V, multiple outputs.
- VPRE output 5.0 V to 6.35 V, up to 2.5 A.
- VCORE output 0.8 V to 5.0 V, up to 3.5 A.
- LDO1 and LDO2, from 1.0 V or 5.0 V, up to 400 mA.
- TRK1 and TRK2, from 1.0 V or 5.0 V, up to 150 mA.
- VREF accuracy regulator for external ADC reference up to 80 mA.
- FS0B/LIMP, FS1B external safety pins.
- USB to SPI and I^2C protocol for easy connection evaluation GUI.
- LEDs that indicate signal or regulator status.
- OTP fuse programming.
- Advance system monitoring via AMUX, and ADCs, and digital IOs.
- Analog variable resistor to test external VMON_EXT.

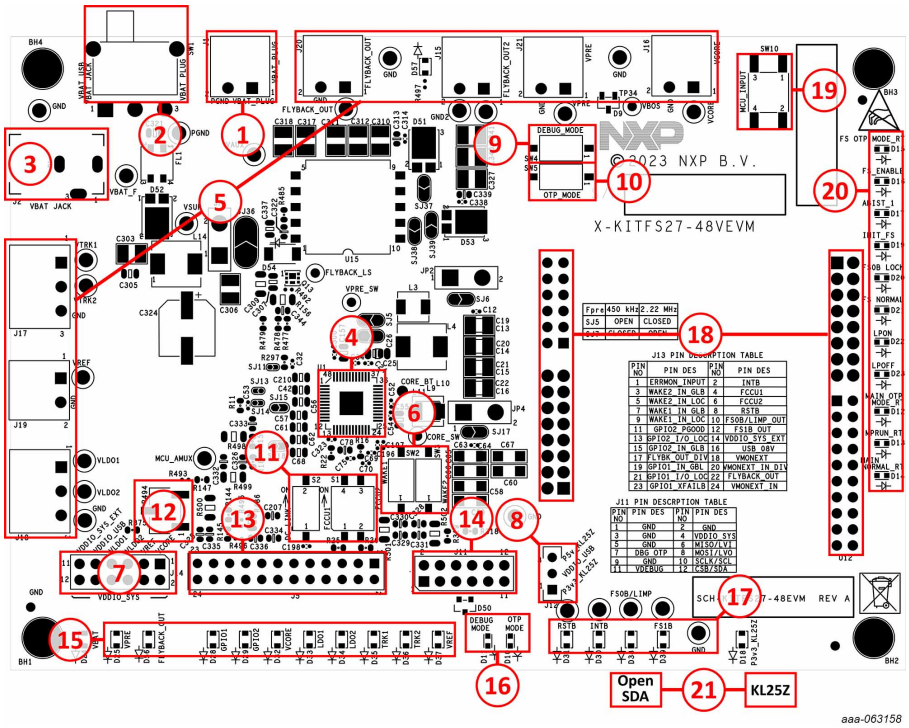
5.1.1 Schematic, board layout, and bill of materials

The schematic, board layout, and bill of materials for the KITFS27-48VEVM evaluation board are available at http://www.nxp.com/KITFS27-48VEVM.

5.2 Kit featured components

Figure 2 identifies the location of the main KIT features:

1. VBAT Phoenix connector
2. VBAT three position switch
3. VBAT jack connector
4. Soldered device location
5. Regulator outputs
6. WAKE1 and WAKE2 input switches
7. VDDIO selection
8. VDDIO USB voltage level selection
9. DEBUG mode switch
10. OTP mode switch for emulation and programming
11. DC_LINK and FCCU switches
12. VMONEXT variable resistor
13. Signal connector
14. Program connector
15. Regulators output LED indicators
16. DEBUG pin voltage LED indicator
17. Safety outputs LED indicators
18. FRDM-KL25Z board headers (bottom)
19. MCU input switch
20. Device state machine status LEDs
21. FRDM-KL25Z board USB connections (bottom board)
22. Signal connectors compatible with 16-channel logic analyzer (socket board only)
23. Safety isolation switches: FS27 safety ↔ LEDs/FRDM-KL25Z board ADCs and IOs
24. Communication protocol manual select switch
25. VSUP discharge switch (socket board only)
26. COM isolation switches: FS27 ↔ communication lines' level shifters
27. LEDs isolation switches: FS27 regulators ↔ LEDs/FRDM-KL25Z board ADCs



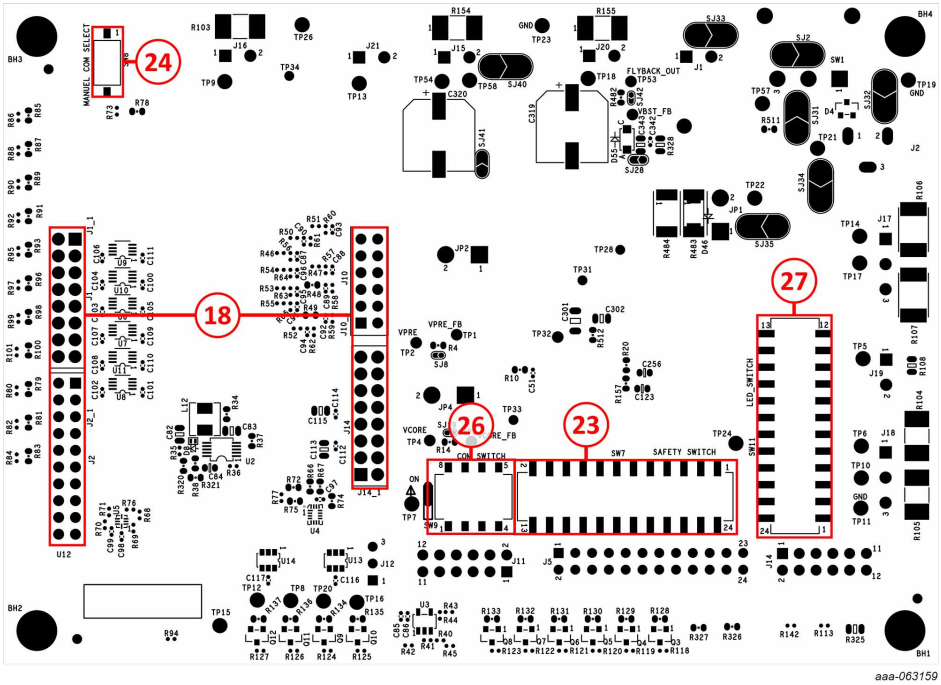


Figure 2. Evaluation board featured component locations

5.2.1 Default board configuration

The default board configuration shown in Figure 3.

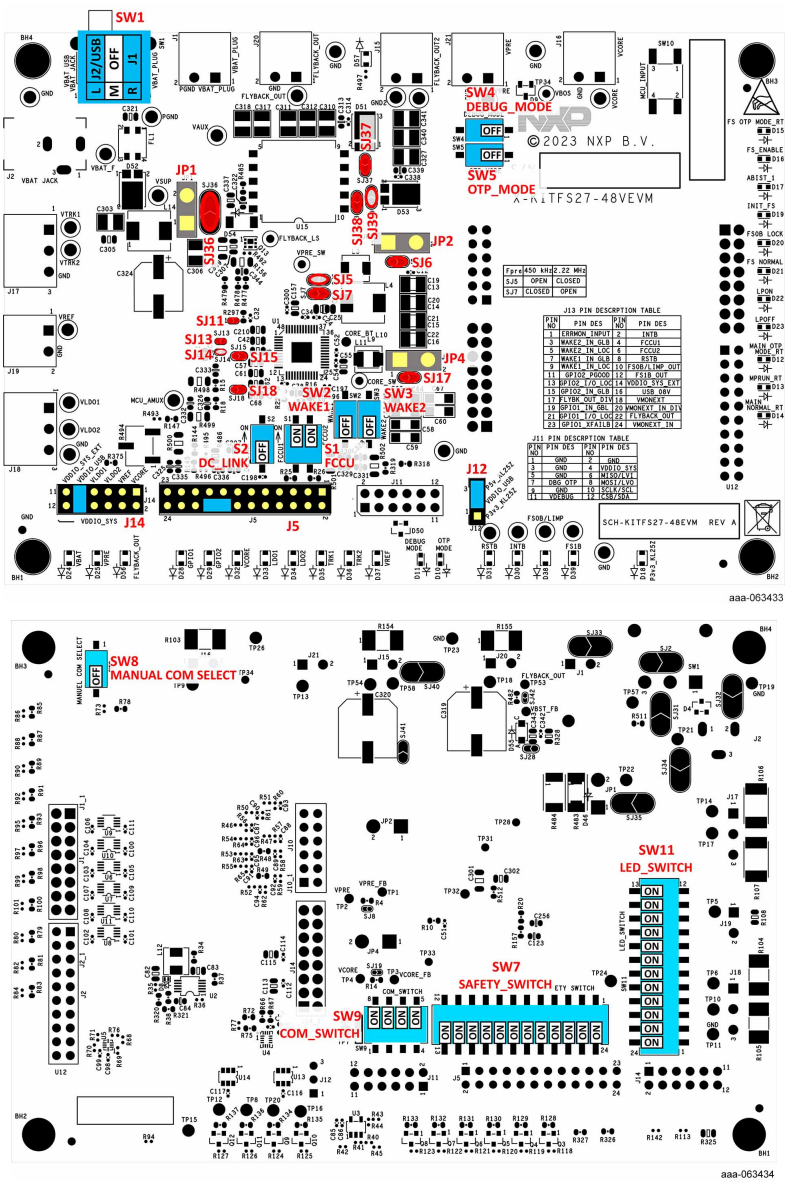


Figure 3. Default board configuration

TThe board configuration legend is shown in Figure 4.

Status	Jumper	Jumper power	Switch	Solder joint
OFF/Open	Jx	JPx	SWx	SJx
ON/Closed	Jx	JPx	SWx	SJx

aaa-062839

Figure 4. Board configuration legend

Table 1. Default board configuration

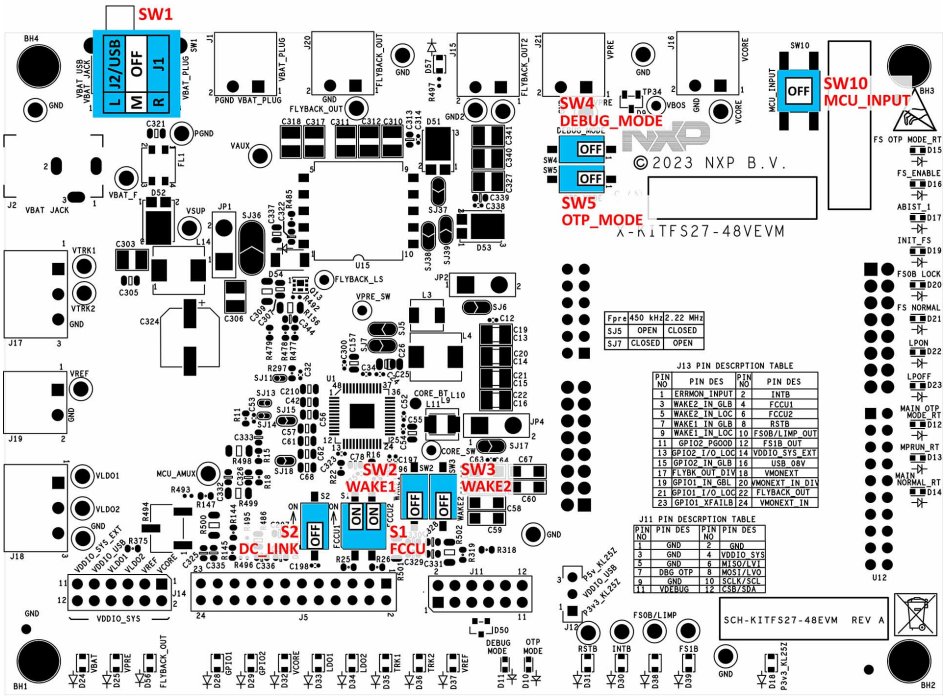
Schematic label	Description	Default setting
JP1	Flyback front-end regulator input inductor current measurement	Open
JP2	VPRE regulator output inductor current measurement	Open
JP4	VCORE regulator output inductor current measurement	Open
SJ2	Bypass SW1: VBAT connected to J1	Closed
SJ5	Connect VPRE_SW to L3 (inductor F_{PRE} = 2.2 MHz)	Open
SJ6	Bypass JP2: jumper for VPRE regulator output inductor current measurement	Closed
SJ7	Connect VPRE_SW to L4 (inductor F_{PRE} = 444 kHz)	Closed
SJ8	Bypass R4: resistor for VPRE regulator stability measurement	Closed
SJ11	Connect GPIO2 pin to GPIO2 input/output external components	Closed
SJ13	Connect GPIO1 pin to GPIO input/output external components	Closed
SJ14	Connect GPIO1 pin to GPIO XFAILB components	Open
SJ15	Connect VPRE regulator output to TRKIN pin	Closed
SJ17	Bypass JP4: jumper for VCORE regulator output inductor current measurement	Closed
SJ18	Connect VPRE regulator output to LDOIN pin	Closed
SJ19	Bypass R14: resistor for VCORE regulator stability measurement	Closed
SJ28	Connect flyback auxiliary winding to VAUX output external components	Open
SJ31 SJ32 SJ33	Bypass FL1: Input common mode filter transformer	Closed
SJ34	Bypass D52: VBAT reverse protection diode	Open
SJ35	Bypass L14: PI filter inductor	Open
SJ36	Bypass JP1: jumper for flyback regulator primary (input) current measurement	Closed
SJ37	Connect flyback secondary 1 winding to FLYBACK_OUT output external components	Closed
SJ38	Connect flyback secondary 1 and secondary 2 windings in parallel	Closed
SJ39	Connect flyback secondary 2 winding to FLYBACK_OUT_2 output external components	Open
SJ42	Bypass R482: resistor for flyback regulator stability measurement	Closed
SJ140 SJ141	Connect flyback secondary 2 winding (isolated output) to ground (no more isolated)	Closed
SW1	VBAT supply	2 (middle)
SW2	WAKE1 switch global	OFF
SW3	WAKE2 switch global	OFF
SW4	Debug mode	OFF
SW5	OTP mode	OFF
SW7	Safety switch (breaker)	All ON

Table 1. Default board configuration*...continued*

Schematic label	Description	Default setting
SW8	Communication protocol manual switch	OFF
SW9	Communication interface switch (breaker)	All ON
SW11	LED switch (breaker)	All ON
S1	FCCU switch	All ON
S2	DC link switch	OFF

5.3 Switches

Kit switch locations are shown in Figure 5.



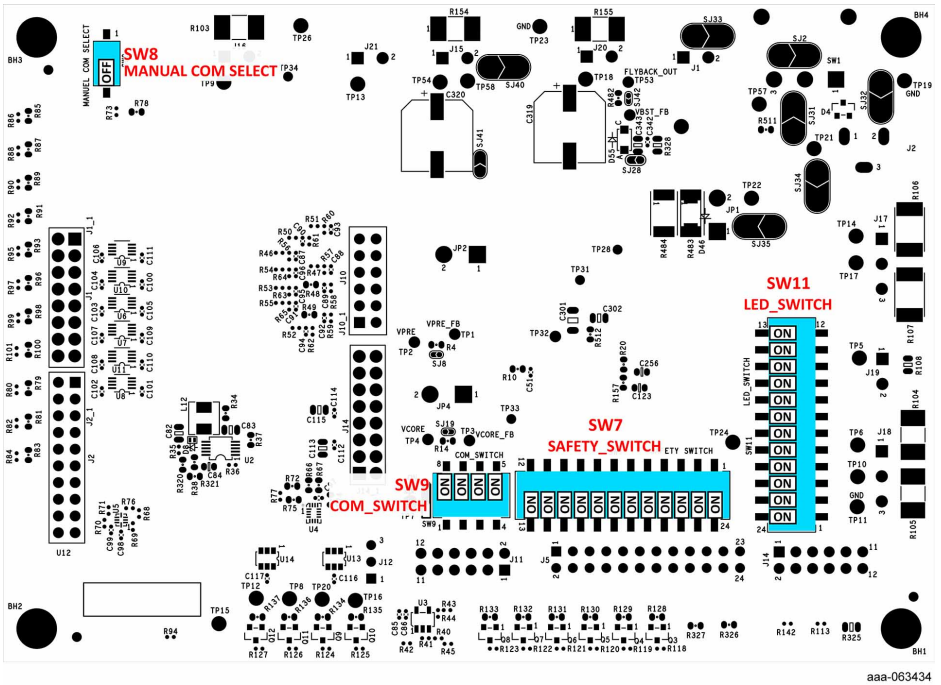


Figure 5. Switch locations

5.3.1 VBAT switch

There are three ways of supplying the board main supply VBAT:

1. Phoenix connector (J1)
2. Jack connector (J2)
3. FRDM-KL25Z board USB

The selection of the supplying connector is done using a three-position switch (SW1). Figure 6 shows related schematic.

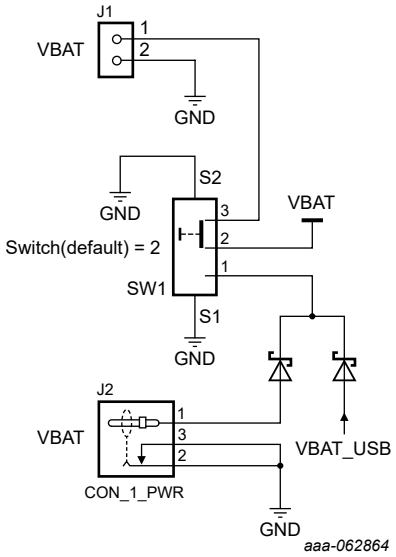


Figure 6. VBAT switch and connectors schematic

Table 2. SW1: VBAT three position connector

Schematic label	Signal name	Description
SW1 position 3 (right)	VBAT Phoenix	Board supplied by Phoenix Connector J1
SW1 position 2 (middle)	-	Board not supplied
SW1 position 1 (left)	VBAT jack/USB	Board supplied by jack connector J2 or VBAT_USB (FRDM-KL25Z board USB generated 24 V supply), which voltage is higher

Nominal VBAT voltage is 24 V, can operate from 20 V up to 60 V.

5.3.2 DEBUG pin voltage control

The DEBUG pin is used to enable specific device operating modes for evaluation purposes by applying different voltages and power-up sequences.

These modes are:

- **Debug mode**: to perform debug by disabling safety reactions.
- **Test mode**: provide access to protected registers for extended diagnostics, OTP emulation (mirrors manipulation).
- **OTP mode** + **Test mode**: for OTP emulation (mirrors manipulation) and OTP programming (burn fuses).

Note: *OTP emulation (mirrors manipulation) can be done at any state when test mode is enabled. It is recommended to emulate the OTP in OTP mode to observe the impact on the power-up sequence.*

Note: *OTP programming (burn fuses) can be done at any state when test mode is enabled, however OTP programming procedure is **only** guaranteed in OTP mode.*

The DEBUG pin voltage V_{DEBUG} to be applied before power-up sequence or low-power modes exit, are:

- **V_{DEBUG} = 0 V:** Normal operation mode, run power-up sequence, debug mode not enabled.
- **V_{DEBUG} = V_{DBG} = 4.5 V:** Enters debug mode and run power-up sequence.
- **V_{DEBUG} = V_{OTP} = 7.8 V:** Enters debug mode, enter OTP mode, and halt before the power-up sequence.

Note: *When in OTP mode, to run power-up sequence, V_{OTP} must be removed (SW5 off) or click "Exit OTP mode" on the GUI.*

The voltage level to be applied to DEBUG pin at any moment, is:

- **V_{DEBUG} = V_{DBG} or V_{OTP} = 7.8 V:** In conjunction with the GUI request, enters **test mode**.

The required voltages are generated on-board, and the V_{DEBUG} can be controlled manually using SW4 and SW5.

The voltage V_{DBG} is generated from the device VBOS pin thought a diode.

The voltage V_{OTP} is generate with an on-board boost regulator supplied by FRDM-KL25Z board USB 5 V supply. As a result, the FRDM-KL25Z board and USB must be plugged in to enter OTP mode.

The SW4 connects V_{DBG} while SW5 connects V_{OTP}.

Note: *V_{OTP} has higher priority than V_{DBG}.*

The yellow LED D11 indicates that at least V_{DBG} is present at DEBUG pin.

The blue LED D10 indicates that V_{OTP} is present at DEBUG pin.

Table 3 shows the possible output voltage level to apply to the DEBUG pin depending on SW6 and SW7 positions.

Table 3. SW4 and SW5: DBG pin voltage V_{DEBUG} selection and associated LED signaling

DEBUG pin voltage applied for	SW5	SW4	D11	D10	V_{DEBUG} voltage (J13.2)
Normal operation (default)	OFF	OFF	OFF	OFF	0 V
Debug and test mode entry	OFF	ON	OFF	ON[1]	4.5 V
OTP mode entry	ON	X	ON	ON	7.8 V

[1] After VBAT (SW1) is ON

Note: *SW4 and SW5 must be set before VBAT (SW1) is applied.*

Figure 7 shows the V_{DEBUG} voltage sources and its selection.

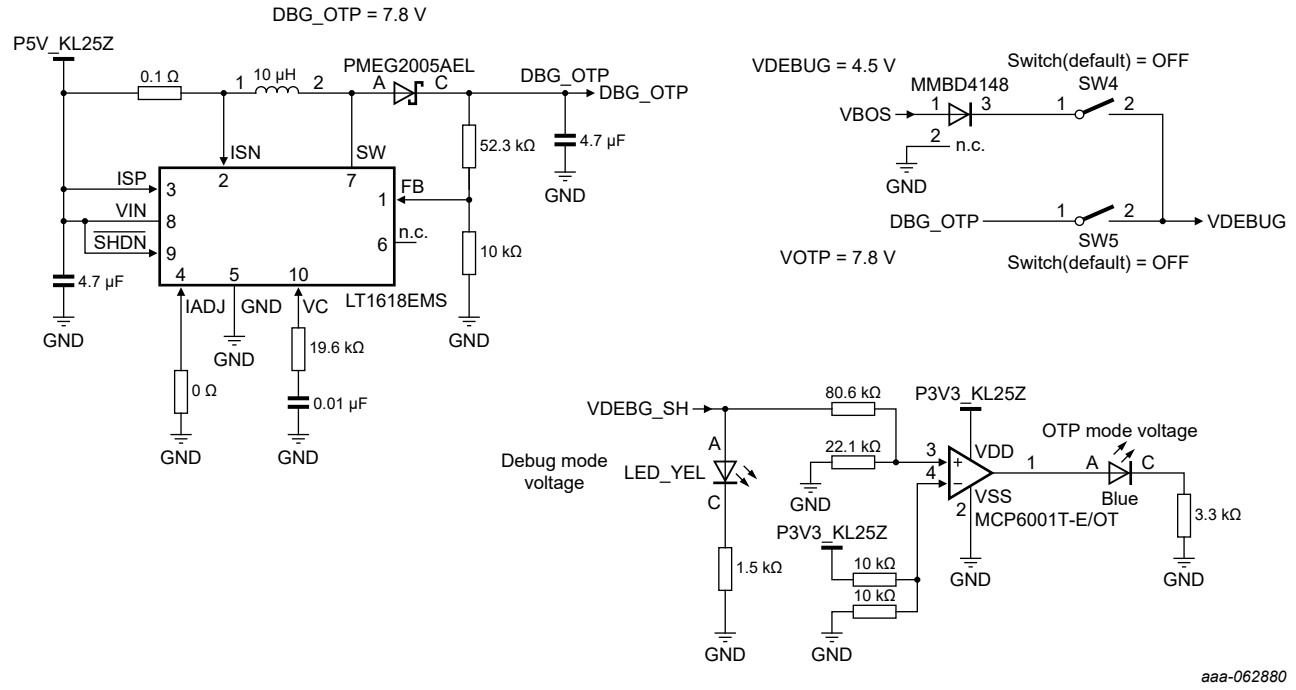


Figure 7. DEBUG pin voltage source selection and signaling schematic

5.3.3 Wake input switches

The global wake inputs can be exercised by switches SW2 for WAKE1_IN_GLOBAL and SW3 for WAKE2_IN_GLOBAL supplied by the battery to VBAT signal.

A local wake command can also be exercised directly on the pin using WAKE1_IN_LOCAL and WAKE2_IN_LOCAL.

WAKE2 pin can also be used for error monitoring. Error monitoring input ERRMON can be controlled by ERRMON_INPUT. R474 must be removed and the pulldown R473 might be populated.

All these signals can be accessed from signal connector J13.

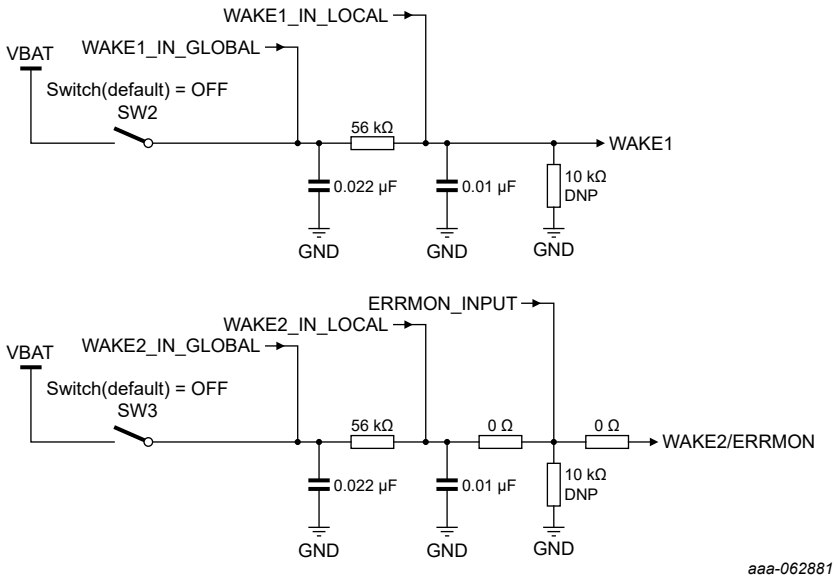


Figure 8. WAKE pins control switches

Table 4. SW2: WAKE1 switch global

Position	Function	Description
OFF	WAKE1 is low logic level	WAKE1 not active
ON	WAKE1 is high logic level	WAKE1 active

Table 5. SW3: WAKE2 switch global

Position	Function	Description
OFF	WAKE2 is low logic level	WAKE2 not active
ON	WAKE2 is high logic level	WAKE2 active

5.3.4 MCU input button

The MCU input button is an interface to the KL25Z state machine supervisor (LED_STATES).

The MCU input button is disabled when "IO PINS" > "State Control Pins" > LED_STATES is disabled.

When MCU input button is hit:

- FRDM-KL25Z board sends commands to update the LED_STATES,
- if LED_STATES shows device in main/FS OTP mode, FRDM-KL25Z board sends commands to quit OTP mode.

Note: *If device is in standby mode (LPON), device may wake-up if communication activity wake-up is enabled.*

Note: *If device is in LPOFF mode, LED_STATES will be reset.*

5.3.5 FCCU and DCLINK switches

The FCCU switch S1 can be used to force the non-error state on the FCCU pins.

Note: *SW7.6 and SW7.7 must be OFF.*

Note: *When SW7.6 and SW7.7 are ON, FCCU pins states are controlled by the FRDM-KL25Z board using the GUI in the "IO PINS" tab or with script commands.*

The DCLINK switch S2 is meant to connect the DC LINK capacitive load to the FCCU1 pin.

Figure 9 shows related schematic.

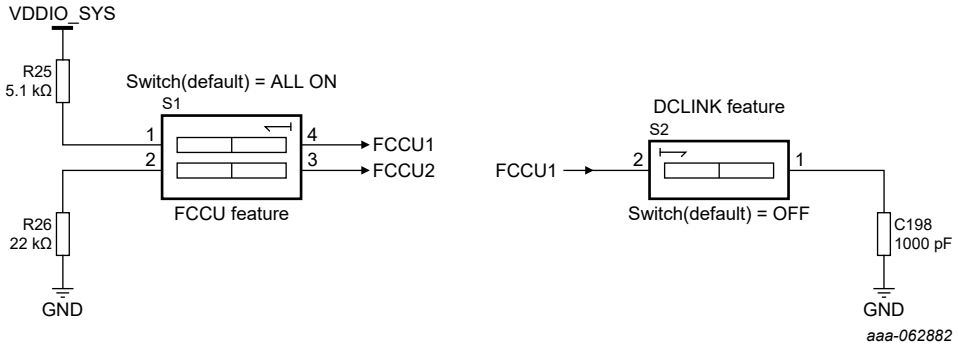


Figure 9. FCCU and DCLINK switches

Table 6. S1: FCCU switches

Switch	Function	Description
1	Set FCCU1 to non-error state	Connects FCCU1 to a 5.1 kΩ pullup to VDDIO
2	Set FCCU2 to non-error state	Connects FCCU2 to a 22 kΩ pulldown to GND

Table 7. S2: DCLINK switch

Position	Function	Description
OFF	Remove DCLINK load from FCCU1	Disconnect C198 from FCCU1 pin
ON	Connect DCLINK load to FCCU1	Connect C198 to FCCU1 pin

5.3.6 Quiescent current measurements

To perform quiescent current measurements, some switches must be turned off, and some components must be removed. All switches in SW7 and SW11 must be turned off to disable LED signaling.

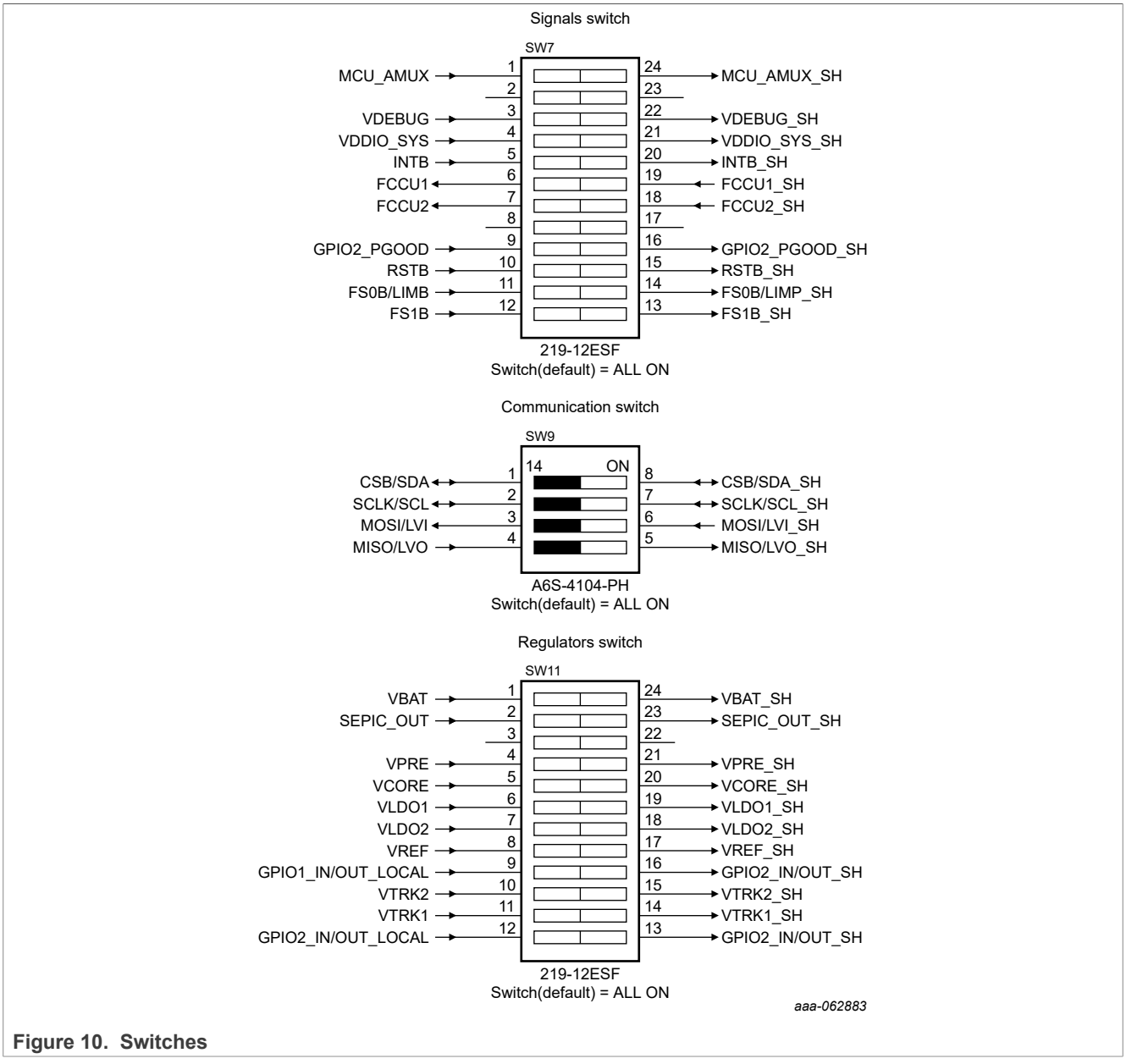


Figure 10. Switches

Table 8. SW7: Signal switches

Switch	Function	Description
1	MCU_AMUX_SH switch	Disconnects MCU_AMUX net
2	n.c.	
3	VDEBUG_SH switch	Disconnects VDEBUG net
4	VDDIO_SYS_SH switch	Disconnects VDDIO_SYS net
5	INTB_SH switch	Disconnects INTB net

Table 8. SW7: Signal switches*...continued*

Switch	Function	Description
6	FCCU1_SH switch	Disconnects FCCU1 net
7	FCCU2_SH switch	Disconnects FCCU2 net
8	n.c.	
9	n.c.	
10	RSTB_SH switch	Disconnects RSTB net
11	FS0B/LIMP_SH switch	Disconnects FS0B/LIMP net
12	FS1B_SH switch	Disconnects FS1B net

Table 9. SW9: Communication switches

Switch	Function	Description
1	CSB/SDA_SH switch	Disconnects CSB/SDA net
2	SCLK/SCL_SH switch	Disconnects SCLK/SCL net
3	MOSI/LVI_SH switch	Disconnects MOSI/LVI net
4	MISO/LVO_SH switch	Disconnects MISO/LVO net

Table 10. SW11: Regulators switches

Switch	Function	Description
1	VBAT_SH switch	Disconnects MCU_AMUX net
2	FLYBACK_OUT_SH	Disconnects FLYBACK_OUT net
3	FLYBACK_OUT_2_SH	Disconnects FLYBACK_OUT_2
4	VPRE_SH switch	Disconnects VPRE net
5	VCORE_SH switch	Disconnects VCORE net
6	VLDO1_SH switch	Disconnects VLDO1 net
7	VLDO2_SH switch	Disconnects VLDO2 net
8	VREF_SH switch	Disconnects VREF net
9	GPIO1_IN/OUT_SH switch	Disconnects GPIO1_IN/OUT_SH net
10	VTRK2_SH switch	Disconnects VTRK2 net
11	VTRK1_SH switch	Disconnects VTRK1 net
12	GPIO2_PGOOD_SH switch	Disconnects GPIO2_PGOOD net

5.4 Jumpers

Jumper locations are shown in Figure 11.

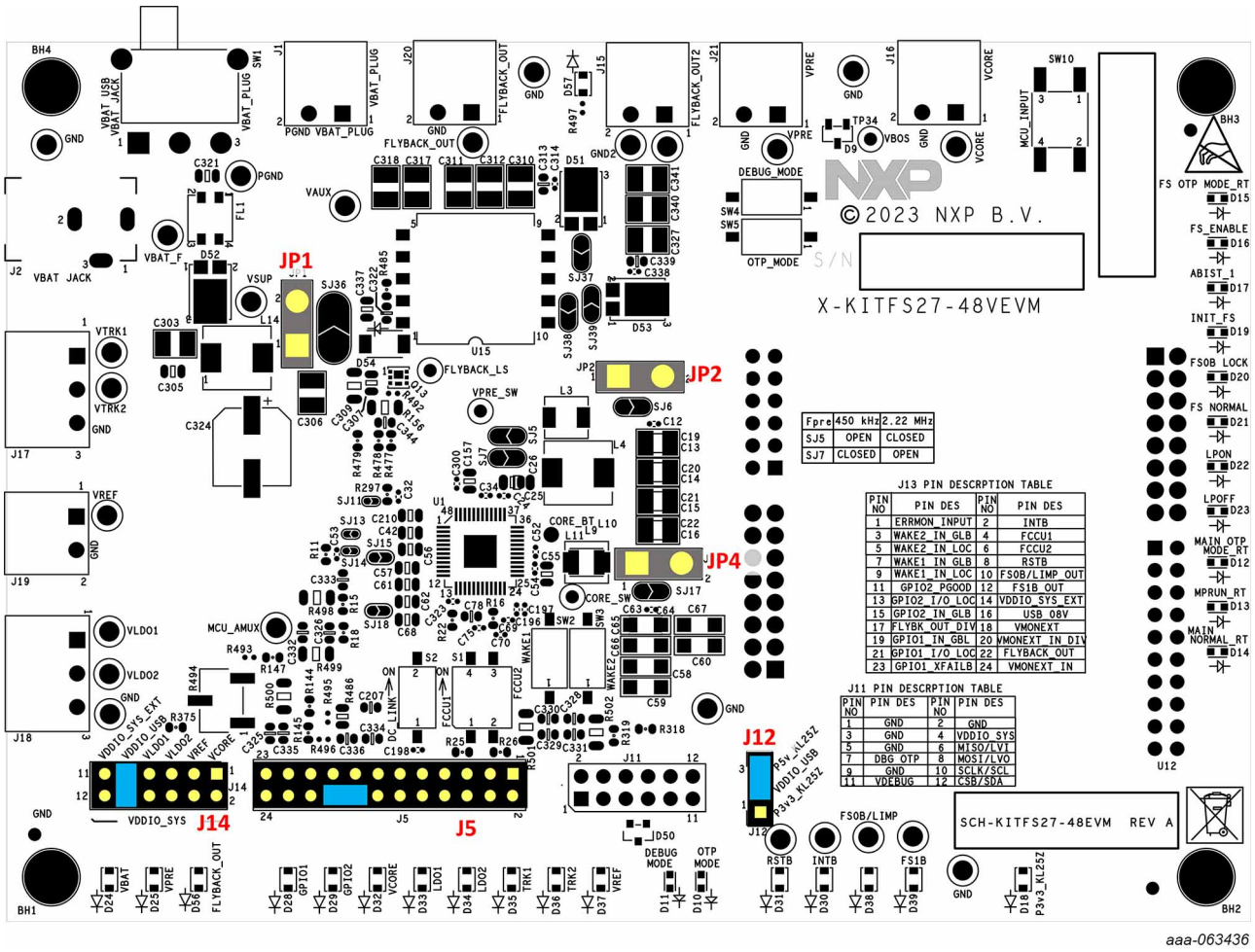


Figure 11. Jumper locations

Jumpers for current measurement are described in Table 11.

Other jumpers are described in the following sections.

Table 11. Jumpers for current measurement descriptions

Name	Function	Pin number	Note
JP1	Flyback regulator input inductor current measurement	1−2	SJ36 must be open
JP2	VPRE regulator output inductor current measurement	1−2	SJ6 must be open
JP4	VCORE regulator output inductor current measurement	1−2	SJ17 must be open

5.4.1 VDDIO selection

VDDIO pin (VDDIO_SYS net) can be 1.8 V, 3.3 V, or 5.0 V, depending on the system requirements.

J14 shown in Figure 12 allows to connect VDDIO_SYS to a device regulator, to a FRDM-KL25Z board rail from USB, or to an external source on VDDIO_SYS_EXT (J13.20).

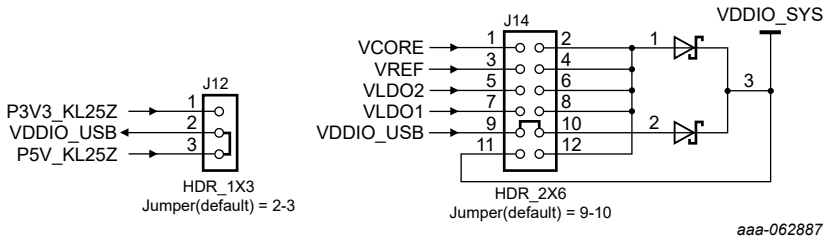


Figure 12. VDDIO pin supply source selector headers

J14 allows selection of the VDDIO_SYS source, description is shown in Table 12.

The diodes are used to compose an OR supply, two jumpers can be placed on J14, so VDDIO_SYS is supplied by VDDIO_SUB and a regulator. As a result, the user can start the device in emulation mode, then disconnect the USB cable, without loosing the VDDIO_SYS supply. The diodes prevent VDDIO_USB from supplying the regulator output and the opposite.

The diodes can be bypassed if needed, but then only one supply is then allowed. Position 9-11 is used for VDDIO_USB without diode, or any regulator position 1-2, 3-4, 5-6, 7-8 plus 11-12 to bypass the diode.

Table 12. J14: VDDIO_SYS header

Jumper position	VDDIO_SYS source	VDDIO_SYS value
1-2	VCORE	VCORE regulator output voltage through diode
3-4	VREF	VREF regulator output voltage through diode
5-6	VLDO1	LDO1 regulator output voltage through diode
7-8	VLDO2	LDO2 regulator output voltage through diode
9-10 (default)	VDDIO_USB	VDDIO_USB (see J12) through diode
9-11	VDDIO_USB	VDDIO_USB (see J12) without diode
11-12	VDDIO_SYS_EXT	1-2, 3-4, 5-6, 7-8 diode bypass

J12 allows selection of the VDDIO_USB source. The description is shown in Table 13.

Table 13. J12: VDDIO_USB header

Jumper position	VDDIO_USB source	VDDIO_USB value
1-2	P3V3_KL25Z	3.3 V
2-3 (default)	P5V_KL25Z	5.0 V

5.4.2 VMONEXT: external voltage monitoring

The VMONEXT monitoring pin can monitor 0.8 V and 5.0 V targets. The kit-related scheme is show in Figure 13.

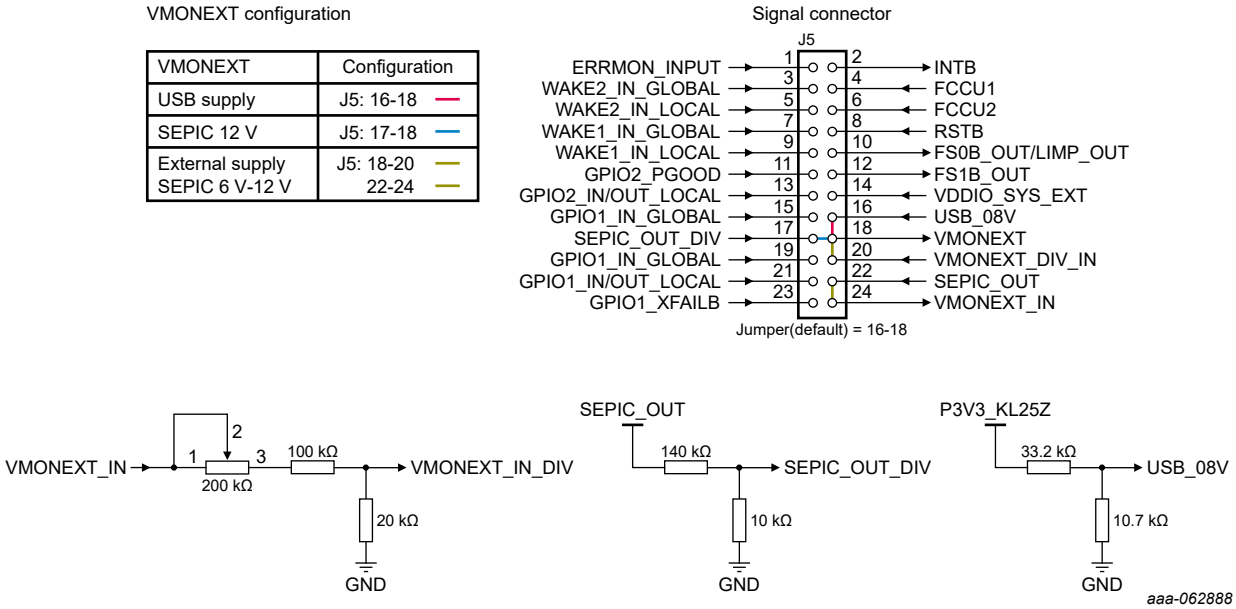


Figure 13. VMONEXT monitoring resistor bridge schematic

VMONEXT pin can be connected to multiple sources thought J5 shown in Table 14, such as SEPIC regulator at 12 V with a fixed resistor bridge, the line VMONEXT_IN in a range from 6.0 V to 12 V with a variable resistor bridge, FRDM-KL25Z board 3.3 V rail with a fixed external resistor bridge (for debug purposes). VMONEXT_IN can be connected to SEPIC_OUT.

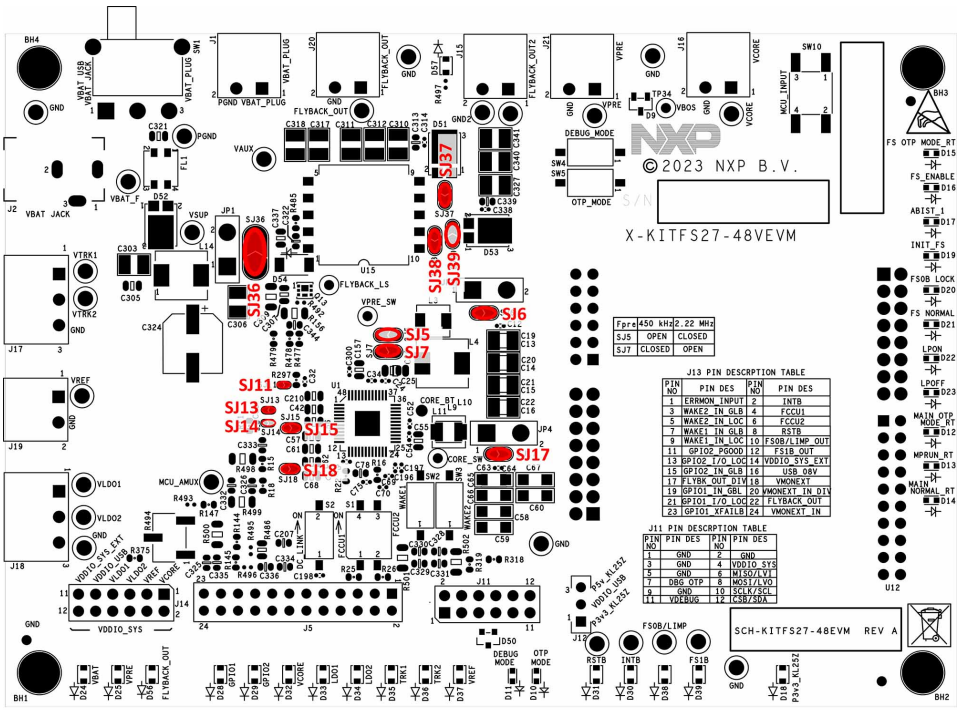
VMONEXT_IN can be connected to any source or regulator, the variable external bridge must adjusted using a screwdriver on potentiometer. The VMONEXT voltage should around 0.8 V when enabled.

Table 14. J5: Signal connector header (VMONEXT highlight)

Jumper position	VMONEXT source	VMONEXT value
16-18	USB supply	0.8 V for evaluation (no error)
17-18	SEPIC_OUT	SEPIC regulator at 12 V
18-20 22-24	SEPIC_OUT	SEPIC regulator from 6.0 V to 12 V, adjustable with variable resistor

5.5 Solder joints

Solder joint locations are Shown in Figure 14.



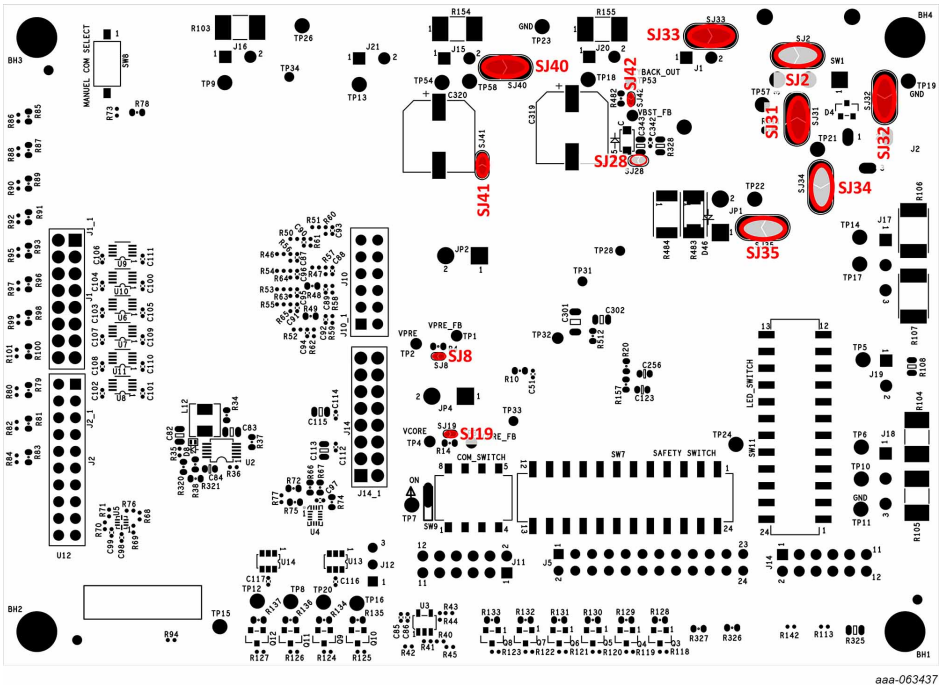


Figure 14. Solder joint locations

Solder joints are described in Table 15.

Table 15. Solder joints descriptions

Name	Function	Default state	Note
SJ2	Bypass SW1: VBAT connected to J1	Closed	
SJ5	Connect VPRE_SW to L3 (inductor F_{PRE} = 2.2 MHz)	Open	SJ7 must be open
SJ6	Bypass JP2: jumper for VPRE regulator output inductor current measurement	Closed	
SJ7	Connect VPRE_SW to L4 (inductor F_{PRE} = 444 kHz)	Closed	SJ5 must be open
SJ8	Bypass R4: resistor for VPRE regulator stability measurement	Closed	
SJ11	Connect GPIO2 pin to GPIO2 input/output external components	Closed	
SJ13	Connect GPIO1 pin to GPIO1 input/output external components	Closed	SJ14 must be open
SJ14	Connect GPIO1 pin to GPIO1 XFAILB components	Open	SJ13 must be open
SJ15	Connect VPRE regulator output to TRKIN pin	Closed	
SJ17	Bypass JP4: jumper for VCORE regulator output inductor current measurement	Closed	
SJ18	Connect VPRE regulator output to LDOIN pin	Closed	
SJ19	Bypass R14: resistor for VCORE regulator stability measurement	Closed	
SJ28	Connect flyback auxiliary winding to VAUX output external components	Open	
SJ31 SJ32 SJ33	Bypass FL1: Input common mode filter transformer	Closed	
SJ34	Bypass D52: VBAT reverse protection diode	Open	
SJ35	Bypass L14: PI filter inductor	Open	
SJ36	Bypass JP1: jumper for flyback regulator primary (input) current measurement	Closed	
SJ37	Connect flyback secondary 1 winding to FLYBACK_OUT (main) output external components	Closed	
SJ38	Connect flyback secondary 1 and secondary 2 windings in parallel	Closed	
SJ39	Connect flyback secondary 2 winding to FLYBACK_OUT_2 (secondary) output external components	Open	
SJ42	Bypass R482: resistor for flyback regulator stability measurement	Closed	
SJ140 SJ141	Connect flyback secondary 2 winding (isolated output) to ground (no more isolated)	Closed	

5.5.1 VPRE external components

This board is delivered with VPRE external components for 444 kHz. JP2 can be used for inductor current measurements when SJ6 is open.

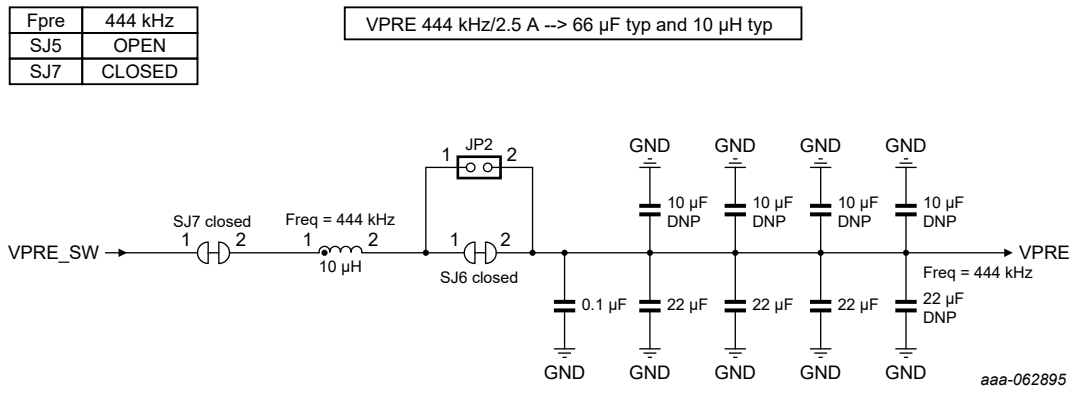


Figure 15. VPRE external components

5.5.2 VCORE external components

This board is delivered with VCORE external components (inductor 0.47 uH, output capacitor 4x 88 uF) for 0.8 V to 1.35 V up to 3.5 A. JP4 can be used for inductor current measurements when SJ17 is open.

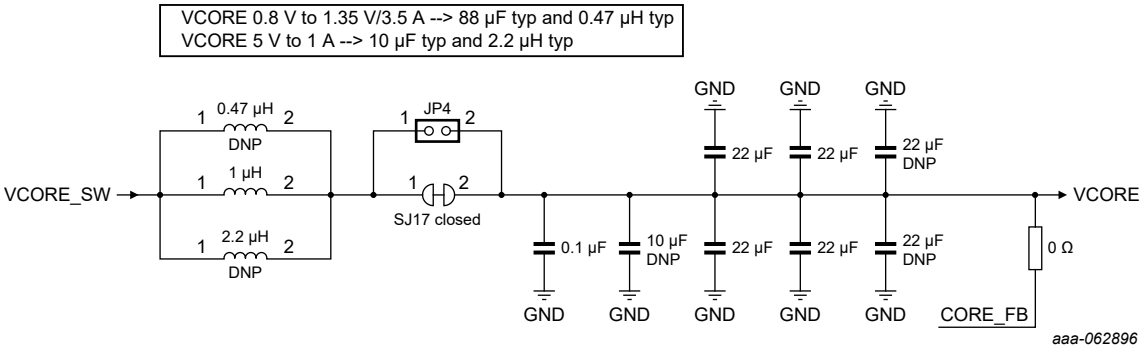


Figure 16. VCORE external components

5.5.3 LDOIN and TRKIN connection

LDOIN and TRKIN are connected by default to VPRE through solder joints.

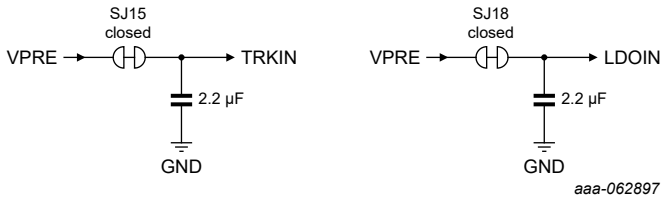


Figure 17. LDOIN and TRKIN schematics

5.5.4 GPIO1 and GPIO2

The GPIO1 and GPIO2 can be used as output, local input and global input (default).

Jumpers J52 and J51 headers, shown in Figure 18, allow to choose between input and output external components.

Note: *If the internal pullups or pulldowns are not enabled or are not strong enough, external pullups/pulldowns can be populated on R110, R111, R109, and R469.*

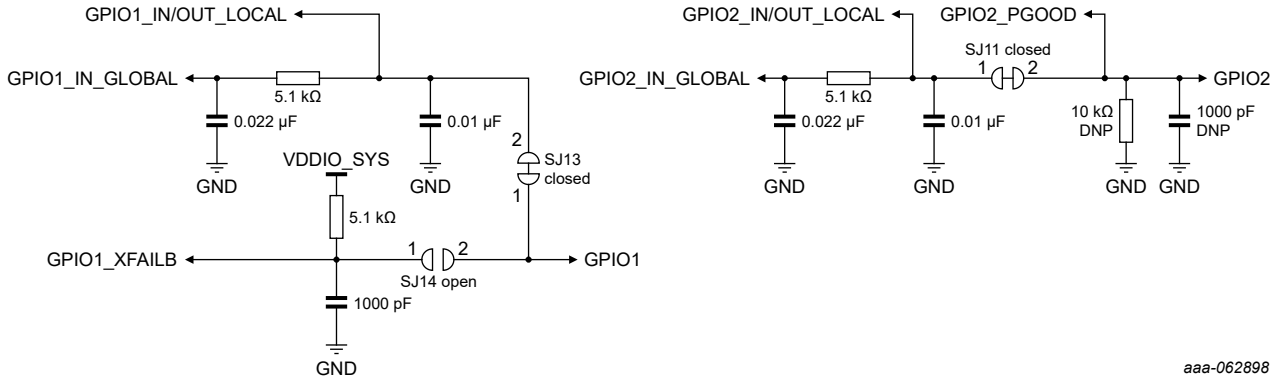


Figure 18. GPIO1 and GPIO2 schematics

All input/output access points are available at J13.

Note: *The external pullups and pulldowns for the GPIO are not populated. If the internal pullups or pulldowns are not enabled by OTP, the user can add external PU/PD through J13.*

5.6 Connectors

Figure 19 shows the location of connectors on the board.

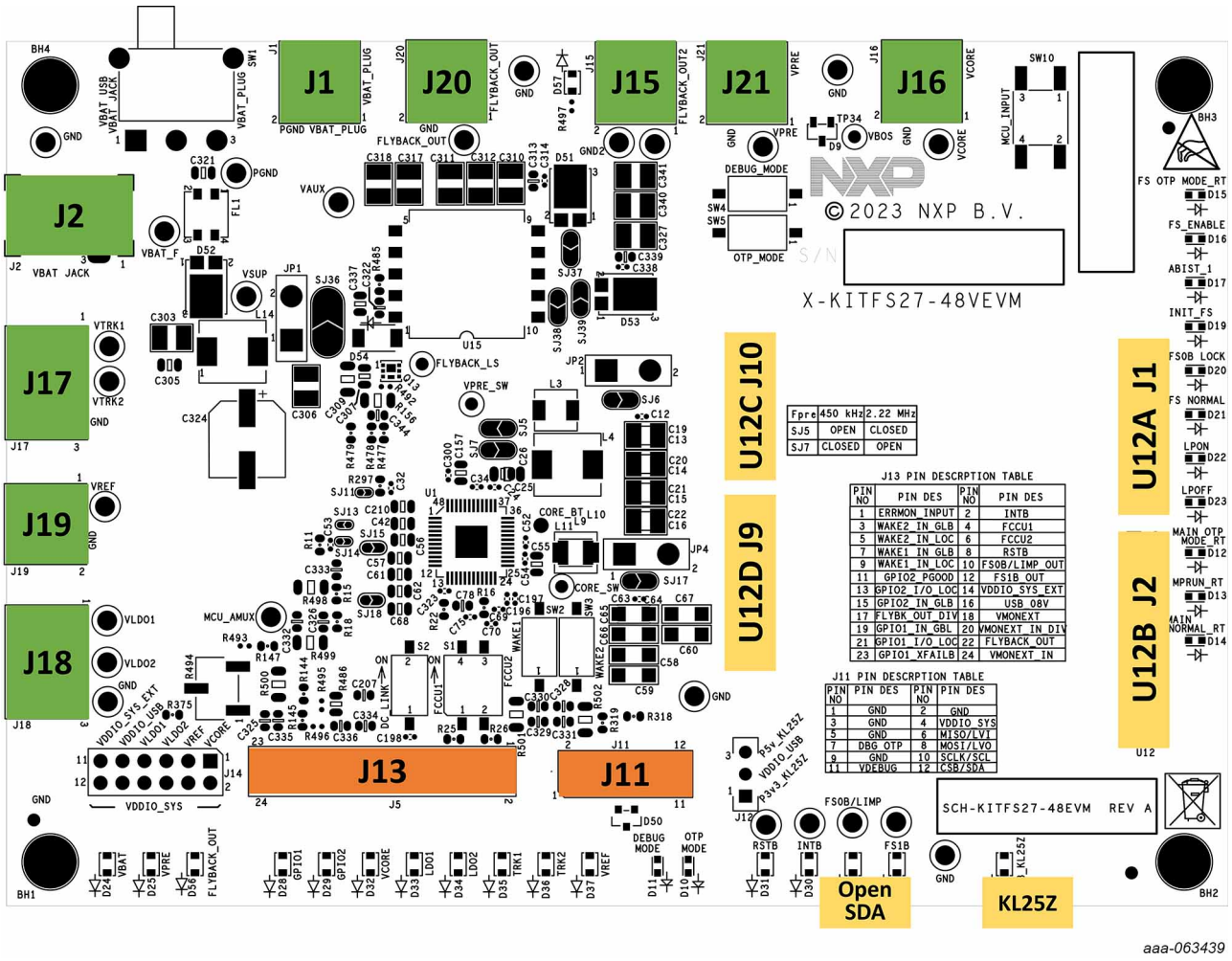


Figure 19. Connector locations

Table 16. J1: VBAT Phoenix connector

Pin	Signal name	Description
1	VBAT	Battery voltage supply input
2	GND	Ground

5.6.1 Output power supply connectors

Output regulators are accessible through test points and Phoenix connectors in order to take measurements or to plug loads. Male connectors are included on this kit to plug or unplug wires easily. All output regulators are located at the left and top edge of the board as shown in Figure 2.

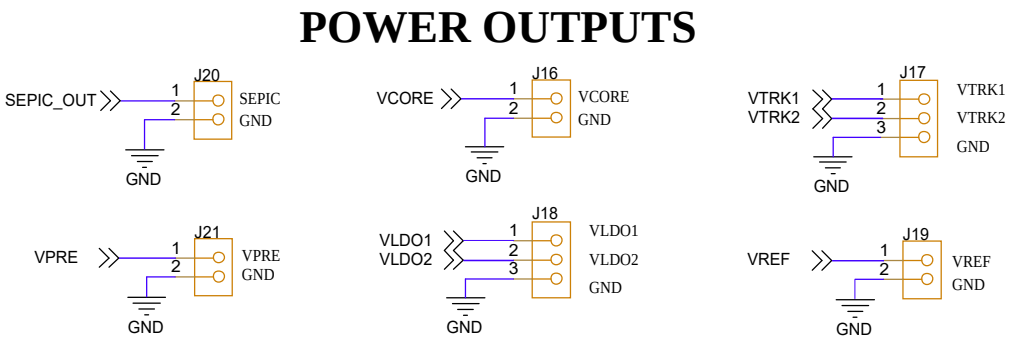


Figure 20. Power output Phoenix connectors

Table 17. J20: FLYBACK OUT connector

Pin	Signal name	Description
1	FLYBACK_OUT	Flyback regulator output
2	GND	Ground

Table 18. J15: FLYBACK OUT 2 connector

Pin	Signal name	Description
1	FLYBACK_OUT_2	Flyback regulator output 2 (not regulated)
2	GND	Ground

Table 19. J21: VPRE connector

Pin	Signal name	Description
1	VPRE	VPRE regulator output
2	GND	Ground

Table 20. J16: VCORE connector

Pin	Signal name	Description
1	VCORE	VCORE regulator output
2	GND	Ground

Table 21. J18: VLDO1/VLDO2 connector

Pin	Signal name	Description
1	LDO1	LDO1 regulator output

Table 21. J18: VLDO1/VLDO2 connector...*continued*

Pin	Signal name	Description
2	LDO2	LDO2 regulator output
3	GND	Ground

Table 22. J17: VTRK1/VTRK2 connector

Pin	Signal name	Description
1	VTRK1	VTRK1 regulator output
2	VTRK2	VTRK2 regulator output
3	GND	Ground

Table 23. J19: VREF connector

Pin	Signal name	Description
1	VREF	VREF regulator output
2	GND	Ground

5.6.2 Signal and program connectors

Signal and program connectors provide access to most of the device signals to program the device externally or to perform debug and diagnosis.

Figure 21. Signal and debug headers connectors

Table 24. J11: Program connector

Pin	Signal name	Description
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	VDDIO_SYS	VDDIO pin access
5	GND	Ground
6	MISO/LVO	MOSI/LVO pin access
7	DBG_OTP	DBG_OTP power supply (7.8 V) access
8	MOSI/LVI	MOSI/LVI pin access
9	GND	Ground
10	SCLK/SCL	SCLK/SCL pin access
11	VDEBUG	DEBUG pin voltage
12	CSB/SDA	CSB/SDA pin access

Table 25. J13: Signal connector

Pin	Signal name	Description
1	ERRMON_INPUT	Error monitoring (WAKE2 pin) input
2	INTB	Interrupt output for MCU
3	WAKE2_IN_GLOBAL	WAKE2 input connection when used as a global input
4	FCCU1	FCCU1 pin access
5	WAKE2_IN_LOCAL	WAKE2 input connection (WAKE2 pin) when used as a local input
6	FCCU2	FCCU2 pin access
7	WAKE1_IN_GLOBAL	WAKE1 input connection when used as a global input
8	RSTB	Reset output for MCU
9	WAKE1_IN_LOCAL	WAKE1 input connection (WAKE1 pin) when used as a local input
10	FS0B_OUT/LIMP_OUT	Safety output 0 (FS0B pin) access
11	GPIO2_PGOOD	GPIO2 access (GPIO2 pin) when used as PGOOD
12	FS1B_OUT	Safety output 1 (FS1B pin) access
13	GPIO2_IN/OUT_LOCAL	GPIO2 access (GPIO2 pin) when used as local input or output
14	VDDIO_SYS_EXT	Optional external supply for VDDIO. A jumper between J14 11-12 pins is required
15	GPIO2_IN_GLOBAL	GPIO2 access (GPIO2 pin) when used as global input

Table 25. J13: Signal connector*...continued*

Pin	Signal name	Description
16	USB_08V	0.8 V regulator
17	SEPIC_OUT_DIV	SEPIC regulator voltage divider 15:1. Connect to VMONEXT when SEPIC is set to 12 V.
18	VMONEXT	External voltage monitoring (VMONEXT pin) access
19	GPIO1_IN_GLOBAL	GPIO1 access (GPIO1 pin) when used as global input
20	VMONEXT_IN_DIV	VMONEXT adjustable divider output. Connect to VMONEXT and input at VMONEXT_IN.
21	GPIO1_IN/OUT_LOCAL	GPIO1 access (GPIO1 pin) when used as local input or output
22	SEPIC_OUT	SEPIC regulator output
23	GPIO1_XFAILB	GPIO1 access (GPIO1 pin) when used as XFAILB
24	VMONEXT_IN	VMONEXT adjustable divider input

5.6.3 FRDM-KL25Z board connectors

Table 26. FRDM-KL25Z board USB connectors

Schematic label	Signal name	Description
FRDM-KL25Z	N/A	USB connector used to communicate with the GUI
OpenSDA	N/A	USB connector used to flash the KL25Z MCU

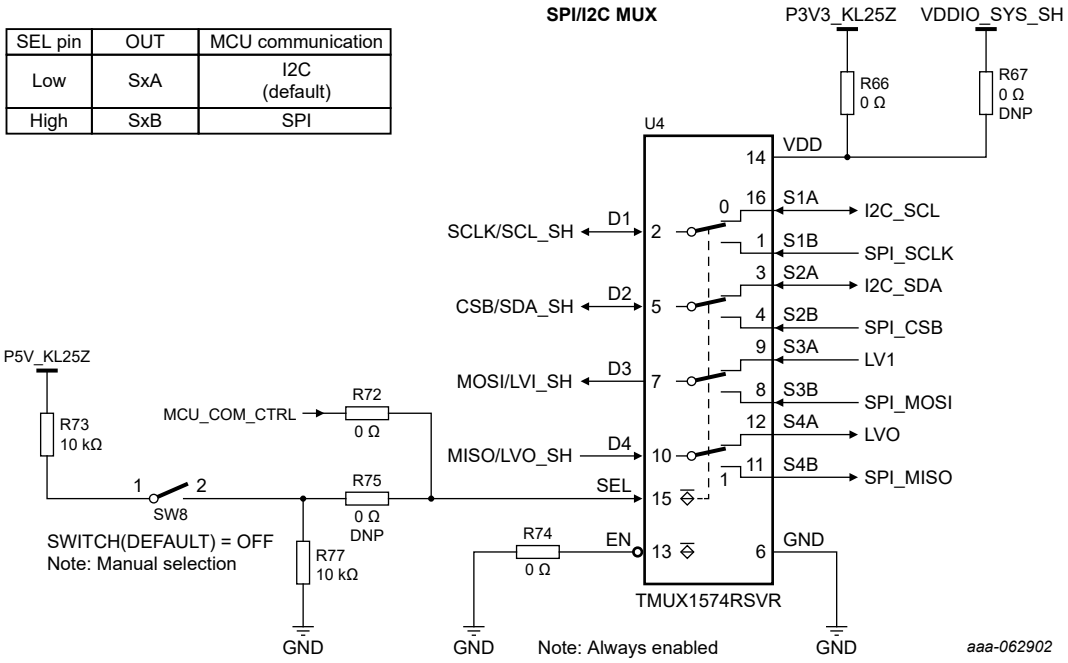
Table 27. U12A: FRDM-KL25Z board safety outputs, IOs, and SPI connector

Pin	Signal name	Description
1	SPI_MISO_MCU	SPI MISO connection to KL25Z
2	LVI_MCU	LVI connection to KL25Z
3	MCU_COM_CTRL	Not connected
4	RSTB_MCU	Reset sense to KL25Z (active low-logic level)
5	n.c.	Not connected
6	n.c.	Not connected
7	SPI_CSB_MCU	SPI CSB connection to KL25Z
8	n.c.	Not connected
9	SPI_SCLK_MCU	SPI SCLK connection to KL25Z
10	FS0B/LIMP_MCU	FS0B/LIMP sense connection to KL25Z
11	SPI_MOSI_MCU	SPI MOSI connection to KL25Z
12	INTB_MCU	Interruption (active low-logic level)
13	n.c.	Not connected
14	n.c.	Not connected
15	LVO_MCU	LVO sense connection to KL25Z
16	INPUT_BUTTON_MCU	Button SW10 connection to KL25Z

Table 28. U12B: FRDM-KL25Z board I^2C, FCCU, and main states M_STATEx connector

Pin	Signal name	Description
1	FCCU1_MCU	FCCU1 connection to KL25Z
3	FCCU2_MCU	FCCU2 connection to KL25Z
6	M_STATE0	MCU output for LED D12 - MAIN_OTP_MODE_RT
8	M_STATE1	MCU output for LED D13 - LPRUN_RT
10	M_STATE2	MCU output for LED D14 - MAIN_NORMAL_RT
14	GND	Ground
18	I2C_SDA_MCU	I^2C serial data line connection to KL25Z
20	I2C_SCL_MCU	I^2C serial clock line connection to KL25Z
Others	n.c.	Not connected

Figure 22 show the MUX used to split SPI and I²C signals. The communication protocol is selected automatically by the GUI using the FRDM-KL25Z board output MCU_COM_CTRL.



SEL pin	OUT	MCU communication
Low	SxA	I2C (default)
High	SxB	SPI

Figure 22. SPI and I²C MUX

Figure 23 show the level shifters used to connected SPI and I²C signals to the FRDM-KL25Z board inputs.

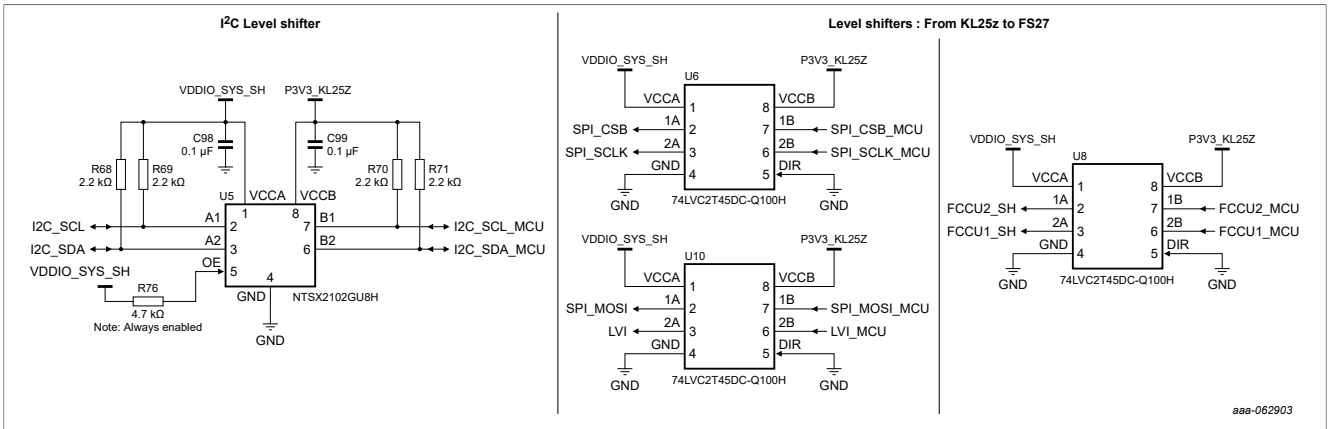


Figure 23. SPI and I²C level shifters

Table 29. U12C: FRDM-KL25Z board ADC connector

Pin	Signal name	Description
1	VLDO2_ADC	LDO2 regulator output to KL25Z ADC
2	VPRE_ADC	VPRE regulator output to KL25Z ADC
3	VREF_ADC	VREF regulator output to KL25Z ADC
4	n.c.	Not connected
5	VTRK1_ADC	TRK1 regulator output to KL25Z ADC
6	VDEBUG_ADC	DEBUG pin voltage to KL25Z ADC
7	VTRK2_ADC	TRK2 regulator output to KL25Z ADC

Table 29. U12C: FRDM-KL25Z board ADC connector...*continued*

Pin	Signal name	Description
8	VDDIO_SYS_ADC	VDDIO pin voltage to KL25Z ADC
9	n.c.	Not connected
10	AMUX_ADC	AMUX_MCU voltage to KL25Z ADC
11	VCORE_ADC	VCORE regulator output to KL25Z ADC
12	VLDO1_ADC	LDO1 regulator output to KL25Z ADC

The measurements related to the AMUX are accessible on "ACCESS" > "AMUX".

The measurements performed by the FRDM-KL25Z board are accessible on "IO PINS" > "ADC Measurements".

Figure 24 show the resistors bridge connected to Table 29.

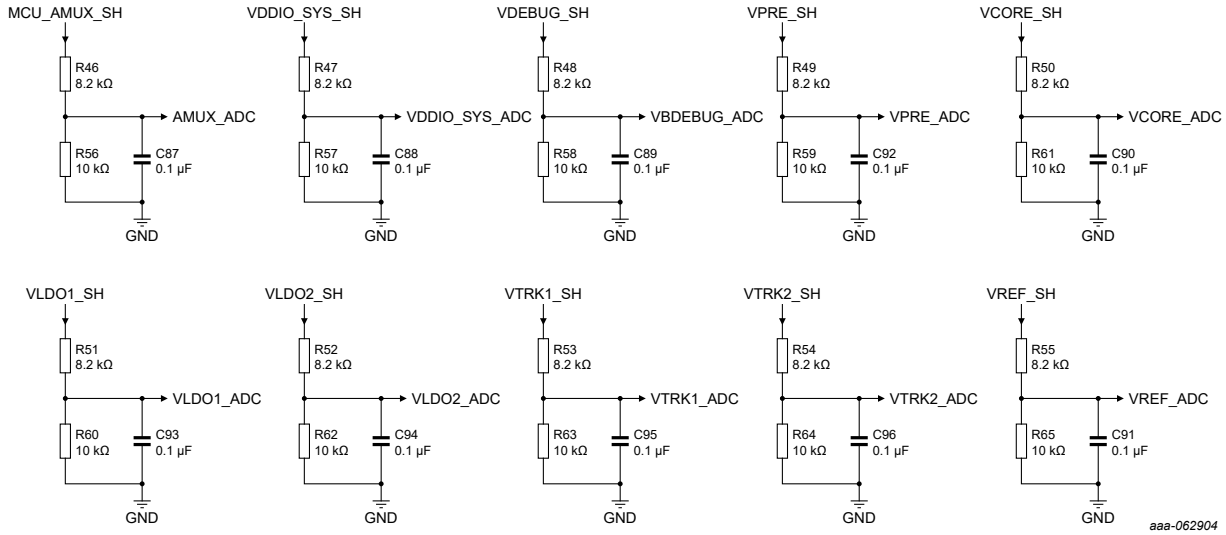


Figure 24. ADC resistor bridges

Table 30. U12D: FRDM-KL25Z board supply and fail-safe states FS_STATEx connector

Pin	Signal name	Description
1	FS_STATE0	MCU output for LED D15 - FS_OTP_MODE_RT
2	n.c.	Not connected
3	FS_STATE1	MCU output for LED D16 - FS_ENABLE/ABIST
4	P3V3_FRDM-KL25Z	3.3 V generated from FRDM-KL25Z board USB
5	FS_STATE2	MCU output for LED D17 - FS_DBG_MODE_RT
6	n.c.	Not connected
7	FS_STATE3	MCU output for LED D19 - INIT_FS
8	P3V3_FRDM-KL25Z	3.3 V generated from FRDM-KL25Z board USB
9	FS_STATE4	MCU output for LED D20 - FS0B_LOCK
10	P5V_FRDM-KL25Z	5.0 V from FRDM-KL25Z board USB
11	FS_STATE5	MCU output for LED D21 - FS_NORMAL
12	GND	Ground

Table 30. U12D: FRDM-KL25Z board supply and fail-safe states FS_STATEx connector*...continued*

Pin	Signal name	Description
13	FS_STATE6	MCU output for LED D22 - LPON
14	GND	Ground
15	FS_STATE7	MCU output for LED D23 - LPOFF
16	n.c.	not connected

5.7 LED indicators

LED indicators present on the board display the status of VBAT, regulators, safety outputs, GPIOs, and device state machines (FSM) states. LEDs are green for VBAT, regulators, and GPIOs, indicating that the rail is powered on. LEDs are green for FSM states. LEDs are red for safety outputs and interrupt, indicating when the pins are asserted.

Figure 25 show LED indicators location.

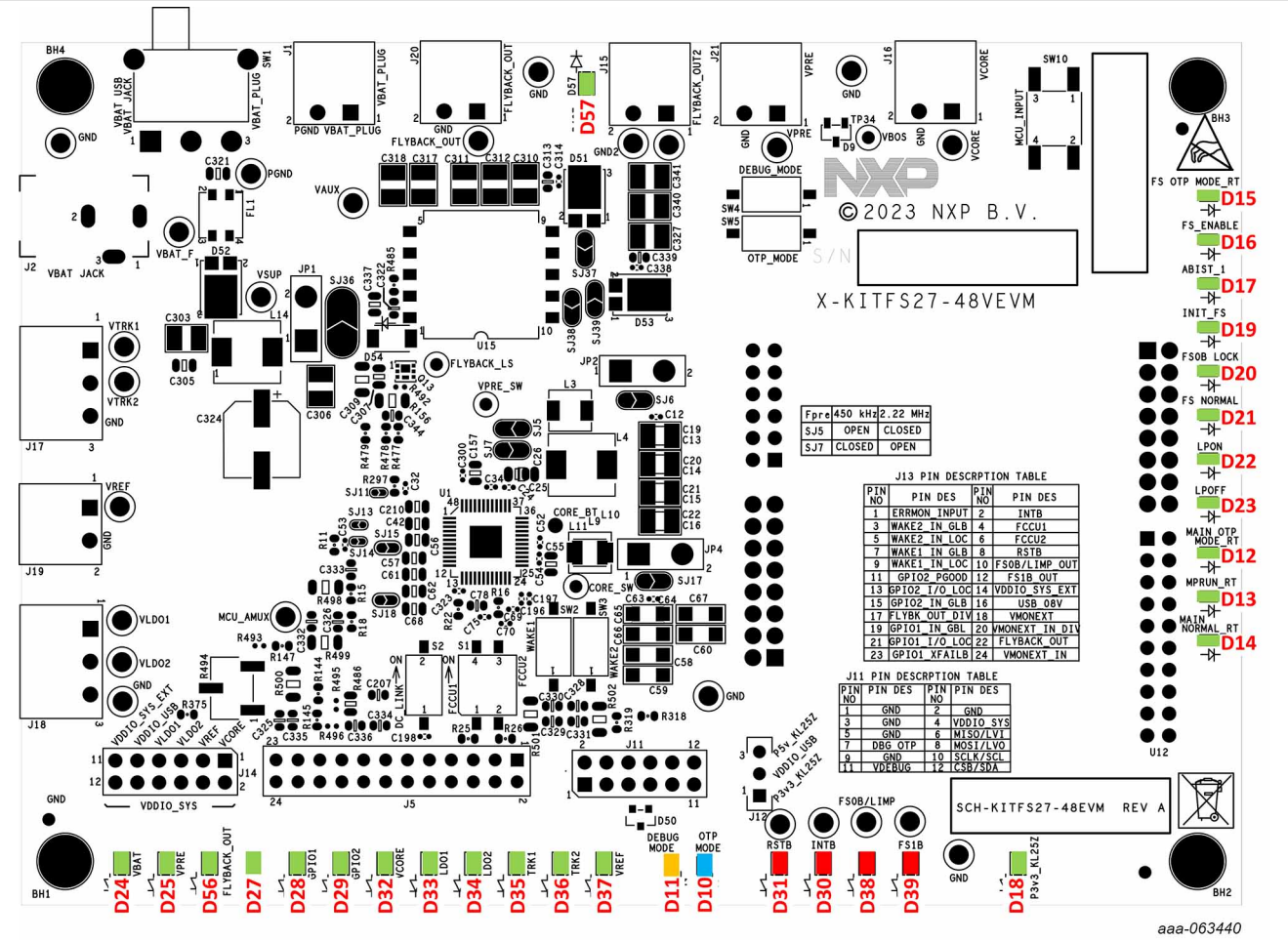


Figure 25. LED indicators location

The general indicators are listed in Table 31.

Table 31. Safety IO's indicators description

Label	Name	Color	Description
D30	INTB	Red	INTB pin state indicator
D31	RSTB	Red	RSTB pin state indicator
D38	FS0B/LIMP	Red	FS0B/LIMP pin state indicator
D39	FS1B	Red	FS1B pin state indicator
D51	PGOOD	Green	PGOOD pin state indicator

The supply indicators are listed in Table 32.

Table 32. Supply indicators description

Label	Name	Color	Description
D10	OTP mode	Blue	DEBUG pin voltage ≥ 7.8 V (OTP programming)
D11	DEBUG mode	Yellow	DEBUG pin voltage ≥ 3.5 V (debug mode)
D18	P3V3_KL25Z	Green	FRDM-KL25Z board 3.3 V rail indicator
D24	VBAT	Green	VBAT rail led

The regulators and GPIOs indicators are listed in Table 33.

Table 33. Regulators and GPIO indicators description

Label	Name	Color	Description
D25	VPRE	Green	VPRE regulator output indicator
D26	SEPIC_OUT	Green	SEPIC regulator output indicator
D28	GPIO1	Green	GPIO1 pin state indicator
D29	GPIO2	Green	GPIO2 pin state indicator
D32	VCORE	Green	VCORE regulator output indicator
D33	LDO1	Green	LDO1 regulator output indicator
D34	LDO2	Green	LDO2 regulator output indicator
D35	TRK1	Green	TRK1 regulator output indicator
D36	TRK2	Green	TRK2 regulator output indicator
D37	VREF	Green	VREF regulator output indicator

The states indicators of the two state machines are listed in Table 34. These indicators can be disabled using the GUI on "IO PINS" > "State Control Pins" > LED_STATES.

Table 34. Main/fail-safe state machines state indicators description

Label	Name	Color	Description
D15	FS_OTP_MODE_RT	Green	Fail-safe state machine in FS_OTP_MODE_RT (FS_OTP_MODE_RT = 1)
D16	FS_ENABLE/ABIST	Green	Fail-safe state machine in: • FS_ENABLE, when main state machine in LPRUN mode or, • waiting ABIST start, if the OTP_MODE switch is ON, or, • RSTB is asserted externally (blinking), if the OTP_MODE switch is ON.
D17	FS_DBG_MODE_RT	Green	Fail-safe state machine DEBUG mode is active (FS_DBG_MODE_RT = 1)
D19	INIT_FS	Green	Fail-safe state machine in INIT_FS. Fail-safe state machine in MCU flash mode (blinking).
D20	FS0B_LOCK	Green	Fail-safe state machine in FS0B_LOCK
D21	FS_NORMAL	Green	Fail-safe state machine in FS_NORMAL
D22	LPON	Green	Main state machine in LPON (standby) mode
D23	LPOFF	Green	Main state machine in LPOFF mode
D12	MAIN_OTP_MODE_RT	Green	Main state machine in OTP mode (MAIN_OTP_MODE_RT = 1)
D13	LPRUN_RT	Green	Main state machine in LPRUN_RT (LPRUN_RT = 1)
D14	MAIN_NORMAL_RT	Green	Main state machine in MAIN_NORMAL (MAIN_NORMAL_RT = 1)
All	All	Green	Wake-up from deep fail-safe (blink 2x 2 times with shift)

The LED indicators supply is VLED, taken from the USB generated DBG_OTP supply when the USB is connected, otherwise from VPRE, when powered on. This arrangement allows the LEDs to be powered on when VPRE is off.

These LEDs can be disconnected manually at any time with the switch SW7 and SW11 to avoid undesired losses and obtain more accurate current consumption measurements.

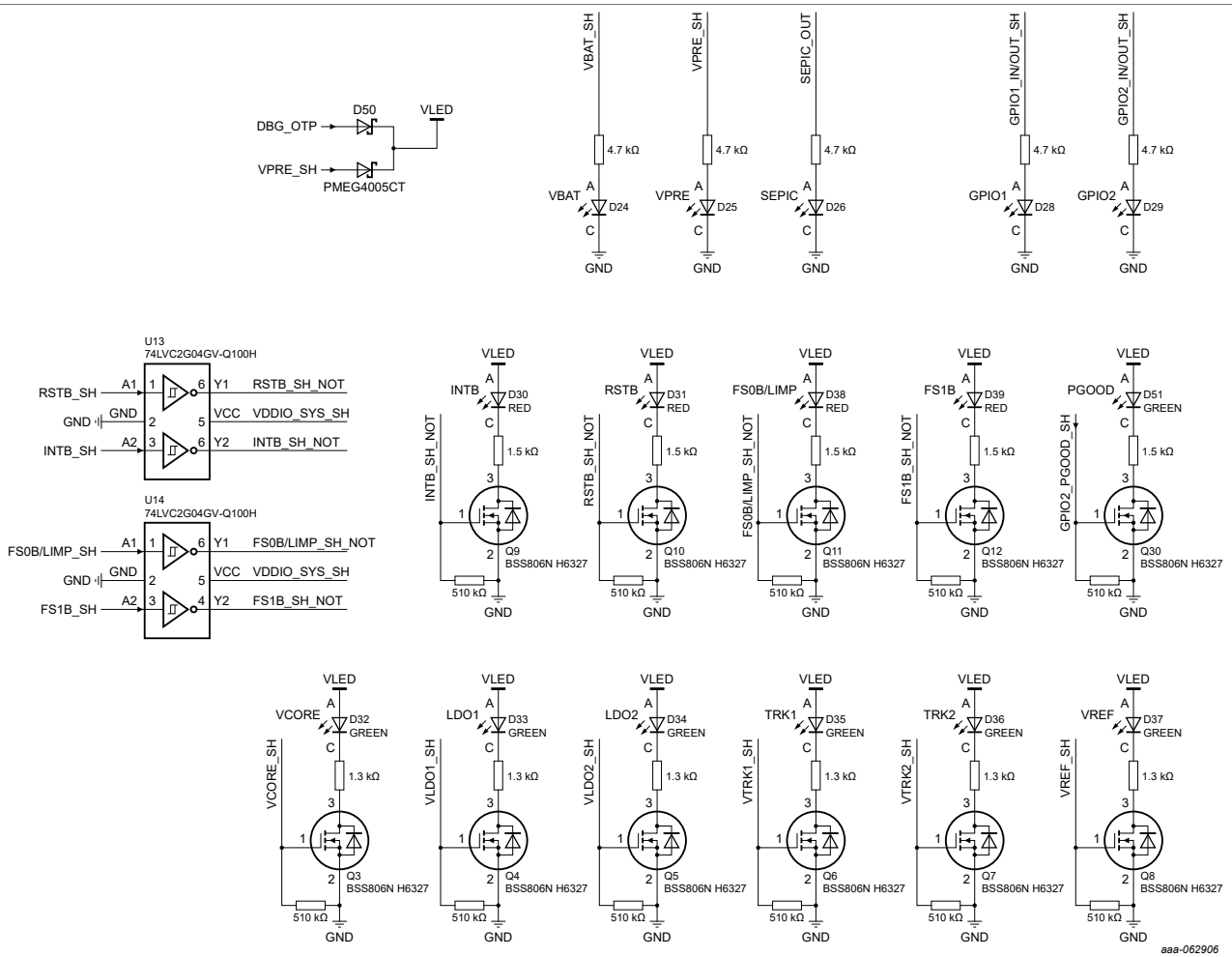
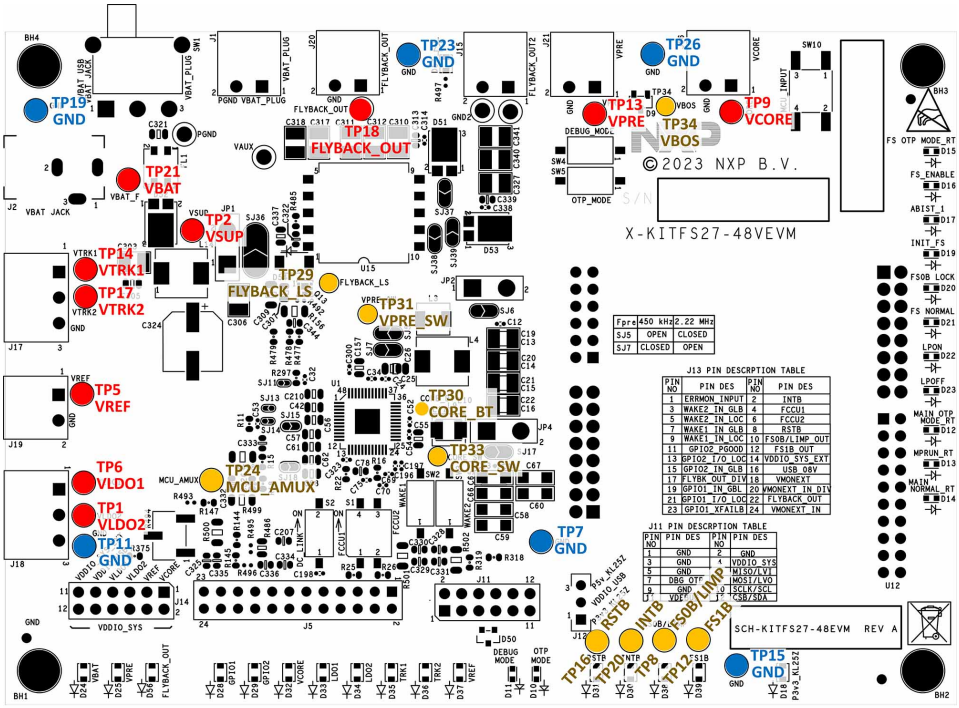


Figure 26. Power regulators and LED indicators connections

5.8 Test points

Test point locations are Shown in Figure 27.



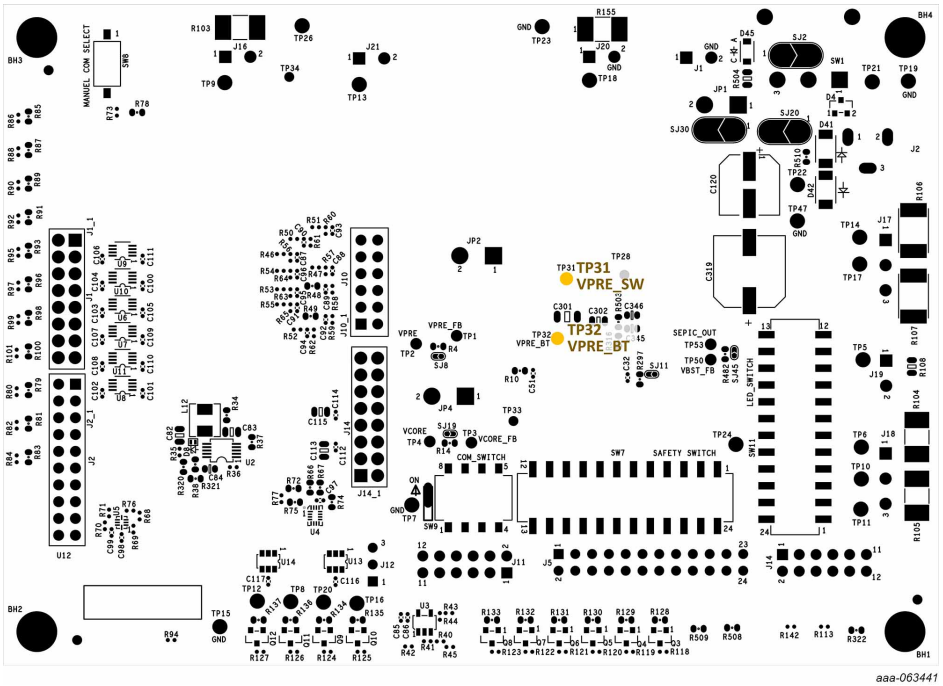


Figure 27. Test points locations

The test points are color coded:

- Orange: Test loop access to device signals, such as safety outputs, analog pins, and regulator switch nodes.
- Red: Test loop access for power supplies.
- Black: Test loop access to GND.
- Dark orange: Test pad access to regulator bootstrap capacitor.

The test points connections as shown in Figure 28.

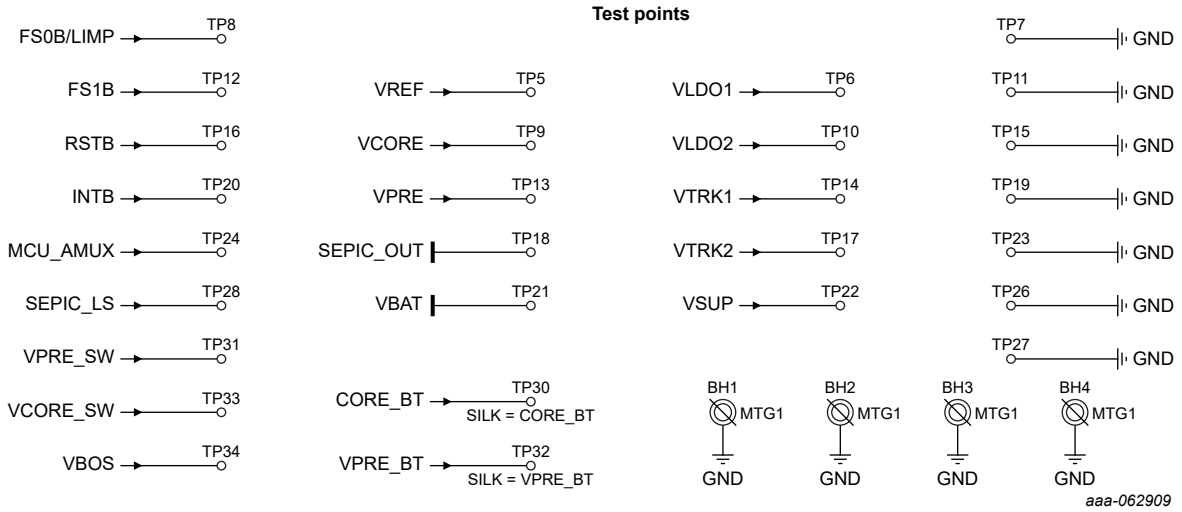


Figure 28. Test points connections

Table 35. Test points

Test point name	Signal name	Description
TP5	VREF	VREF regulator output (VREF pin) access
TP6	VLDO1	LDO1 regulator output (LDO1OUT pin) access
TP7	GND	Ground
TP8	FS0B/LIMP	FS0B/LIMP pin access
TP9	VCORE	VCORE regulator output access
TP10	VLDO2	LDO2 regulator output (LDO2OUT pin) access
TP11	GND	Ground
TP12	FS1B	FS0B pin access
TP13	VPRE	VPRE regulator output (VPRE_FB pin) access
TP14	VTRK1	TRK1 regulator output (TRK1 pin) access
TP15	GND	Ground
TP16	RSTB	RSTB pin access
TP17	VTRK2	TRK2 regulator output (TRK2 pin) access
TP18	FLYBACK_OUT	Flyback regulator main (secondary 1) output access
TP19	GND	Ground
TP20	INTB	INTB pin access
TP21	VBAT	VBAT access

Table 35. Test points*...continued*

Test point name	Signal name	Description
TP22	VSUP	VSUP pin access
TP23	GND	Ground
TP24	MCU_AMUX	MCU_AMUX signal access
TP26	GND	Ground
TP27	GND	Ground
TP28	FLYBACK_LS	Flyback regulator low-side MOSFET drain access
TP30	CORE_BT	VCORE regulator bootstrap pin (CORE_BT pin) access
TP31	VPRE_SW	VPRE regulator switching node (VPRE_SW pin) access
TP32	VPRE_BT	VPRE regulator bootstrap pin (VPRE_BT pin) access
TP33	CORE_SW	VCORE regulator switching node (CORE_SW1/2 pin) access
TP34	VBOS	VBOS pin access
TP54	FLYBACK_OUT_2	Flyback regulator secondary (secondary 2) output access
TP55	VAUX	Flyback regulator auxiliary output access

6 Installing and configuring software tools

The software tools are available on http://www.nxp.com/NXP GUI for Automotive PMIC Families or from our "Secure Files" portal at https://www.nxp.com/mynxp/secure-files if device is not in production.

The NXP GUI for Automotive PMICs Families is delivered with the EVB firmware. The EVB firmware allows the GUI to connect the device in the EVB, providing access to all device features.

The EVBs are always delivered with the BOOTLOADER and firmware flashed, and if no firmware update is required, these steps can be ignored.

If the firmware is malfunctioning or must be updated, follow the instructions in the next section.

6.1 Flashing or updating the Freedom board firmware on Windows 7/10/11

The Freedom board firmware is composed of two items: the BOOTLOADER (*.SDA) and the firmware file (*.bin).

If the FRDM-KL25Z board is already operational, that is, the GUI is capable to communicate with the EVB, the BOOTLOADER is installed, so only firmware updated might be required.

6.1.1 BOOTLOADER installation steps

BOOTLOADER installation steps are:

1. Disable the Storage Service and Windows Search: Run Services, double-click, and stop them as shown in Figure 29.

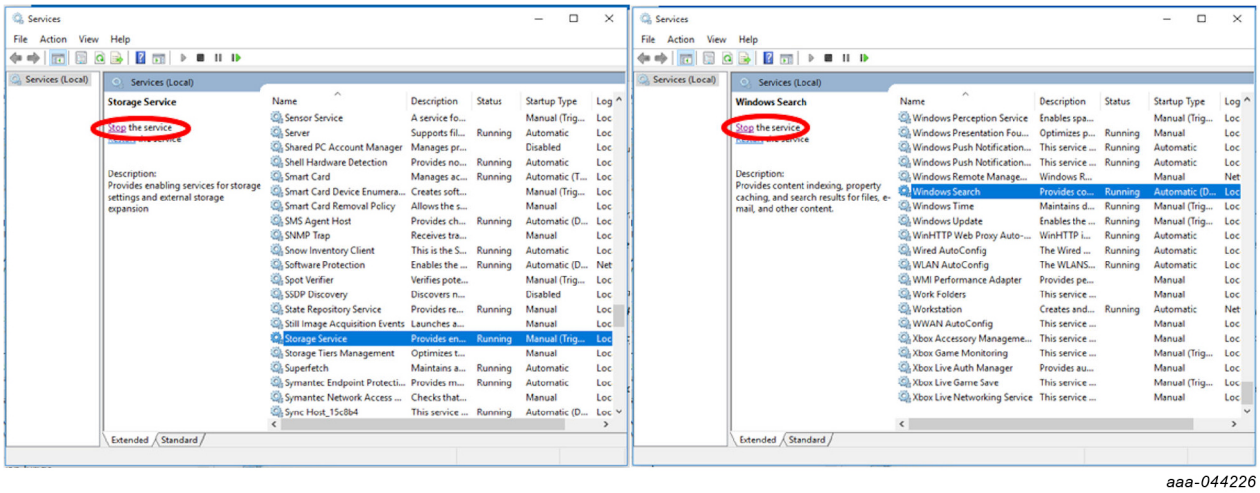


Figure 29. Services configuration

2. Press the RST button and connect the USB cable to the SDA port on the Freedom Board.
   - A new BOOTLOADER device appears on the left pane of the File Explorer.
3. Drag and drop the specific file "MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA" to the BOOTLOADER drive.
   Ensure that there is enough time for the firmware to be saved in the BOOTLOADER.
4. Disconnect the USB cable from the SDA port.

6.1.2 Firmware installation/update steps

Firmware installation/update steps are:

1. WITHOUT pressing the RST button, connect the USB cable to the SDA port on the Freedom Board.
   - The FRDM-KL25Z device appears on the left pane of the File Explorer as pictured in Figure 30.

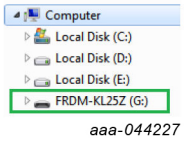


Figure 30. FRDM-KL25Z in left pane

2. Locate the **<device>** specific file with the required **<revision>** from the package, such as "nxp-gui-fw-frdm-kl25z-usb_hid-<device>_<revision>.bin".
3. Drag and drop this file into the FRDM-KL25Z device.
   - Ensure that there is enough time for the firmware to be saved.
   - The Freedom board firmware is successfully loaded.
4. Disconnect the USB-cable.

6.2 Installing the NXP GUI software package

To install the FS2700-B0 NXP GUI, download or obtain the NXP GUI package, unzip an open 1-NXP_GUI_Setup folder:

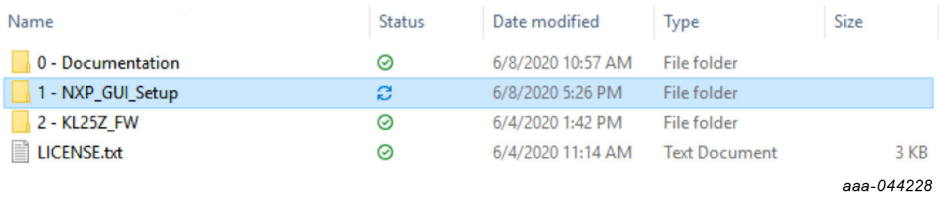


Figure 31. NXP_GUI_Setup folder

Then double-click on the NXP_GUI_version-Setup.exe and follow the instructions.

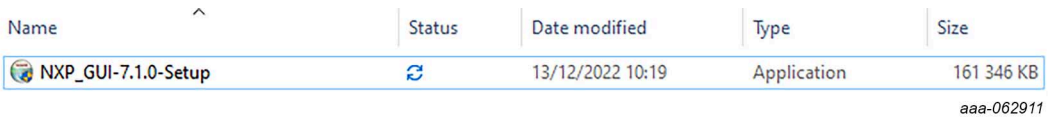


Figure 32. NXP_GUI_version_Setup.exe

To install the application on a Windows PC, proceed with the following pop-up windows:

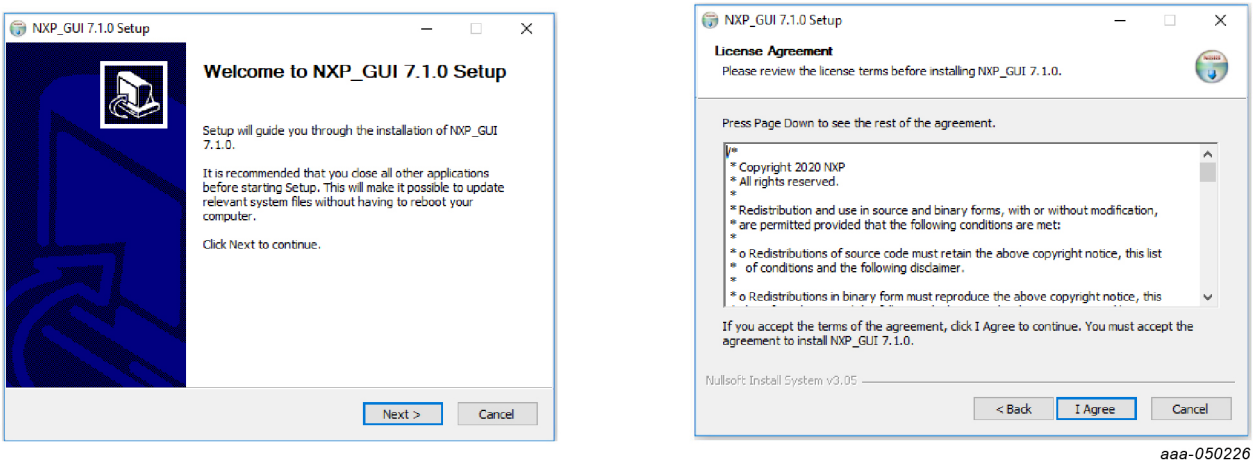


Figure 33. NXP GUI setup

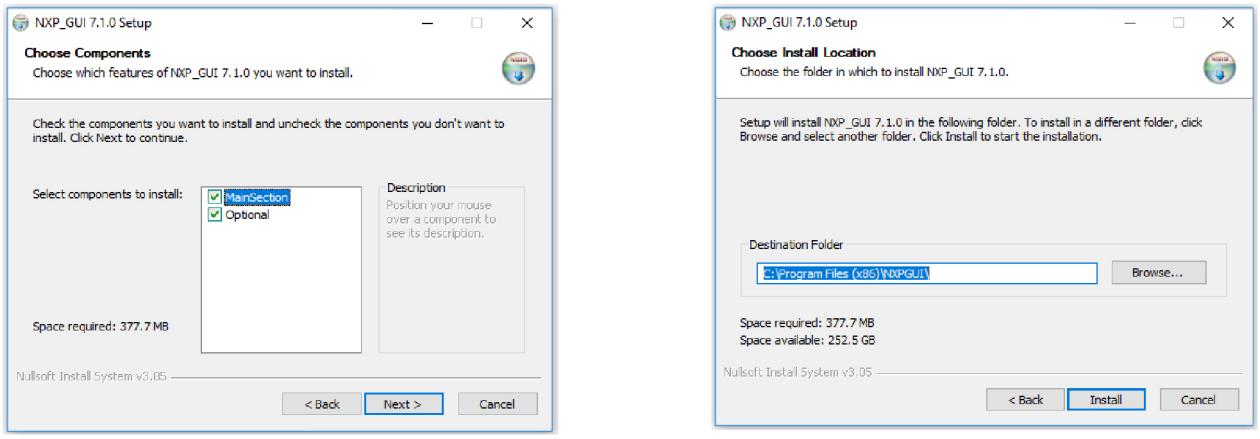


Figure 34. NXP GUI setup configuration

Select the following options before completing the installation of the setup:

- Run NXP_GUI
- Show Readme

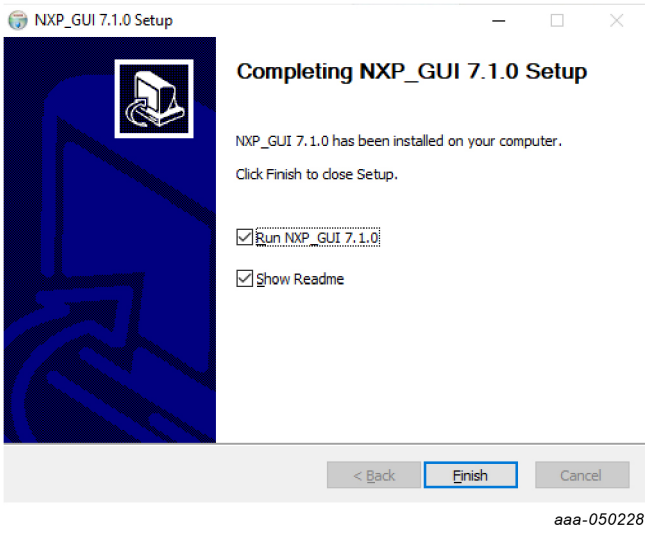


Figure 35. NXP GUI setup completion

Select **Finish** to complete the installation.

When the installation is finished, find the application by searching for *NXPGUI* in the Windows search bar. Click to launch.

7 Using the FS2700-B0 NXP GUI for Automotive PMIC Families

To follow the steps in this section, ensure that the board is connected using the appropriate hardware configuration.

Always use the latest version of the NXP GUI for Automotive PMIC Families.

7.1 Starting the FS2700-B0 NXP GUI for Automotive PMIC Families

When the kit is ready and the NXP GUI for Automotive PMIC Families is installed, click to launch the kit from the Windows search bar. When the pop-up window appears, choose **FS2700-B0** and click **OK**.

To avoid the kit selection window on every launch, check the "Use this configuration and do not ask again" box.

To show the kit selection window on the next launch, check the first option on the "File" menu.

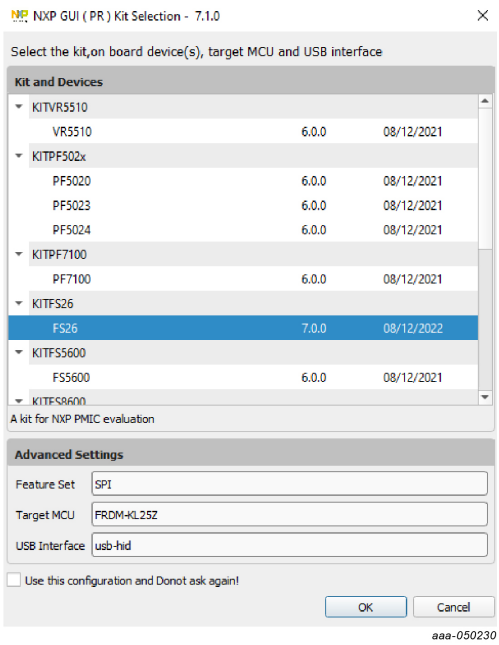


Figure 36. KIT selection window

The GUI is loaded, and its interface such as in Figure 37 is shown.

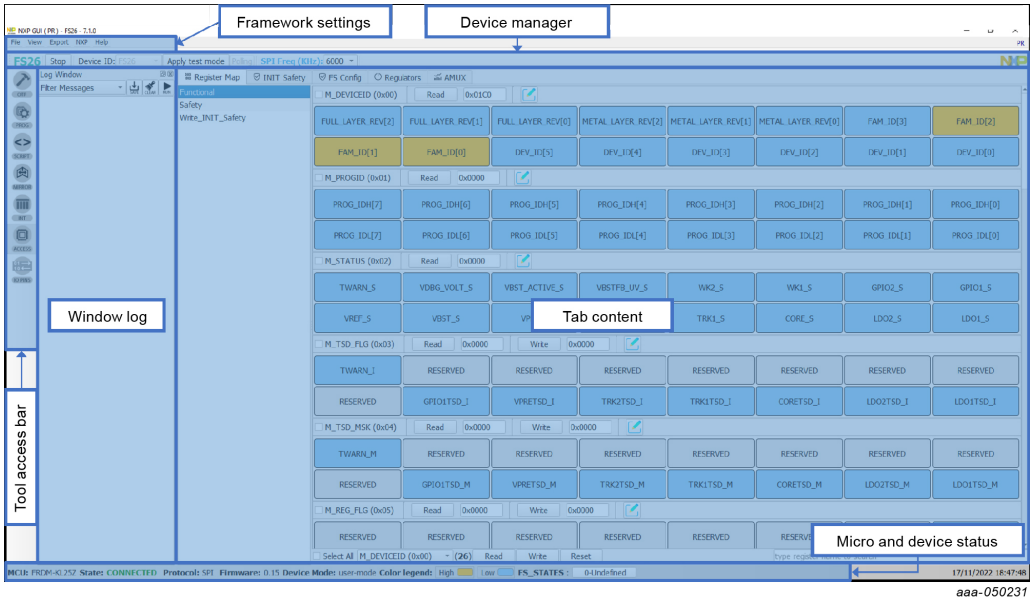


Figure 37. NXP GUI framework

The NXP GUI for Automotive PMIC Families interface is now in use. It can be divided in several parts:

- **Settings:** Import or export files; configure framework
- **Device Manager:** Start communication with the device; enter or exit test mode; SPI communication settings
- **Tool Access Bar:** Quick access to the evaluation tools and features
- **Window Log:** Microcontroller and device communication events
- **Tab Content:** Content of each tool or tab – there can be more tabs, boxes, or windows
- **Micro and Device Status:** Displays whether USB or device is connected or disconnected; displays Firmware and GUI version; displays the current state of the FS state machine – click **Display** button to refresh

Note: *The tool access bar shows the GUI tools in the sequence that they must be used. The first step is to verify device POWER dissipation and then configure the OTP. When the power is verified and OTP is done, the device can be programmed or emulated with a SCRIPT. MIRROR registers can be read/modified to a configuration validation. To verify states and configure safety reactions, the Access tab allows manipulation of the registers.*

7.2 Framework settings

The NXP GUI for Automotive PMIC Families main menu has five elements: File, View, Export, NXP, and Help.

7.2.1 File

Load or save a configuration or exit the application. Load and save are only enabled when the OTP tool tab is active.

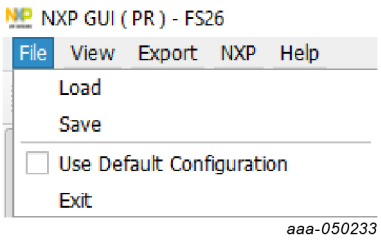


Figure 38. File options

- **Load**: Loads an existing configuration file previously exported from the OTP tool, to continue to modify it on the OTP tool. This file has a .cfg extension. It is identified as: <device>_ProgIDASILlevel_CONFIG.cfg. Example: <device>_A0D_CONFIG.cfg.
- **Save**: Saves the current configuration of the OTP tool as a .cfg file.
- **Use default configuration**: Check to show Kit selection window.
- **Exit**: Exits NXP GUI application.

7.2.2 View

This main menu has options related to the GUI display.

- **Display**: It consists of the Connection Tool Bar (enabled by default) option.
  To show or hide, go to **View** → **Display** and then select **Connection Tool Bar**.

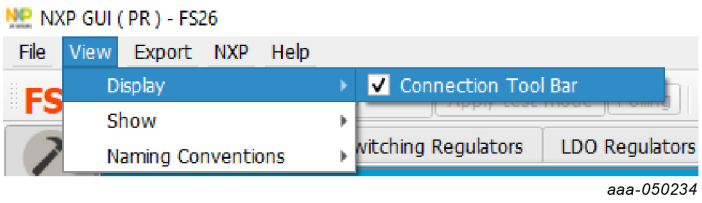


Figure 39. Display options

- **Show**: This option can be used to access various sections of the GUI.

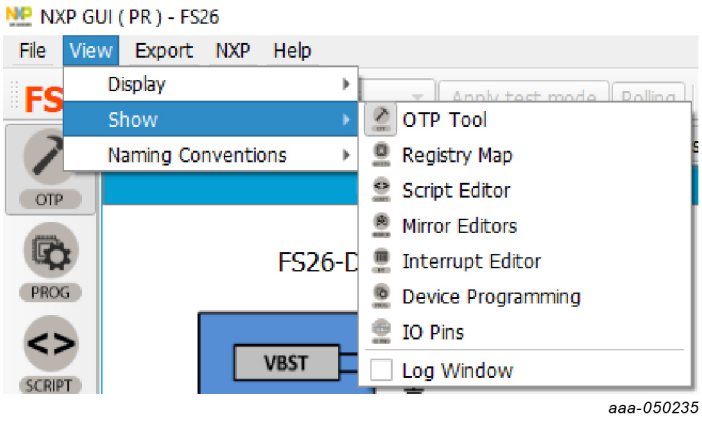


Figure 40. Show options

- **Naming Conventions**: Select Friendly or Register name display for the OTP tool. This option is enabled only when the OTP tool is active.

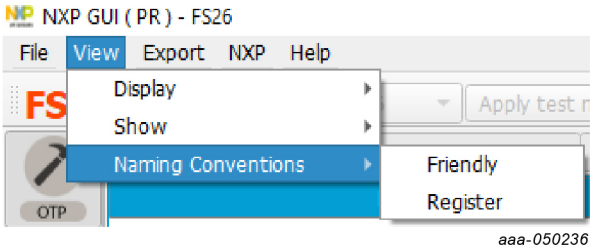


Figure 41. Naming conventions options

  - **Friendly**: Go to View → Naming Conventions → Friendly. This mode helps to view the register names as user-friendly names throughout the OTP tool.

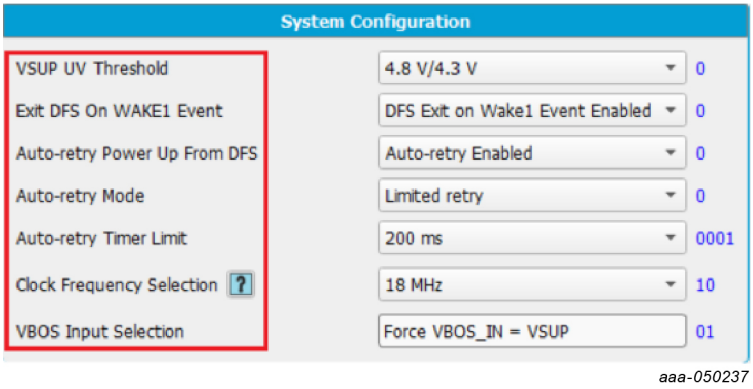


Figure 42. Friendly mode

  - **Register**: Go to View → Naming Conventions → Register. This mode helps to view the register names as the registers' technical names throughout the OTP Tool.
    Example: VSUP UV threshold → VSUP_UVTH_OTP

7.2.3 Export

This option allows the user to export the current OTP from the OTP tool into different script formats.

- **OTP**: Exports OTP configuration into an OTP script file.
- **TBB**: Exports OTP configuration into a TBB script file for **programming**and **emulation**.
- **I-HEX**: Exports to Intel Hex script file.
- **S-HEX**: Exports to Simple Hex script file.

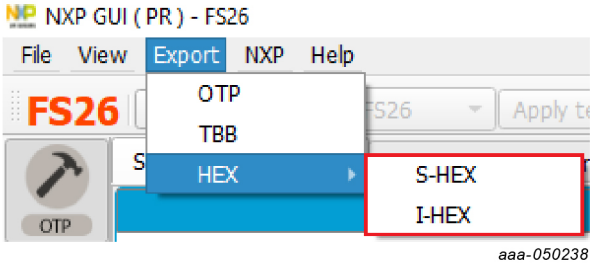


Figure 43. KIT selection window

This option is enabled only in the OTP Tool, and remains disabled in other sections of the GUI.

7.3 OTP tab

The OTP tool allows the configuration of OTP registers and generates scripts for OTP emulation or OTP programming. These scripts program parameters that the main state machine and the fail-safe state machine control.

The OTP tool includes four tabs:

- System Configuration
- Switching and LDO Regulators
- Voltage Monitoring
- System Safety Configuration
- OTP ID

These five tabs are used to define the entire FS27 OTP configuration.

When the OTP configuration is defined, TBB/OTP scripts can be generated using the *Export* menu. Generate a TBB file for emulation and an OTP file for OTP programming.

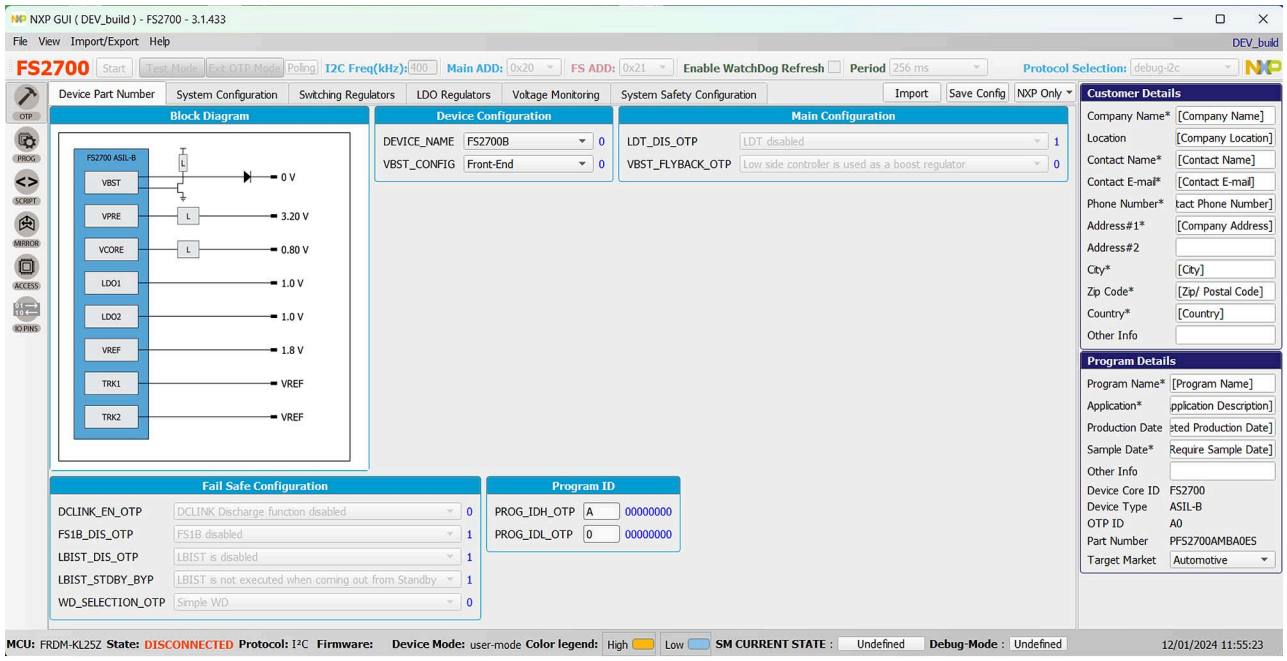
It is possible to save a configuration to use or to modify it later. To export the OTP configuration, click **Save Config**. To import a configuration initially saved from the OTP tool or the Mirrors tab, click the **Import** button.

7.3.1 Device Part Number tab

The system configuration tab has several sections:

- **Block Diagram**: This graphic shows the output voltage set for each supply rail (VBST, VPRE, VCORE, ...).
- **Device Configuration**: Used to set device versioning (DEVICE_NAME) and VBST regulator configuration.
- **Main Configuration**: Shows the main configuration based on device versioning.
- **Fail-safe Configuration**: Shows the fail-safe configuration based on device versioning.
- **Program ID**: Shows the device ID chosen.

Figure 44 shows an OTP configuration example.



aaa-062912

Figure 44. OTP Device Part Number tab

7.3.2 System Configuration tab

The system configuration tab has several sections:

- **System Configuration**: Used to configure the VSUP undervoltage threshold, VBOS transitions, clock frequency spread spectrum, and others.
- **Communication**: Used to device address and communication protocol type.
- **GPIO1 Configuration**: Used to configure the GPIO1.
- **GPIO2 Configuration**: Used to configure the GPIO2.
- **WAKE Configuration**: Used to configure WAKE1 and WAKE2.
- **Regulator Power Sequencing**: Used to define the power sequencing of the device.
- **Power Sequencing Configuration**: Used to define the power sequencing enhancement, such as slot transition conditions.
- **Sequence Diagram**: This diagram reflects the power-up sequence depending on the OTP configuration – the power-up sequence timing may not be 100 % accurate.

Figure 45 shows an OTP configuration example.

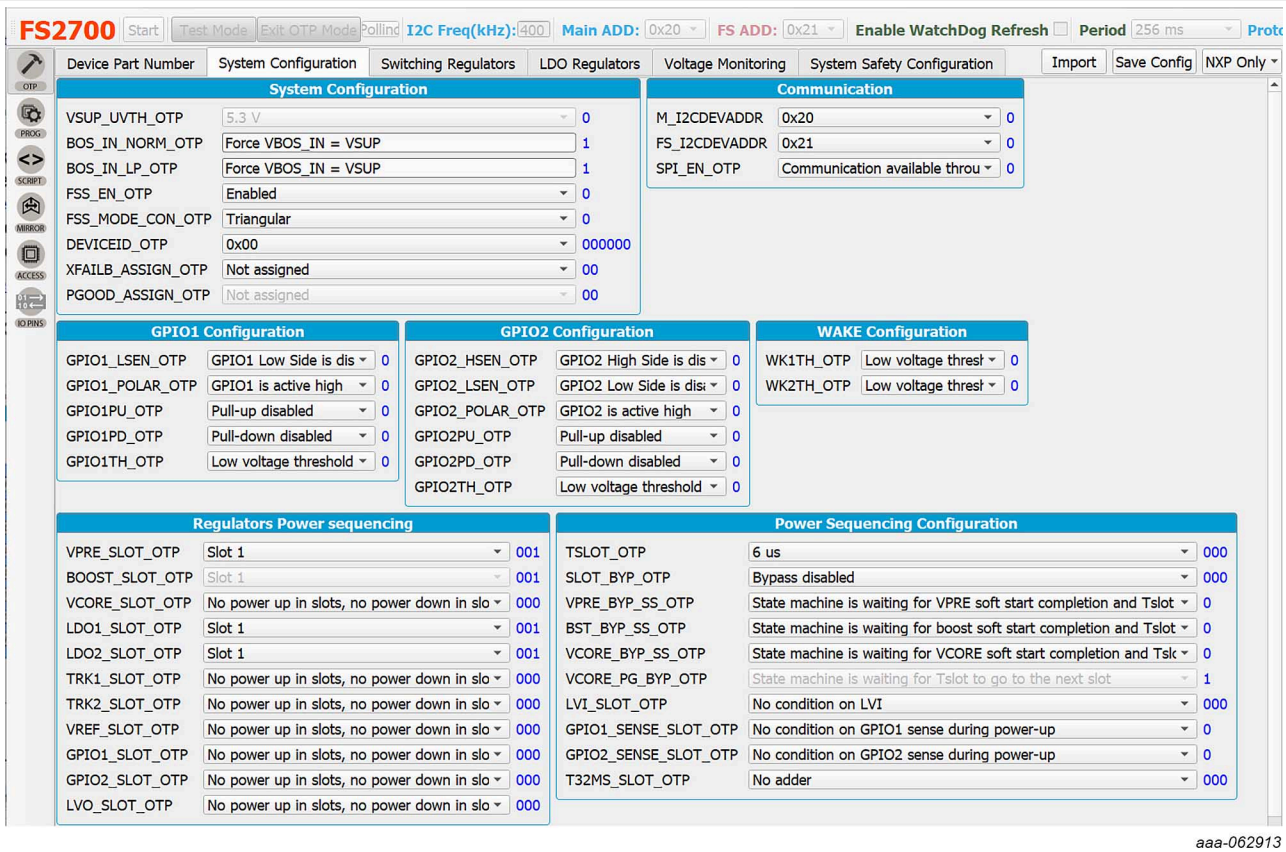


Figure 45. OTP System Configuration Tab

7.3.3 Switching Regulators tab

The Switching Regulators tab shown in Figure 46 has three sections:

- **VBST Configuration**: VBST minimum ON time is already set. Other parameters can be chosen.
- **VPRE Configuration**: Minimum ON and OFF time in PFM mode and the slope compensation are set and cannot be modified. Also, VPRE transition voltage when going to Standby mode (VPRE_BOS_OTP) is linked to VPRE output voltage in Standby mode (VPRE_LP_OTP). Other parameters can be chosen.
- **VCORE Configuration**: VCORE control mode is already set. Other parameters can be chosen.

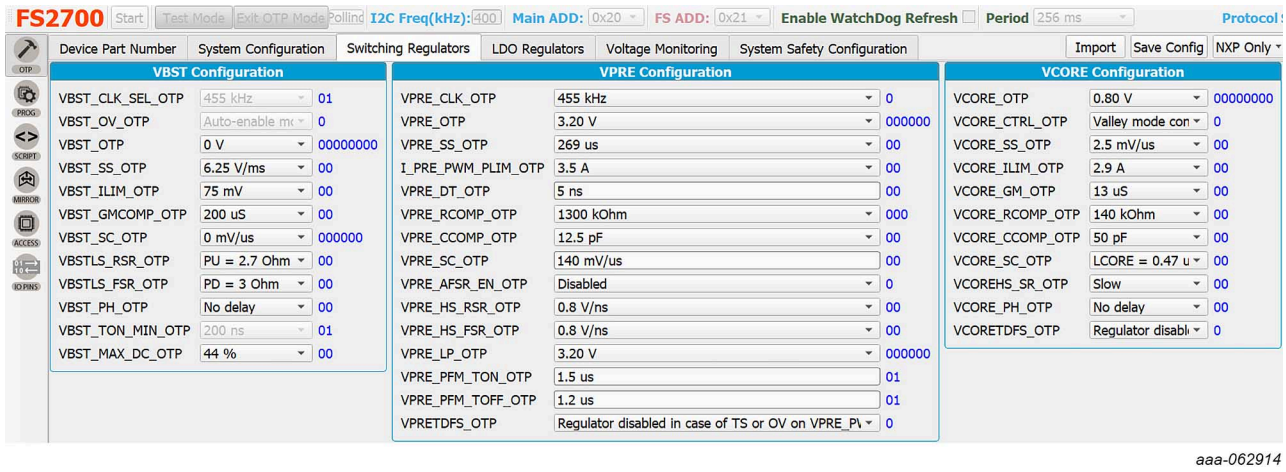


Figure 46. OTP SMPS regulators Configuration tab

Regulators VPRE and VCORE can be configured individually to trigger a transition to deep fail-safe (<regulator>TDFS_OTP bit field) when an OV is detected.

7.3.4 LDO Regulators tab

The LDO Regulators tab shown in Figure 47 has five sections:

- **LDO1/LDO2 Configuration**: Linear dropout regulators configuration.
- **VREF Configuration**: High-precision voltage linear dropout regulator configuration.
- **Internal LDO REF Configuration**: High-precision voltage linear dropout internal regulator configuration.
- **TRK1/TRK2 Configuration**: Voltage tracking regulators configuration. Can track LDO2, VREF, or the internal LDO REF, in any combination.

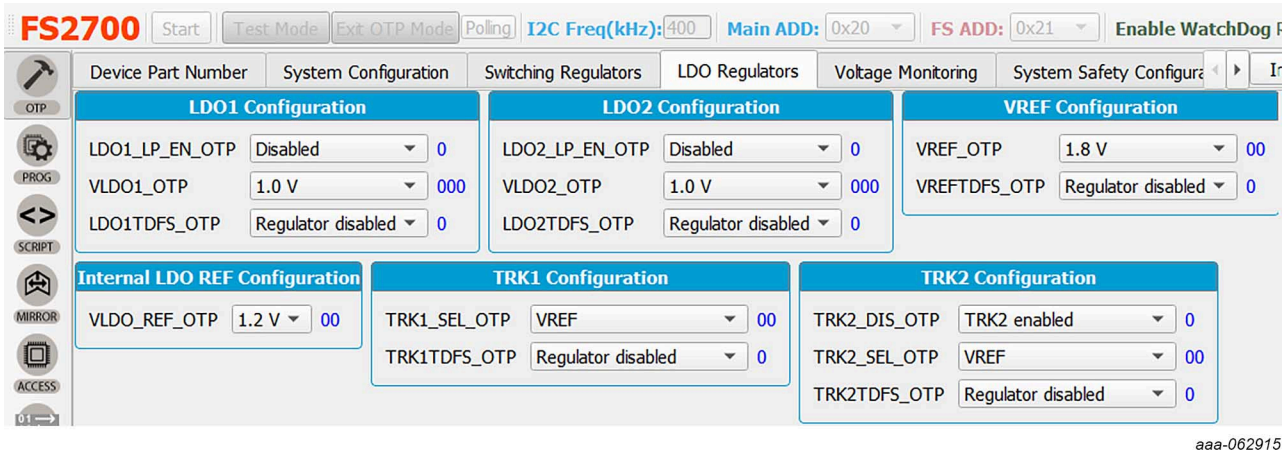


Figure 47. OTP LDO Regulators Configuration tab

Each regulator can be configured individually to trigger a transition to deep fail-safe (<regulator>TDFS_OTP bit) when an OV is detected.

7.3.5 Voltage Monitoring tab

The Voltage Monitoring tab shown in Figure 48 has the following sections:

- **VMONPRE, VMONCORE, VMONTRK1, VMONTRK2, VMONEXT Configuration**: Defines OV/UV thresholds and deglitch timings for VPRE, VCORE, TRK1 and TRK2 regulators. The monitoring voltages are bound to the respective regulator voltage set in the Switching/LDO Regulators tab (except for VMONEXT). VMONEXT monitoring target can be set to 5.0 V when VBST is in the back-end at 5.0 V.
- **VMONLDO1, VMONLDO2, VMONREF Configuration**: Defines OV/UV thresholds, normal or degraded UV (except for VREF), and deglitch timings for LDO1, LDO2, and VREF regulators.
- **Pin Lift Configuration**: Used to disable pin lift detection on VREF, LDO1, and LDO2 regulators.

Figure 48. OTP Voltage Monitoring Configuration tab

7.3.6 System Safety Configuration tab

The System Safety Configuration tab shown in Figure 49 has two sections:

- **Deep fail-safe Configuration**: Used to disable transition to deep fail-safe (development only), to go to deep fail-safe when fault error counter in incremented, auto retry strategy.
- **ABIST1 Configuration**: Used to enable ABIST1 execution for each available monitoring.
- **System Safety Configuration**: Used to set the behavior of FS1B, Watchdog, LBIST, RSTB, and others.

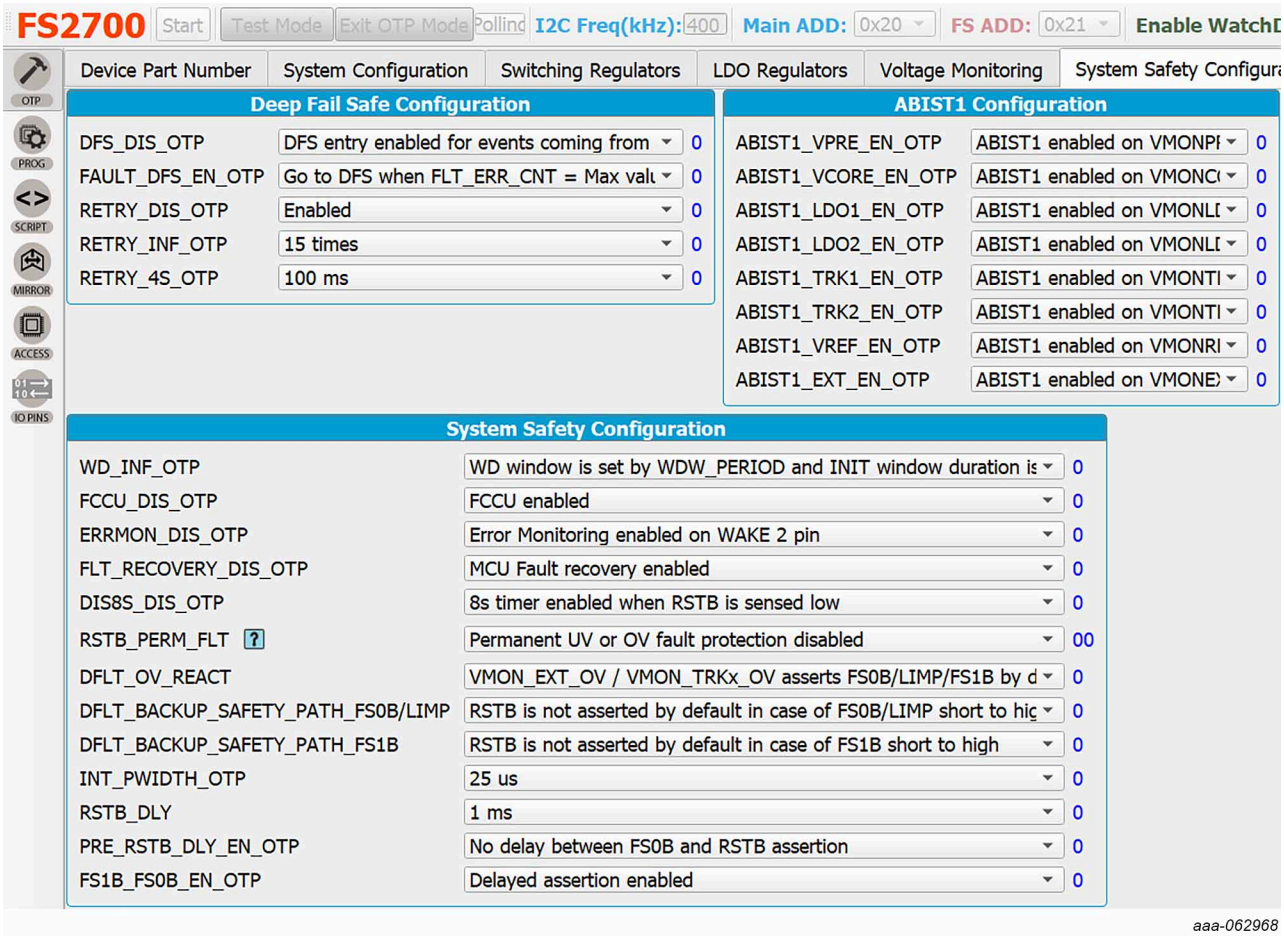


Figure 49. OTP System Safety Configuration tab

7.4 Device programming

The Device Programming tab shown in Figure 50 allows the user to burn the OTP using a script initially generated by the OTP tool. To enable this window, the device must be in test mode.

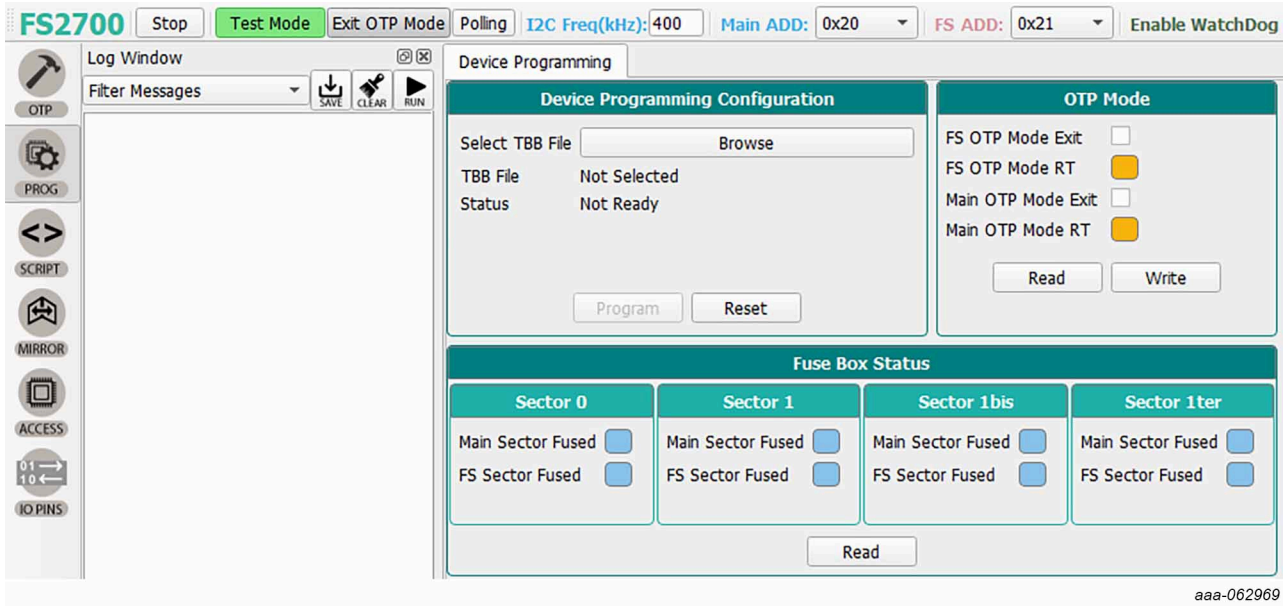


Figure 50. Device programming tab

To program an OTP configuration, the V_{OTP} voltage must be applied to the DEBUG pin. To do so, the user must turn on SW5 to apply 8.0 V to the device DEBUG pin.

Click **Browse** to select an OTP script file, then click the **Program** button to run the script. If the DEBUG pin voltage is not set to V_{OTP}, a pop up appears to ask the user to turn on SW5.

If the required conditions are met (sectors are available), the programming process starts. Otherwise, the execution is canceled. To verify that the sectors are available, click **Read** from the Fuse Box Status window.

Blue or '0': Available

Yellow or '1': Not available

OTP is programmed into one sector of Main and fail-safe, the first one available in the following sequence: "Sector 1", then “Sector 1bis”, then "Sector 1ter".

When a new sector is programmed, the previous ones cannot be used/accessed anymore.

"Sector 0" is reserved for NXP only.

When programming is complete, a pop up appears to ask the user to turn off SW5 or click "Exit OTP Mode".

If the device was programmed correctly, the power-up sequence starts. The fuse box status can be read to check whether sectors are burned. In some conditions, a power-up could be required.

7.5 Script tab

The registers and OTP emulation can be configured with the Script editor shown in Figure 51. The Script editor is useful for trying various OTP configurations in OTP Emulation mode.

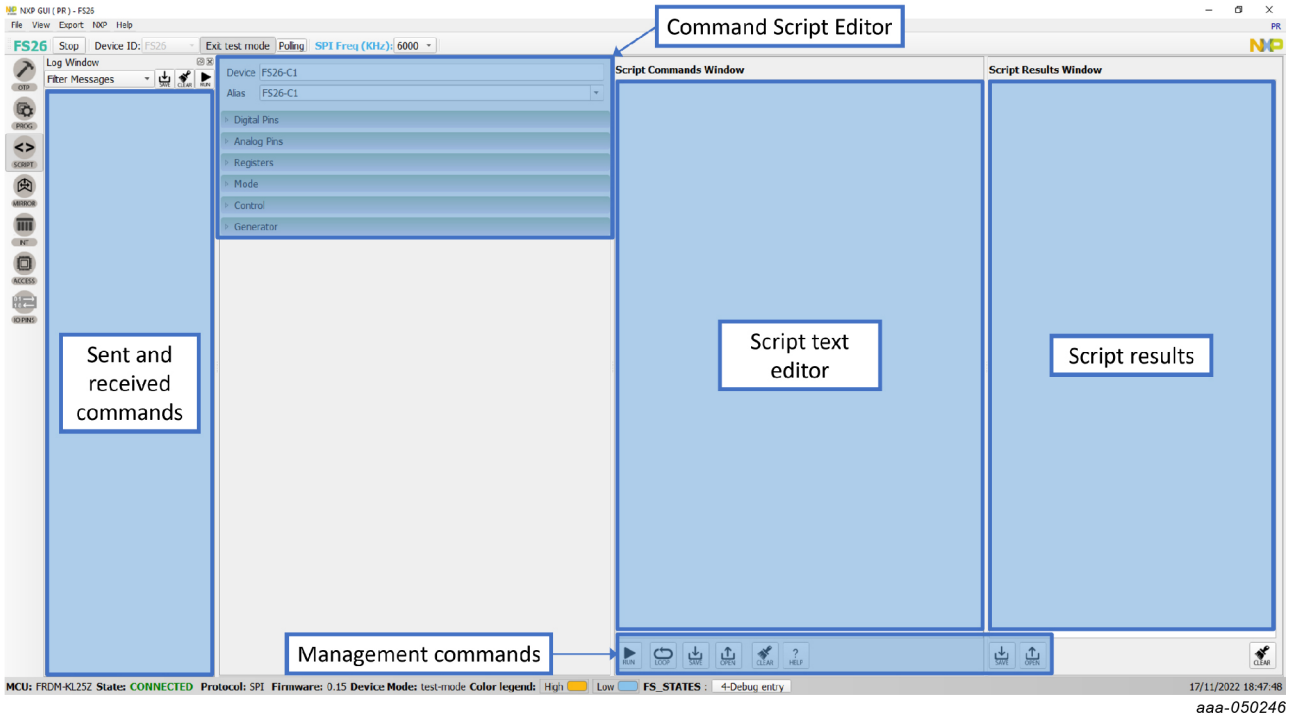


Figure 51. Script editor

The main subareas of this panel are:

- **Command Script Editor**: Builds commands to be sent to the device.
- **Script Text Editor**: Sends a sequence of register configurations from a text file or from a command edited directly in this area.
- **Script Results**: Displays result status of each command sent to the device.
- **Sent and Received Commands**: Displays a summary of commands sent and received from the device.
- **Management Commands**: These commands are used for scripts.

7.5.1 Command script editor

Using the script editor, the user can execute any command either directly or from a file. It is also possible to save and modify a script. Using the brush symbol, it is possible to clean windows if necessary.

All commands must follow a specific syntax. The Help menu describes the commands available in the script editor and the syntax to be used.

Figure 52 shows an example of building a command from the panel.

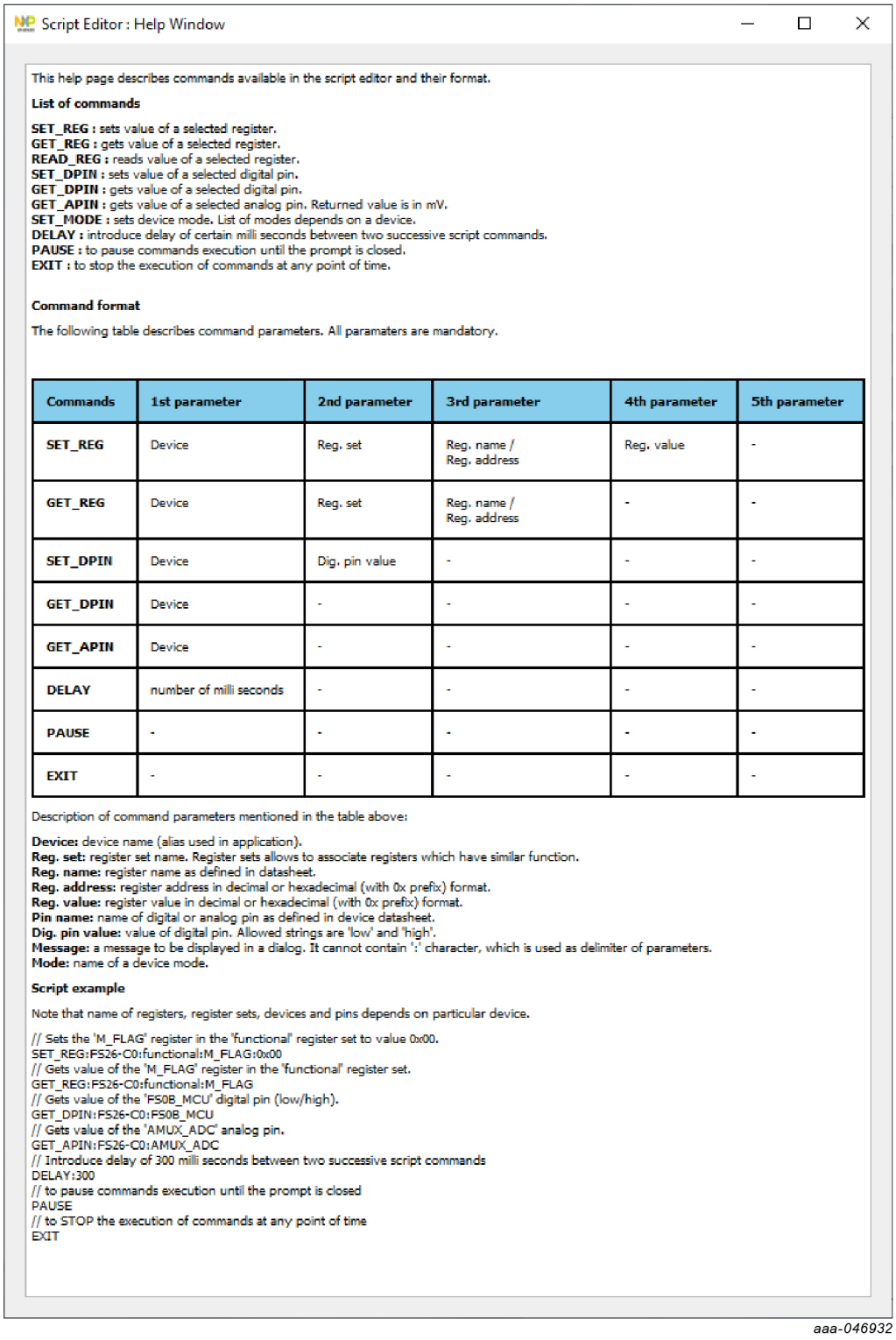


Figure 52. Script Editor: Help window

7.5.2 Management commands

Some commands are used for formatting the scripts. Figure 53 shows the description of each button.

Figure 53. Script editor commands

- **Run**: Runs the script once.
  Note: While running a script, click "Run" again to stop script execution.
- **Loop**: Runs the script continuously in a loop.
- **Save**: Save the script that is present in the script command window in a text file.
- **Open**: Open a saved script from the desired location.
- **Clear**: Clears the script command window.
- **Script Editor Help Window**: Describes the commands available in the script editor and their formats.

7.5.3 Script editor

The script editor allows the user to create or send existing sequences to the device. The user can read/write registers, to I/Os, or analog pins. The user can emulate an OTP configuration as well with this tab.

This tab can be accessed from Toolbar → SCRIPT or View → Show → Script Editor.

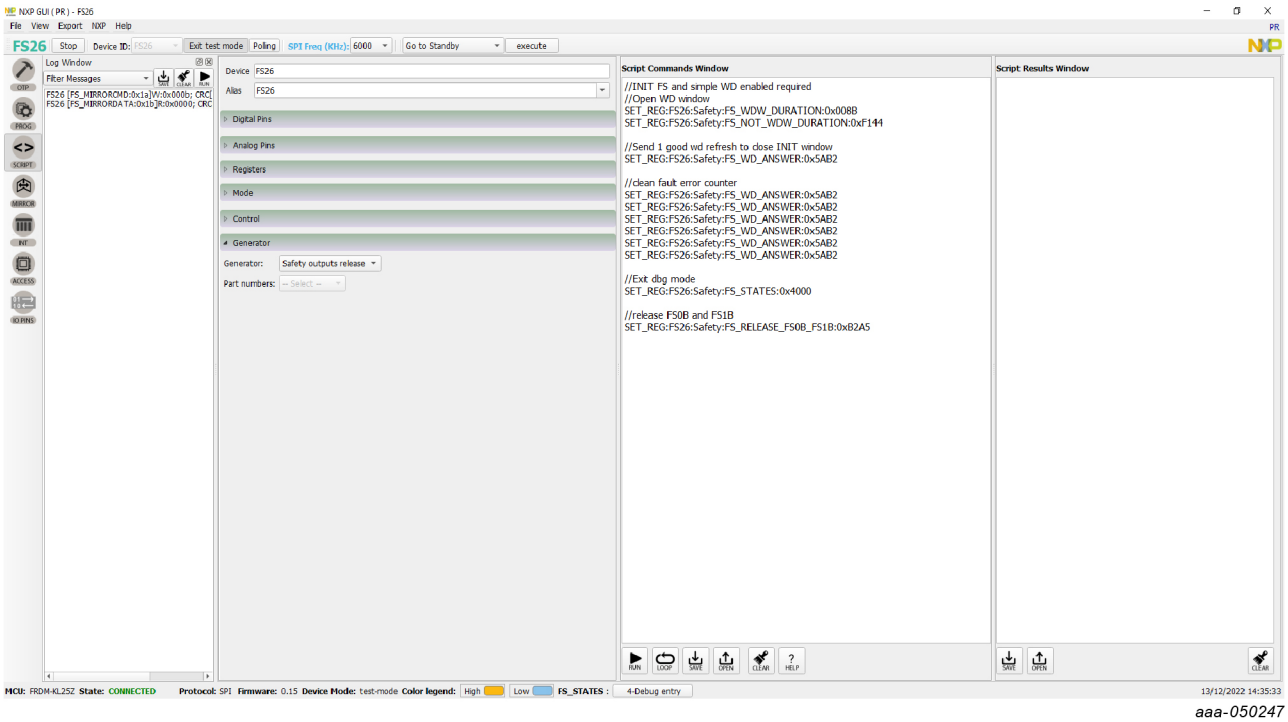


Figure 54. Script Editor

The script can be written by selecting and configuring the script commands available in the script editor or by loading a previously exported .txt file.

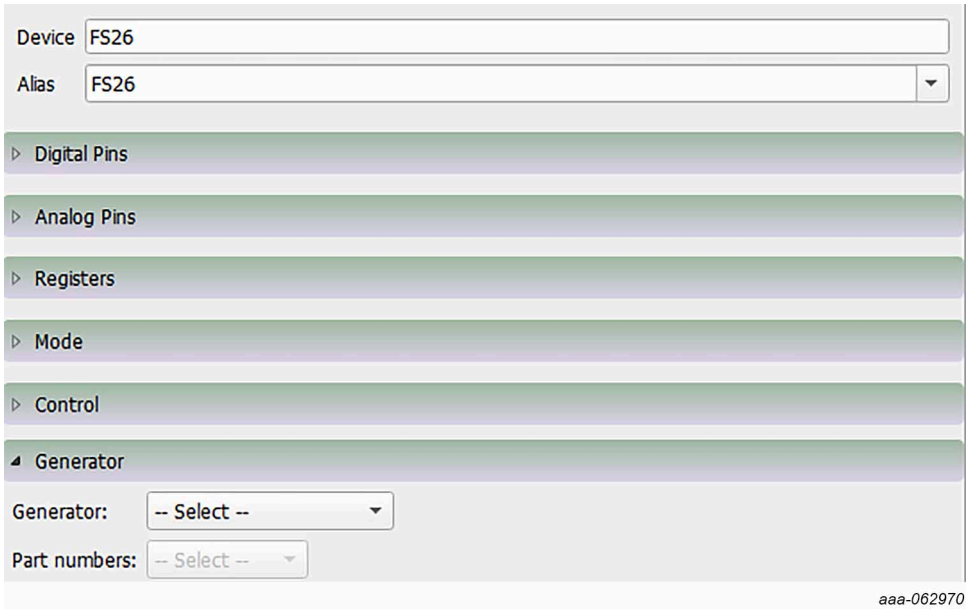


Figure 55. Use a script editor to access more commands

Click one type of command to access more options, until the command to build the sequence is found.

- Digital pins: Select the pin name, then the pin state (HIGH or LOW). The command is automatically added to the script.

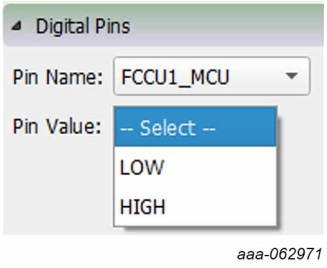


Figure 56. Digital Pins

- Analog pins: Select the pin name and the command is added to the script editor automatically.

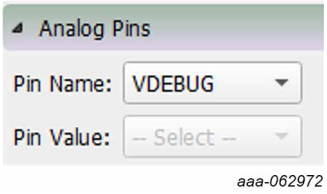


Figure 57. Analog Pins

- Registers: Select the Operation (read/write).
  - Read: Select the register group, then the register name. The register is added to the script editor automatically.

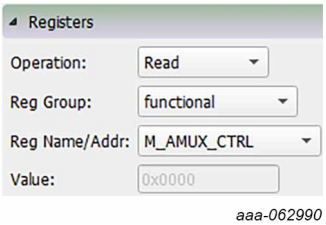


Figure 58. Registers: Read

  - Write: Select the register group, then the register name, write the value, then hit "enter" on the keyboard to add the command to the editor.

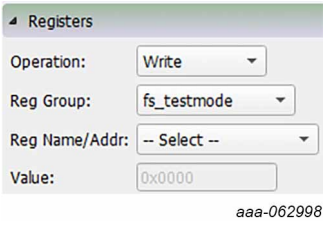


Figure 59. Registers: Write

- Mode: Write a command to exit or enter different device modes.
  - **Test mode**: send main and fail-safe test mode entry keys.
  - **User mode**: exit test mode if the device is in test mode.
  - **Exit OTP mode**: exit OTP mode if the device is in OTP mode.
  - **Exit debug mode**: exit debug mode if the device is in debug mode.
  - **Update status**: update GUI status.

- Generator: Select an existing script to add to the script editor. Some options may require to be in a specific mode or state.

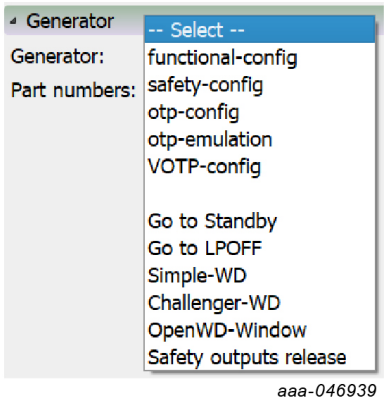


Figure 60. Generator

- Script operations:
  The script operations can be found at the bottom of the script editor window and are responsible for:
  - Execution of script
  - Script management: Create, Open, Save, Run
  - Logging feature: Load, Save, Clear

- Script flow controls:
  - **RUN**: Start/stop script execution
  - **LOOP**: When enabled, the script runs continuously in a loop when RUN is hit and until RUN is hit again
  - **SAVE**: Saves the script that is present in the script command window in a text file
  - **OPEN**: Opens a saved script from the desired location
  - **CLEAR**: Clears the script command window
  - **Script Editor Help Window**: This section describes the commands available in Script Editor, and their formats. This option can be accessed from Menu → SCRIPT → Help or View → Show → Script Editor → Help.

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Figure 61. Script editor controls

7.6 Mirrors tab

Test mode must be applied to enable the Mirrors tab.

This tab allow to modify the current device configuration loaded from the OTP registers.

This tab is divided into main and fail-safe mirrors registers, shown in Figure 62 and Figure 63, respectively.

The **Read All** and **Write All** buttons can be used to read/write the entire set of mirrors registers.

The Mirrors configuration can be exported and imported in the OTP tool as an OTP configuration to generate TBB/OTP scripts files.

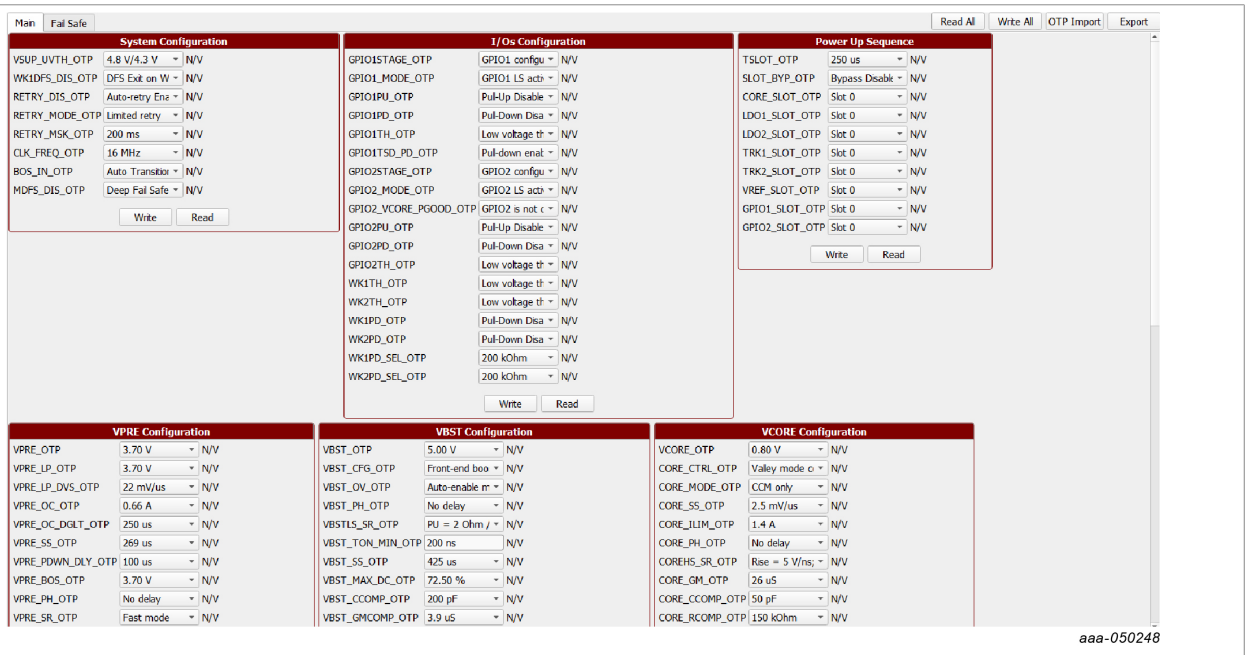

Figure 62. Main mirrors tab

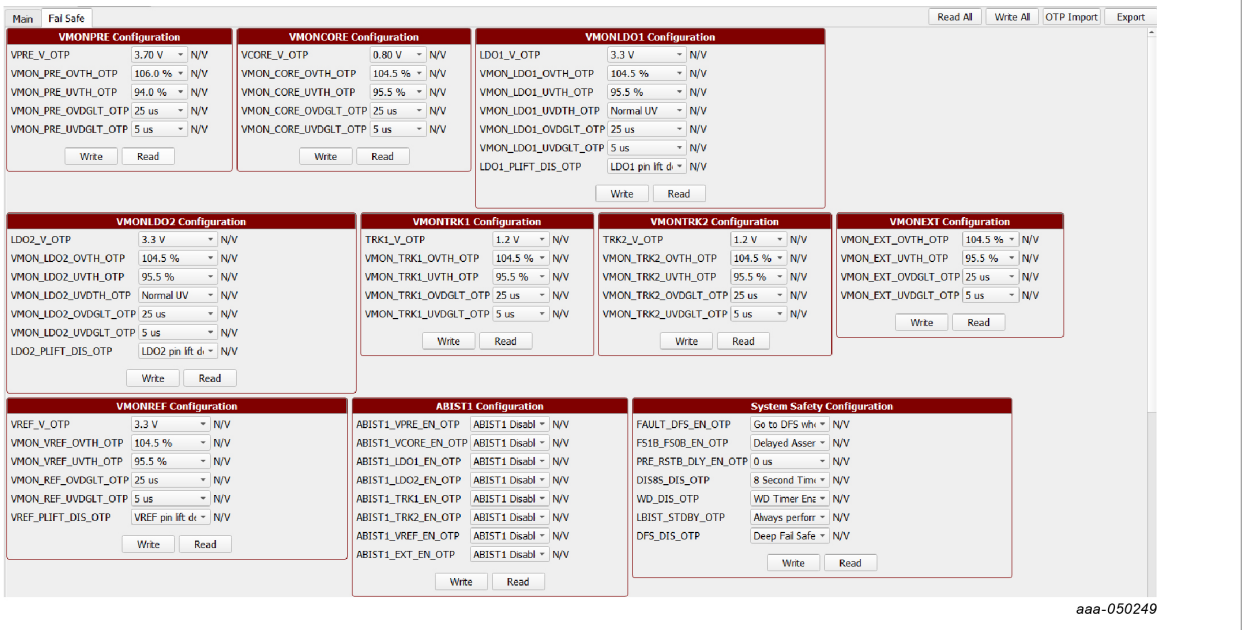

Figure 63. Fail-safe mirrors tab

7.6.1 Read/write operation

To read a bit group, click **Read** from a box. Read values are displayed to the right of each register.

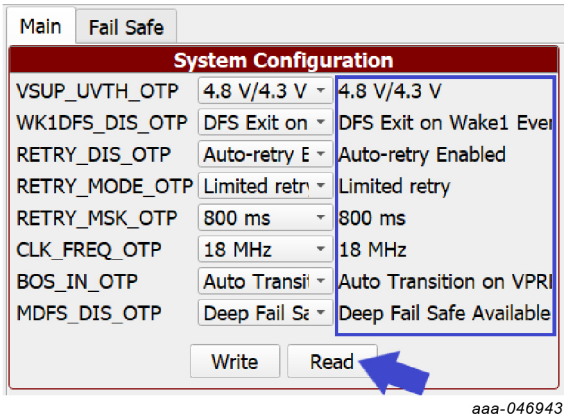

Figure 64. Read bit group

To write to a bit group, modify the controls of each register, then click **Write**.

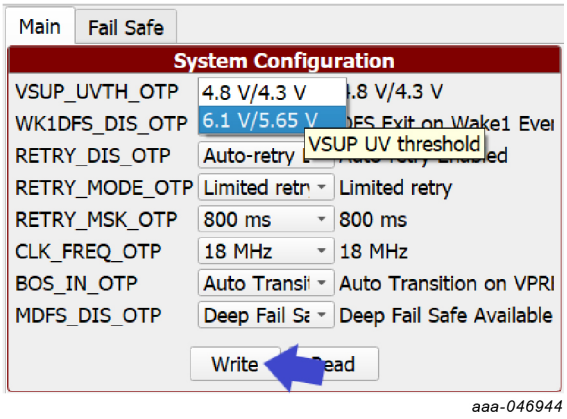

Figure 65. Write bit group

7.6.2 Read/write all and write all operation

Read All reads the bits of each block from all mirror registers.

Read values also appear at the right of each register in the window log.

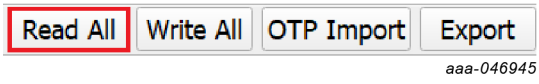

Figure 66. Read all

To write all OTP bit groups configuration, click **Write All**.

7.6.3 Mirror registers export option

This operation generates a configuration file, which is saved as a text file in the local device. The configuration file can be imported into this tab later. Figure 67 shows the generated .txt configuration file.

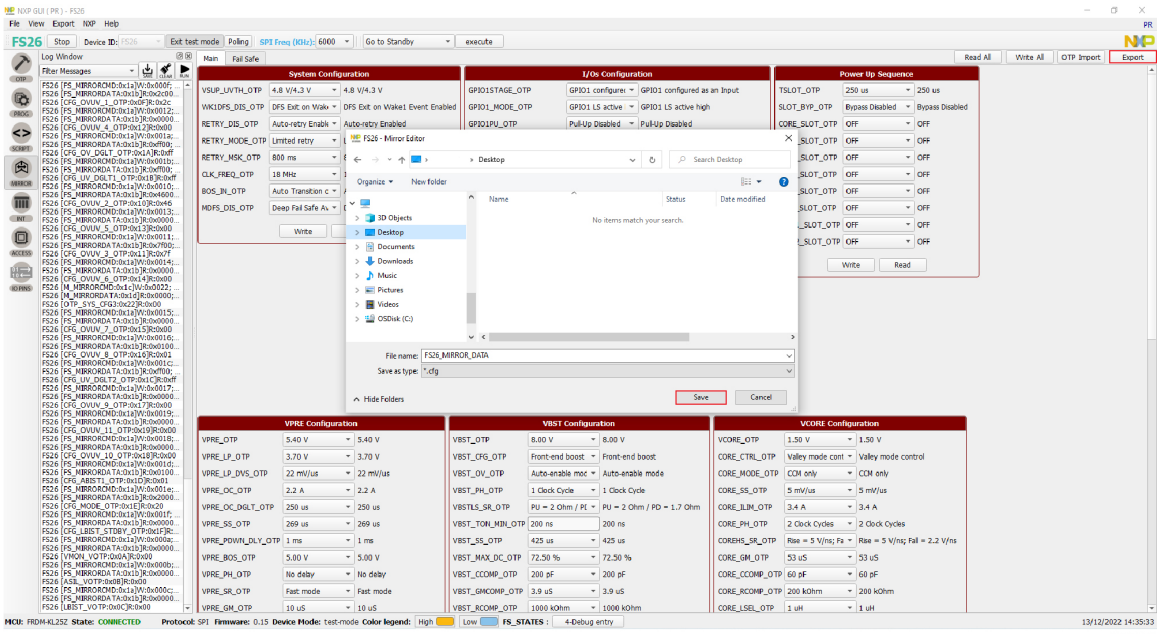

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Figure 67. Export option for reference

7.6.4 OTP import to mirror registers

This option is used to import the configuration file previously saved. Click **OTP Import** and select the .txt configuration file previously saved from this tab.

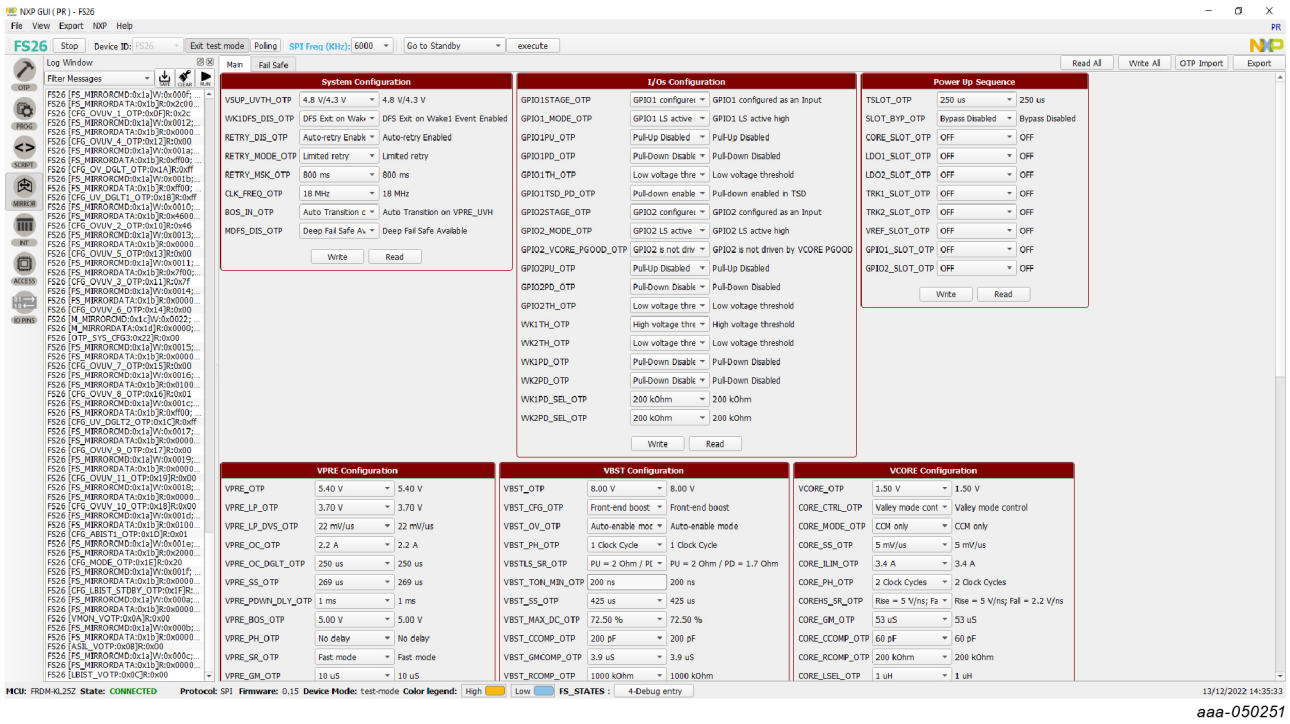

Figure 68. OTP Import for reference

7.7 Access tab

7.7.1 Register map

All registers can be accessed in write and read mode using this tab shown in Figure 69. These registers are divided into three sections:

- **Functional**: Main functional registers, such as flags for diagnostics, regulator state and configuration, and other controls.
- **Safety**: Safety registers, such as flags for diagnostics, Watchdog window, and period, ABIST2, safety output release.
- **Write_INIT_Safety**: Safety registers that can be manipulated only during INIT FS state, such as safety configurations and reactions.

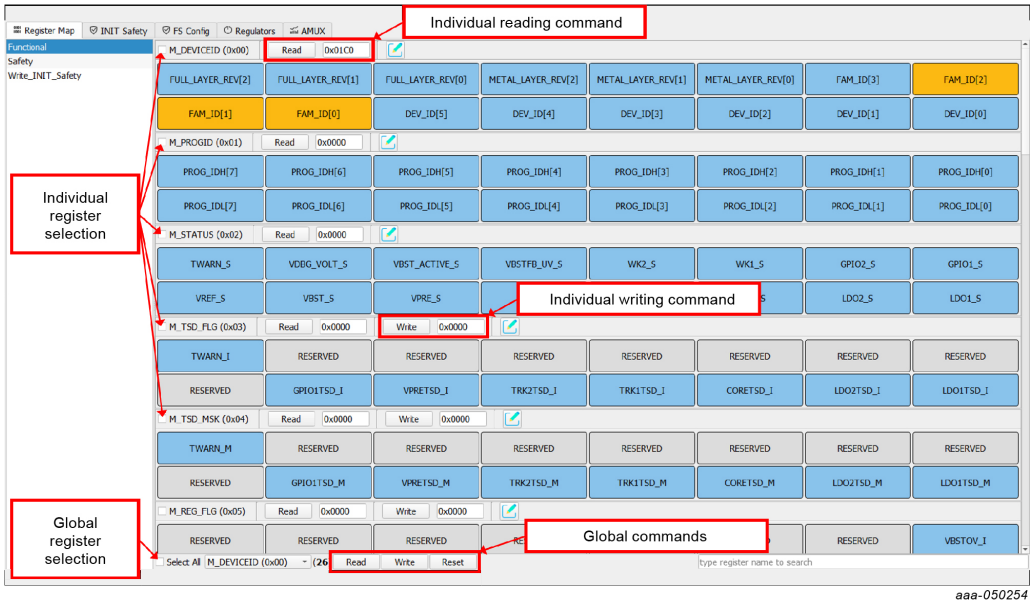

Figure 69. Register map access

To read the values of a register, click the **READ** button. The value is read from the device and is displayed on a label near the **READ** button. It is also displayed in the log window.

To write the bit values individually, click the desired bit. The corresponding bit button color changes. The value is updated in the log window. Click the **WRITE** button to write to the register. To write the values through a text box near the **WRITE** button, enter the appropriate write value. Then click the **WRITE** button to write to the register.

When registers have been selected, global commands can also be used:

- **WRITE**: Writes data to the selected registers at once.
- **READ**: Reads data back from the selected registers at once.
- **RESET**: Resets the write field of the selected registers at once.

The value can also be written by selecting the Edit option near the **WRITE** button. Bits and corresponding values are displayed in a pop window as shown in Figure 70. Select the options of all write bits, close the input dialog box, and click the **WRITE** button. Selected input combinations are written to the register.

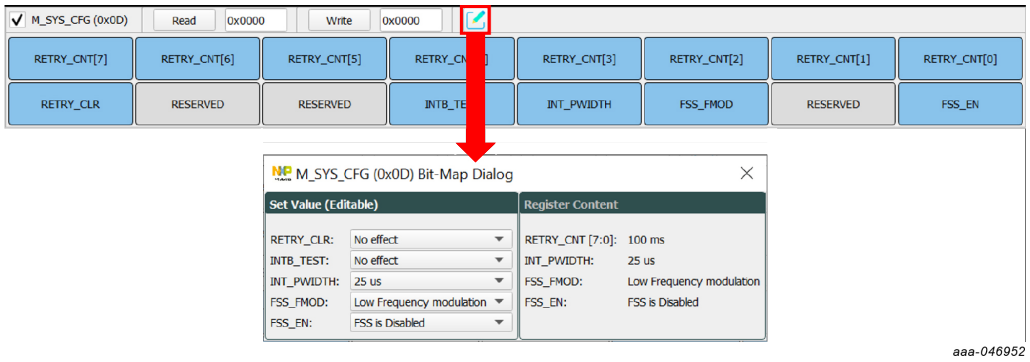

Figure 70. Bit map dialog

Writing an INIT safety register automatically updates the corresponding NOT register.

7.7.2 INIT safety tab

This tab allows the configuration of a safety output reaction in case of fault for voltage monitoring, FCCU, ERRMON, Watchdog, as shown in Figure 71. See the device data sheet for a complete description of these registers.

It is required to be in **INIT_FS** state to configure these registers.

- **Fault Impact**: Used to set FS0B/LIMP and FS1B reaction in case of fault.
- **FS1B Configuration**: Used to set FS1B delay and pulse duration.
- **Safety Inputs**: Used to set FCCU and ERRMON configuration.
- **Error Count Limit**: Used to set each error counter limit.
- **Miscellaneous**: Used to set some safety state machine behaviors.

Click the combo box controls to select the desired configuration, then click **Write**.

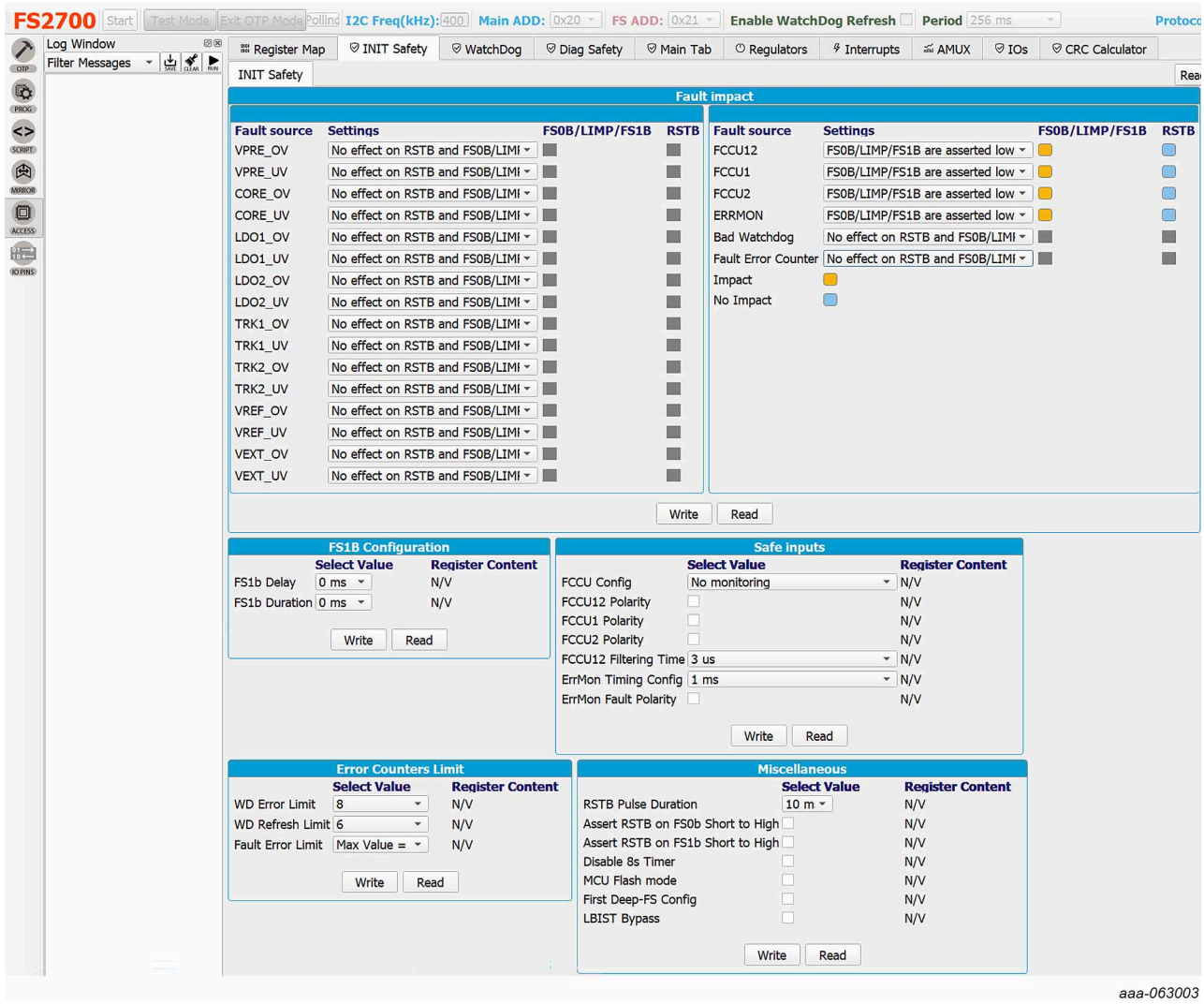

Figure 71. INIT safety tab

Read All and **Write All** buttons are implemented to facilitate configuration.

7.7.3 FS Config tab

This tab helps to configure safety features, such as Watchdog and Fault Error counter. Click **Read All** to get the current configuration.

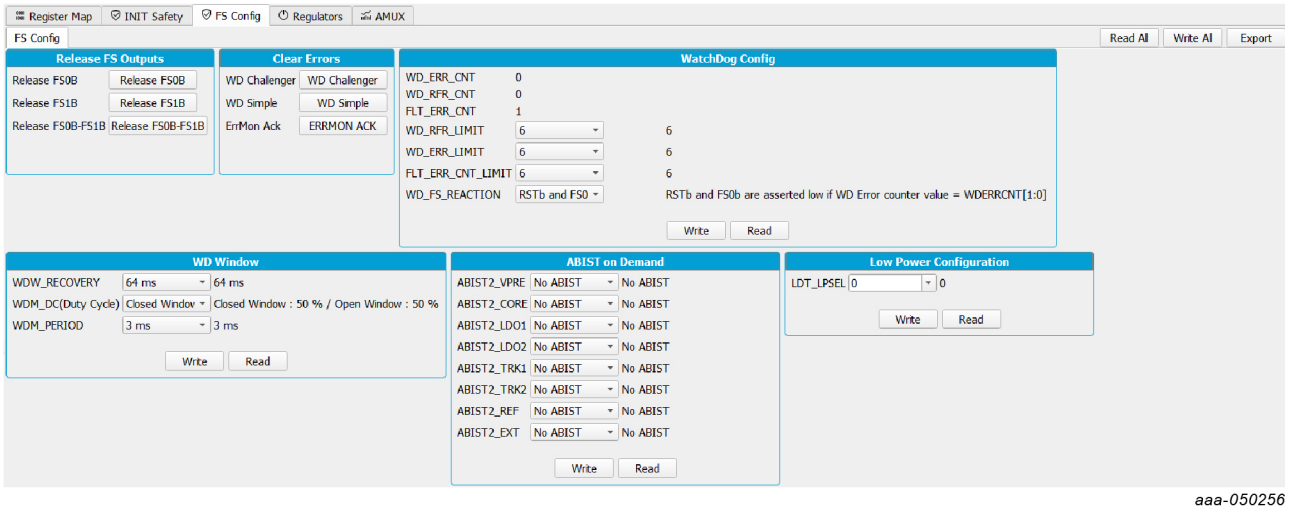

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Figure 72. FS Config tab

7.7.4 Regulators tab

This tab helps to manipulate the status of FS27 SMPSs, LDOs, and GPIOs. I²C/SPI commands can enable or disable any of them, excluding VPRE. Check the enable (EN) or disable (DIS) box, then click the **Write** button.

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Figure 73. Regulators tab

7.7.5 INT tab

To access the Interrupt Editor window, click Menu → INT or View → Show → Interrupt Editor.

The Interrupt Editor window has two tabs: the Interrupt Configuration tab and the Safety Diagnostic tab.

7.7.5.1 Interrupt Configuration tab

The Interrupt Configuration tab shown in Figure 74 allows the monitoring of the regulators, the wake inputs, the I/Os, and the communication events or status. It also allows the reading, writing and polling of overvoltage/ undervoltage, overtemperature, and overcurrent.

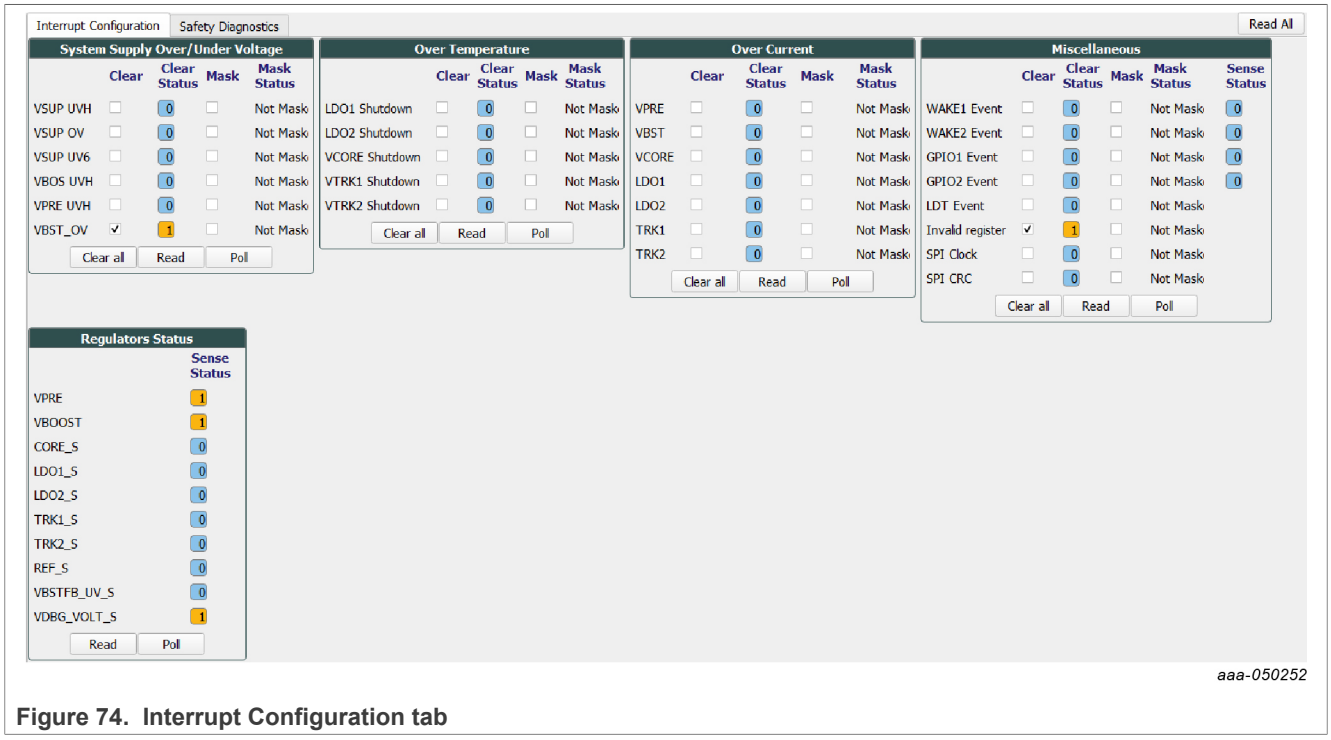

Figure 74. Interrupt Configuration tab

These commands can be used to manage the interrupts:

- **Clear all**: All interrupts in the box are cleared. The user can also click the individual check boxes from the **Clear** column.
- **Read**: Gives the status of all interrupts in the box.
- **Poll**: Reads interrupts' values in a loop.
  A few tips are given below to help the user:
- **Blue** means Low or not activated.
- **Yellow** means High or activated.
- To **mask** a specific interrupt, the user can check the interrupt's box from the **Mask** column.
- Click **Read** on each box to read the status or **Read All** to update the whole tab.

7.7.5.2 Safety Diagnostics tab

The Safety Diagnostics tab allows the monitoring of safety events such as VMON status, bad WD, SPI communication errors, FCCU pins, safety outputs, ABIST1 and ABIST2 status.

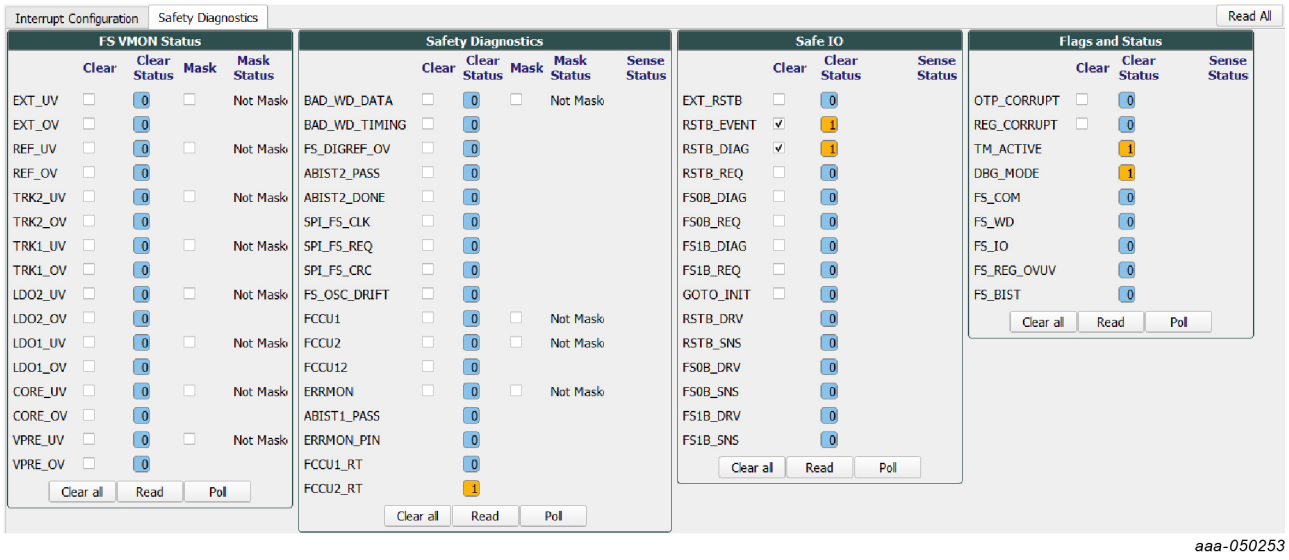

Figure 75. Safety Diagnostics tab

ABIST1_PASS yellow means that the ABIST1 is done and its status is PASS, since the user can read '1' from its register. '0' or blue after execution means fail.

Sense status can only be read (RSTB_DRV, RSTB_SNS, FS0B_DRV, ...).

7.7.6 AMUX tab

The AMUX tab shown in Figure 76 allows the selection of an AMUX pin channel. The pin channel gets its current value by using the FRDM-KL25Z board AMUX ADC pin. The user can do a single read, or display various channels dynamically on the voltage or temperature graph.

The displayed values already apply the divider and temperature formulas. Voltage regulators are also monitored independently on the FRDM-KL25Z board ADC pins.

To use the dynamic graph, select the channel then click the **+** button to add to the graph. To start polling, click the **Poll** button. Click the **Poll** button again to stop measurements.

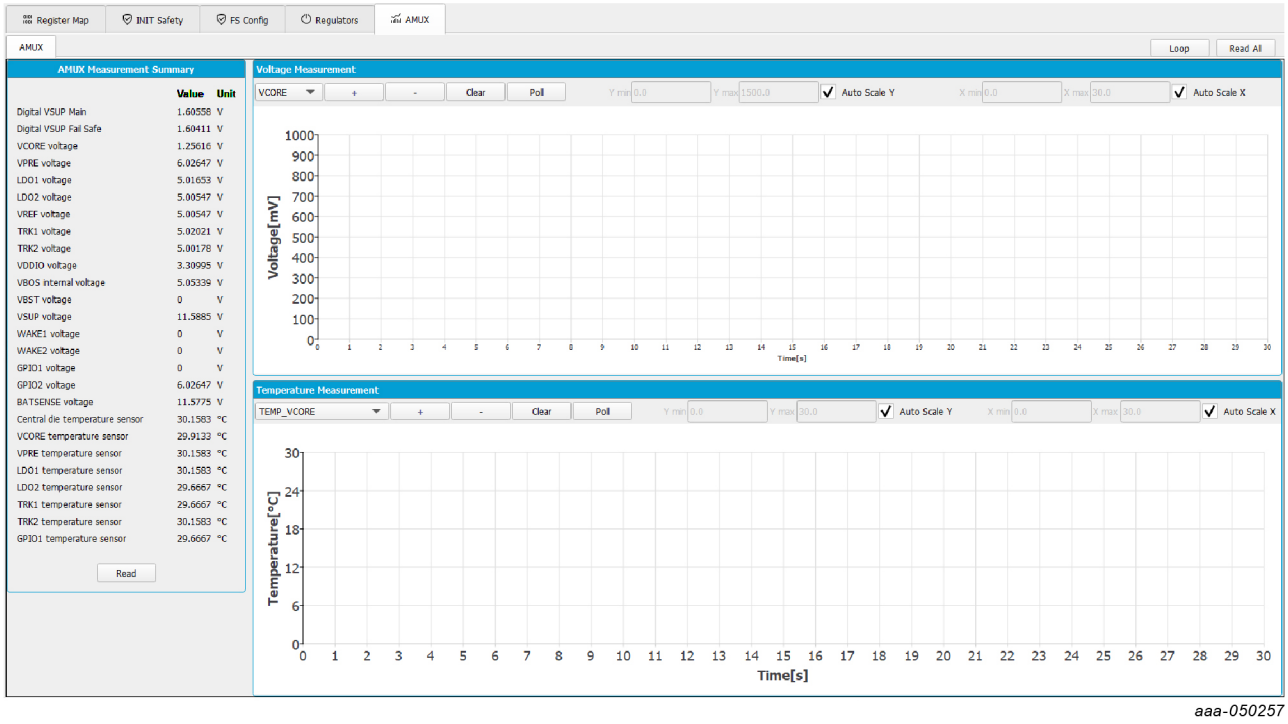

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Figure 76. AMUX measurements

7.8 I/O pins tab

This GUI section can control FS27 I/Os connected to the FRDM-KL25Z board. The GUI can read the FS27 safety outputs and control pins, such as FCCU and LVI.

The GUI also manages the FS27 communication protocol MUX by changing the MCU_COM_CTRL output.

Note: *The GUI can identify the current device protocol without user intervention.*

Moreover, the GUI provides access to the ADC Measurements from the FRDM-KL25Z board.

Voltage sources in order to apply sequences to apply Debug mode without moving any switches.

The input pins are the pins that can be read from the MCU. They are input pins from the MCU point of view. This section contains the safety outputs FS0B, FS1B, and RSTB. It can be read once with the **Read** button, or the user can select at which frequency the user wants to read the pins. Select the duration, then start polling with the **Poll** button.

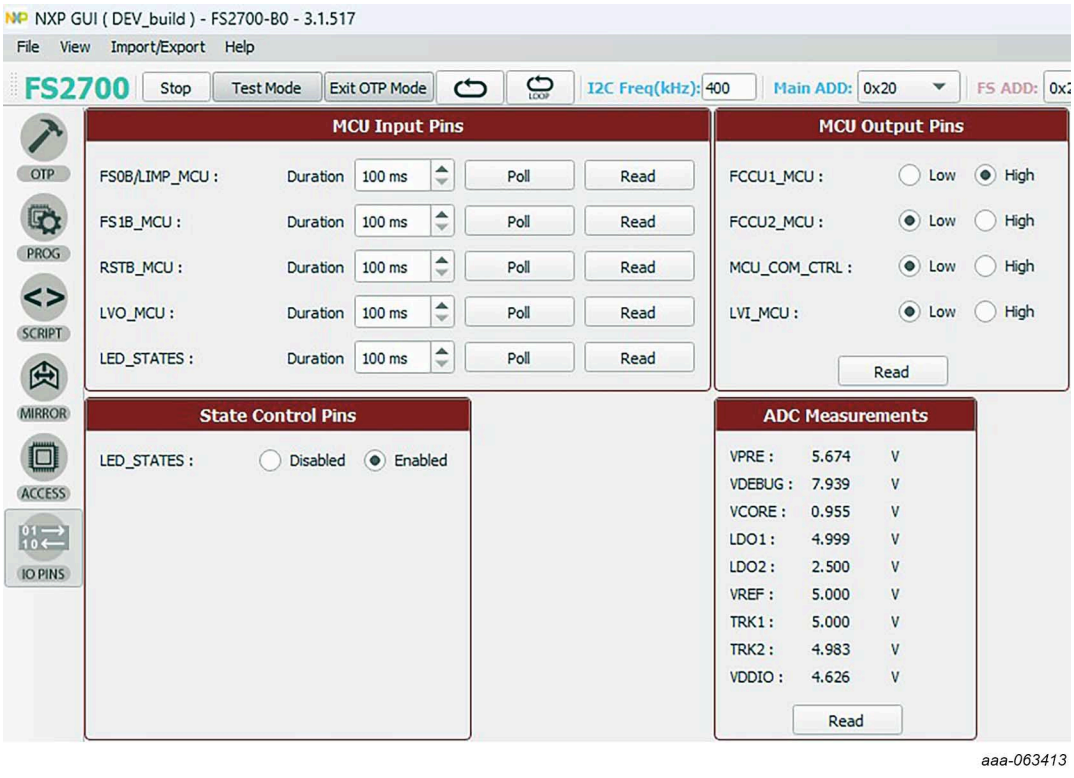

Figure 77. I/O pins tab

8 Using an FS27 evaluation board

Before starting the process, consult the development board scheme.

The device has a high level of flexibility due to the configurations available in the OTP that impacts the functionality of the device.

The OTP-related operations can only be performed in OTP mode (emulation or programming). When using emulation mode, the device loses the configuration when the power supply is switched off, when the device enters deep fail-safe, or when it enters standby mode.

Once the NXP GUI is installed (Section 6), follow these instructions for a quick power-up (Section 8.1), debug (Section 8.3), programming, or to enter the various operating modes (Section 8.4, Section 8.8, Section 8.9).

8.1 Power-up

Make sure that the board has the correct jumper configuration required for the application. Every kit is delivered with a default configuration shown in Figure 3.

Verify that the FRDM-KL25Z board is plugged in and the USB cable on the FRDM-KL25Z board USB connector side. USB cable connection enables communication with the NXP GUI, provides voltages and references to some circuits on the board, and generates the VDDIO reference for the IC (J14 is set to VDDIO_USB by default).

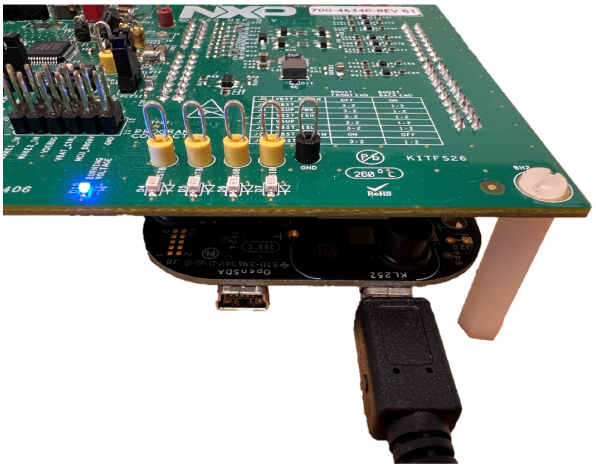

Figure 78. USB cable connection

After validating or considering all the previous statements, use switch SW1 to power on the board. See section Section 5.3.1. NXP recommends setting the power supply to an initial value of 12 V and limiting the current to 1.0 A.

If the device OTP configuration was programmed, connect a power supply to the VBAT Phoenix connector, the VBAT jack connector, or use the USB supply.

If the OTP configuration has safety features enabled, the device may restart or power-down after a few seconds. To prevent this issue, enter Debug mode to waive some safety features.

8.2 Establishing the connection between the NXP GUI for Automotive PMIC Families and the hardware

The device manager allows the connection of the FS27 development board with the NXP GUI for Automotive PMIC Families.

Before plugging the FRDM-KL25Z board USB port USB to the computer, the MCU is in a "NOT DETECTED" state.

Figure 79. MCU state is NOT DETECTED

After plugging in the USB, the MCU state changes to "DISCONNECTED". **If the state does not change, press the RST button on the Freedom board.**

Figure 80. MCU state is DISCONNECTED

In this state, the communication with the MCU can be started.

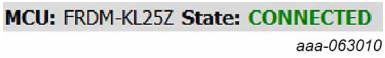

Figure 81. MCU state is CONNECTED

The MCU state changes to "CONNECTED" and the firmware version is displayed.

To start the communication with the device, click the **Start** button.

Figure 82. Click the Start button

When the communication has started successfully, the device name becomes to Green.

Figure 83. Device name is now green

When the device starts with the DEBUG pin voltage at V_{OTP} (on the EVBs: SW5 ON, OTP mode led D10 ON), the state machine stops at the Main/FS OTP Mode state.

The current mode can be read using the refresh button and loop refresh button highlighted in red. Clicking refresh reads the state one time. Clicking the loop refresh latches and reads the state periodically until a new click deactivates it.

When the "Exit OTP mode" button is green, as shown in Figure 84, the device is in OTP mode. When in OTP mode, device I^2C register addresses are the default values 0x20 for main and 0x21 for fail-safe. An “Exit OTP mode” button click sends commands to the main and the fail-safe state machines to exit OTP mode and initiate device start-up. The addresses are automatically updated to keep device communication.

Figure 84. GUI and device in OTP mode

Test mode can be enabled and disabled by clicking the Test Mode button when DEBUG pin voltage at V_{OTP} (on the EVBs: SW5 ON, OTP mode led D10 ON). When the button is green, as shown in Figure 85, Test mode is activated. The button state can also be refreshed by clicking the arrow loop buttons.

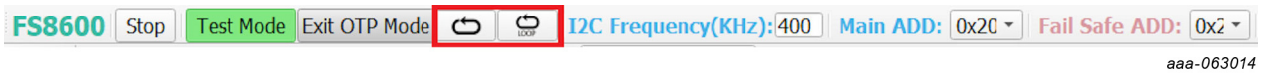

Figure 85. GUI and device in test mode

The current device mode (user/test) is shown on the device status bar.

Test mode can be entered when the device is not in OTP mode.

When in OTP mode, the device is necessarily in Debug mode.

8.3 Debug mode entry

The **Debug mode** is intended for MCU programming (MCU flash mode) and software debugging. During the power-up sequence, the Fail-safe state machine starts in Debug mode and goes directly to the INIT_FS state. To enter Debug mode without first entering OTP Emulation mode, follow the next steps once the kit is ready:

1. Make sure that the device is powered off (SW1 in middle position).
2. Turn on SW4 to apply V_{DBG} (~4.5 V) to the DEBUG pin.
3. Power on VBAT (SW1) and the device enters Debug mode.

In this mode, the Watchdog windowing is disabled, the RSTB 8 s counter is disabled, and FS0B is low and cannot be released.

To check that the device is in Debug mode, read the Debug-Mode status in the **Micro and Device Status**.

To check on the registers, go to the NXP GUI register map window (ACCESS tab), read the FS_DBG_MODE_RT bit in the FS_STATES register (latched information).

Figure 86. Debug Mode bit FS_DBG_MODE_RT active in FS_STATES register and Micro and Device Status bar

8.4 Test mode entry

To enter test mode, switch SW5 or SW4 must be on, and the appropriate key sequence must be written to the device.

Test mode can be enabled from the NXP GUI device manager or writing the keys in the script editor.

From the device manager:

Click the **Test Mode** button to send the Main and Fail-safe test mode entry keys.

From the script editor:

Add the following instruction:

SET_MODE:FS2700-B0:test-mode

Click **Run** script.

8.5 Emulate an OTP configuration

OTP mode is intended for OTP emulation (mirror manipulation) and OTP programming (burn fuses). When an OTP configuration is emulated, the configuration remains available until the POR of the digital circuitry. The Fail-safe configuration is lost in Deep Fail Safe and low power mode (LPOFF mode or Standby mode) since the Fail-safe digital is off in these modes. The Main digital configuration is lost when $V_{BOS} < V_{BOS\_POR}$, which means the device supply is removed.

To emulate an OTP configuration, the device must be started in OTP mode by switching on the OTP mode switch SW5 and then supply VBAT using SW1. When the device starts, the Main and the Fail-safe state machines stops prior to starting the regulators. The GUI button "Exit OTP Mode" must be green.

In the script editor, click "OPEN" load the OTP configuration script (TBB) to be emulated and click "RUN" to load the mirrors registers.

When the script is completed, the device can be powered up in a GUI click "Exit OTP Mode" or when SW5 is switched off. The Fail-safe state machine starts in Debug mode.

A TBB script usually contains the test mode entry keys. If they are not present in the script, see Section 8.4 to enter test mode.

After running the script, read the mirror registers to verify the loaded OTP configuration in the OTP Mirrors tab. Turn the SW5 off to apply 0 V on the DEBUG pin to start the power-up sequence and move to the **INIT_FS** state.

8.6 Programming the device with an OTP configuration

Instructions in this section are intended to burn an OTP configuration permanently into the fuses. Each sector in the OTP device can be programmed only **one time**. Make sure that a sector is available for programming.

The user can program an OTP configuration from the **PROG**/**Device Programming** tab.

1. Start the device in OTP Mode, see Section 8.5. **Exit OTP Mode** button must be green.
2. Click **Test Mode** to enable Test mode, the button must be green too.
3. Go to the Device programming tab (**PROG**) on the left panel.
4. Click **Read** to get the device current fuse box status.
5. Click **Browse** and select the desired OTP configuration script.
6. Click **Program** to initiate the device programming.
7. Wait until OTP programming is complete.
8. Click the **Exit OTP Mode** button to start the device.
9. Enabled regulators should have their respective LEDs turned on.
10. The device is in debug mode and FS state machine must be **INIT_FS** state.

8.7 Go to INIT_FS

Use these instructions before powering up the device, to get to the INIT_FS state from Debug mode or from OTP Emulation mode.

In **Debug mode**, when the device is programmed:

1. The device is powered off (SW1 in the middle position).
2. Switch on the SW4 to access Debug mode.
3. Power on the device (using SW1).
4. If the device is in OTP Mode (SW5 ON), click the **Exit OTP Mode** button or turn off SW5.
5. The power sequence is complete and the device is now in INIT_FS state (read the SM CURRENT STATE in the **Micro and Device Status**).

In **OTP Emulation mode**:

1. The device is powered off (SW1 in the middle position).
2. Switch on the SW5 to access OTP Mode.
3. Power on the device (using SW1).
4. The device state machines stop in Main/FS OTP mode.
5. Update GUI status: **Exit OTP Mode** button must be green.
6. Enable **Test Mode**.
7. The user can load an OTP configuration using a script or modify the current mirror content directly.
8. Click the **Exit OTP Mode** button must be green or turn off SW5 to resume the device power-up sequence.
9. The power sequence is complete.
10. The device is in debug mode and FS state machine must be **INIT_FS** state (read the SM CURRENT STATE in the **Micro and Device Status**).

In Figure 86, **Micro and Device Status** SM CURRENT STATE shows "INIT_FS".

8.8 Go to Normal mode

To enter **Normal mode** from the GUI, the user must be in Debug mode and in INIT_FS state. When using the simple Watchdog (WD), the user can send a script to release the device safety output pins FS0B and FS1B. If the Watchdog is set to challenger, the sequence must be sent manually.

Using the Script Editor

1. Once in INIT_FS state, the user must verify that ABIST1 is PASS from the Safety diagnostics tab.
2. Configure or check the Watchdog type from the Mirrors tab.
3. Use one of the following scripts to release the safety output pins. Use script A for simple Watchdog or script B for challenger Watchdog. The script to release the safety output pins is available in the device manager Script tab: from Script editor tab → Generator → Safety outputs release → Run.

   a. Sequence to enter Normal mode with a simple Watchdog:

```
// Open WD window
SET_REG:FS2700-B0:FS:FS_WDW_DURATION:0x008B
SET_REG:FS2700-B0:FS:FS_NOT_WDW_DURATION:0xF144
// Send 1ast good wd refresh to close INIT window
SET_MODE:FS2700-B0:simple-WD_good_refresh
// clear fault error counter
SET_MODE:FS2700-B0:simple-WD_good_refresh
SET_MODE:FS2700-B0:simple-WD_good_refresh
SET_MODE:FS2700-B0:simple-WD_good_refresh
SET_MODE:FS2700-B0:simple-WD_good_refresh
SET_MODE:FS2700-B0:simple-WD_good_refresh
SET_MODE:FS2700-B0:simple-WD_good_refresh
// Exit dbg mode
SET_MODE:FS2700-B0:exit-debug-mode
// release FS0B/LIMP_FS1B
SET_MODE:FS2700-B0:FS0B/LIMP_FS1B_release_command
// Update FS_STATES
GET_REG:FS2700-B0:SAFETY:FS_STATES
```

   b. Sequence to enter Normal mode with a challenger Watchdog:

```
// Open WD window
SET_REG:FS2700-B0:SAFETY:FS_WDW_DURATION:0x0080
SET_REG:FS2700-B0:SAFETY:FS_NOT_WDW_DURATION:0xF54F
// Send one good wd refresh to close INIT window
SET_MODE:FS2700-B0:challenger-WD_good_refresh
// clear fault error counter
SET_MODE:FS2700-B0:challenger-WD_good_refresh
SET_MODE:FS2700-B0:challenger-WD_good_refresh
SET_MODE:FS2700-B0:challenger-WD_good_refresh
SET_MODE:FS2700-B0:challenger-WD_good_refresh
SET_MODE:FS2700-B0:challenger-WD_good_refresh
SET_MODE:FS2700-B0:challenger-WD_good_refresh
// Exit dbg mode
SET_MODE:FS2700-B0:exit-debug-mode
// release FS0B/LIMP_FS1B
SET_MODE:FS2700-B0:FS0B/LIMP_FS1B_release_command
// Update FS_STATES
GET_REG:FS2700-B0:SAFETY:FS_STATES
```

Sending commands manually

To release the safety output pins manually and step by step, proceed with the following instructions:

1. Configure the WD window.
   Since it is not possible to send a WD refresh periodically, the user must disable the WD window. From the **WatchDog** tab (ACCESS tab on the left panel), click **Read**, set the **WD Window Period** box to **"Infinite open Window"**, and click **Write**.

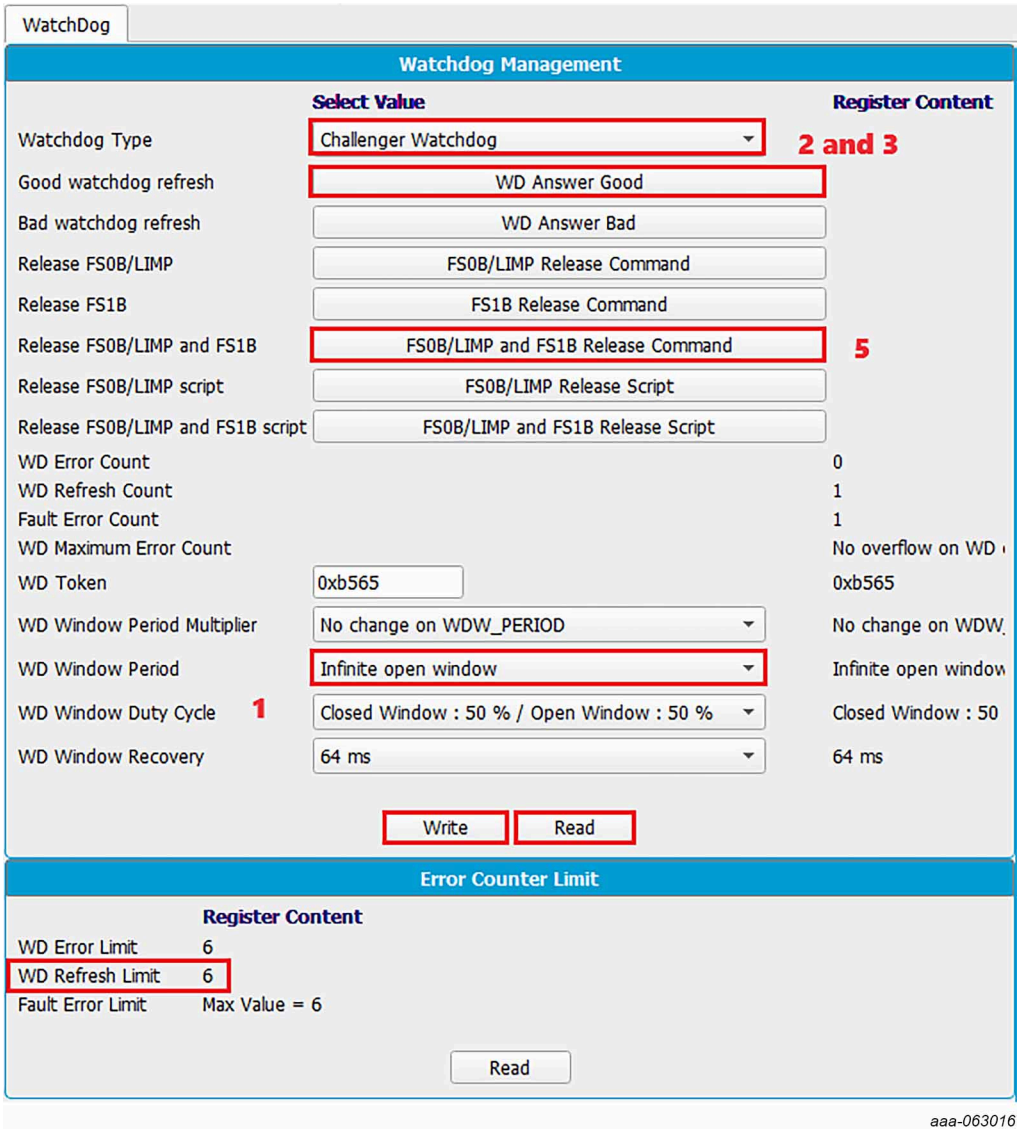

Figure 87. Warchdog Management

   Or execute it from the Script editor: Generator → OpenWD-Window → Run.
2. Send good WD refresh to close INIT phase.
   From the same tab, select the **Watchdog Type** appropriately, then click, **WD Answer Good** one time to send a first good WD refresh and move on the Fail-safe state machine.
   Or execute it from the Script editor: Generator → Simple-WD_good_refresh or Challenger-WD_good_refresh → Run.
3. Send the right number of good WD refreshes @WD_RFR_LIMIT[1:0] to clear the Fault Error counter.
   Example: The default number is 6. Click six times on **WD Answer Good** button. Verify that the Fault Error counter is now 0 (FLT_ERR_CNT[3:0]) in the **WatchDog** tab.

4. Exit Debug mode.
   Go to the **Register Map** tab, then in the Safety registers, set the **FS_DBG_EXIT** to 1 to exit Debug mode.

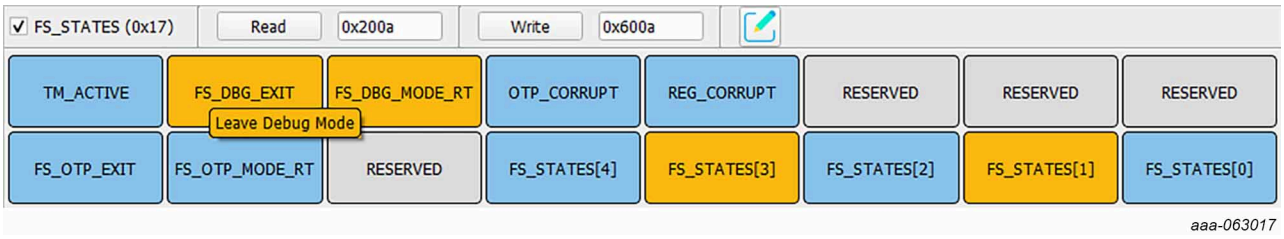

Figure 88. Set FS_DBG_EXIT to 1 and click Write

5. Send a "FS0B/LIMP Release Command" or a "FS0B/LIMP and FS1B Release Command" command to move to Normal mode.
   Find the commands on the **WatchDog** tab (ACCESS tab on the left panel).
6. Once these steps are completed, the device should be in Normal mode. To verify the current state, read the SM CURRENT STATE in the **Micro and Device Status** bar, or click it to update.

Figure 89. Fail-safe state machine in Normal Mode

All other fail-safe states reported on "SM CURRENT STATE" field are described on Table 36.

Table 36. Device Status fail-safe state machine FS_STATES[4:0] "SM CURRENT STATE" labels description

FS_STATES[4:0]	Label	Note
xxh	FS_OFF/undefined	
04h	OTP MODE	
05h	FS_ENABLE/LPRUN	
06h	wait ABIST start	Available if OTP_MODE switch SW5 is ON
08h	EXT_RSTB	Available if OTP_MODE switch SW5 is ON
09h	INIT_FS	
0Ah	FS0B LOCK	
0Bh	NORMAL	
1Fh	FLASH MODE	

8.9 Go to Low Power mode

FS27 cannot operate in low power mode when using the SEPIC or flyback as front-end regulator.

As a result, script commands “Go to Standby” (standby/LPON mode) and "Go to LPOFF" (LPOFF mode) cannot be used.

Note: *LPRUN mode cannot be used because requires going to standby mode.*

9 References

[1] **FS27 data sheet** — Safety System Basis Chip with low power for ASIL D / ASIL B
https://www.nxp.com/webapp/sd/collateral/170500567037572509671 9

[2] **FS27 website** — Detailed information on FS27
http://www.nxp.com/FS27
During the development phase:
- **Secure files** — https://www.nxp.com/sp/170486428760370231525 9

[3] **KITFS27-48VEVM evaluation board website** — Kit website
http://www.nxp.com/KITFS27-48VEVM

[4] **NXP GUI for Automotive PMIC Families** — Software GUI for NXP Automotive PMIC products
https://www.nxp.com/PMIC-GUI-SW
During the development phase:
- **GUI** — https://www.nxp.com/webapp/sd/collateral/1743434874352718281871
- **Firmware** — https://www.nxp.com/webapp/sd/collateral/1743433649143735879386
- **OTP configuration examples** — https://www.nxp.com/webapp/sd/collateral/17488765156607393777 79
- **Kit scheme** — https://www.nxp.com/sp/170486428760370231525 9?#design-resources

10 Revision history

Revision history

Rev	Date	Description
UM12356 v.1.0	28 October 2025	Initial version

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