

UM12292

KITPF09FRDMEVB Evaluation board

Rev. 1.0 — 20 November 2025

User manual

Document information

Information	Content
Keywords	PF09 NXP GUI, SBC, PF09, NXP GUI, SBC, ISO 26262, IMX9x, NXP GUI
Abstract	The KITPF09FRDMEVB evaluation board user guide is intended for the engineers involved in the evaluation, design, implementation, and validation of PF09 fail-safe system basis chips.



1 Introduction

The KITPF09FRDMEVB board user manual is intended for engineers involved in the evaluation, design, implementation, and validation of PF09 PMIC for high-performance applications.

The KITPF09FRDMEVB enables development on the PF09 family of devices. This document covers connecting the hardware, installing the NXP GUI software, configuring the environment, and using the kit. It includes guidance on how to use the registers, try OTP configurations, and burn the part.

The KITPF09FRDMPGM board is a socketed board supporting PF09 PMIC with 5 SMPS and three LDOs. In this document, "PF09" refers to these supported devices.

The devices can be placed and removed from the board using the socket.

2 Finding kit resources and information on the NXP website

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on <http://www.nxp.com>.

The information page for KITPF09FRDMEVB board is at <https://www.nxp.com/products/PF09>. The information page provides overview information, documentation, software, and tools, parametric, ordering information.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, asking and answering technical questions, and receiving input on just about any embedded design topic.

The NXP community is at <http://community.nxp.com>.

3 Getting ready

Working with the KITPF09FRDMEVB requires the kit contents, more hardware, and a Windows PC workstation with installed software.

3.1 Kit contents

The KITPF09FRDMEVB kit contains the following items:

- Assembled and tested evaluation board with preprogrammed KL25Z microcontroller in an antistatic bag
- 3.0 ft USB-STD A to USB-B-micro cable
- Six Phoenix connectors, two positions, straight, 10 mm
- Jumpers mounted on board

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary and is beneficial when working with this kit:

- Power supply capable of providing 5 V

3.3 Minimum system requirements

This evaluation board requires a Windows PC workstation.

- USB-enabled computer with Windows 7 or Windows 10
- FTDI USB serial port driver (for FT230X basic UART device)

3.4 Software

Installing software is necessary to work with the KITPF09FRDMEVB evaluation board.

All listed software is available on the information page of the evaluation board at [9-Channel PMIC for High-Performance Applications, ASIL D and SIL-2](#).

- NXP GUI for automotive family installation package - latest version

4 Getting to know the hardware

The KITPF09FRDMEVB kit provides an integrated platform for evaluating designs based on the PF09 Family of NXP. All PF09 Family features can be accessed and monitored in a test environment using NXP GUI software to access the registers in Read and Write mode. All regulators are accessible through connectors. Nonuser signals are mapped on test points. Digital signals (I²C, RSTB, and so forth) are accessible through connectors.

4.1 Kit overview

The hardware of the kit consists of the KITPF09FRDMEVB evaluation board embedded with a KL25Z microcontroller, and the USB cable required to connect the board to the PC.

The KITPF09FRDMPGM evaluation board features a socket that allows the user to fuse an individual PF09 Family using the device's two time programmable (OTP) feature without extra tools. Connectors, jumpers, and switches on the board can be used to configure an evaluation environment that meets specific design requirements. The board also contains LEDs and test points that provide a means of monitoring performance in real time. An emulation mode allows the user to test as many configurations as needed before programming the part.

The KL25Z is soldered on the bottom side of the KITPF09FRDMEVB board. The role of the KL25Z is to manage I²C communication between the KITPF09FRDMEVB board and the GUI installed on the PC. The KL25Z draws power either from the USB cable connected to the PC or from the battery supply (when not connected to the GUI).

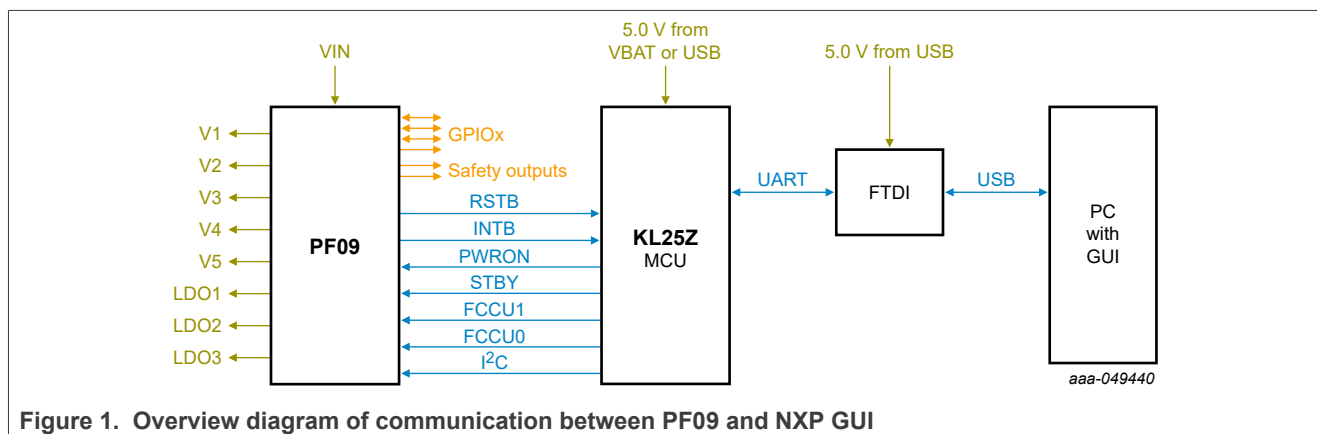


Figure 1. Overview diagram of communication between PF09 and NXP GUI

Note: This document uses the PF09 as a default configuration. Specificities for PF are explained in the flow if necessary. Otherwise, the features are common to PF09.

4.2 Board features

- Phoenix (10 mm) male connector or jack connector for power supply input
- Phoenix (10 mm) male connectors for PMIC switcher outputs

- Header connectors for I/O configuration
- Selectable power input for programming
- Access pin connectors for accessing inputs and outputs
- Indicator LEDs red and green LEDs to indicate signal or regulator status
- Blue LED to indicate that the OTP 8 V burning voltage is set
- Advanced system monitoring via the KL25Z MCU
- Embedded USB to I²C protocol for easy connection to the software GUI through the KL25Z MCU

4.3 KITPF09FRDMEVB featured components

[Figure 2](#) shows the placement of connectors, configuration headers, and LEDs signaling. For information on the default jumper and switch configuration for PF09, see [Section 7.1](#).

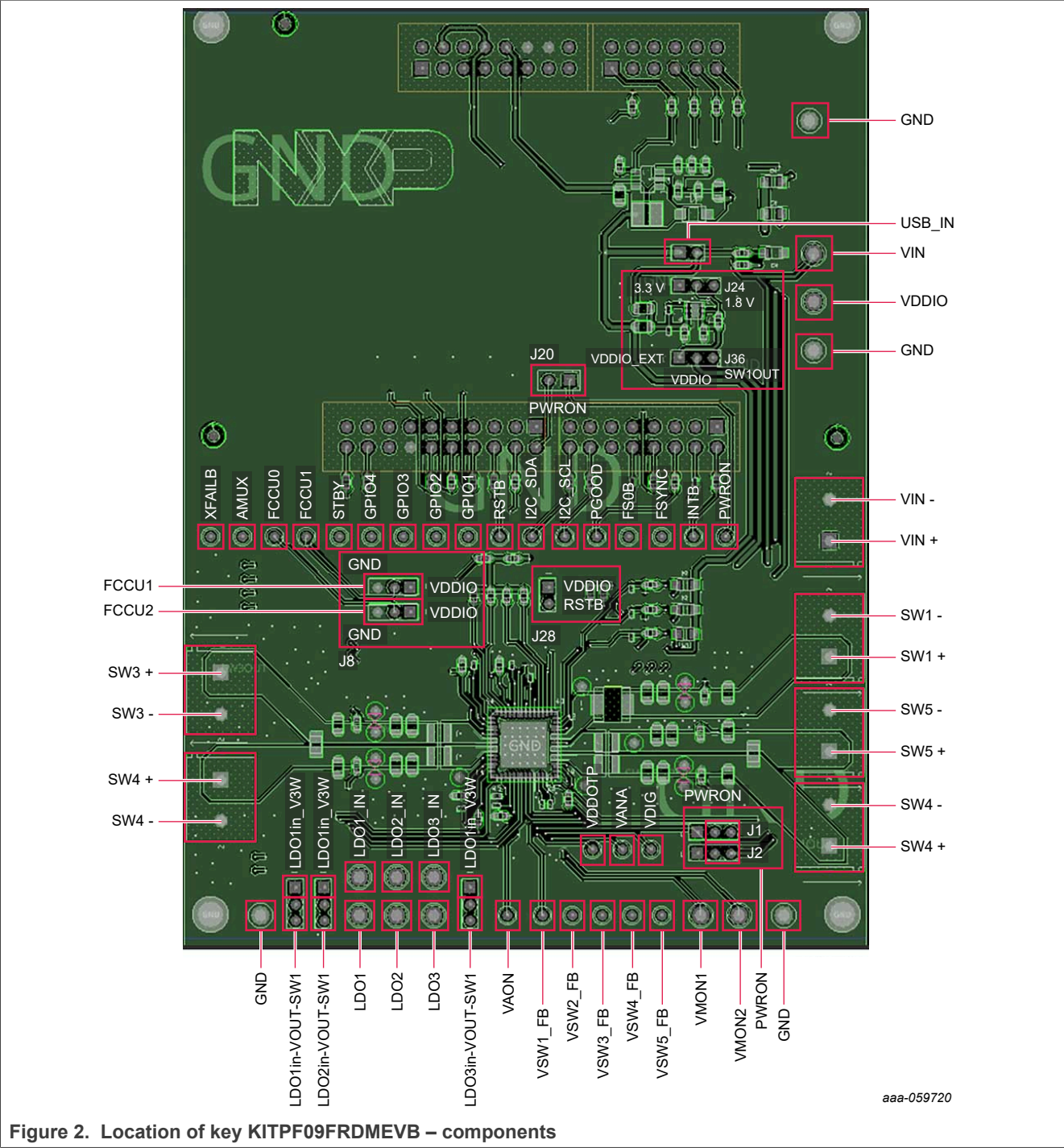


Figure 2. Location of key KITPF09FRDMEVB – components

4.4 KITPF09FRDMEVB evaluation board

This section describes the KITPF09FRDMEVB evaluation board by explaining the features associated with each jumper and switch, giving information on hardware configuration to enable these features, and providing advice on LED signaling and test points available on the board.

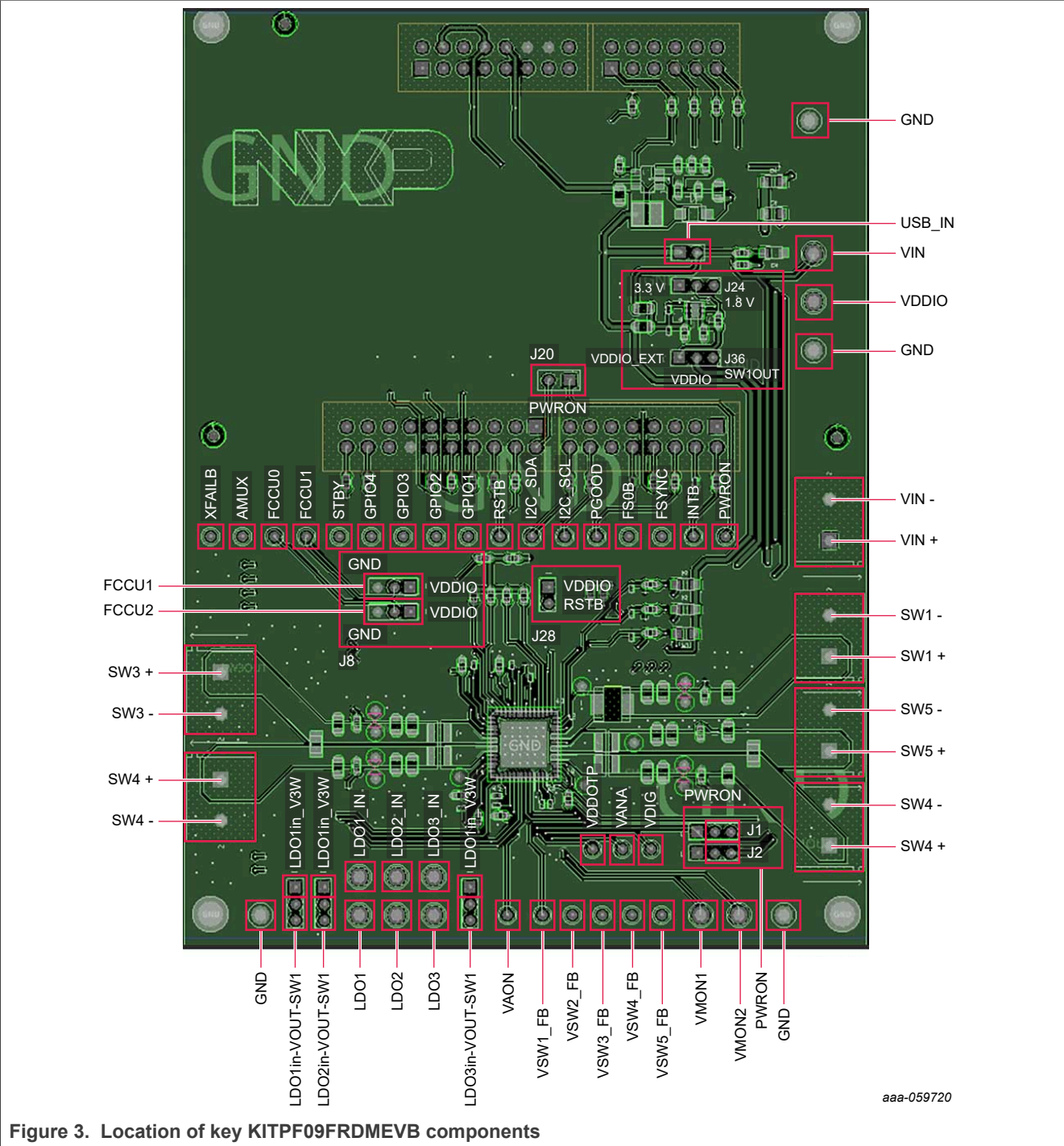


Figure 3. Location of key KITPF09FRDMEVB components

Note: The silkscreen on the board gives hints on the jumper positioning depending on the functions implemented.

The default debug configuration enables the board to be fully controlled by the KL25Z MCU (via I²C) and the GUI. [Figure 3](#) shows the default jumper and switch configuration for PF09. See below for PF09 default jumpers and switches configuration.

Table 1. Configuration Jumpers

Reference	Description	Settings for Configuration		External Configuration
J1	PWRON pullup voltage selection.	Pins: 1 to 2	VIN	Open
		Pins: 2 to 3	VAON	Open
J2	VDDOTP connection.	Pins: 1 to 2	VDIG	Open
		Pins: 2 to 3	VDDOTP_BST	Connected
J9	FCCU0 input level connection.	Pins: 1 to 2	VDDIO	–
		Pins: 2 to 3	GND	–
J10	FCCU1 input level connection.	Pins: 1 to 2	VDDIO	–
		Pins: 2 to 3	GND	–
J20	Power on connection to interface system.	Pins: 1 to 2	Connected	Connected
J24	Selection of external VDDIO voltage (1 to 2: 1.8 V <=> "2 to 3":3.3 V).	Pins: 1 to 2	1.8 V	–
		Pins: 2 to 3	3.3 V	Connected
J29	RSTB pullup to VDDIO, connect for operation.	Pins: 1 to 2	Connected	Connected
J36	VDDIO power Input election.	Pins: 1 to 2	External	Connected
		Pins: 2 to 3	SW1	–
J48	LDO1 Input voltage.	Pins: 1 to 2	VSW_IN	Connected
		Pins: 2 to 3	SW1_OUT	–
J49	LDO2 Input voltage.	Pins: 1 to 2	VSW_IN	Connected
		Pins: 2 to 3	SW1_OUT	–
J50	LDO3 Input voltage.	Pins: 1 to 2	VSW_IN	Connected
		Pins: 2 to 3	SW1_OUT	–
J54	USB Jumper. Used to connect to USB power. Open for using external power supply (VIN). Connect external power for correct operation.	Pins: 1 to 2	Used – USB power Open – External power supply	Open

Table 2. Phoenix Contact/PCB terminal functions

Reference	Function	Description
J39	SW2 output	PMIC switcher 2 output voltage. Direct connection to PMIC pin.
J40	SW3 output	PMIC switcher 3 output voltage. Direct connection to PMIC pin.
J41	SW4 output	PMIC switcher 4 output voltage. Direct connection to PMIC pin.
J42	SW5 output	PMIC switcher 5 output voltage. Direct connection to PMIC pin.
J43	SW1 output	PMIC switcher 1 output voltage. Direct connection to PMIC pin.
J47	VIN	Input voltage supply can come from the power supply. Range from 3.3 V to 5.0 V; according to specification.

Table 3. Access point functions

Reference	Function	Description	Color
BH1	GND	Board grounds direct connection -4 easy access points.	Black
BH2			
BH3			
BH4			
TP119	LDO1IN	Monitoring point for the LDO1 input voltage.	Red
TP120	LDO2IN	Monitoring point for the LDO2 input voltage.	Red
TP121	LDO3IN	Monitoring point for the LDO3 input voltage.	Red
TP61	VLDO1	Monitoring point for the LDO1 output.	Red
TP60	VLDO2	Monitoring point for the LDO2 output.	Red
TP59	VLDO3	Monitoring point for the LDO3 output.	Red
TP15	VAON	Monitoring point for the VAON output.	White
TP90	SW1 FB	Monitoring point for the SW1 feedback.	White
TP86	SW2 FB	Monitoring point for the SW2 feedback.	White
TP87	SW3 FB	Monitoring point for the SW3 feedback.	White
TP91	SW4 FB	Monitoring point for the SW4 feedback.	White
TP92	SW5 FB	Monitoring point for the SW5 feedback.	White
TP78	VMON1	Monitoring point for the external monitor VMON1.	Orange
TP79	VMON2	Monitoring point for the external monitor VMON2.	Orange
TP65	XFAILB	XFAILB PMIC access point – bidirectional pin.	White
TP57	GPIO1	GPIO1 access point – bidirectional pin.	White
TP20	GPIO2	GPIO2 access point – bidirectional pin.	White
TP56	GPIO3	GPIO3 access point – bidirectional pin.	White
TP8	GPIO4	GPIO4 access point – bidirectional pin.	White
TP4	I2C-SDA	I ² C SDA access point – bidirectional pin.	White
TP5	I2C-SCL	I ² C SCL access point – bidirectional pin.	White
TP9	FSYNC	FSYNC access point – bidirectional pin.	White
TP55	AMUX	Analog multiplexer output monitoring point.	White
TP12	RSTB	System reset signal output monitoring point.	White
TP3	FS0B	Fail-safe output monitoring point.	White
TP10	INTB	INTB output monitoring point.	White
TP52	FCCU0	FCCU0 fault monitoring input pin access point.	White
TP53	FCCU1	FCCU1 fault monitoring input pin access point.	White
TP6	STBY	STBY input pin access point.	White
TP2	PGOOD	PGOOD input pin access point.	White
TP7	PWRON	Power on input pin access point.	White

Note: Test-points are routed directly to the pins.

4.4.1 Voltage selection and configuration

The input voltage supply can come from a power supply via a Phoenix contact (VIN) or from the USB line. Close the J54 for using the USB connection and open for external voltage. The use of an external power supply is recommended as the USB capability may be limited. Input range is from 3.3 V to 5 V and matching to VIN in OTP configuration.

VDDOTP requires 8 V for PMIC programming (VDDOTP_BST), place the jumper J2 in pins 2 and 3 for programming, or 1 and 2 for normal operation and debugging.

VDDIO voltage selection through jumpers J24 and J36. Jumper J36 selects whether the use for VDDIO is external or PMIC SW1 output.

Define LDOs input voltage, use J48, J49, J50, to configure individually between the VIN or the SW1 output voltage.

Table 4. Voltage selection and configuration

Reference	Description	Configuration	
J47	VIN	Input voltage supply can come from the power supply. Range from 3.3 V to 5.0 V; according to specification.	
J2	VDDOTP connection.	Pins: 1 to 2	VDIG
		Pins: 2 to 3	VDDOTP_BST
J24	Selection of external VDDIO voltage	Pins: 1 to 2	1.8 V
		Pins: 2 to 3	3.3 V
J36	VDDIO power input selection.	Pins: 1 to 2	External
		Pins: 2 to 3	SW1
J54	USB jumper.	Pins: 1 to 2	Open
J48	LDO1 input voltage.	Pins: 1 to 2	VSW_IN
		Pins: 2 to 3	SW1_OUT
J49	LDO2 input voltage.	Pins: 1 to 2	VSW_IN
		Pins: 2 to 3	SW1_OUT
J50	LDO3 input voltage.	Pins: 1 to 2	VSW_IN
		Pins: 2 to 3	SW1_OUT

4.4.2 Power on configuration

PWRON input to provide a wake-up event. It uses two modes of operations, level or edge sensitive, per-device configuration.

Connect J20 to ensure control from the PF09 controller. Use J1 to select the power supply used for PWRON. When J1 pins 1 and 2 are connected, PWRON is pulled up to VIN, and for J1 pins between 2 and 3, PWRON is pulled to VAON, an internal, low power, power supply.

Table 5. PWRON configuration

Reference	Description	Configuration	
J1	PWRON pullup voltage selection.	Pins: 1 to 2	VIN
		Pins: 2 to 3	VAON
J20	Power on connection to Interface system.	Pins: 1 to 2	Connected

4.4.3 External power monitoring

FCCUx (fault collection and control unit) inputs “0” and “1” monitoring. Use Jumpers 9 and 10 to define the state of the inputs.

Table 6. FCCUx configuration

Reference	Description	Configuration	
J9	FCCU0 input level connection.	Pins: 1-2	VDDIO
		Pins: 2-3	GND
J10	FCCU1 input level connection.	Pins: 1-2	VDDIO
		Pins: 2-3	GND

4.4.4 RSTB pullup

RSTB, in a functional safety output. Use jumper J29 to ensure

Table 7. RSTB configuration

Reference	Description	Configuration	
J29	RSTB pullup to VDDIO, connect for operation.	Pins: 1-2	Connected

4.4.5 Output voltages

All buck switchers and LDOs can be configured at different output voltage, up to 3.3 V. LDOs can also be configured as a simple load switch. Output voltage uses discrete values and not all values are available. This is done via OTP configuration or I²C communication.

Table 8. Output voltage

Reference	Function	Output voltage range
J39	SW2 output	From 0.3 V to 3.3 V
J40	SW3 output	From 0.3 V to 3.3 V
J41	SW4 output	From 0.3 V to 3.3 V
J42	SW5 output	From 0.3 V to 3.3 V
J43	SW1 output	From 0.5 V to 3.3 V
TP61	VLDO1	From 0.75 V to 3.3 V
TP60	VLDO2	From 0.65 V to 3.3 V
TP59	VLDO3	From 0.65 V to 3.3 V

4.4.6 MCU communication I²C selection

Table 9. MCU communication I²C selection

Schematic label	Signal name	Description
J16-16-PTC9	SDA	I ² C is selected as the MCU communication protocol.
J16-14-PTC8	ISCL	I ² C is selected as the MCU communication protocol.
J19-18-PTC9	SDA	I ² C is selected as the MCU communication protocol.
J19-20-PTC8	ISCL	I ² C is selected as the MCU communication protocol.

4.4.7 Debug and OTP configuration

During normal system operation, the DBGOFF (Debug Off), [Section 7.3.1](#), state is a transitory state between a power on event and the power up sequence. It serves as the gating state to ensure that the PMIC is ready to start a power up sequence, and allow synchronization of two or more PMICs providing full power architecture to a complex system.

If a VDDIO supply is provided externally, the device is able to communicate through the I²C bus during the DBGOFF state, allowing the PMIC to operate in development/debugging modes. In such scenarios, the DBGOFF state becomes a full biased OFF state to allow full access to the functional and OTP registers to enable OTP emulation and/or OTP fuse programming.

OTP mode is active when the DEBUG pin is set to 8 V. Once in OTP mode, specific keys are necessary to enter test mode, see [Section 7.3.2](#) or OTP programming process.

4.4.8 LED signaling

LED signaling displays the state of the following signals:

- Signals: PGOOD, INTB, FS0B
- Power supply: VIN
- OTP control: VDDOTP - 5 V, VDDOTP - 8 V

The VIN LED is permanently on. OTP control LEDs are either 5 V or 8 V status control signals. Consider them with current consumption measurements for better analysis.

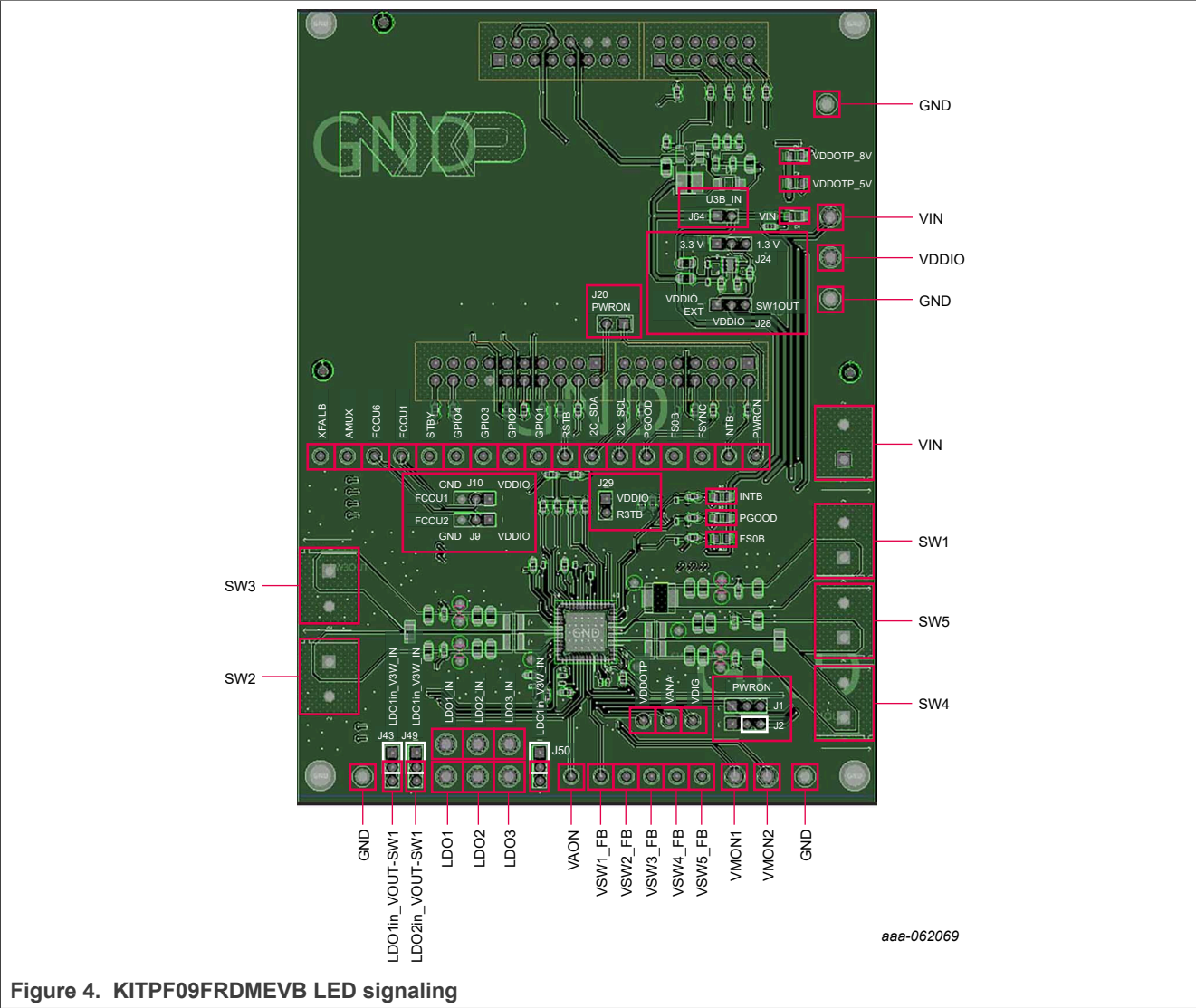


Figure 4. KITPF09FRDMEVB LED signaling

4.4.9 Test points

The KITPF09FRDMEVB board has several test points that facilitate access and measurements. This section summarizes the available test points, how they are color-coded, and whether they are a test point component with a part number or a pad test point with no part number.

Yellow: Test loop access to safety outputs, communication, control lines, and analog signals.

Table 10. Test points list

Item	Test point name	Item	Test point name	Item	Test point name	Item	Test point name	Item	Test point name
1	SW1_Lx	6	VMON1	11	FCCU1	16	GPIO1	21	FS0B
2	SW5_Lx	7	VMON2	12	STBY	17	RSTB	22	FSYNC
3	SW4_Lx	8	XFAILB	13	GPIO4	18	SDA	23	INTB
4	SW2_Lx	9	AMUX	14	GPIO3	19	SCL	24	PWRON
5	SW3_Lx	10	FCCU0	15	GPIO2	20	PGOOD	—	—

Red: Test loop access for power supplies (inputs and outputs)

Black: Test loop access to GND

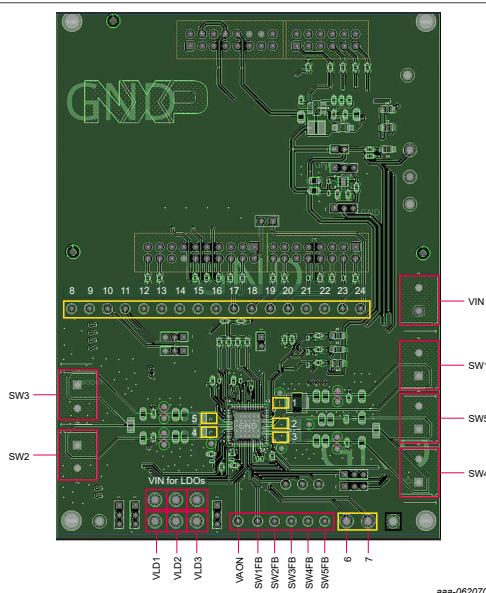


Figure 5. KITPF09FRDMEVB -Test points

4.4.10 Schematic layout and bill of materials

The board layout and bill of materials for the KITPF09FRDMEVB evaluation board are available at <https://www.nxp.com/products/PF09>.

5 Installing and configuring software tools

Note: This section will use the PF09 as an example to explain software installation, configuration, and use. Specific explanations for PF09 are added on the side if necessary. Otherwise, the method is general to PF09.

5.1 Flashing KL25Z MCU GUI firmware

The KITPF09FRDMEVB is delivered with the KL25Z firmware already flashed.

5.2 Installing the PF09 NXP GUI software package

To install the PF09 NXP GUI, first download or obtain the NXP GUI package, then follow the instructions below:

1. Open the NXP GUI package. Unzip and open the 1-NXP_GUI_Setup folder. Current version: v3.1.499). Same installation procedure.

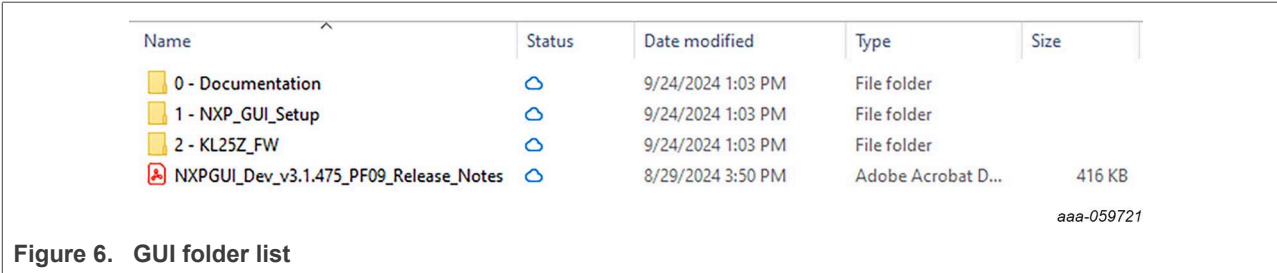


Figure 6. GUI folder list

2. Double click **NXP_GUI-version-Setup.exe** to launch the application and follow the instructions.



Figure 7. NXP_GUI-version-Setup.exe

3. Click **Next** when the initial application setup window appears.
4. On the License Agreement window, read the license information and click **I Agree**.

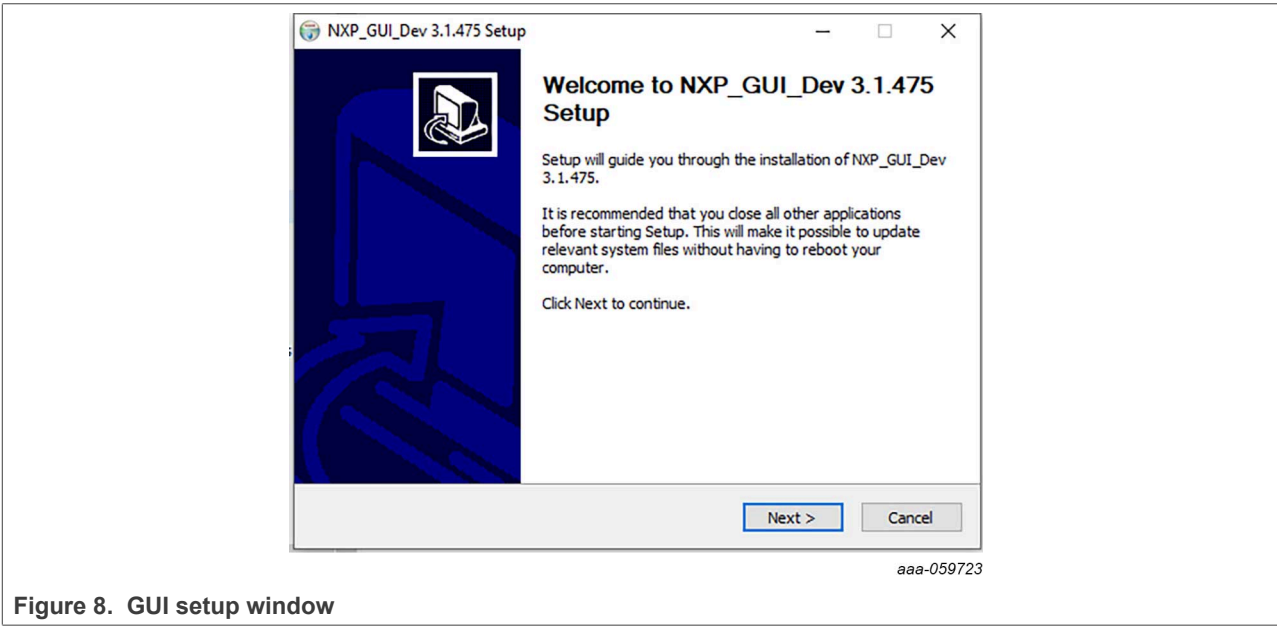


Figure 8. GUI setup window

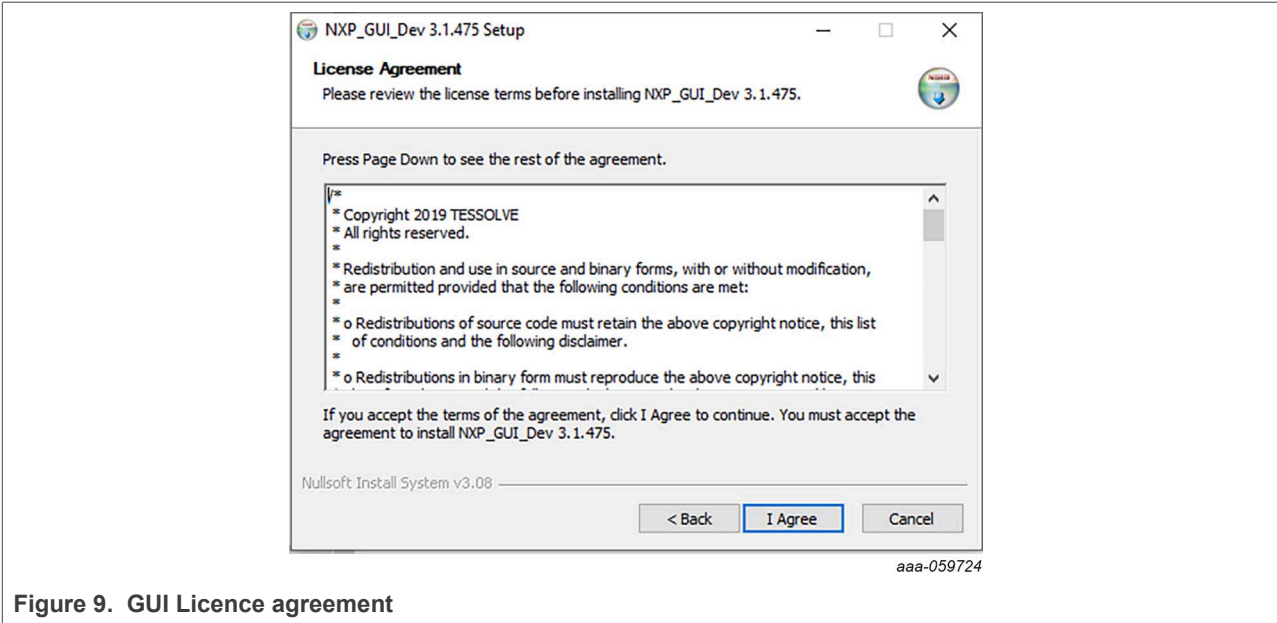


Figure 9. GUI Licence agreement

5. In the Choose Components window, select the GUI components to install, then click **Next**.

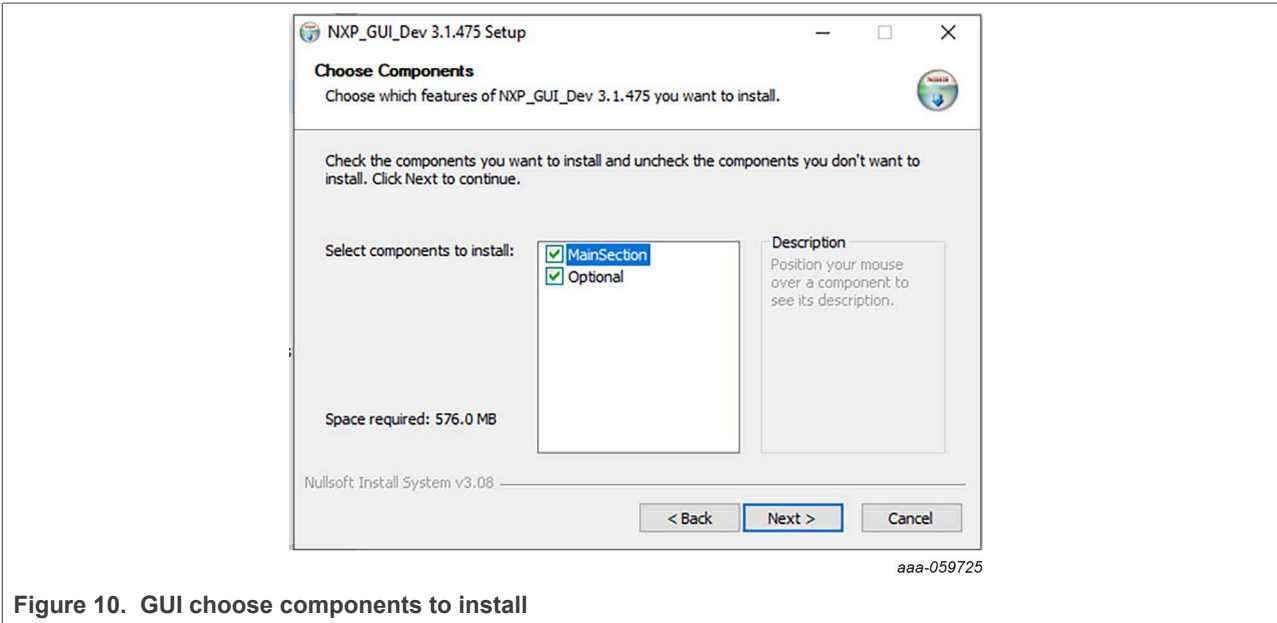
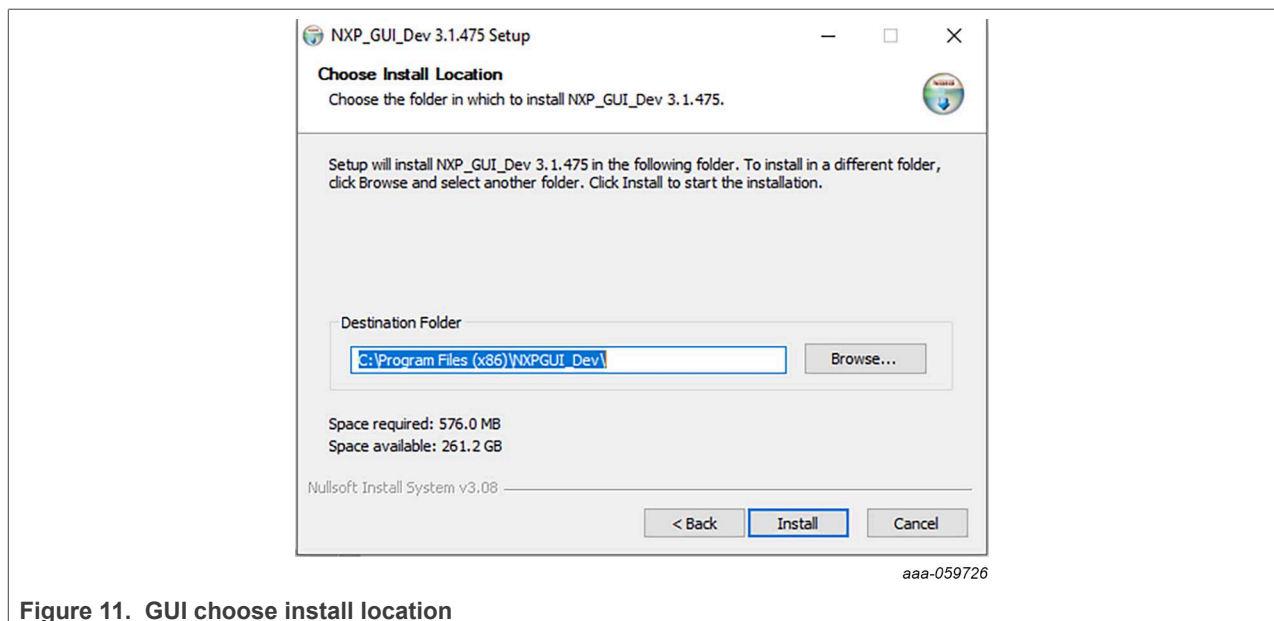
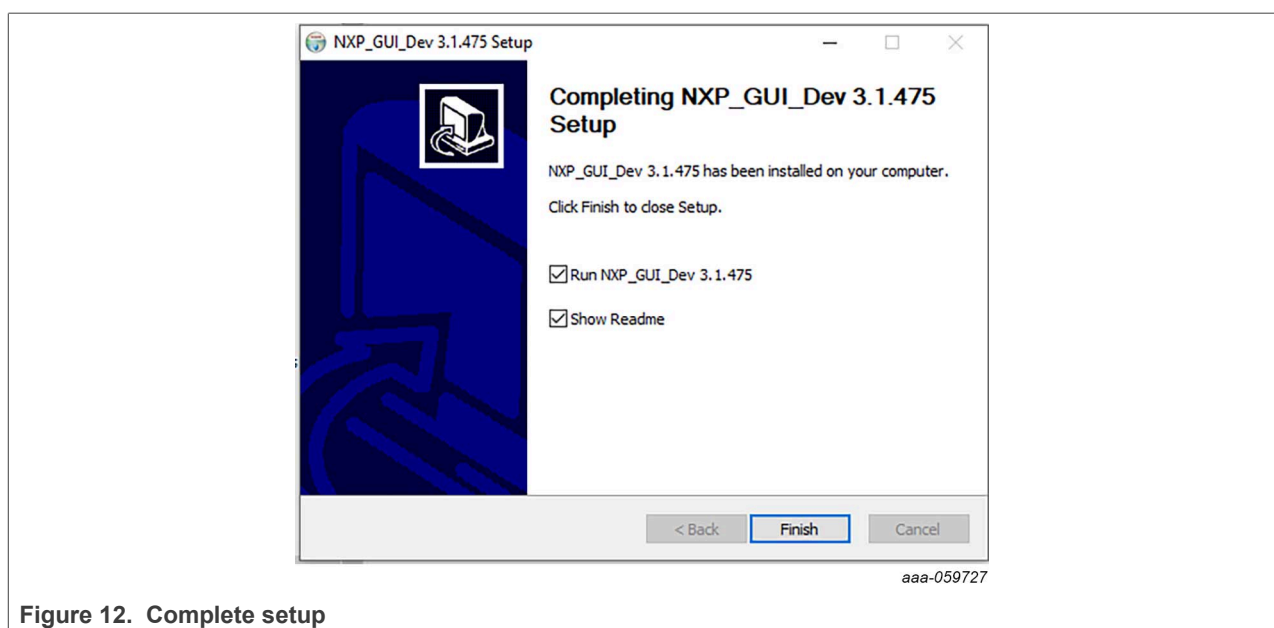


Figure 10. GUI choose components to install

6. In the "choose install location window", choose the folder to install the GUI.



7. In the Completing Setup window, select the following options:
 - Run NXP_GUI
 - Show readme
8. Then click **Finish** to complete the installation.



5.3 Launching the PF09 NXP GUI

When the KITPF09FRDMEVB kit is set up and the GUI is installed, follow the steps below to launch the GUI:

1. Click the Windows icon (bottom-left corner) and locate NXPGUI in the Windows all apps bar, then click the NXPGUI icon to launch the GUI.

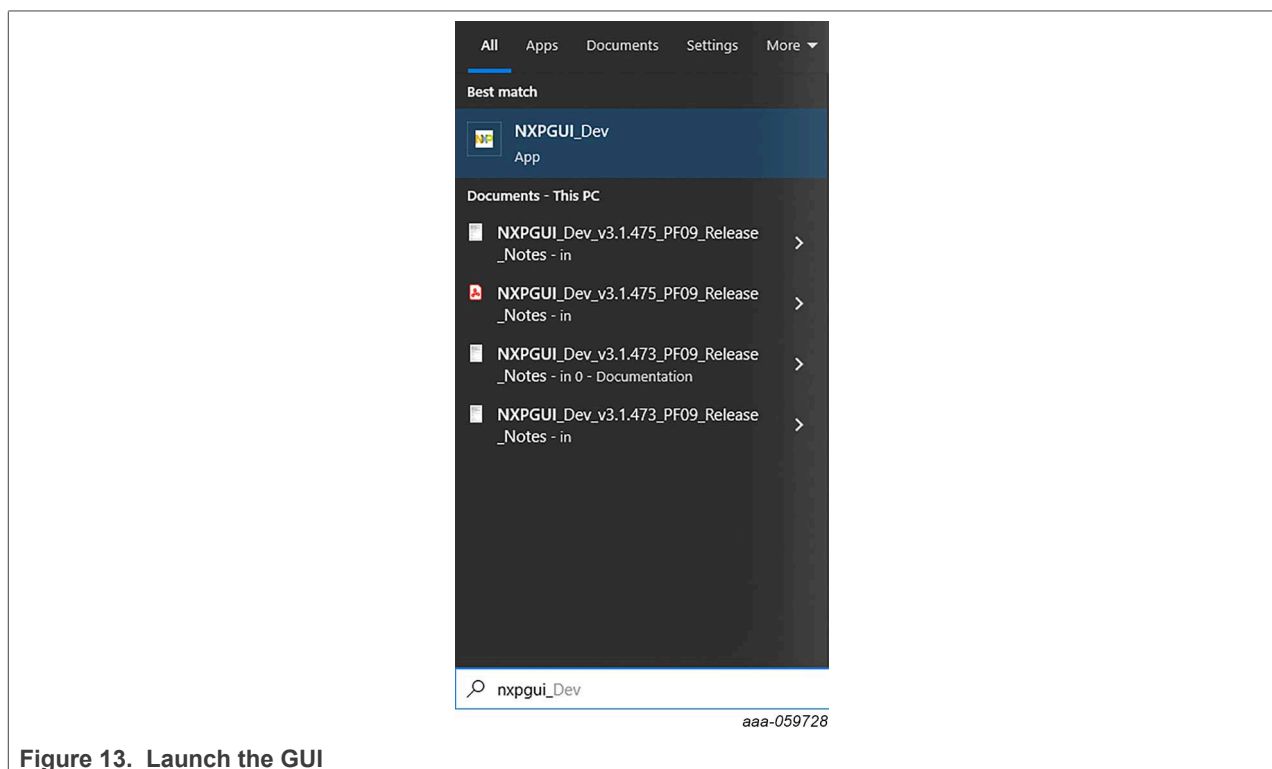
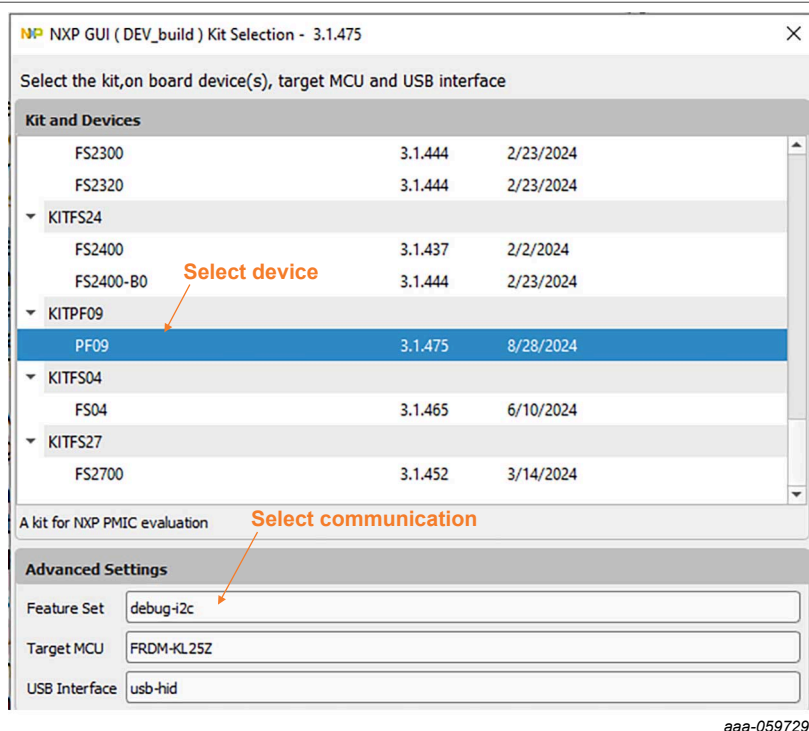


Figure 13. Launch the GUI

2. When the GUI opens, the first window to appear is the Kit Selection window. In the Kit Selection window, select the settings shown below. When finished selecting the settings, click **OK**



aaa-059729

Figure 14. GUI settings

Note: For PF09, select the corresponding device name.

For the PF09 part the communication protocol is I²C.

To avoid the Kit selection window on every launch, check the box "Use this configuration and do not ask again". The Kit selection window can be enabled/disabled through the File main menu item once the GUI is launched by checking/ unchecking the "Do not display GUI Kit selection at Start box".

6 PF09 NXP GUI

This section gives guidance on use of the PF09 NXP GUI.

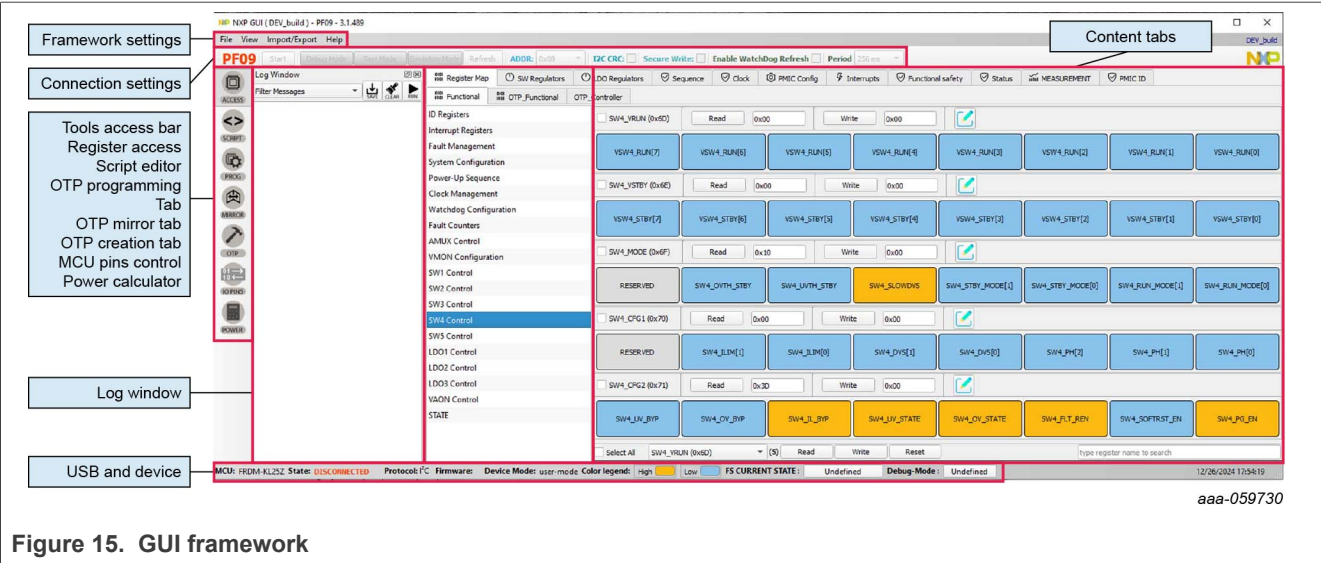
6.1 NXP GUI framework window

The framework window consists of the following sections:

- **Connection toolbar:** Used to start communication with the device, enter or exit Test/OTP modes, fix I²C frequency and I²C main address, enable watchdog.
- **Framework settings:** Manages file import/export and framework configuration.
- **Window log:** Reports USB and Device communication events.
- **USB and device status:** Indicates if USB or Device is connected or disconnected, shows communication protocol (I²C), shows firmware and GUI version, displays current device mode.
- **Tools access bar:** Provides quick access to the PF09 evaluation tools and features.

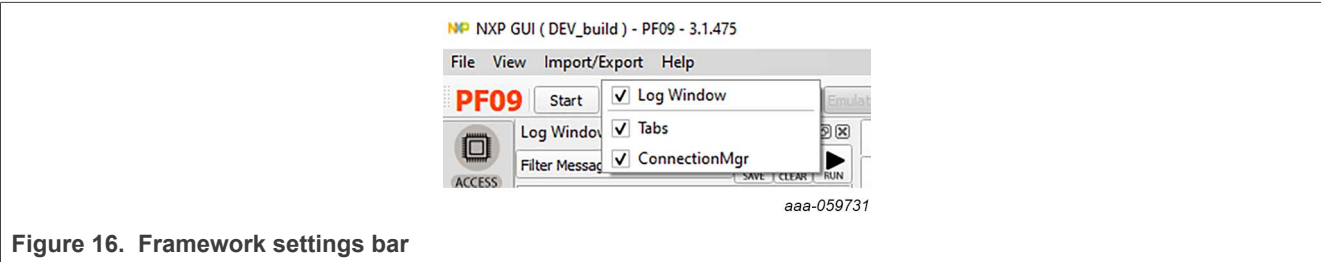
Note: Power tool is unavailable.

- **Tab content:** Shows the content of each tool or tab. There may be several tabs, boxes, or windows inside.



If the Log window, Tools access bar, or connection toolbar do not appear on the screen, right-click on the framework settings bar. This action displays three selection boxes (checked if the display is active):

- Log window
- The tab corresponds to the tools access bar
- Connection toolbar

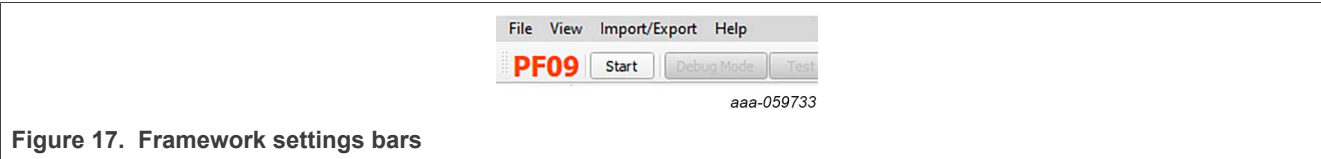


Note: Right click the Framework or Connection toolbar.

6.2 Framework settings bar

The framework settings section appears at the top left corner of the Framework window. It consists of four items:

- File
- View
- Import/export
- Help



6.2.1 File menu item

To choose to load/save a configuration and to choose to display or not the GUI Kit selection at **Start** or **Exit** the application.



Figure 18. File menu

- **Do not display GUI Kit selection at Start:** Check this box to always open NXP GUI as the current GUI version. Uncheck this box to display the product selection box at NXP GUI startup.
- **Exit:** Exits the NXP GUI application.

6.2.2 View menu item

The view menu contains the following options:

- **Display:** To enable or disable the Connection toolbar (enabled by default).

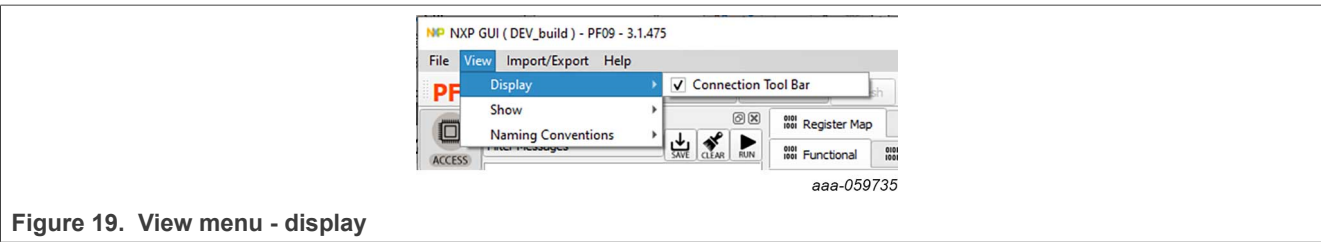


Figure 19. View menu - display

- **Show:** Allows the user to access various sections of the GUI and display the Log window.

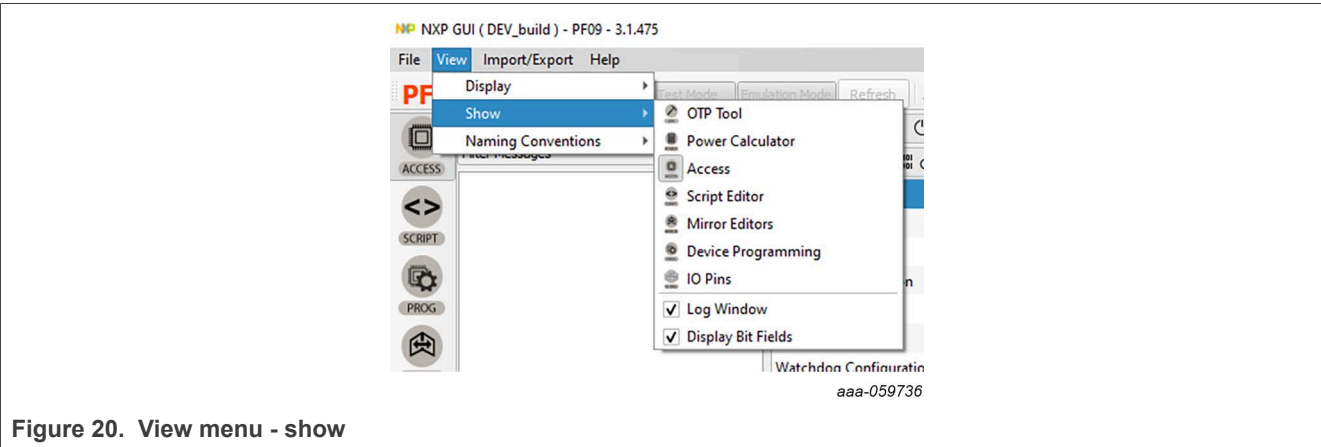


Figure 20. View menu - show

- **Naming conventions:** Allows the user to select **Friendly** or **Register** name display for OTP tool. Option enabled only when OTP tool is active.

The naming convention options are:

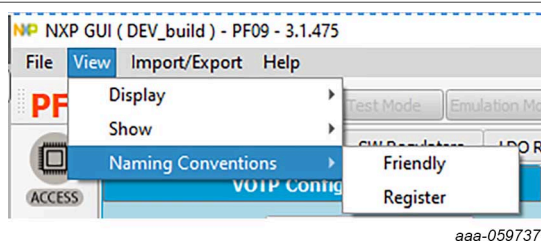


Figure 21. View menu - naming conventions

- **Friendly:** Register names are displayed as user-friendly names in the OTP tool.
- **Register:** Register names are displayed by their technical name in the OTP tool. Example: SW1 power-up sequence \Leftrightarrow OTP_SW1_SEQ.

6.2.3 Import/export menu item

The **import/export** menu item allows the user to manage the files needed for Mirror emulation, for the PROG tool, and for GUI configuration. This menu item is only active when the OTP tool has been selected. See [Section 6.5.2](#) for details.

- **TBB:** Exports the OTP configuration into a TBB script file that can be used to load the Mirror registers using SCRIPT tool. The same file can be used by the PROG tool to burn OTP fuses.

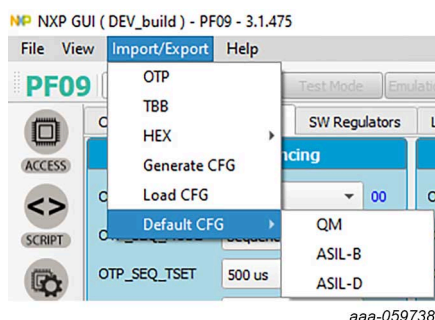


Figure 22. Import/export menu

- **HEX:** Outputs the OTP configuration in Intel-Hex (I-HEX) or Simple Hex (S-HEX) script file format.
- **Save CFG:** To save the current configuration as a CFG file.
- **Load CFG:** To load a previously saved configuration from a CFG file.
- **Default CFG:** To load a predefined OTP configuration in QM or ASIL B to use as a starting point.

6.2.4 Help menu item

The **Help** menu button contains links to additional information, displays GUI and firmware version numbers, and a glossary for acronyms.

- **Documentation:** Lists online NXP documentation related the PF09 GUI.
- **About:** Displays the version number of the GUI currently installed.

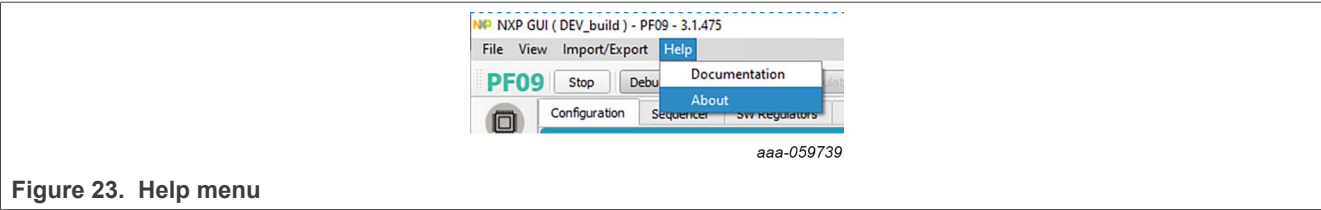


Figure 23. Help menu

6.3 Connection toolbar

The Connection toolbar menu is located directly below the Framework settings menu in the top-left corner of the Framework window.



Figure 24. Connection toolbar

Note: The Connection toolbar is not displayed if not selected in the Frameworks setting→View→Display menu item.

The Connection toolbar allows the user to start or stop communication with the device, enter, or exit Test mode and OTP mode, fix I²C frequency (depending on the chosen MCU communication protocol at start) and I²C main address, enable watchdog.

The Connection toolbar consists of the following items:

- **Start/stop:** To open or close communication with the device.
- **Mode:** To enter or exit Test mode, and exit OTP mode.
- **Main ADD:** To assign the I²C address to the device.
- **Enable watchdog refresh:** To enable/disable the Watchdog refresh.
- **Period:** To set the watchdog period.

6.3.1 Device connection

The device connection boxes appear first in the Connection toolbar menu.



Figure 25. Device connection – Start/stop

When the KL25Z MCU is not connected through the USB port, the State indicator in the USB and Status bar shows **Undefined**, the PF09 header text appears red, and the **Start** button is not available.

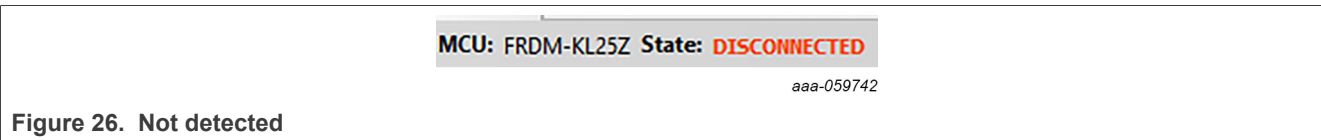


Figure 26. Not detected

After the USB cable is connected, the State indicator displays **Disconnected** and the **Start** button becomes available.



Figure 27. Disconnected

Click **Start** to start communication with the PF09.
At this point, the State indicator displays **Connected** and PF09 header text changes from red to green.



Figure 28. Connected

Usually, once connected, the next step is to load an OTP configuration and write it in the *mirror registers*.

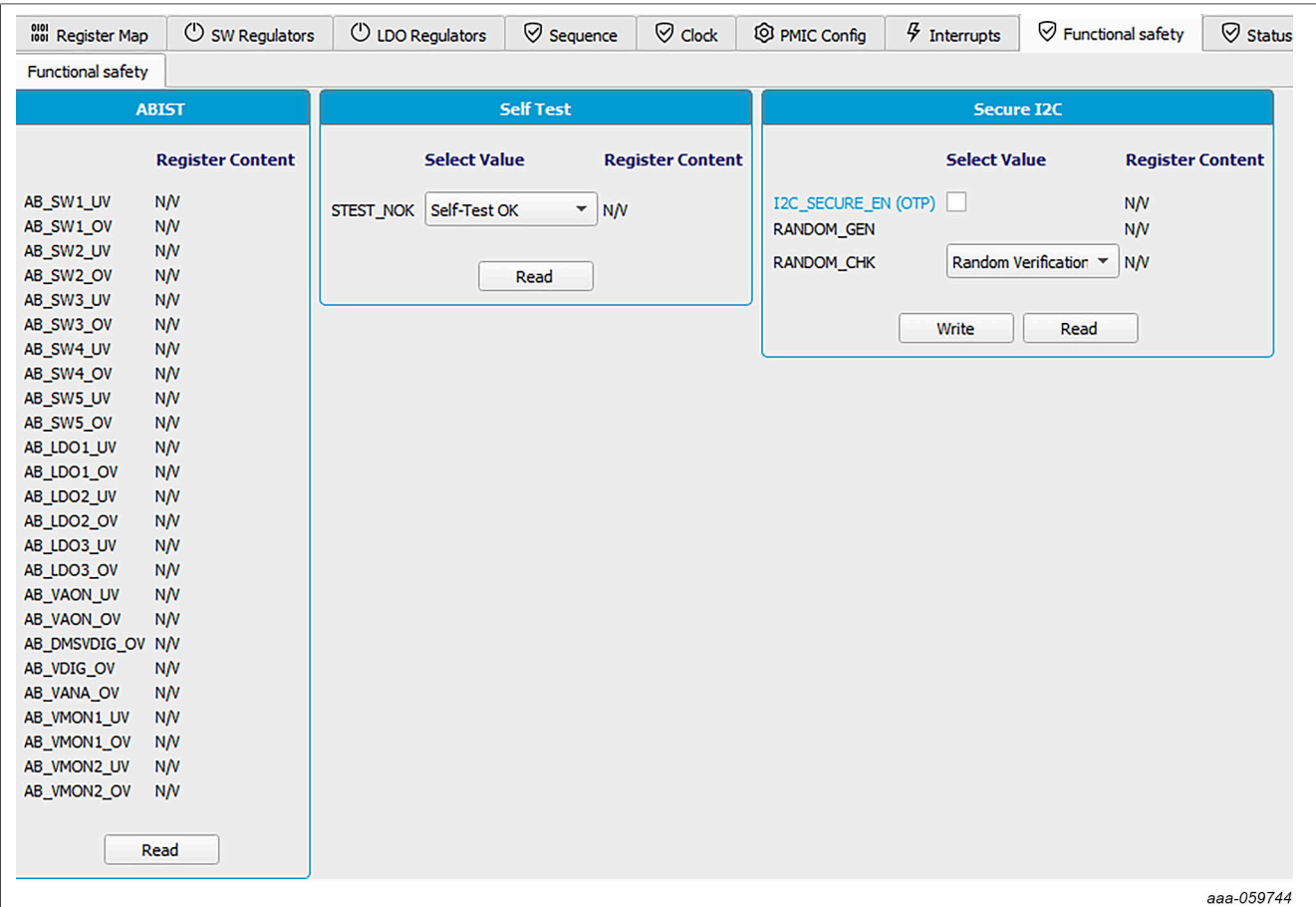


Figure 29. Watchdog enablement and configuration

6.3.2 I²C communication configuration

The PF09 supports both I²C communication protocol. I²C configuration settings for MCU side appear in the *connection toolbar*, allowing to choose the protocol applicable parameters.

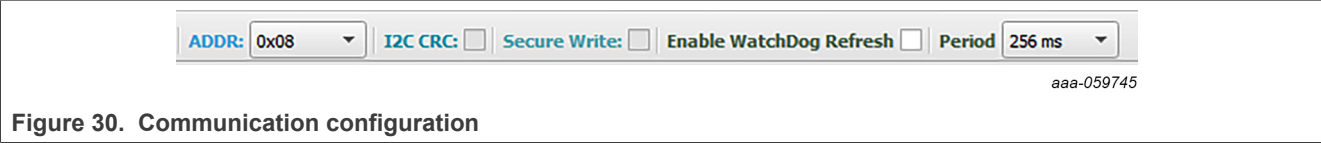


Figure 30. Communication configuration

6.3.3 Watchdog management

The PF09 provides watchdog monitoring with keys as a functional safety feature. Watchdog monitoring requests synchronize actions from the MCU. The watchdog feature can be disabled in QM version only. The watchdog is always enabled for an ASIL B part.

6.3.3.1 Watchdog enablement and configuration

On the PF09 side, when the part is QM, watchdog disablement is possible by OTP. Watchdog monitoring default configuration is done via I²C via the ACCESS tool.

6.3.3.2 Watchdog configuration on MCU side

On the KL25Z MCU side, actions are configured with the watchdog management boxes in the Connection toolbar menu.

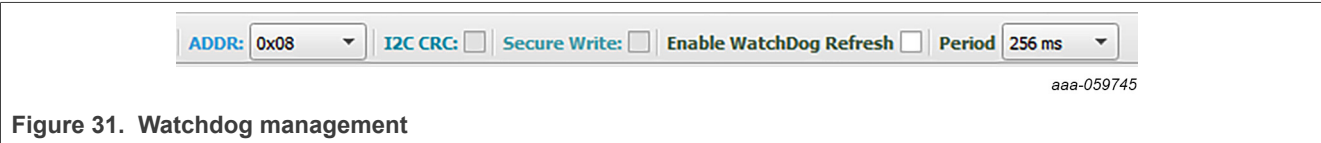


Figure 31. Watchdog management

The mechanism is fully operative when both PMIC and MCU actions are enabled and have matching configurations.

The steps for watchdog enablement are described by [Figure 32](#).

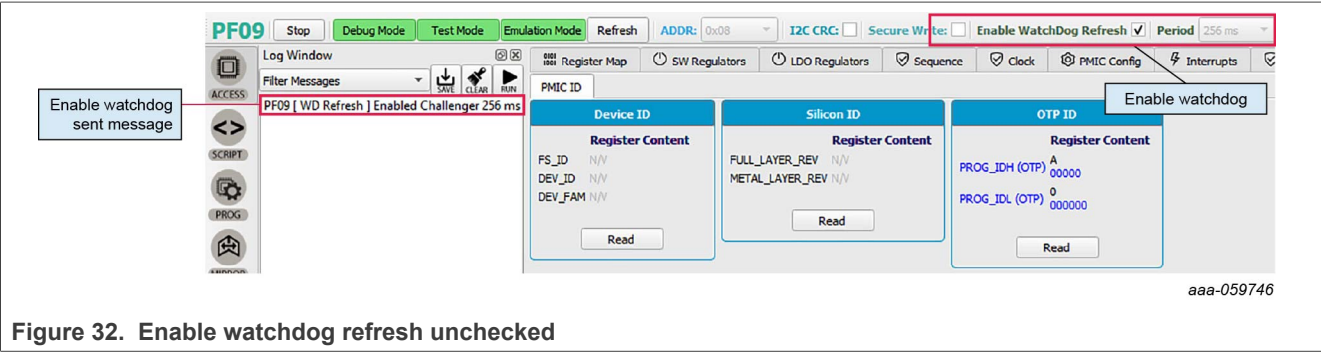
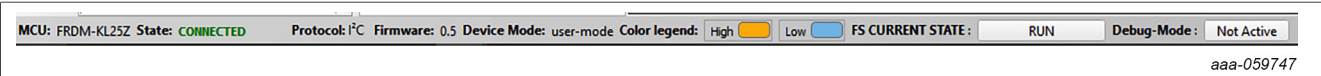


Figure 32. Enable watchdog refresh unchecked

1. Select the *watchdog* period via the *period* selection box in the *connection* toolbar.
 2. *Enable watchdog refresh* by checking the corresponding box to enable watchdog monitoring on the MCU side.
 3. A message is displayed in the *log window* with the selected period and type values.
- If the *period selection* box is unavailable, verify that *enable watchdog refresh* is unchecked.

6.4 USB and device status bar

The *USB and device* status bar is at the bottom of the *Framework* window. This toolbar gives information on the GUI and firmware version, on the USB connection status, and on PF09 active modes.




aaa-059747

Figure 33. USB and device status bar

6.5 Tools access bar

The *tools access* bar appears in a vertical row along the left side of the *Framework* window. The bar provides access to tools that implement various GUI functions. The *tools access* bar consists of nine items:

Table 11. Tool access bar

	ACCESS	Provides access to I ² C registers via Register map or thematic tabs
	SCRIPT	To create, open, save, and run scripts
	PROG	To manage OTP fuse-burning process
	MIRROR	Provides access to Mirror registers
	OTP	To create and save OTP configuration files, with customer and program details
	IO PINS	To read and set MCU I/O pins
	POWER	To compute power dissipation of the device in a given application

aaa-059748

Figure 34. Tool access bar

6.5.1 POWER

The POWER tool is used to compute the power dissipation of the device in a given application.

[Figure 35](#) shows how to use the POWER tool. Input values are selected the interface from keyboard inputs or selection boxes. Results are shown in the green boxes. Power dissipation graphs can be displayed from the interface using System or IC POWER dissipation buttons. *Load and save POWER configuration* buttons are used to resume the power dissipation calculation later, by saving and loading a text file.

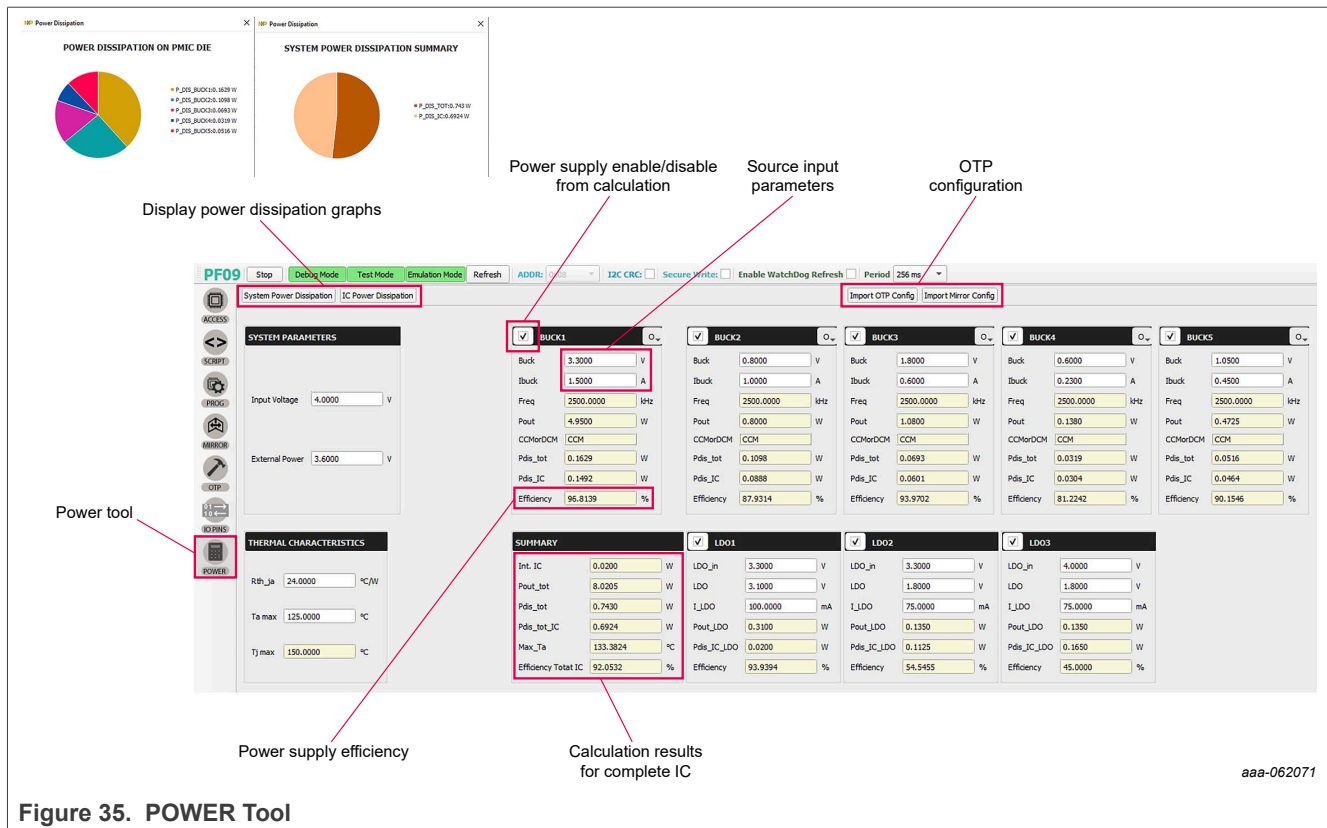


Figure 35. POWER Tool

6.5.2 OTP

The OTP tool is used to enter an OTP configuration. The OTP configuration can be saved as a CFG file or exported as a TBB file:

- The CFG file is used by the GUI to log all of the configuration information. The CFG file can be used to save an OTP configuration or load *mirror registers* with the MIRROR tool in *Debug mode*.
- The TBB file can be created with a .txt extension. The TBB file can be used to load the *mirror registers* with the SCRIPT tool in *Debug mode* or to burn OTP fuses using the PROG tool.

In the OTP tool, the displayed parameters differ depending on the selected device type (ASIL B or QM) in the program Details box. The OTP configuration is not addressed here. For information on OTP configuration contents, refer to the [PF09](#). For information on OTP and *mirror registers*, see [Section 7.6](#).

The OTP tool's main panel is divided into two windows:

- OTP parameters setting
- OTP details

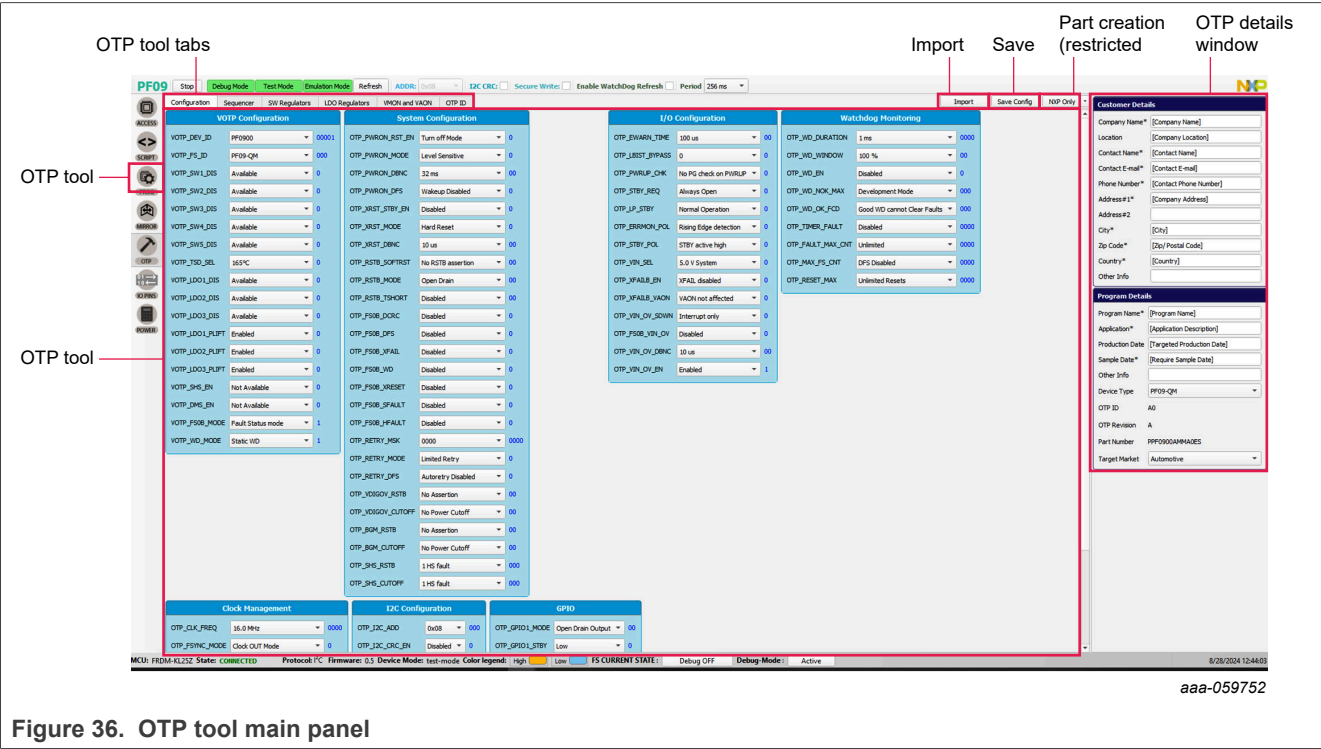
6.5.2.1 OTP parameters setting window

The OTP parameters setting section is organized into five tabs.

Note: The Functional Safety window differs depending on the selected safety level. Windows are the same for QM and ASIL B parts for all other tabs. Safety level can be selected in the Program Details box of [Section 6.5.2.1.1](#).

6.5.2.1.1 System configuration tab

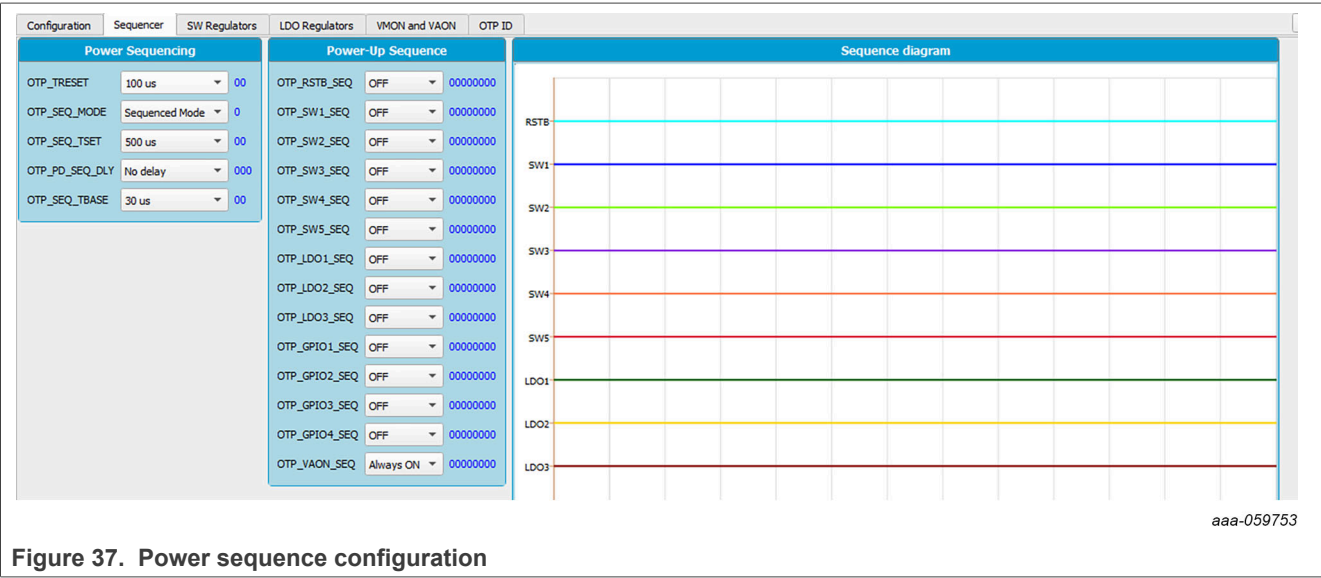
The *system configuration* tab provides a means of setting miscellaneous PF09 system configuration parameters, including clock, I/Os, and power-up sequence configuration.



6.5.2.1.2 System sequencer tab

The tab displays the set power-up sequence as graph in the *sequence diagram* box.

- **Power Sequencing box:** Sequence timing parameters definition.
- **Power-Up Sequence box:** Sequence definition.



6.5.2.1.3 SW regulators tab

The *SW regulators* tab allows the user to set OTP parameters for device outputs. This tab displays a simplified diagram of the selected configuration as a visual crosscheck.

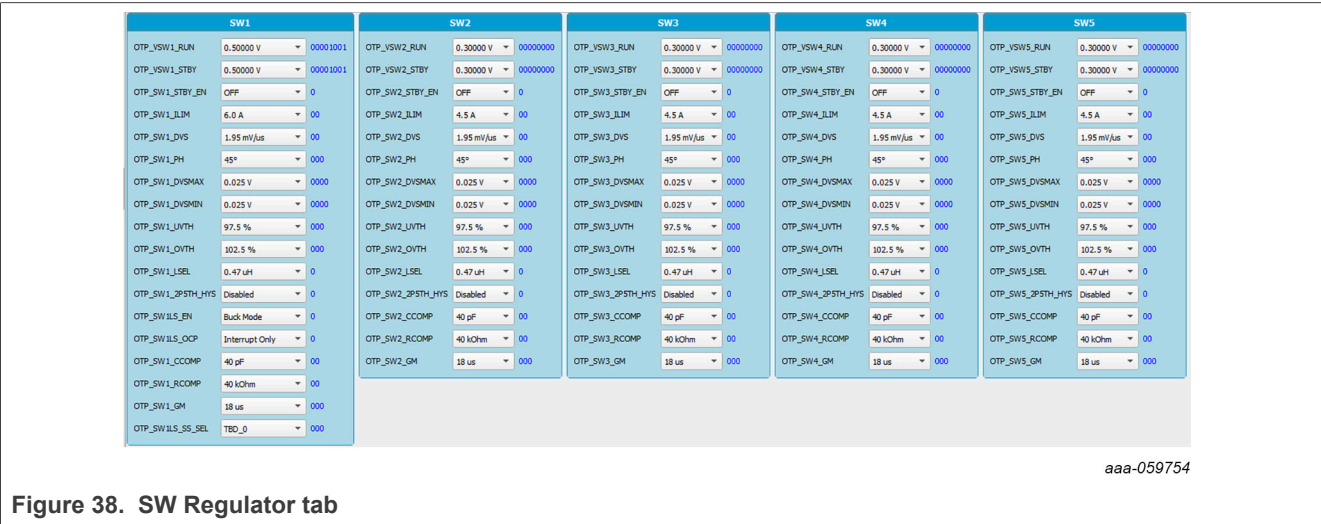


Figure 38. SW Regulator tab

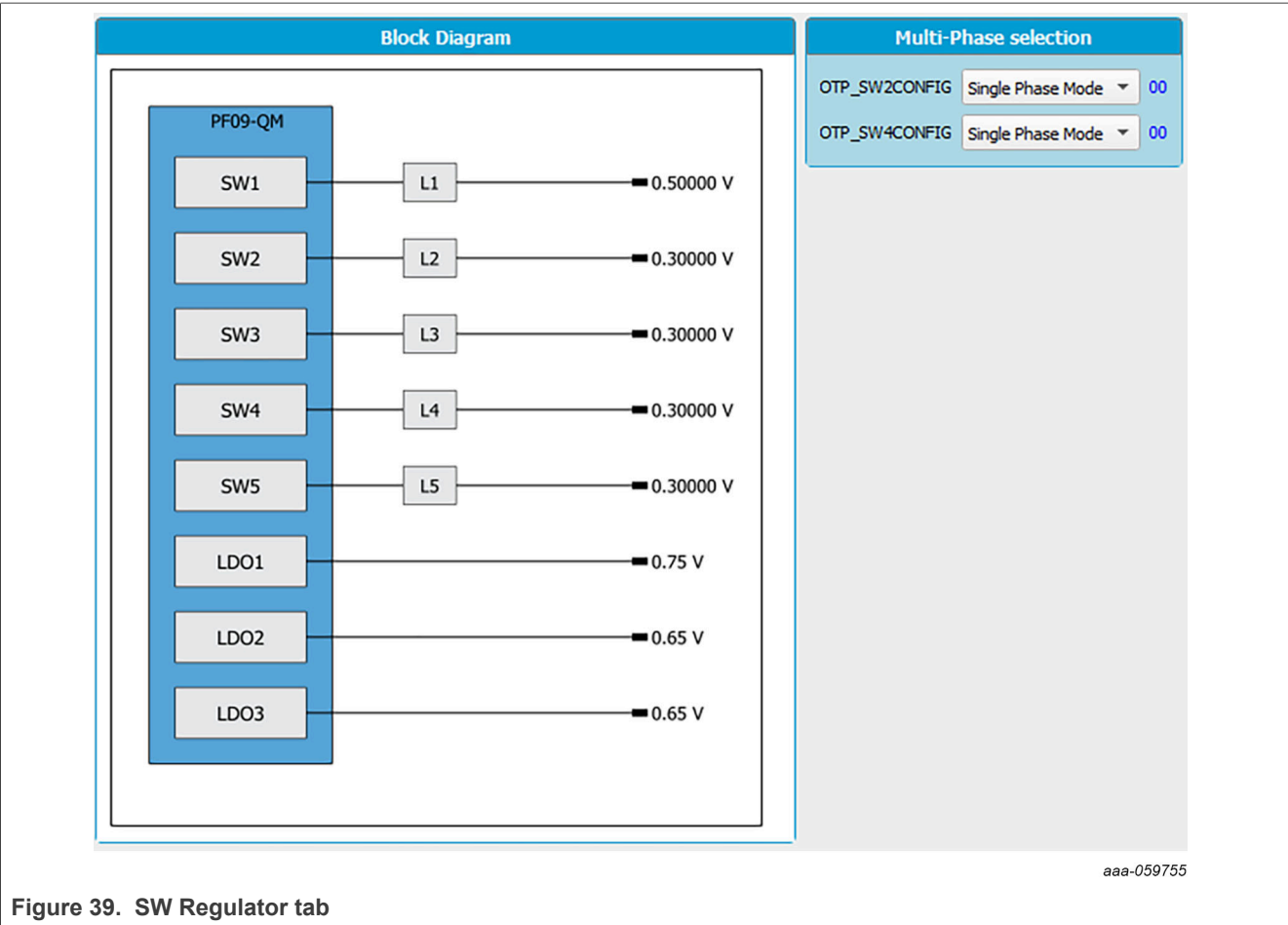


Figure 39. SW Regulator tab

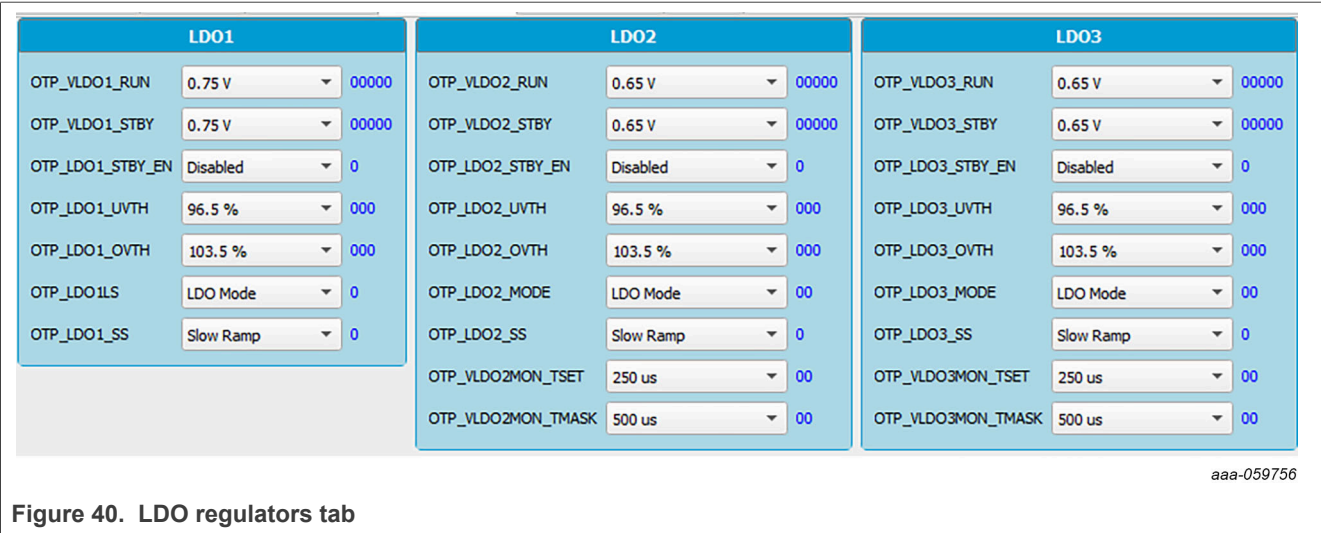


Figure 40. LDO regulators tab

6.5.2.1.4 VMON and VAON tab

The VMON and VAON tab allows the user to set OTP VAON-related parameters, such as under/over-voltage parameters, fault behavior and timer.

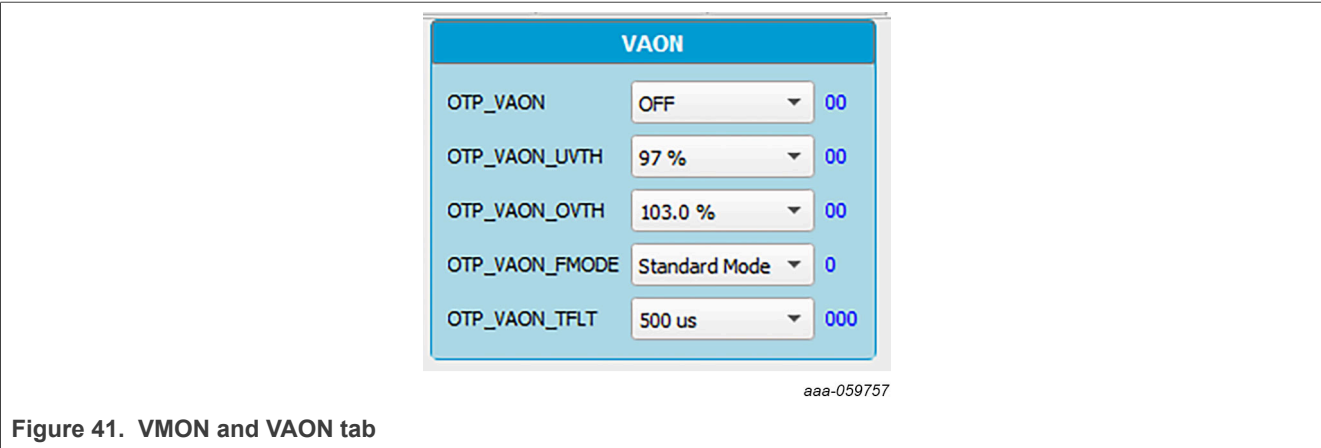


Figure 41. VMON and VAON tab

6.5.2.1.5 Program ID tab

The Program ID tab displays the OTP ID. Only NXP users can create an OTP ID.



Figure 42. Program ID tab

6.5.2.2 OTP Details window

The OTP Details window collects and stores information about the customer and the OTP version. All the information entered in this section will be part of the CFG and TBB files.

This section is organized into two boxes:

Customer Details

Company Name*

[Company Name]

Location

[Company Location]

Contact Name*

[Contact Name]

Contact E-mail*

[Contact E-mail]

Phone Number*

[Contact Phone Number]

Address#1*

[Company Address]

Address#2

City*

[City]

Zip Code*

[Zip/ Postal Code]

Country*

[Country]

Other Info

aaa-059759

Figure 43. Customer details

Note: Collects and displays customer contact information.

Program Details

Program Name*

[Program Name]

Application*

[Application Description]

Production Date

[Targeted Production Date]

Sample Date*

[Require Sample Date]

Other Info

Device Type

PF09-QM

OTP ID

A0

OTP Revision

A

Part Number

PPF0900AMMA0ES

Target Market

Automotive

aaa-059760

Figure 44. OTP program details

Note: In addition to comments related to the application, this window allows the user to: Select device type (see **Functional Safety** tab paragraph for details), display the OTP ID (set by NXP only), display the build part number (set by NXP only), select target market, either automotive or industrial

6.5.3 PROG

The PROG tool provides access to device programming configuration and tools for the OTP burning process.

Note: Use this tab cautiously, as a device can be programmed just twice.

The programming tool is available only in Test mode. The programming screen consists of three sections:

- Device programming configuration window
- OTP mode window
- Fuse box status window

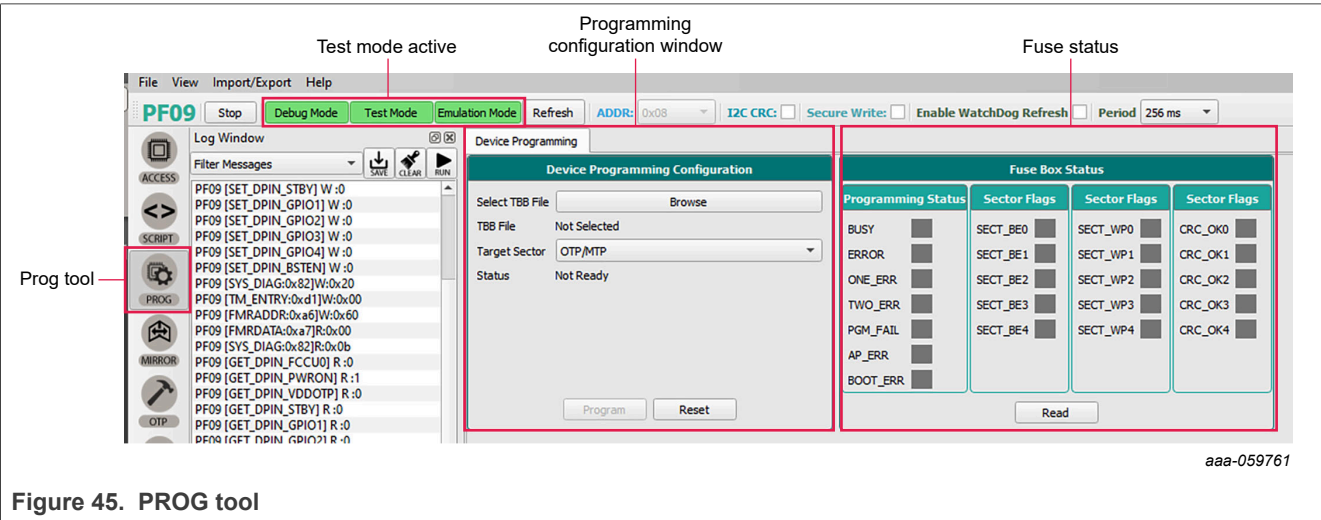


Figure 45. PROG tool

6.5.3.1 Device programming configuration window

From this window, the user can program an OTP operation from a saved TBB file. To program the part by fusing OTP, see [Section 6.5.3](#).

6.5.3.2 OTP mode window

OTP mode window allows the user to:

- Exit OTP mode by sending an I²C frame (by checking OTP mode exit box).
- Verify that the device is in OTP mode (condition: OTP 8 V applied to DBG pin at start-up).

6.5.3.3 Fuse Box Status window

The Fuse Box Status window shows the OTP fuse status. In the indicator boxes, blue indicates the section has not been programmed yet, orange indicates the section has been fused already.

As a reference, an empty part has the same Fuse Box status as shown in [Figure 91](#).

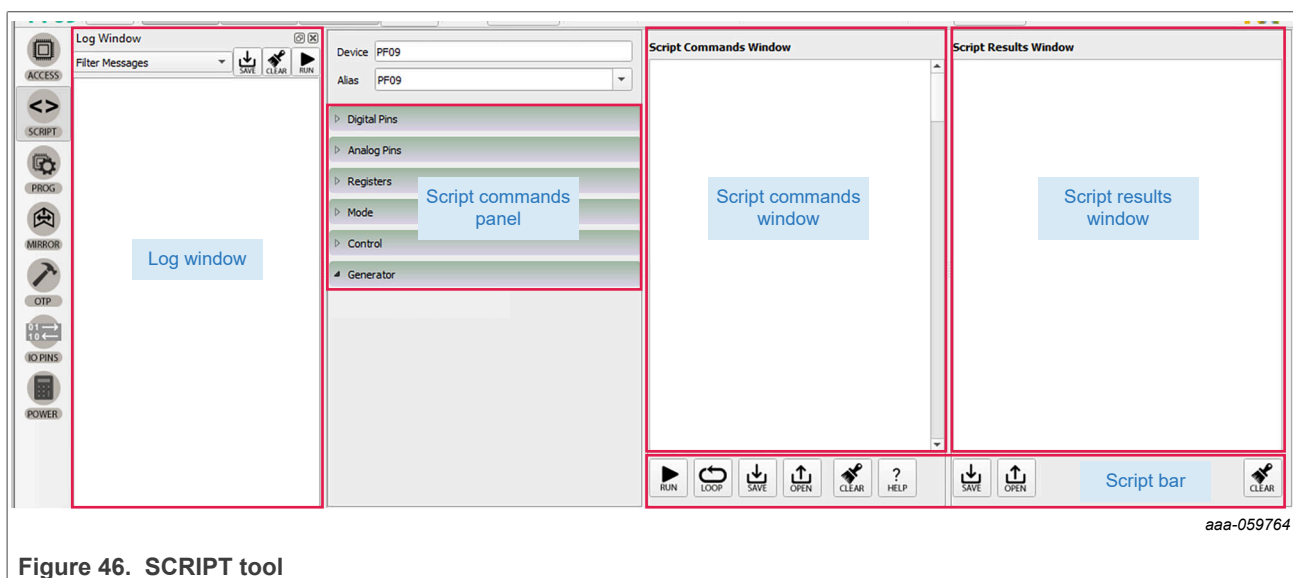
- **OTP** is customer OTP configuration.
- **MTP** is a duplicate of Sector 1 for second time programming. See [Section 7.6](#).

6.5.4 SCRIPT

The Script editor allows the user to create script sequences or to send existing sequences to the device. Commands include reading/writing individually to a register, to a digital pin, or to an analog pin. This tool allows the emulation of an OTP configuration.

The Script editor window consists of four sections:

- **Log window**
- **Script commands** (Window between Log Window and Script Commands Window)
- **Script window and its Script bar** (Under Script Command Window and Script Results Window)
- **Script results window**



6.5.4.1 Log window

The Log window lists events as they occur in real time when the script is executing. The Filter Messages box allows the user to limit log messages to certain events (Register Read, Register Write, Pin Read, Pin Write).

The Log window menu bar also contains buttons for saving the log contents to a file, clearing the log, or running the script in the Script Command window.

The Log window shows the CRC for each sent or received frame.

Note: The Log window content can be saved to a file, then opened as a Script to run it. See [Section 7.9](#).

6.5.4.2 Script commands panel

The Script commands panel allows the user to enter commands into the Script command window by clicking the appropriate command. Facilitated command entry ensures error-free syntax in the command. The commands are organized into functional categories. Opening a panel tab and selecting a specific pin or register makes the associated command appear in the Script command window.

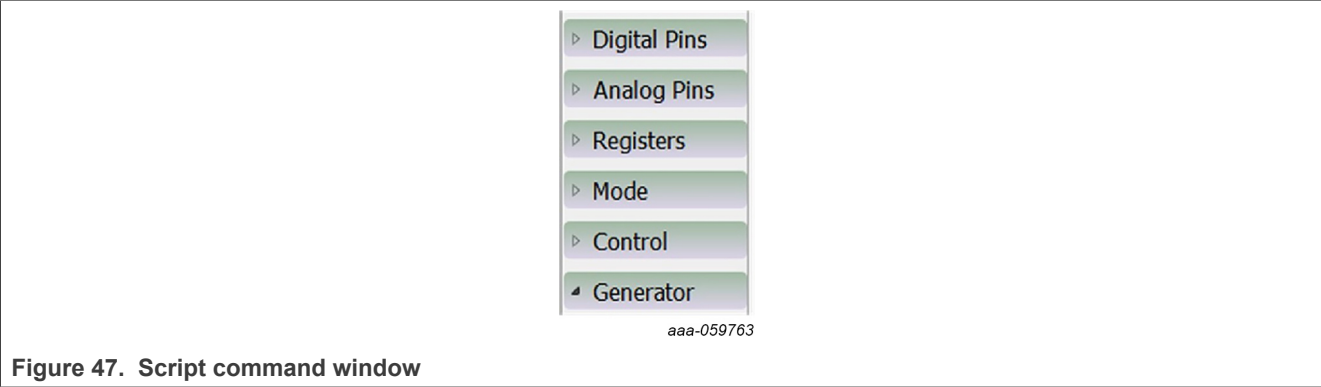


Figure 47. Script command window

- **Digital pins:** To enter a script command to read or write the value of the selected digital pin.
- **Analog pins:** To enter a script command to read the value of the selected analog pin.
- **Registers:** To enter a script command to read or write functional and safety registers.
- **Mode:** To enter a script command setting the desired mode.
- **Control:** To enter a script command to pause script execution (execution halts when the Pause command is encountered and a pop-up window appears, prompting the user to continue execution), to delay script execution (default is 300 ms, editable to any ms value in the Script Commands Window), or to exit script execution.
- **Generator:** To clear the content of the Script Command Window and enters a pre-prepared script sequence.

An INIT script example has been integrated to the Generator tab. The example provides a generic step-by-step procedure to initialize the device with a default configuration and transition to Normal applicative mode.

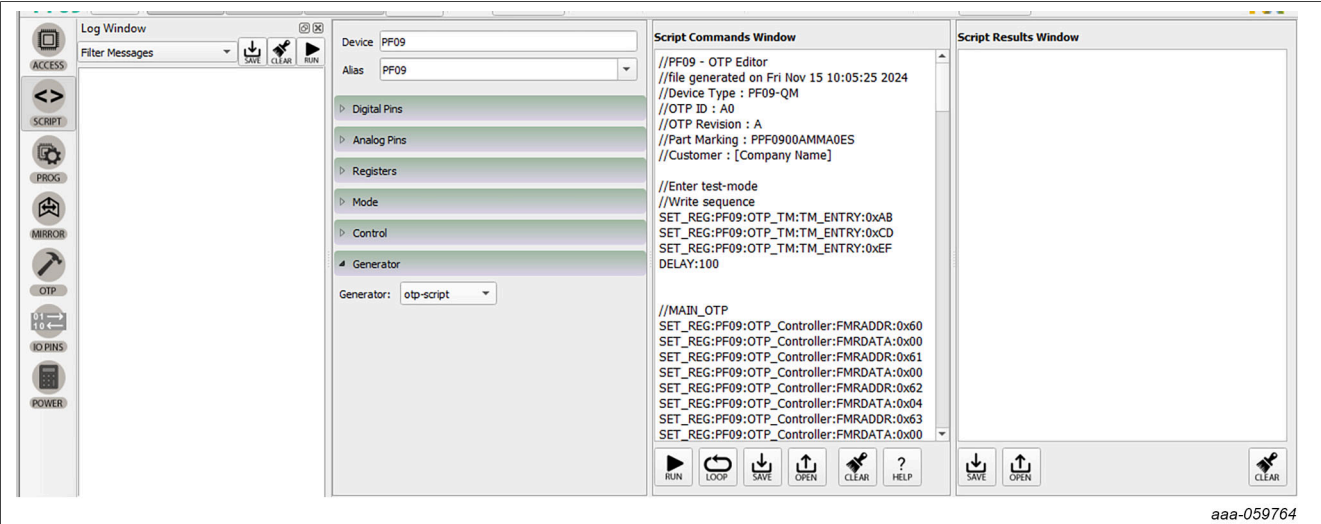


Figure 48. Generate an OTP – mirror registers writing script example (OTP-Script)

Note: *HELP* button in the Script bar gives information on Commands.

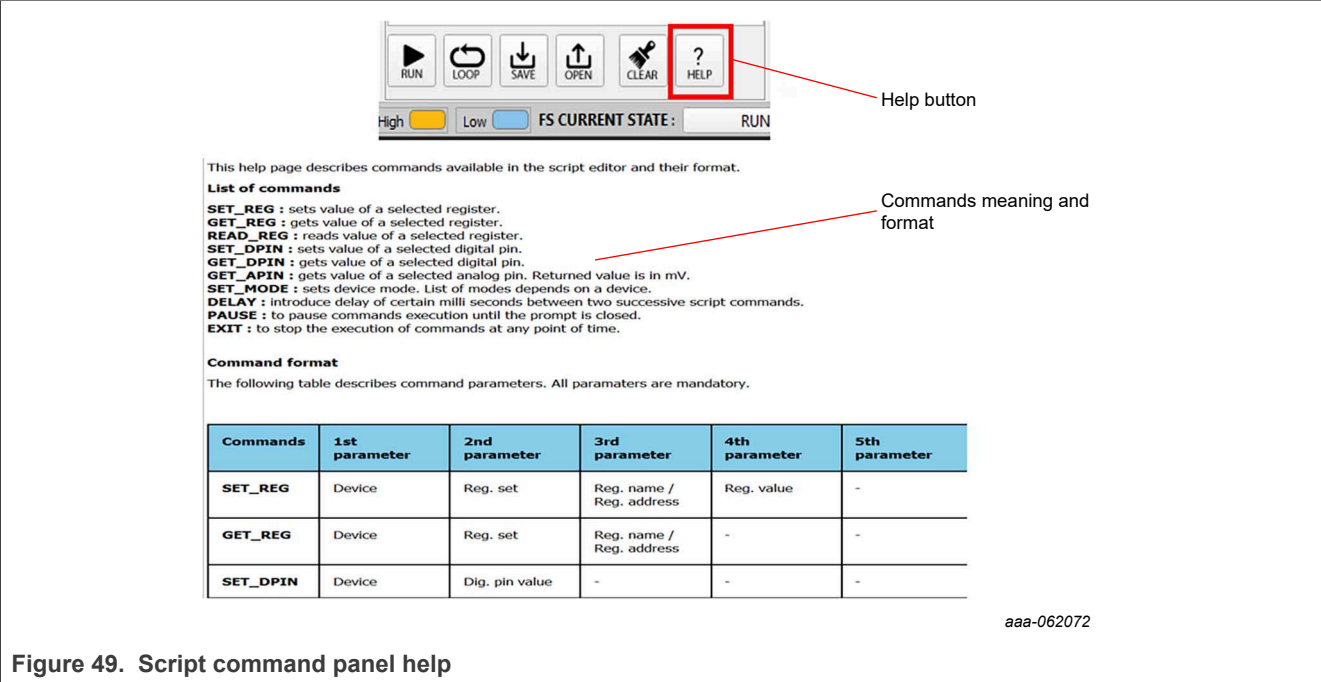


Figure 49. Script command panel help

All menu items work in a similar way. The example below shows a typical process using the Registers menu tab.

How to use the script tool: Click the Register tab brings up the parameters panel shown in [Figure 49](#). A **Write** operation to the CTRL1 register in the functional register group has been selected. The value 0x00 is selected as the value to be written to the register. Hit **Enter** with the cursor in the value field enters the well- formed command in the Script commands window.

To apply the commands on the Script Commands window, click **RUN** in the Script bar. The sent commands are displayed in the Log window and command results are displayed in the Script results window.

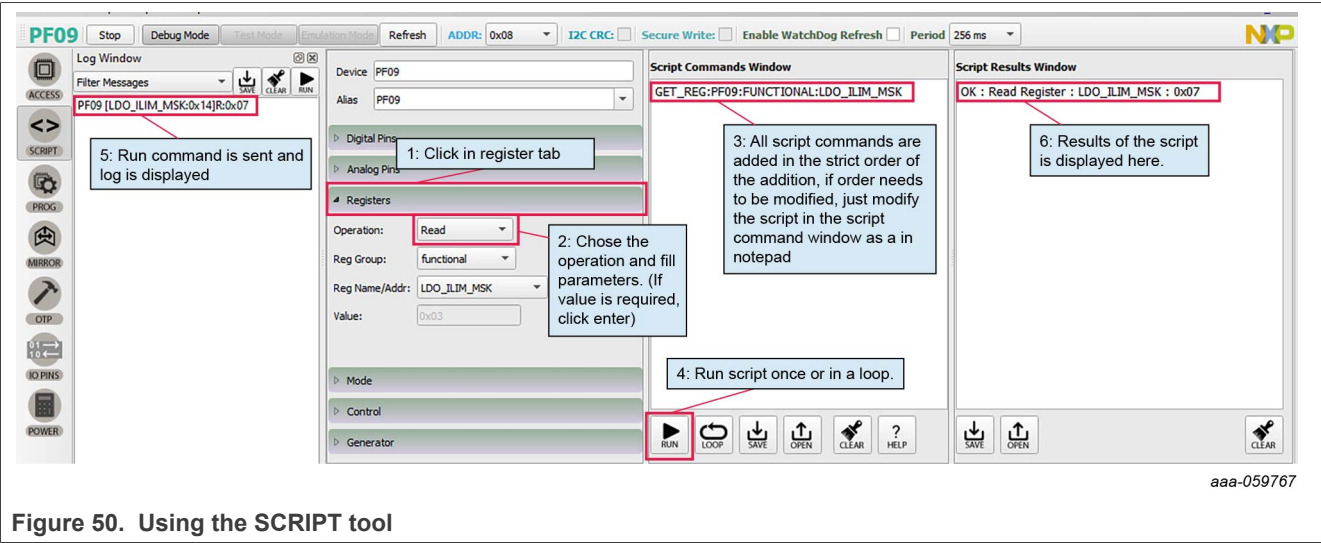


Figure 50. Using the SCRIPT tool

6.5.4.3 Script Commands window

The Script Commands window is the area where existing script files can be loaded in Test mode only and where script commands are entered, edited, and executed.

Another use of the Script tool is to replay a Log commands sequence, for example to run a routine. This specific use is detailed in [Section 7.9](#).

The Script bar at the bottom of the window contains the following six buttons:

- **RUN**: Initiates execution of the script sequence in the Script Command window.
- **LOOP**: Executes the script as a loop. Select **LOOP**, then click **RUN**.
- **SAVE**: Saves the content of the Script Command window as a .txt file that can be reloaded.
- **OPEN**: Clears the current content and loads a previously saved script into the Script Command window.

Note: The loaded file must have a .txt extension.

- **CLEAR**: Clears the current content of the Script command window.
- **HELP**: Shows a list of all script editor commands with their formats.



aaa-059768

Figure 51. Script commands window

6.5.4.4 Script results window

Script results window displays the results of an executed script. The menu bar at the bottom of the window contains the following three buttons:

- **SAVE**: Saves the content of the Script Results window as .txt file that can be subsequently reloaded.
- **OPEN**: Clears the current content and loads a previously saved result file into the Script Results window.
- **CLEAR**: Clears the current content of the Script Results windows.



aaa-059769

Figure 52. Script results window

6.5.5 MIRROR

The MIRROR tool provides access to all Mirror registers. Mirror registers are an emulation of OTP registers. Mirror registers can be read/written multiple times, whereas OTP registers can be burned just twice. In case of a power-on reset, the Mirror registers are reset to the default OTP configuration (empty if OTP sectors are not burned). Mirror registers can be read and written in Test mode only. See [Section 7.3.2](#).

Note: The MIRROR tool display tabs are similar to the corresponding OTP tool tab. To avoid confusion, the tab header background colors are different. The MIRROR tool tab header is purple. OTP tool tab headers are blue.

The MIRROR tool is available only in Test mode. Test mode loads require keys in order to have full access to Mirror registers. This tool allows the user to:

- Read and write Mirror register values.

- Load a CFG file into the Mirror registers and debug the configuration. For further details on CFG file preparation and parameters configuration, see [Section 6.5.2](#).

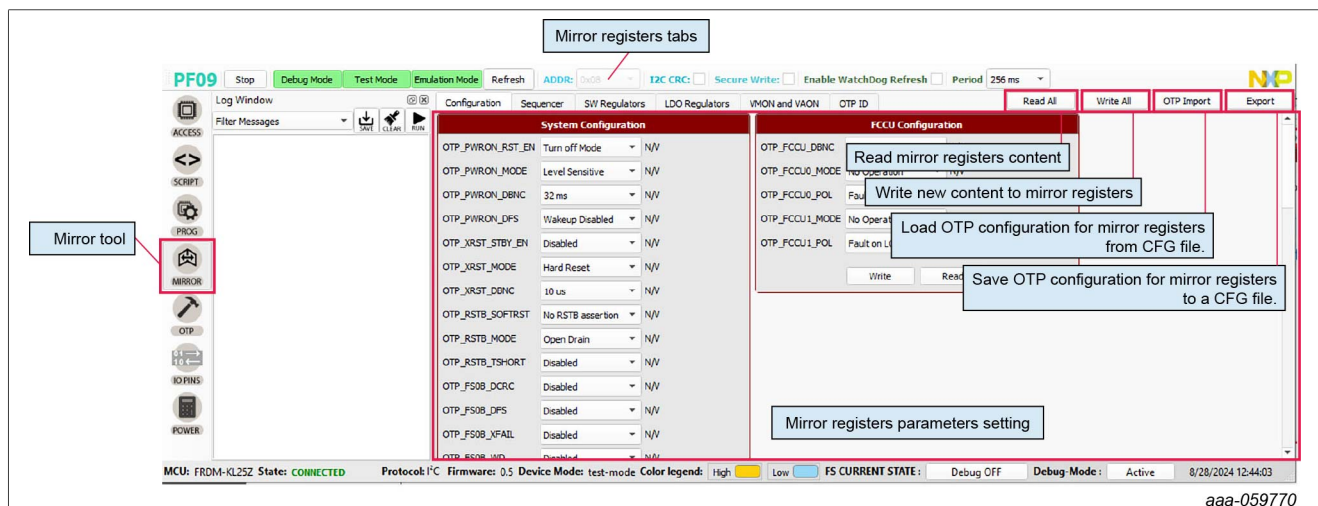


Figure 53. MIRROR tool

6.5.6 ACCESS

The ACCESS tool is the central tool for an evaluation session. This tool gives access to GUI functions that configure, monitor, and control the PF09 device during the evaluation session.

The ACCESS tool provides access all I²C registers, displayed either:

- in a Register Map format with direct access to register bits.
- in thematic tabs with a graphical and more readable view.

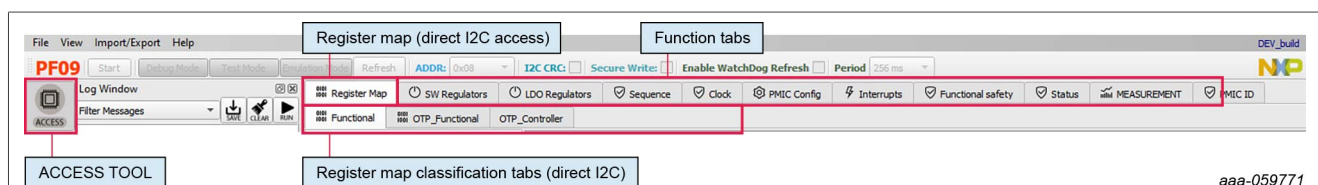


Figure 54. ACCESS tool

The tab content contains 11 tabs:

- Register map
- SW regulators
- LDO regulators
- Sequence
- Clock
- PMIC config
- Interrupts
- Functional
- Safety
- Status
- Measurement
- PMIC ID

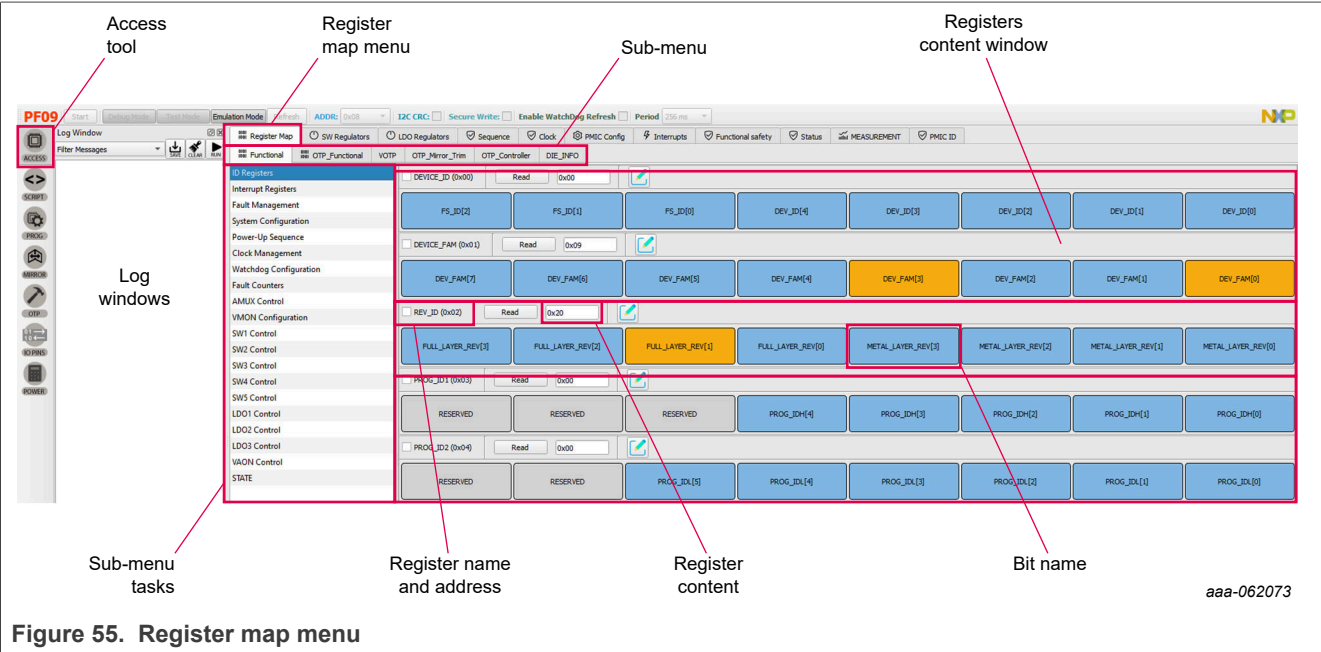
6.5.6.1 Register map

The Register Map tab allows the user to read or write the PF09 I²C registers, bit per bit.

Note: I²C registers are responsible for PF09 flexible device configuration, in opposition to OTP configuration, which is permanent once fuses are burned. The two levels of configuration work together and should be defined accordingly.

The Register Map is composed of three subtabs:

- ID registers
- Interrupt registers
- Fault management
- System configuration
- Clock management
- Watchdog configuration
- Fault counters
- VMON configuration
- SWx control
- LDOx control
- VAON control
- State



6.5.6.1.1 Modifying one bit content by clicking on the bit name

In the Registers Content window, the user can access the PF09 I²C registers. Two types of registers exist:

- Read-only registers (for example, Status) appear with a 'Read button' only,
- Read/Write registers (for example, System configuration, Regulators Control, etc.) appear with both a 'Read' and a 'Write' button.

The user can click a bit name to change its value, when the bit is writable.

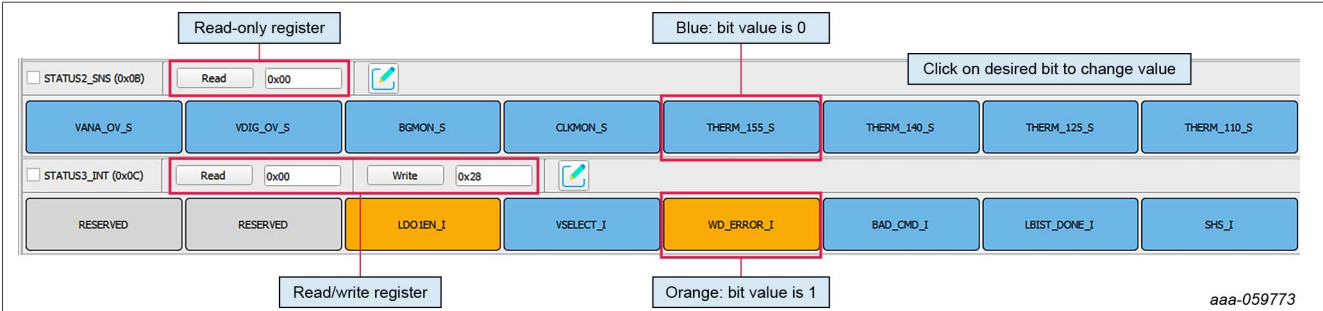


Figure 56. Register content window

6.5.6.1.2 Accessing one register content using Read and Write buttons

In the Registers Content window, the user can read and/or write the PF09 I²C registers using the Read and Write buttons.

To **read** the content of one register:

- Click **Read** next to the corresponding register name,
- The current register content is displayed as a hexadecimal value next to the Read button. To **write** the content of one register:
- Enter the desired register value as a hexadecimal value in the box next to the Write button.
- Click **Write** next to the corresponding register name.
- As a crosscheck, the current register value can be accessed by clicking **Read**.

Note: Click Read to get the register value. Click Write to change the register value.

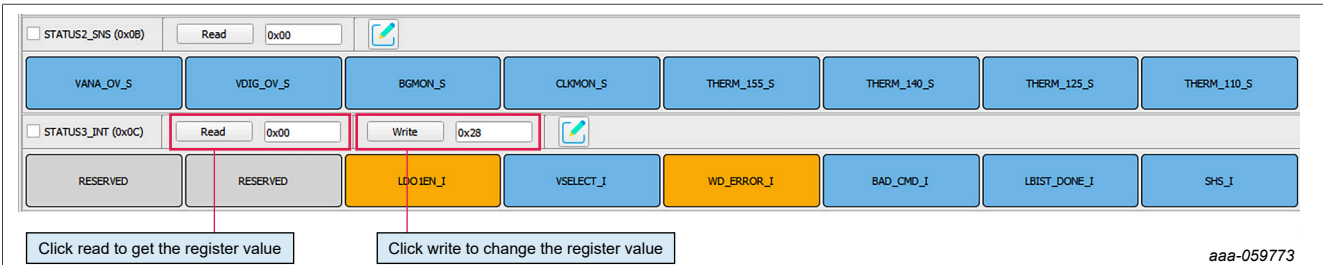


Figure 57. Accessing one register content using Read and Write buttons

6.5.6.1.3 Accessing one register content using Bit-Map Dialog

In the Registers Content window, the user can read and/or write the PF09 I²C registers using the Bit-Map Dialog window.

Clicking the **Green Pencil** next to the corresponding register name opens the Bit-Map Dialog window and shows the name and description of all of the register's bitfields.

The Bit-Map Dialog window:

- Allows the user to change bit values from selection boxes on the left side
- Displays the current register content on the right side.

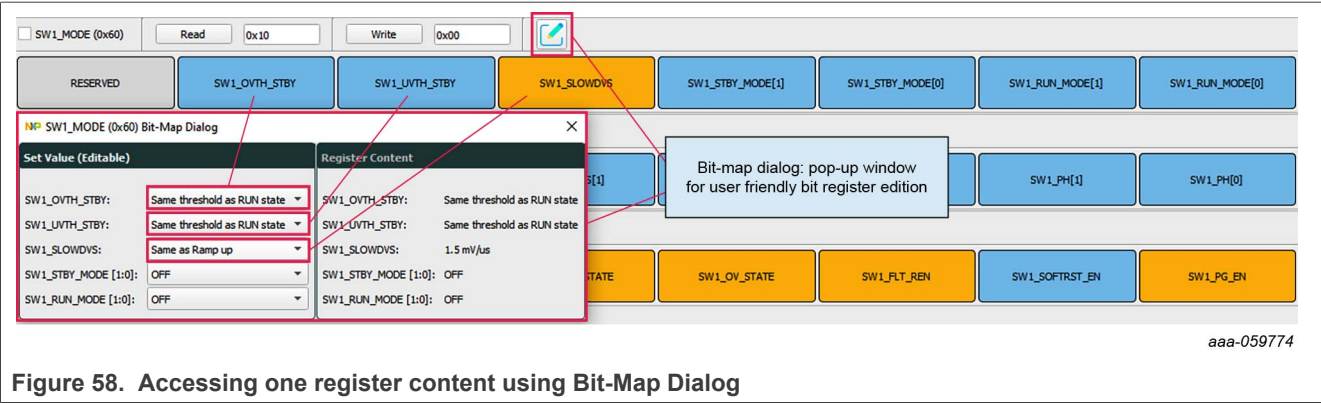


Figure 58. Accessing one register content using Bit-Map Dialog

6.5.6.1.4 Modifying multiple registers using the lower Read/Write/Reset bar

In the Registers Content window, the user can read, write, and/or reset multiple PF09 I²C registers at a time using the lower Read/Write/Reset bar.

- Checkboxes allow the user to select the registers to be read or written.
- Selecting the Select All checkbox allows the user to simultaneously act on all the registers in the Register subtab.
- Read, Write, and Reset buttons allow the user to act on the previously selected registers. The Reset button switches all the bits in the register to 0.

Navigating in the Registers content in the Register subtab can be facilitated using the selection box in the bar.

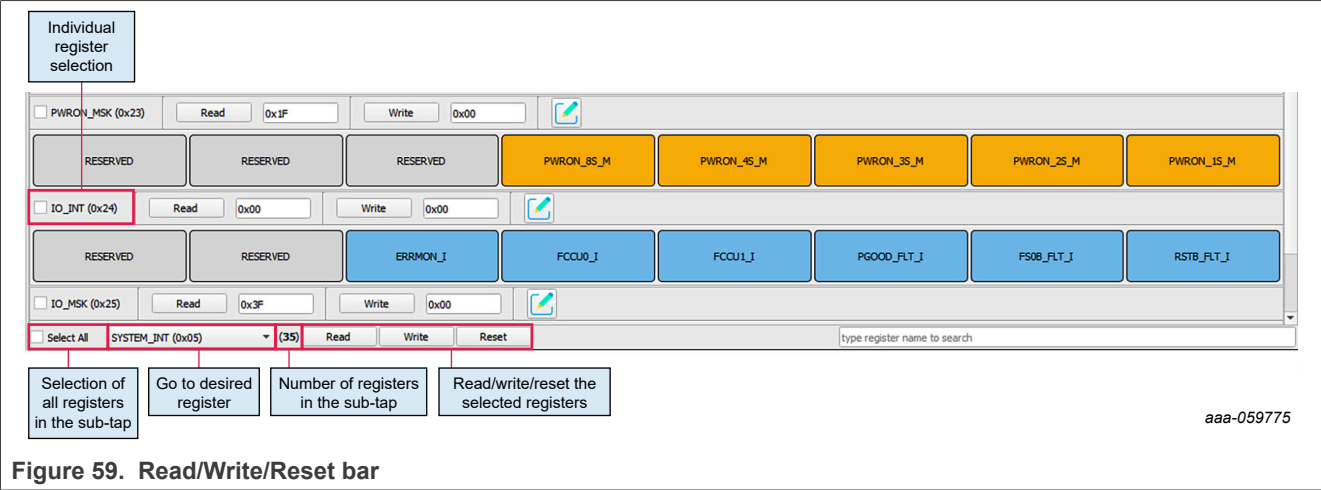


Figure 59. Read/Write/Reset bar

6.5.6.2 SW Regulators

The SW Regulators Tabs allows the user to read or write the parameters related to the Switchers configuration.

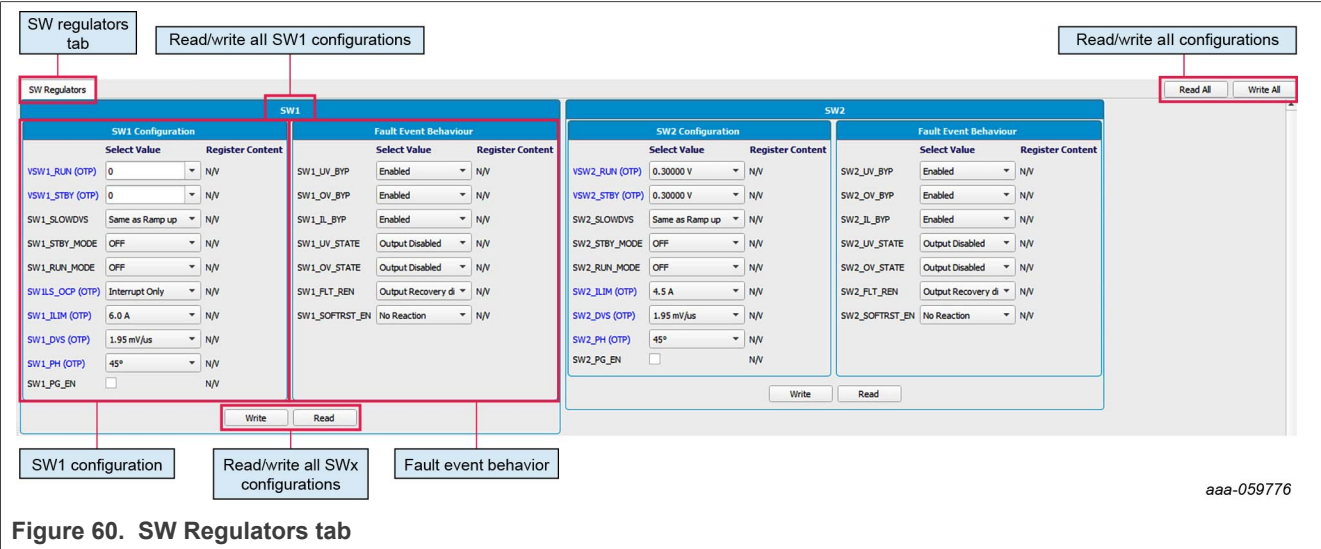


Figure 60. SW Regulators tab

- **SWx configuration:** To choose the switcher x configuration for Run, stand-by, etc.
- **Fault Event Behavior:** Configuration related to the Switcher Fault behavior.

6.5.6.3 LDO Regulators

The SW Regulators Tabs allows the user to read or write the parameters related to the Switchers configuration.

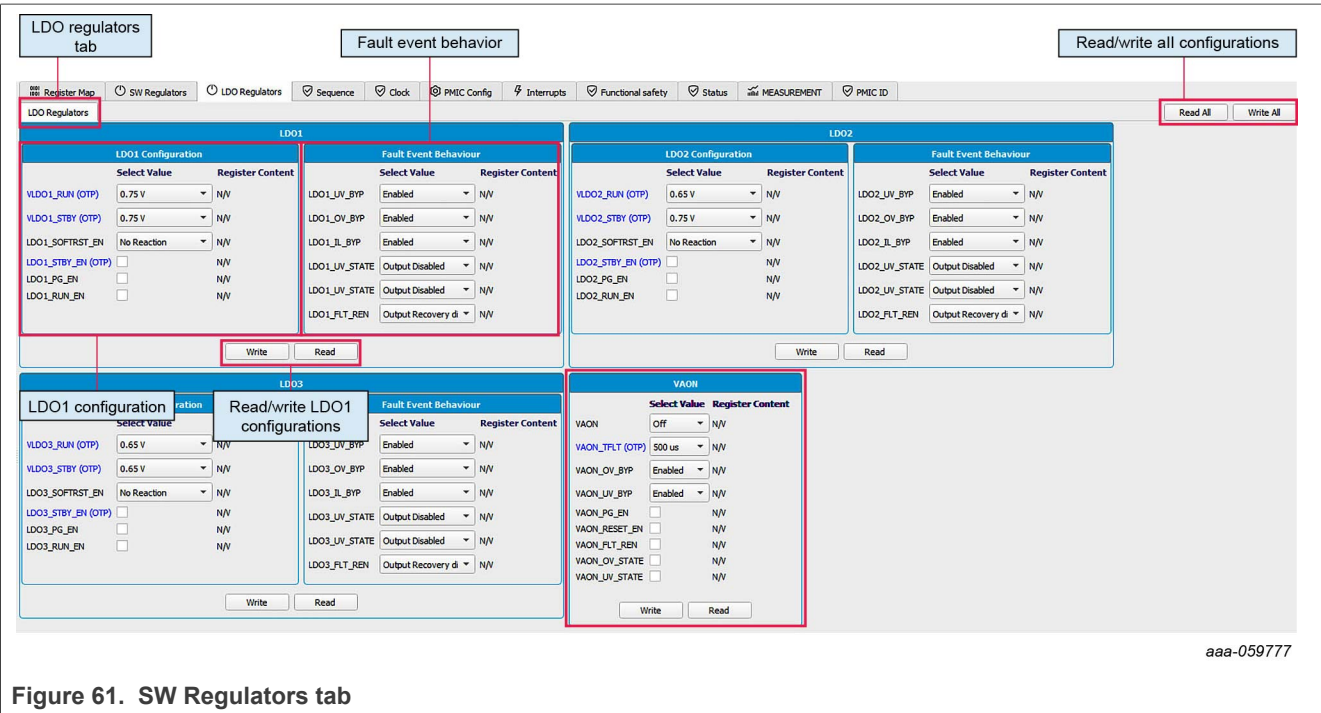


Figure 61. SW Regulators tab

6.5.6.4 Sequence

The Sequence Tab provides all configuration required for sequencing the device.

- **Power Sequencing window:** Timing parameters
- **Power Up Slot window:** Power and monitoring sequence

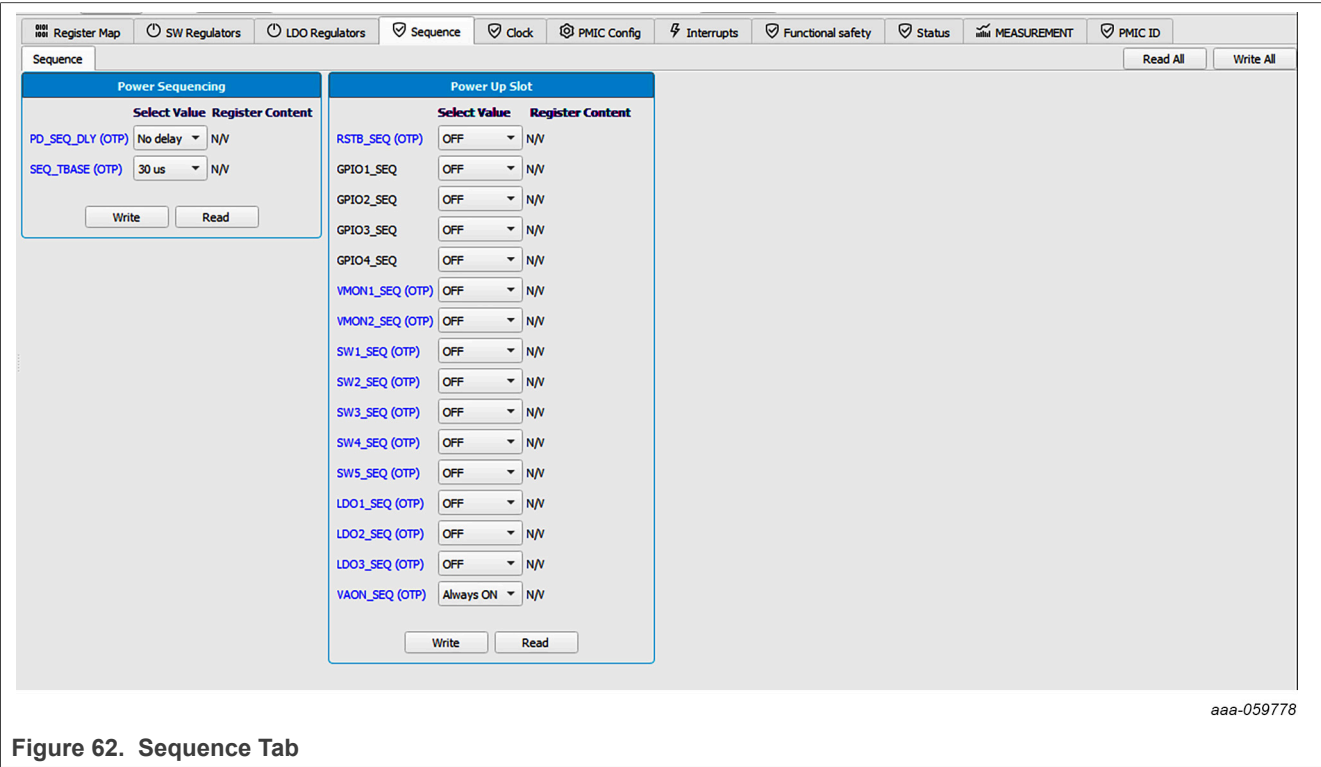


Figure 62. Sequence Tab

6.5.6.5 Clock tab

The Sequence Tab provides all configuration required for external synchronization or synchronization when using more than once device.

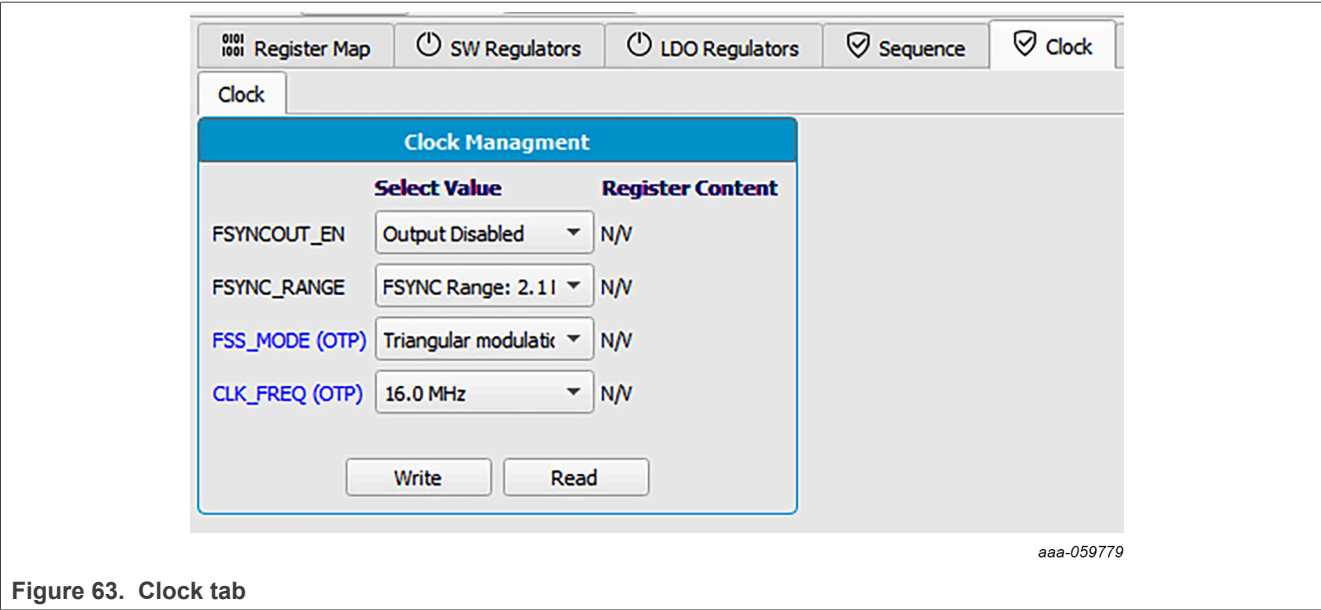


Figure 63. Clock tab

6.5.6.6 PMIC Configuration Tab

The Sequence Tab provides configuration for the Watchdog, VIN Overvoltage, multiplexed functionality and input monitoring (FCCUx).

- **AMUX window:** AMUX
- **VIN Over_Volatage lockout window:** VIN MON
- **WD window:** Watchdog
- **Debounce Monitoring and FCCU Monitoring windows:** FCCUx

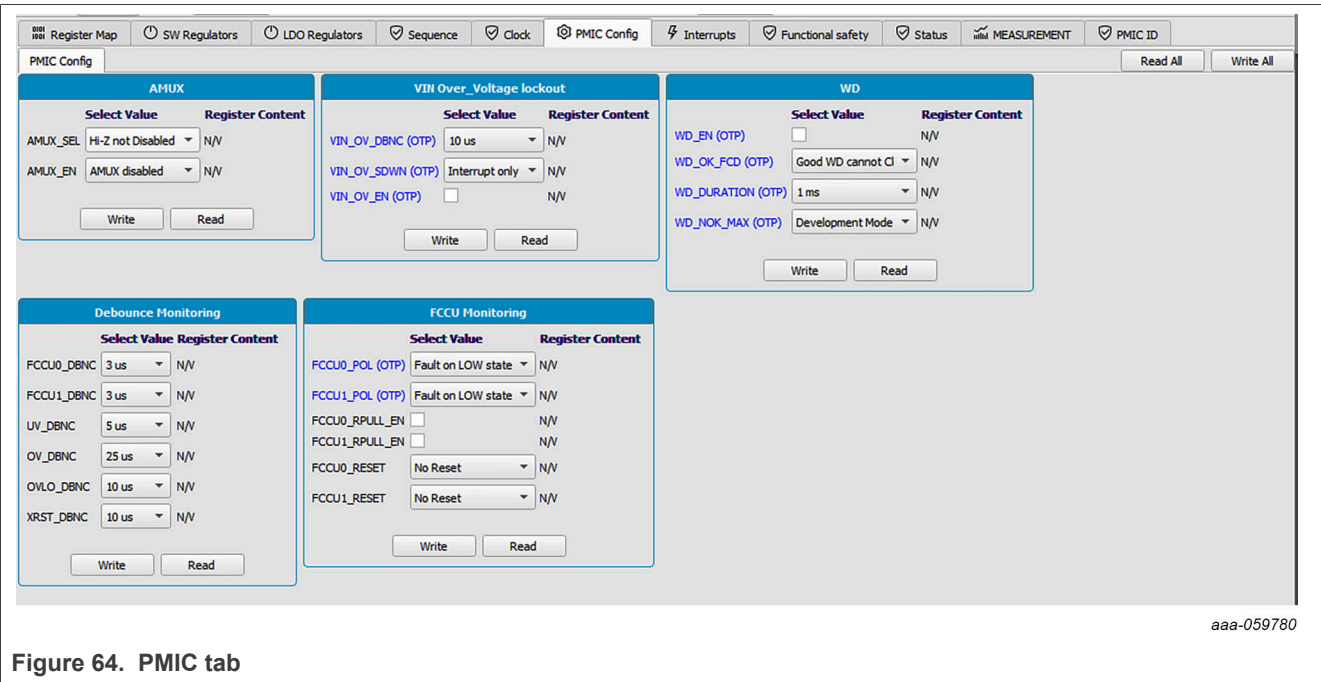
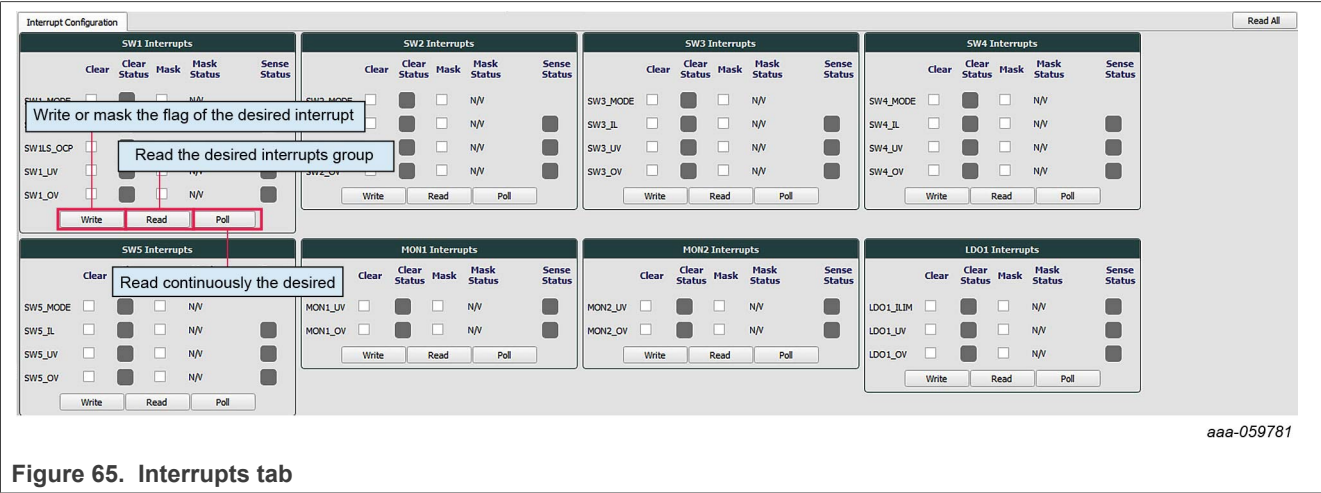


Figure 64. PMIC tab

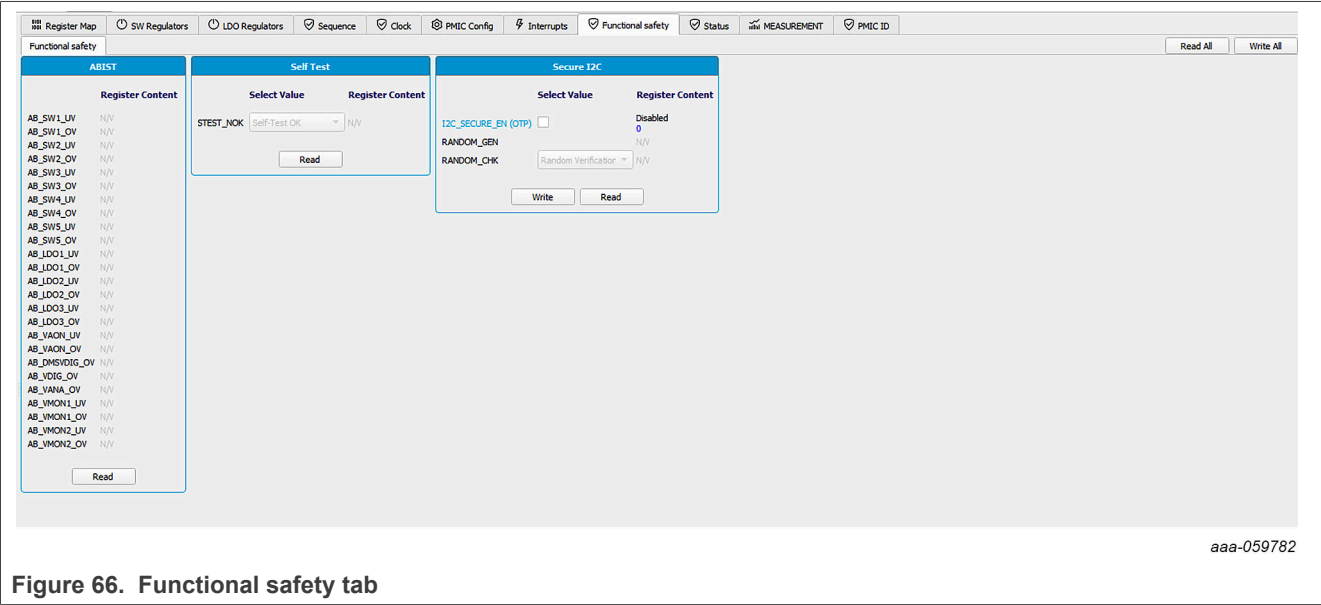
6.5.6.7 Interrupts

The Interrupts tab allows the user to read All Flags related to Interruption, both masked and unmasked.

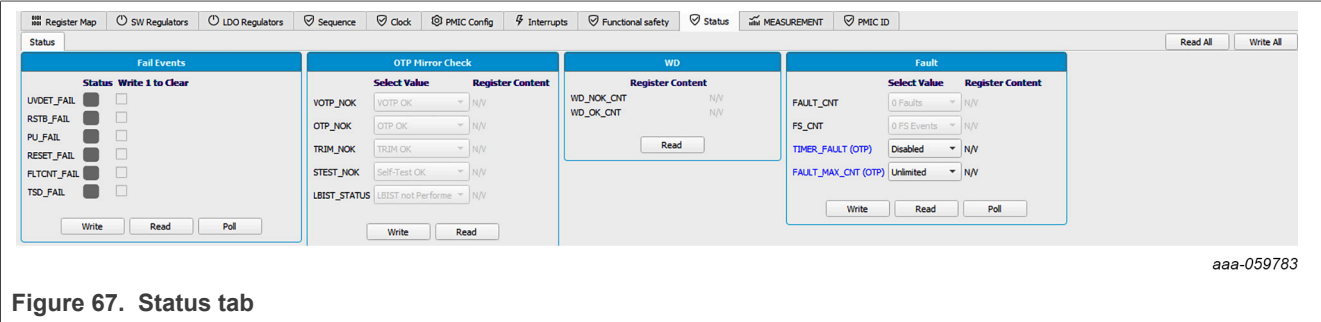


6.5.6.8 Functional safety

The Functional Safety tab allows the user to carry out the safety diagnosis by reading the register content. The Functional Safety tab allows the user to read the ABIST Flags and observe the ABIST status.



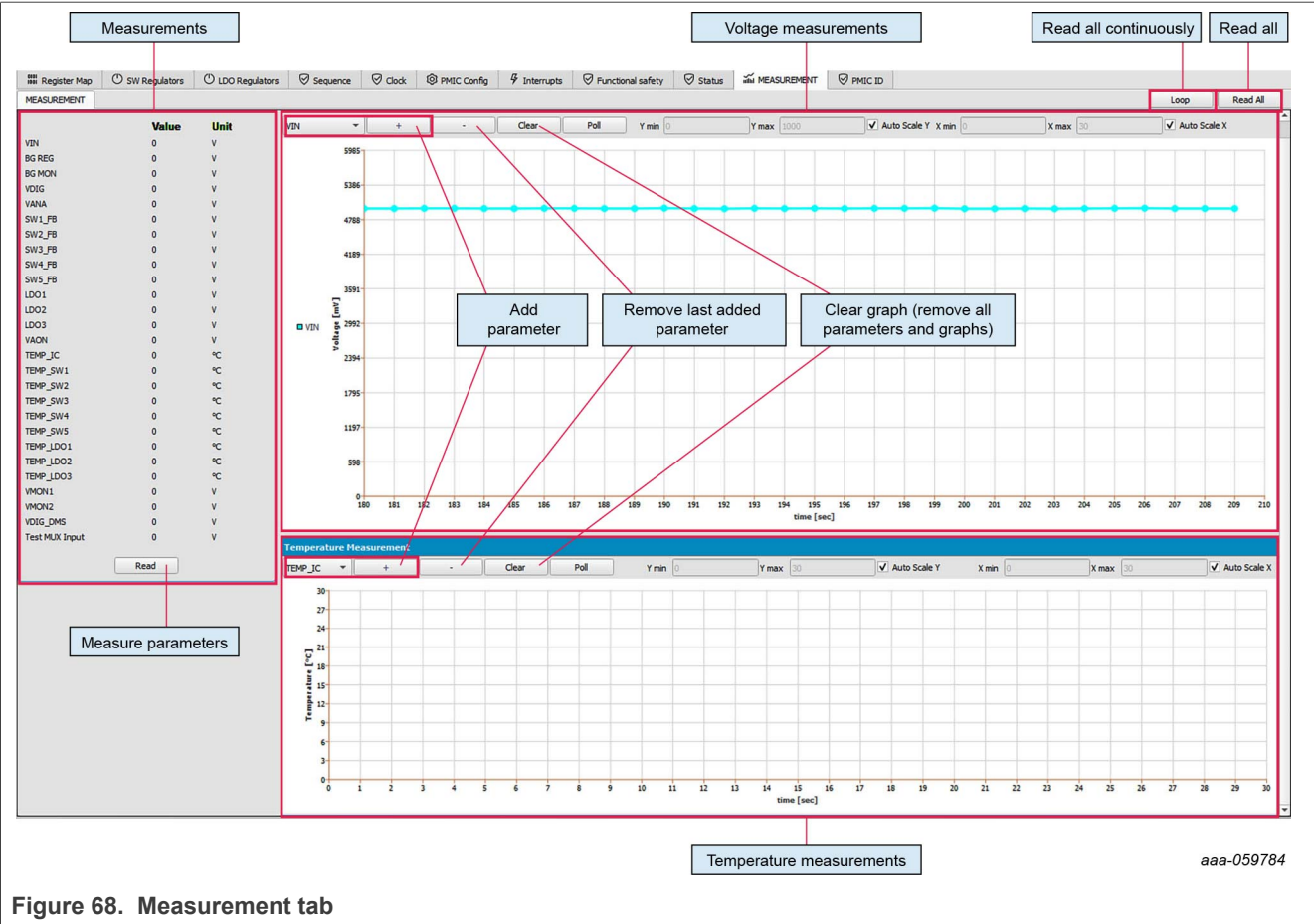
6.5.6.9 Status tab



6.5.6.10 Measurement Tab

The Measurement tab allows the user to measure voltage levels and temperature values of multiple key locations from onboard sensors. The Measurement feature uses one ADC to successively measure multiple points. The Measurement feature must be enabled beforehand.

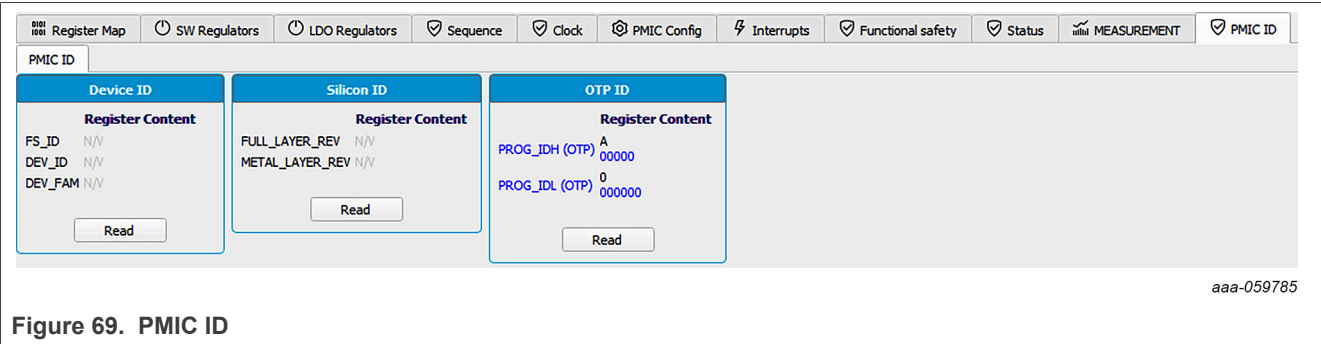
- **AMUX measurement summary:** Displays the measurements of voltage levels and temperature values from sensors placed at key locations. Click **Read** to obtain or refresh the measurements.
- **Temperature measurements graph:** Displays the measurements of the Temperature sensors inside the PMIC in function of time. Click **Clear** to clean the graph or **Poll** for performing the continuous measurements.
- **Voltage measurement graph:** Displays the selected voltage measurement values as a function of time in a graph. Click **Clear** to clean the graph or **Poll** for performing the continuous measurements.



6.5.6.11 PMIC ID

Provide general Device Information.

- **Device ID:** Shows the safety level information
- **Silicon ID:** Provides the silicon revision.
- **OTP ID:** Identifies the device configuration.



6.5.7 I/O PINS

The I/O PINS tool provides a means of reading INTB, FCCU1, PGOOD, RSTB, GPIO1, GPIO2 and BSTEN, and Setting FCCU0, PWRON, VDDOTP, STBY, GPIO1, GPIO2, GPIO3, GPIO4 and BSTEN.

Note: The configuration of GPIOx pins must be done by OTP. Depending on the chosen functionality for GPIOx pins, the hardware must be configured as explained in [Section 4.4](#).

The IO PINS panel consists of three sections:

- **Log window:** Maintains a running log of events initiated during the current session. A drop-down menu in the upper left allows the log to be filtered by register read, register write, pin read, and pin write. Buttons in the upper right allow the Log window contents to be saved, cleared, or run.
- **PF09 Pins Toggling window:** To use the PINS tool, it is mandatory to select the PF09 I/Os settings as inputs in the OTP/Mirror tabs.
- **PF09 Pins Setting window:** To poll the listed Pins as outputs pins during a selected time duration or read the pins.

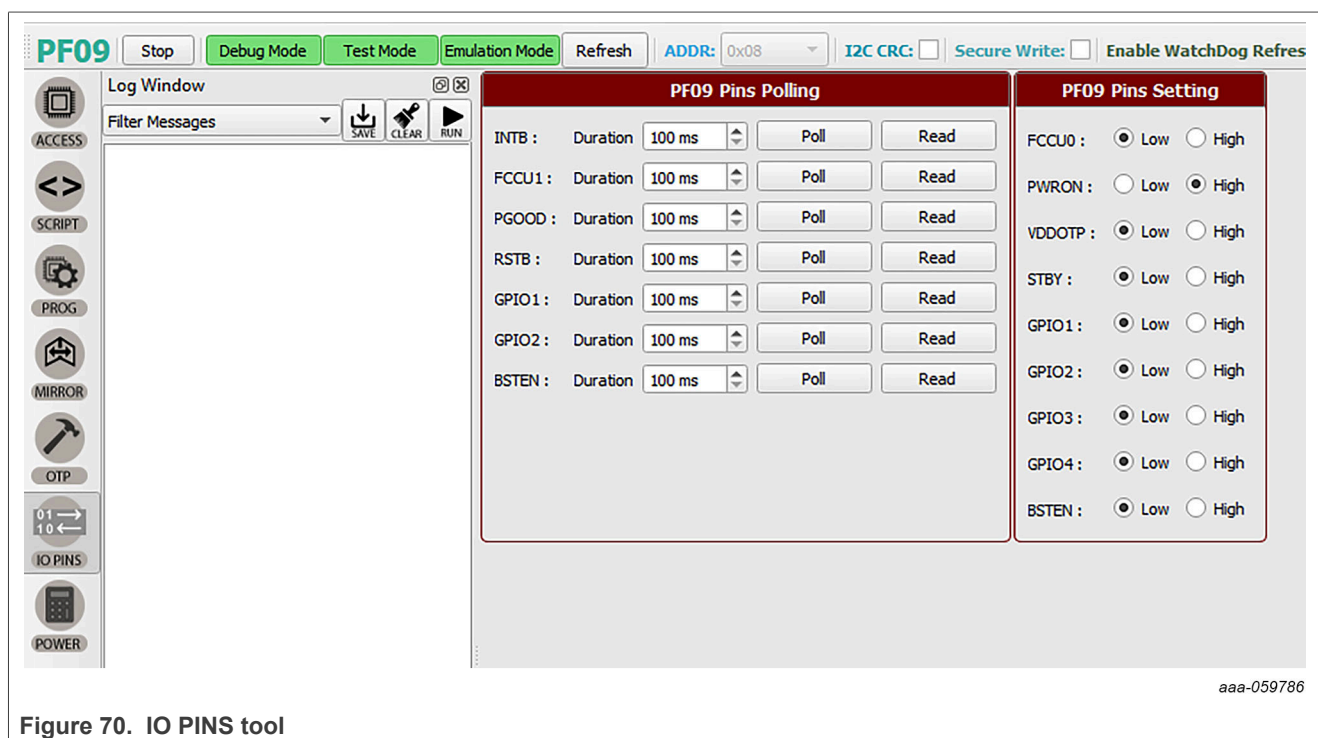


Figure 70. IO PINS tool

7 Setting up and running the KITPF09FRDMEVB

This section gives guidance on how to set up and run the KITPF09FRDMEVB evaluation board and GUI.

The device has a high level of flexibility thanks to the parameter configuration available by using the OTP registers. The user should learn about OTP and Mirror registers before operating with the device.

7.1 Setting up the KITPF09FRDMEVB

The procedure for setting up the KITPF09FRDMEVB board is as follows:

1. Make sure the board has the jumpers and switches configured in their default positions. The default debug configuration enables the board to be fully controlled by the KL25Z MCU (via I²C) and the GUI. [Section 4.4](#) shows the default jumpers and switches configuration for PF09 Family.
2. Connect the power supply to VIN-J47 (Phoenix connector - 10 mm). **The power supply should be set to a nominal value of 5V.**

Note: When connecting loads to the boards, check that the J54 jumper is in Open position to avoid drawing current from the USB line. Place jumper J54 in Close position to supply 5V from the USB line.

3. Make sure the USB cable between the board and the PC is securely connected. This connection is critical because the USB port serves as a communication channel between the PC and the KL25Z MCU onboard, and also provides voltages and references to some onboard circuits.

7.2 Connecting the KITPF09FRDMEVB to the GUI

The procedure for connecting the KITPF09FRDMEVB to the GUI is as follows:

1. To launch the NXP GUI application. See [Section 5.3](#).
2. In the USB and Device Status bar at the bottom of the GUI window, the State message should display "DISCONNECTED" when the USB cable is plugged in, but communication has not yet been established between the KL25Z MCU and the PF09 SBC.

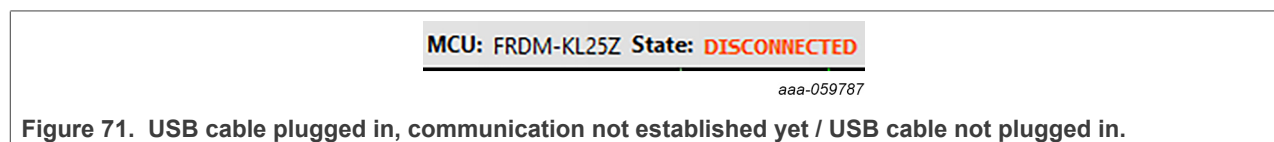


Figure 71. USB cable plugged in, communication not established yet / USB cable not plugged in.

3. To establish communication between the KL25Z MCU and the PF09 and allow the GUI to take control, click **Start** in the Connection toolbar in the top left corner of the GUI window. Once the communication is established, the State message becomes "CONNECTED".



Figure 72. USB cable plugged in, communication established

Note: If the Start button does not light on and stays grey:

- a. Turn off and on, the power supply.
- b. Reset the KL25Z MCU via the button in the KL25Z board.
- c. Verify (disconnect and connect the USB cable from Computer) that Windows is recognizing and installing the USB drivers.

7.3 Operation modes

The KITPF09FRDMEVB provides three distinct operation modes with direct impact on device functionalities. Understanding these modes helps the user interact with the GUI properly.

The voltage level on PF09 DEBUG pin is one condition for entering a given operation mode. [Table 12](#) gives the hardware configuration conditions to enter Normal, Debug or OTP/Test mode.

Table 12. Mode entry hardware conditions

Board signal	Signal name	Signal type	Configuration			
			Run mode	Debug mode ^[1]	Test mode ^[2]	Emulation mode ^[2]
FCCU0	SET_DPIN_FCCU0	PFO9	W:0	W:0	W:0	W:0
PWRON	SET_DPIN_PWRON	PFO9	W:1	→ W:0 → W:1	W:1	W:1
VDDOTP	SET_DPIN_VDDOTP	PFO9	W:0	W:1	W:1	W:1

Table 12. Mode entry hardware conditions...continued

Board signal	Signal name	Signal type	Configuration			
			Run mode	Debug mode ^[1]	Test mode ^[2]	Emulation mode ^[2]
STBY	SET_DPIN_STBY	PFO9	W:0	W:0	W:0	W:
Boost enable	SET_DPIN_BSTEN	Free board	W:0	W:0	W:0	W:0

[1] PWRON off, VDDOTP Activation and PWRON on.
[2] No changes in the control lines.

7.3.1 Run mode

7.3.1.1 Run mode definition

The Normal mode operation is used for final product test in automotive environment. Normal mode entry at power-on reset.

When Normal mode is active, the device operates with all the functionalities enabled by the loaded OTP configuration.

7.3.1.2 Run mode activation

- There are two ways to activate Normal mode:
- With the GUI using mode selection in Connection Toolbar (recommended)
 - Without the GUI (hardware only)

7.3.1.3 With the GUI using mode selection in Connection toolbar (recommended)

1. Set the EVB configuration. See [Section 7.1](#).
2. Plug the USB cable between the PC and the board.
 - The Red LED D11 for OTP 8 V generation is ON, the Blue LED D8 for OTP 5V generation is Off and the Green LED D12 for VIN is OFF.
 - The Green LED D13 for INTB is OFF, the Green LED D2 for PGOOD is OFF and the Blue LED D3 for FS0B is OFF.
3. Apply power supply VBAT.
 - The Red LED D11 for OTP 8 V generation is OFF, the Blue LED D8 for OTP 5V generation is Off and the Green LED D12 for VIN is ON.
 - The Green LED D13 for INTB is ON, the Green LED D2 for PGOOD is OFF and the Blue LED D3 for FS0B is OFF.
4. Open the GUI and start the connection.
 - Click to **Start**.



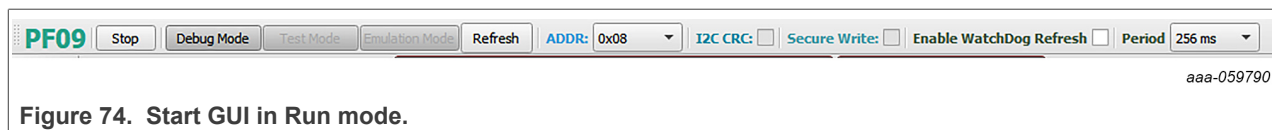


Figure 74. Start GUI in Run mode.

Start changes to **Stop** and **Debug Mode** appears.

5. Check that the GUI started in Run mode from the USB and device status bar:

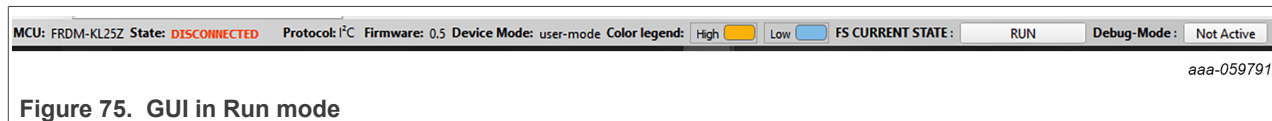


Figure 75. GUI in Run mode

6. RUN The equipment is now set to Run mode.

7.3.1.4 Without the GUI (hardware only)

1. Set the default jumper configuration. See [Section 7.1](#).
2. Apply power supply VBAT.
 - The Red LED D11 for OTP 8 V generation is OFF, the Blue LED D8 for OTP 5V generation is Off and the Green LED D12 for VIN is ON.
 - The Green LED D13 for INTB is ON, the Green LED D2 for PGOOD is OFF and the Blue LED D3 for FS0B is OFF.

7.3.2 Debug mode

7.3.2.1 Debug mode definition

The device starts in Debug mode when the hardware is configured accordingly. This mode requires the VDDOTP pin to be 1 to enter Debug mode automatically at start up. This is done via GUI.

Debug mode works in parallel with Normal mode or Test mode. When Debug mode is active, the device runs with limited functionalities as some functions are disabled.

Note: In Debug mode, OTP Registers cannot be modified.

Debug mode is helpful during software development if the device has those functions enabled by OTP.

7.3.2.2 Debug mode activation

There are two ways to activate Debug mode:

7.3.2.3 With the GUI using mode selection in Connection toolbar (recommended)

1. Set the default jumper configuration. See [Section 7.1](#).
2. Plug the USB cable between the PC and the board.
 - The Red LED D11 for OTP 8 V generation is ON, the Blue LED D8 for OTP 5V generation is Off and the Green LED D12 for VIN is OFF.

- The Green LED D13 for INTB is OFF, the Green LED D2 for PGOOD is OFF and the Blue LED D3 for FS0B is OFF.
3. Apply power supply VBAT.
 - The Red LED D11 for OTP 8 V generation is OFF, the Blue LED D8 for OTP 5V generation is Off and the Green LED D12 for VIN is ON.
 - The Green LED D13 for INTB is ON, the Green LED D2 for PGOOD is OFF and the Blue LED D3 for FS0B is OFF.
 4. Open the GUI and start the connection.
 - Click on **Debug Mode** when button is grey.
 - Button changes to green and **Test Mode** button appears.

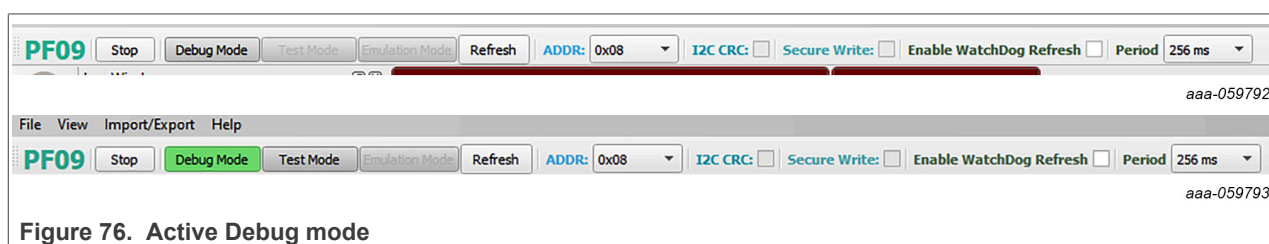


Figure 76. Active Debug mode

5. Check that the GUI has detected Debug mode in the USB and device status bar.

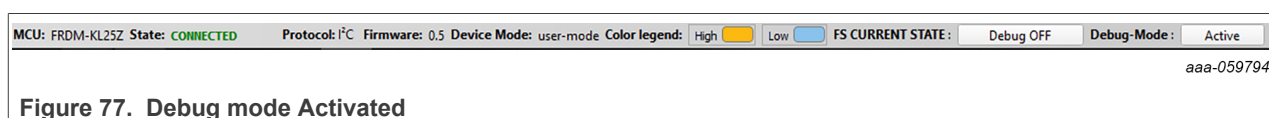


Figure 77. Debug mode Activated

6. The equipment is now set to Debug mode.

7.3.2.4 Without the GUI (hardware only)

1. Set the default jumper configuration. See [Section 7.1](#).
2. Apply power supply VBAT.
3. Sent the sequence
 - SET_DPIN:PF09:PWRON:LOW
 - SET_DPIN:PF09:VDDOTP:HIG
 - SET_DPIN:PF09:PWRON:HIG
 - SET_REG:PF09:FUNCTIONAL:SYS_DIAG:0x24
 - SET_DPIN:PF09:FCCU0:LOW
 - SET_DPIN:PF09:PWRON:LOW
 - SET_DPIN:PF09:PWRON:HIG
 - SET_DPIN:PF09:VDDOTP:HIG
4. The device powers up and operates in Debug mode. The Red LED D11 for OTP 8 V generation is OFF. The Blue LED D8 for Debug is ON.

7.3.2.5 Debug mode deactivation

Once activated, Debug mode can be deactivated by Connection toolbar, removing power or by writing via I2C the SYS_Diag(0x82) with 0x20, read and confirm a 0x04 value.

7.3.3 Test mode

7.3.3.1 Test mode definition

Test mode allows the user to write in the Mirror registers to configure or reconfigure the device for customer evaluation and to burn OTP fuses.

Note: Mirror registers are an emulation of OTP registers. In case of a POR, the Mirror registers are reset to the default OTP configuration (empty if OTP not burned).

Test mode requires **VDDOTP** = +8 V and valid Test mode keys sent by I²C and to permanently fuse all the data stored in Mirror registers to the OTP sectors requires an extra key command, available in the PROG tool. The OTP fuse burning process is explained in [Section 7.8](#).

When the Mirror registers configuration is done, the user can move back to Normal mode to power up the device with the given configuration.

7.3.3.2 Test mode activation: hardware and software

In order to start the device with a configuration loaded in the Mirror registers, follow the instructions below:

1. Set the default jumper configuration. See [Section 7.1](#).
2. Plug the USB cable between the PC and the board.
 - The Red LED D11 for OTP 8 V generation is ON, the Blue LED D8 for OTP 5V generation is Off and the Green LED D12 for VIN is OFF.
 - The Green LED D13 for INTB is OFF, the Green LED D2 for PGOOD is OFF and the Blue LED D3 for FS0B is OFF.
3. Apply power supply VBAT.
 - The Red LED D11 for OTP 8 V generation is OFF, the Blue LED D8 for OTP 5V generation is Off and the Green LED D12 for VIN is ON.
 - The Green LED D13 for INTB is ON, the Green LED D2 for PGOOD is OFF and the Blue LED D3 for FS0B is OFF.
4. Open the GUI and start the connection.
 - Click on **Test Mode** button while grey to turn green.
 - **Emmulation Mode** button activates after.



Figure 78. Activate Test mode

5. Check that the GUI has detected Debug mode in the USB and device status bar:

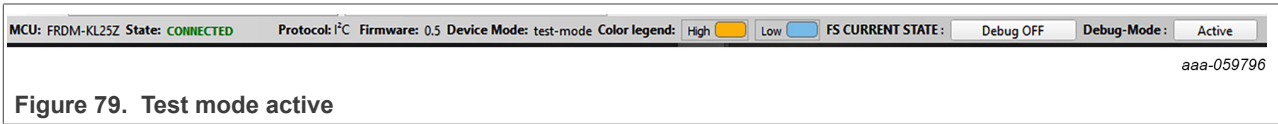


Figure 79. Test mode active

6. The equipment is now set to Test mode.

7.3.3.3 Test mode deactivation

Once activated, Test mode can be deactivated using the GUI by clicking on the green Test mode button from the Connection toolbar, removing power or by writing via I²C the SYS_Diag(0x82) with 0x20, read and confirm a 0x04 value, this will set the device in normal mode.

7.3.3.4 Test mode operation

Operating in Test mode allows the user to create and test a preliminary version of a desired configuration in the Mirror registers, prior to submitting the configuration to the OTP fuse burning process.

There are two ways to load Mirror registers:

- With a TBB script via SCRIPT tool. See [Generate a TBB script](#).
- With the MIRROR tool. See [OTP and Mirror registers](#).

These methods are functional with an empty or burned part. The procedure is explained in [Section 7.7](#).

7.3.4 Emulation mode

7.3.4.1 Emulation mode definition

Emulation mode has the same capabilities as Test mode, plus diagnostic capabilities. Emulation mode requires **VDDOTP** = +8 V and valid Test mode keys sent by I²C.

When the Mirror registers configuration is done, the user can move back to Normal mode to power up the device with the given configuration.

7.3.4.2 Test mode activation: hardware and software

In order to start the device with a configuration loaded in the Mirror registers, follow the instructions below:

1. Set the default jumper configuration. See [Section 7.1](#).
2. Plug the USB cable between the PC and the board.
 - The Red LED D11 for OTP 8 V generation is ON, the Blue LED D8 for OTP 5V generation is Off and the Green LED D12 for VIN is OFF.
 - The Green LED D13 for INTB is OFF, the Green LED D2 for PGOOD is OFF and the Blue LED D3 for FS0B is OFF.
3. Apply power supply VBAT.
 - The Red LED D11 for OTP 8 V generation is OFF, the Blue LED D8 for OTP 5V generation is Off and the Green LED D12 for VIN is ON.
 - The Green LED D13 for INTB is ON, the Green LED D2 for PGOOD is OFF and the Blue LED D3 for FS0B is OFF.
4. Open the GUI and start the connection.
 - a. Click **Emulation Mode** button while grey to turn green.

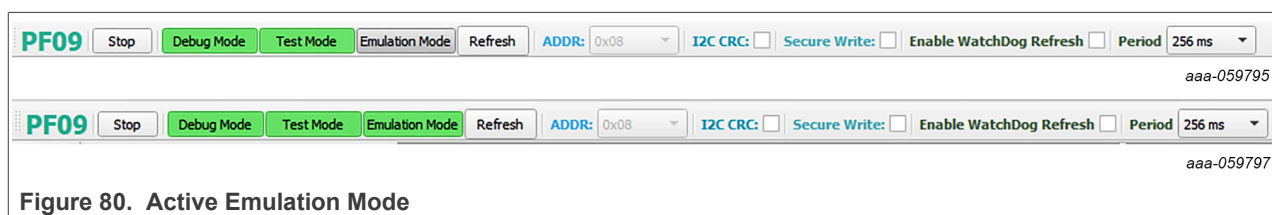


Figure 80. Active Emulation Mode

5. Check that the GUI has detected Emulation mode in the USB and device status bar:

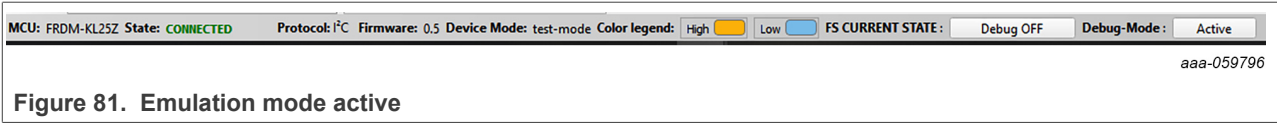


Figure 81. Emulation mode active

6. The equipment is now set to Emulation mode

7.3.4.3 Test mode deactivation

Once activated, Test mode can be deactivated using the GUI by clicking on the green Emulation mode button from the Connection Toolbar, removing power or by writing via I2C the SYS_Diag(0x82) with 0x20, read and confirm a 0x04 value, this will set the device in normal mode.

7.3.4.4 Test mode operation

Operating in Emulation mode allows the user to create and test a preliminary version of a desired configuration in the Mirror registers, prior to submitting the configuration to the OTP fuse burning process.

There are two ways to load Mirror registers:

- With a TBB script via SCRIPT tool. See [Generate a TBB script](#)
- With the MIRROR tool. See [OTP and Mirror registers](#)

These methods are functional with an empty or burned part. The procedure is explained in section [7.7](#).

7.4 Generate a TBB script

A TBB file is needed to burn OTP fuse or to emulate an OTP configuration by filling the Mirror registers through the Script tool.

To generate a TBB file, follow the procedure:

1. Go to OTP tool from the Tool Access bar:
2. Configure the OTP parameters to fit the application’s needs or import OTP configuration from a previously saved CFG file. Be aware that the displayed parameters differ depending on selected device type (ASIL B or QM) in Program Details box.
3. Enter Customer and Program details in the window on the right side.
4. When done, export directly the OTP configuration to a TBB script by clicking **Export** in the Framework settings bar and choosing TBB:
5. Select the desired folder to save the TBB script:

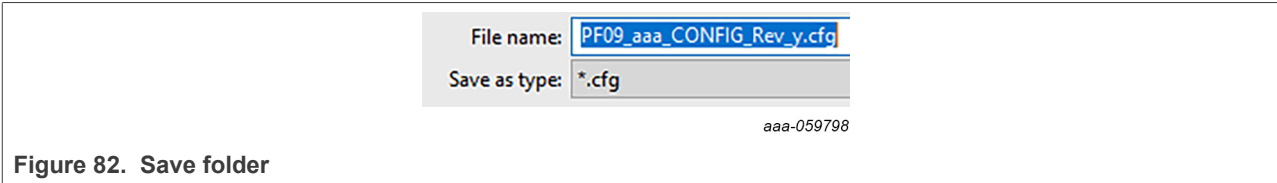
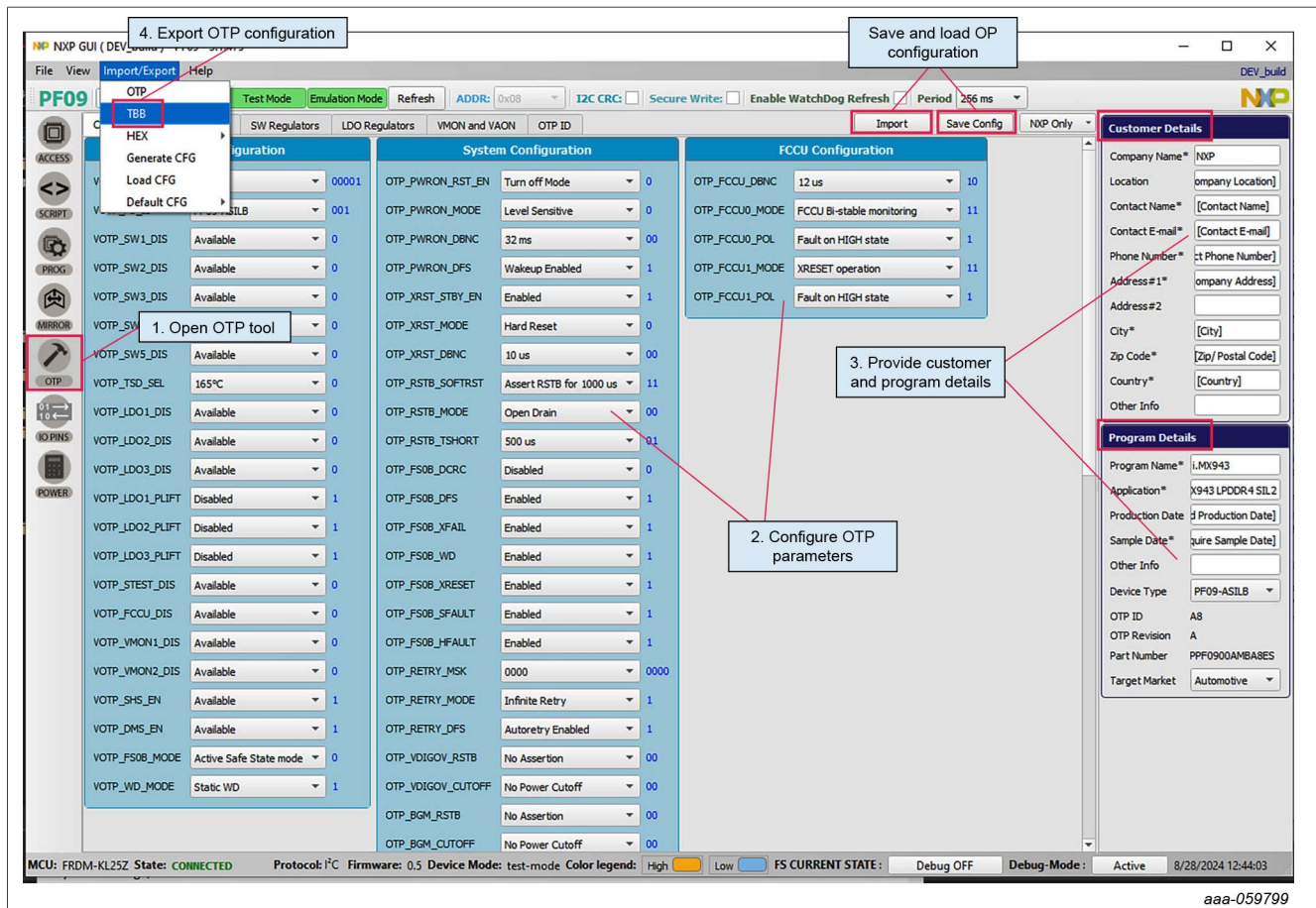


Figure 82. Save folder

Note: The script file must have a “PF09” prefix, with “aaa” being the part version and “y” the revision of the part version.

6. TBB is now generated and saved.



aaa-059799

Figure 83. TBB script

7.5 First-start procedure: configure Watchdog as Infinite Time Out

This procedure is to be used as a first-start and allows the user to enter system-level Normal mode execution with the Watchdog configured with infinite timeout and window fully opened (equivalent to disabled).

1. Set up and connect the KITPF09FRDMEVB to the GUI using [Section 7.1](#) and [Section 7.2](#).
2. If the PF09 part is empty or if the configuration loaded from OTP should be modified:
 - a. Enter test mode using [Section 7.3.3](#).
 - b. Load a configuration in MIRROR tool, then write the configuration in the Mirror registers.
 - c. Exit test mode from the Connection toolbar.
3. Go to ACCESS→PMIC Config and click **Read all** to check that the device is in Normal, Debug, and INIT mode.
4. Go to ACCESS→PMIC Config→WD and configure WD_NOK_MAX(OTP) with Development mode.

[Figure 84](#) shows the location of the watch dog parameter to update in ACCESS tool:

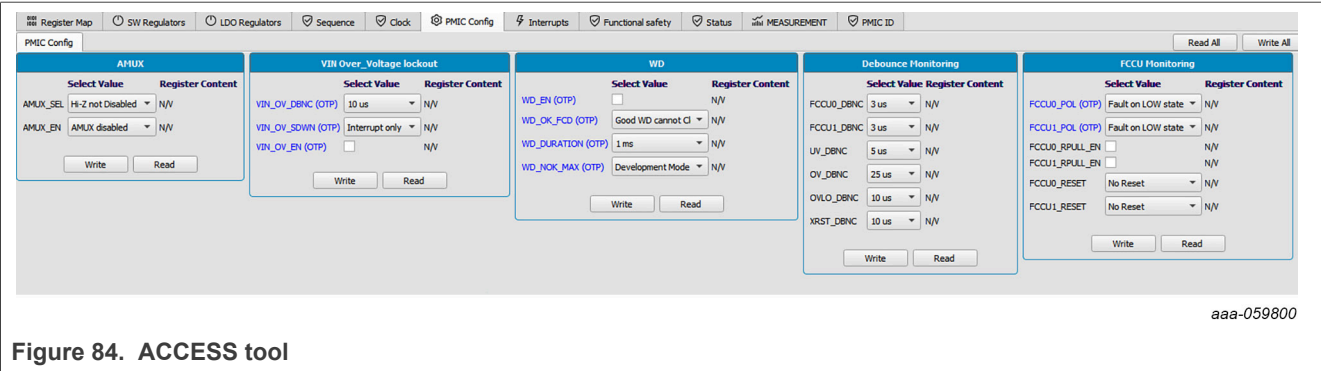


Figure 84. ACCESS tool

7.6 OTP and Mirror registers

The device incorporates one OTP block for configuration. The OTP block is shared for main parameters and fail-safe parameters. Two sectors, OTP and MTP, are available so the device can be fused twice. The device configuration scheme is shown in [Figure 85](#).

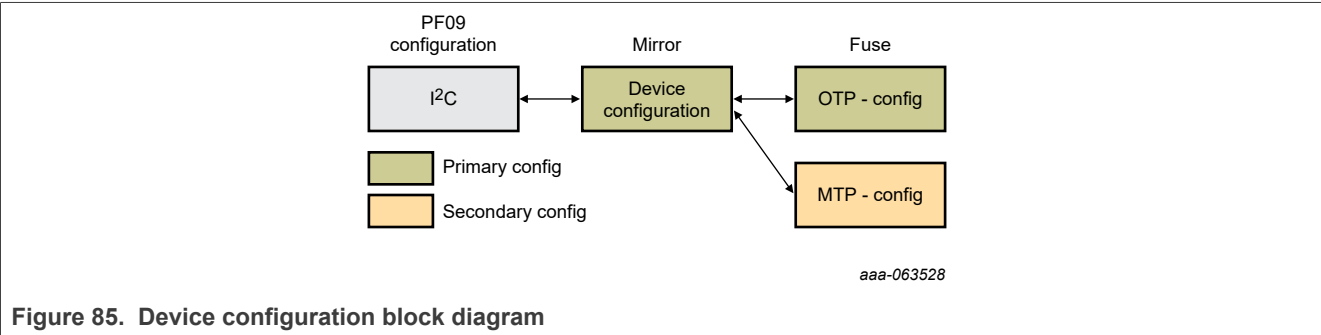


Figure 85. Device configuration block diagram

At device start up, the content of the last-programmed sector is loaded into the Mirror registers. The Mirror registers content is accessible from the NXP GUI. See [Section 6.5.5](#). The NXP GUI manages the Mirror configuration, which facilitates access and content manipulation for OTP emulation. See [Section 7.7](#).

The NXP GUI provides a tool to perform OTP programming, see [Section 7.8](#). The first sector to be burned is S1, the second is S1bis. The NXP GUI automatically manages the second sector programming. It is not possible to revert to the previous sector. Once the user has reached MTP, it is not possible to burn the part again. However, OTP emulation mode is still available.

7.7 Operate OTP emulation by loading configuration in the Mirror registers

Mirror registers are an emulation of device registers (OTP/MTP). Mirror registers can be read/written multiple times, whereas device configuration registers can be burned twice.

Mirror registers can be read and written in Test mode only. See [Section 7.3](#).

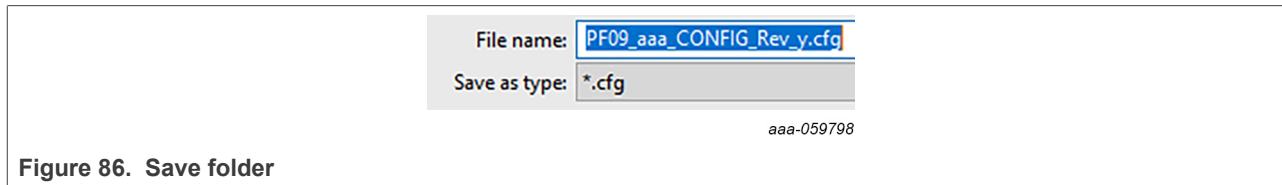
In case of a power-on reset, the Mirror registers are reset to the default OTP configuration (empty if OTP sectors not burned).

The MIRROR tool provides access to all Mirror registers with a similar disposition to OTP tool.

7.7.1 Modify the Mirror registers with a TBB script

From a Test/Emulation mode active environment, the Mirror registers can be configured using the SCRIPT tool. See [Section 6.5.4](#).

1. Open the configuration file:



Note: The script file must have a “PF09” prefix, with “aaa” being the part version and “y” the revision of the part version.

2. In the SCRIPT tool, click **OPEN** (fourth button) in the Script bar to load the TBB script file into the Script command window.



Note: The script file must have a “PF09” prefix, with “aaa” being the part version and “y” the revision of the part version.

3. To execute the TBB script, click **RUN** (first button) in the bar at the bottom of the Script command window:



4. Deactivate Test mode to start device with given configuration and load the I²C functional registers with the Mirror registers content.

As a crosscheck, open the ACCESS tool and check the fields in the Regulators tab, for example. If the operation completed without problems, all fields should display expected configuration.

7.7.2 Modify the Mirror registers with the MIRROR tool

To configure the Mirror registers, the MIRROR tool can be used to write/read directly into Mirror registers. See [Section 6.5.5](#). This requires Test mode to be activated.

1. Open the MIRROR tool from the tool access bar:

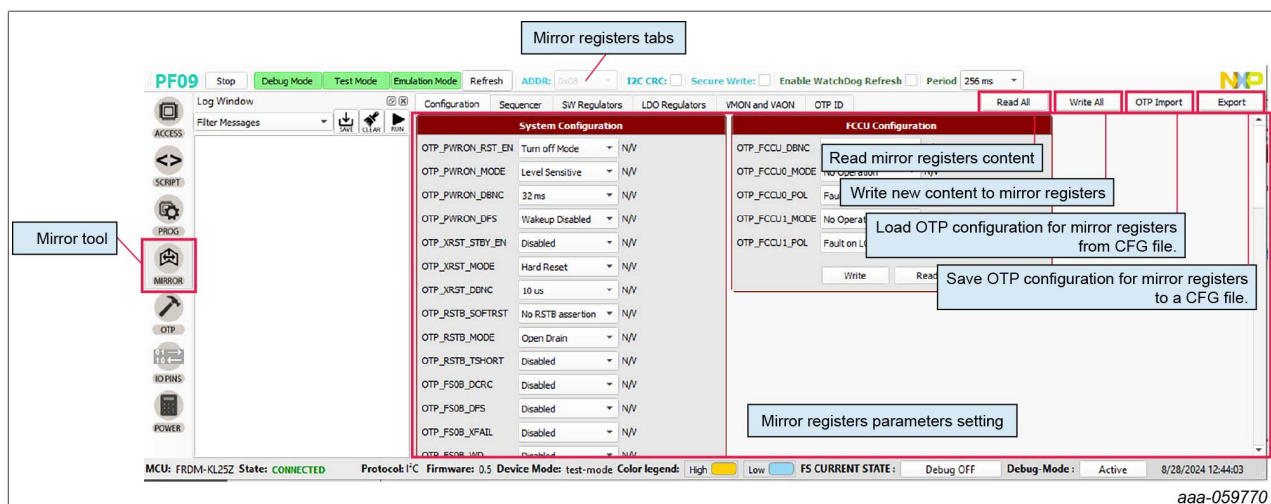


Figure 89. MIRROR tool

- Configure Mirror registers to fit the application or load an existing configuration by importing a CFG file.
Note: It is possible to load a configuration from a previously made configuration saved as a CFG file, using the Load CFG button in the top-right corner of the Mirror tool.
- Once done, click **Write All**. As a crosscheck, click **Read all**. If the operation completed without problems, all fields should display expected configuration.
- Deactivate test mode to load the Mirror registers with the given configuration and start the device.
Note: It is possible to save a current mirror registers configuration as a CFG file, using the Save CFG button in the top-right corner of the Mirror tool.

7.8 Programming an OTP configuration

The PROG tool is used to permanently burn the PF09 fuses with the customer's OTP configuration from a TBB script file. See [Section 6.5.3](#).

The TBB script can be generated from an OTP configuration. See [Section 7.4](#).

Note: The script file must have a "PF09" prefix, with "aaa" being the part version and "y" the revision of the part version.

An PF09 device can be burned just twice.

Requirement: Make sure that the socket contains a device that has not yet been burned before starting the burning process.

Follow this procedure to verify that the part is empty:

- Set the default jumper configuration. See [Section 7.1](#).
- Plug the USB cable between the PC and the board.
- Apply power supply VBAT.
- Open the GUI and start the connection.
- Switch to Test/Emulation mode.
- Open the PROG tool from the tool access bar.
- Make click in "Read" in the "Fuse Box status" section.
- Check the flags in the Sector flags section of the Fuse box status window. See [Section 6.5.3](#).

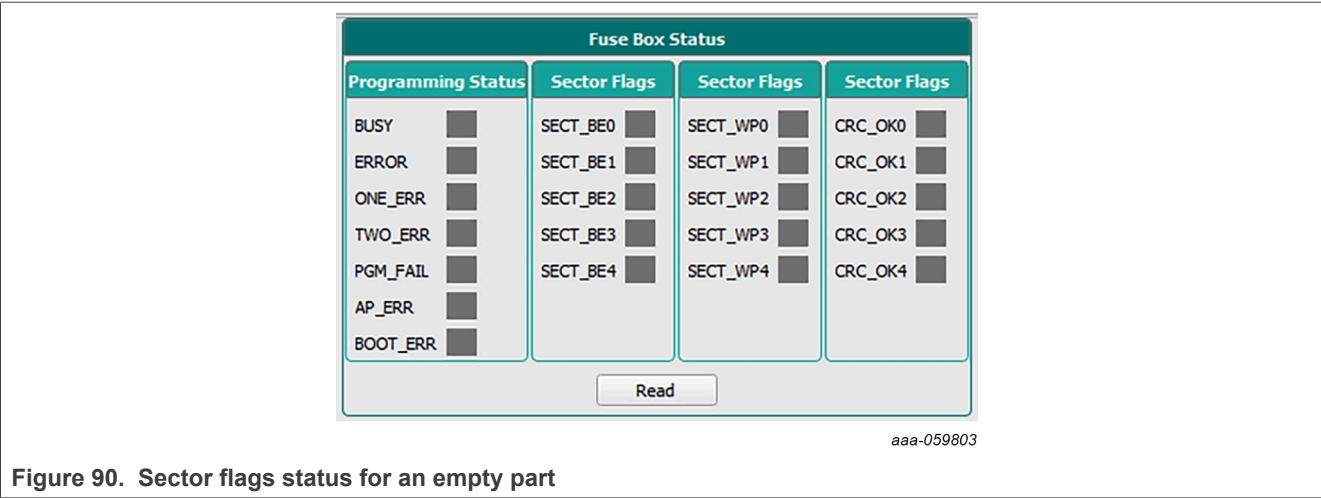


Figure 90. Sector flags status for an empty part

The device is empty and capable of being burned. It is not fused.

Figure 91 shows the Sector Flags status in the Programming interface for a VOTP section burned. It is VOTP fused.

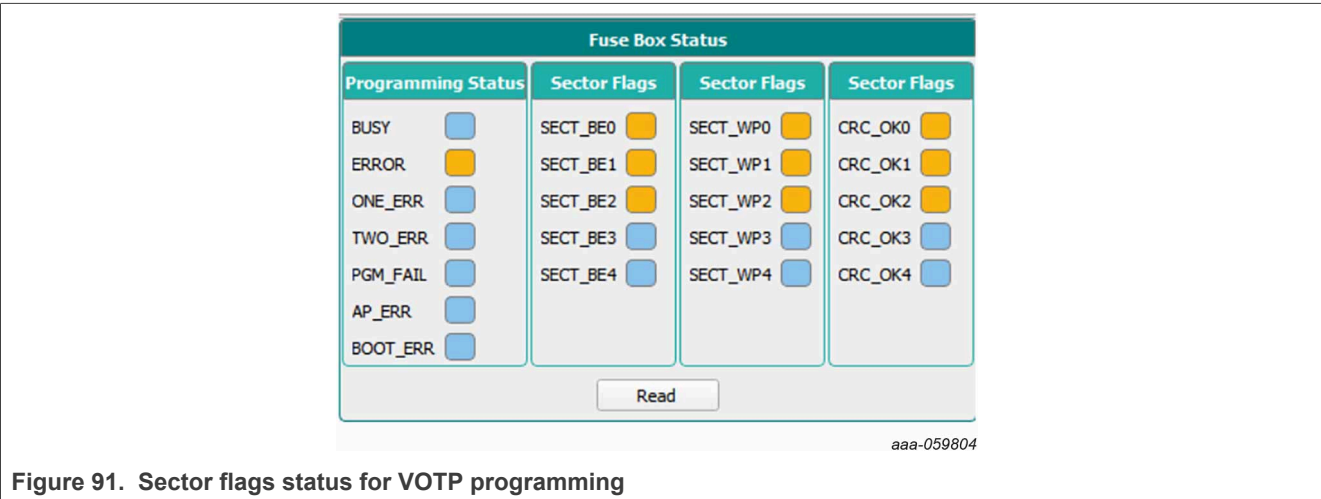


Figure 91. Sector flags status for VOTP programming

Figure 92 shows the Sector flags status in the Programming interface for a part burned once. It is OTP fused.

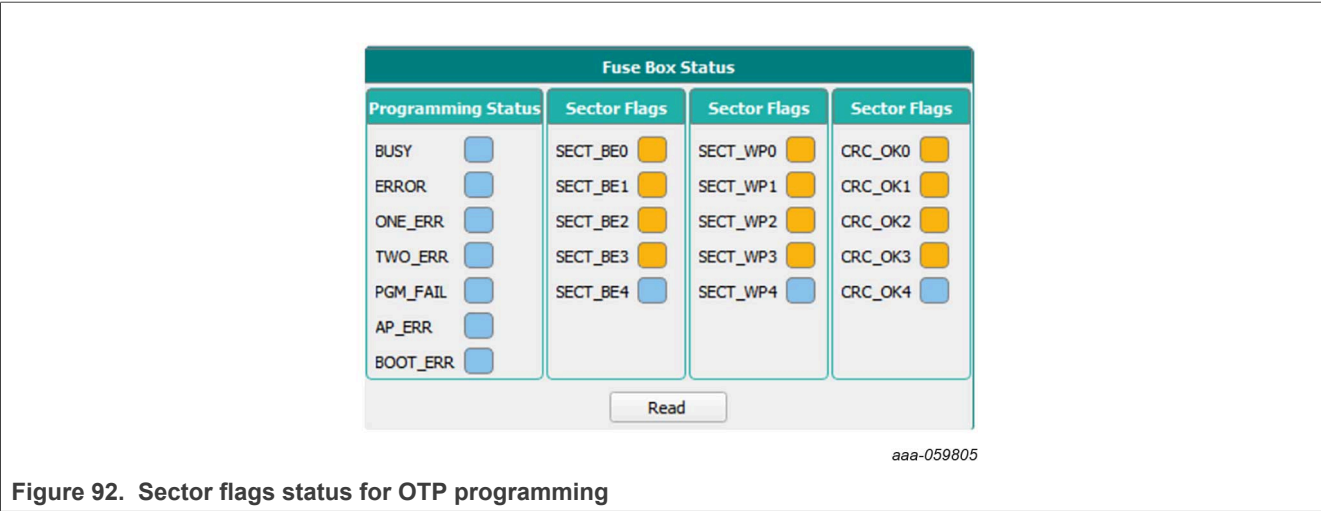


Figure 92. Sector flags status for OTP programming

Figure 93 shows the Sector flags status in the Programming interface for a part burned twice. It is MTP fused.

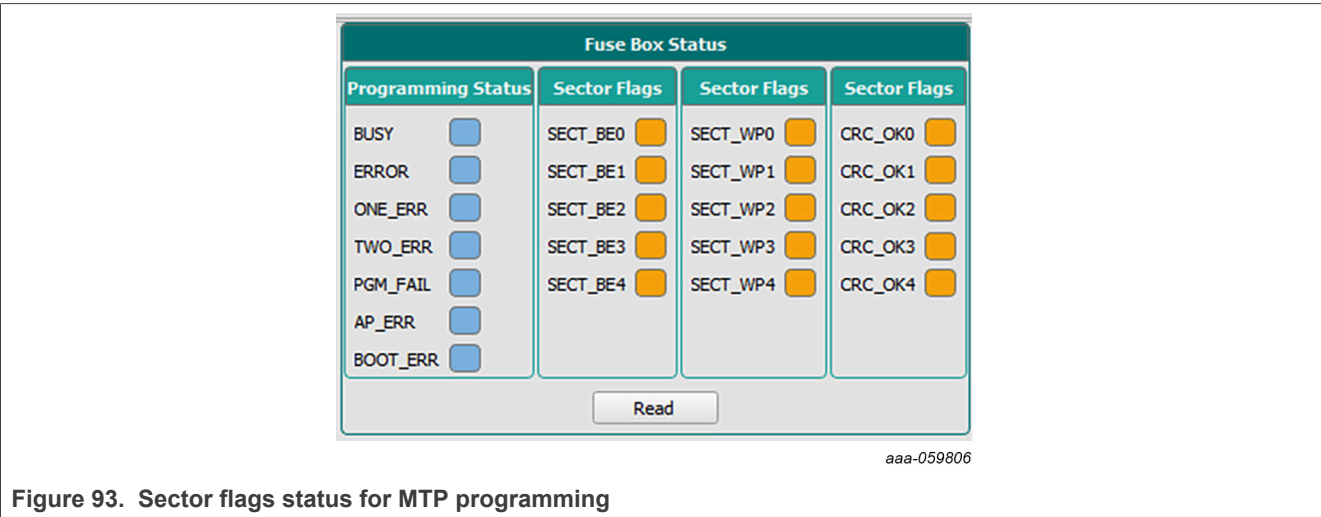


Figure 93. Sector flags status for MTP programming

Programming procedure:

1. Set the default jumper configuration. See [Section 7.1](#).
2. Plug the USB cable between the PC and the board.
3. Apply power supply VBAT.
4. Open the GUI and start the connection.
5. Switch to Test/Emulation mode.
6. Open the PROG tool from the tool access bar.
7. Select TBB File
8. Click **Program** to start the burning process.

7.9 Save a routine from Log window then Run it as a Script

The Log window shows the requests and answers transiting between the KL25Z MCU and the PF09 device. The commands are sent using I²C.

Requests are sent to PF09 after a user action on the graphical interface. Answers are received by MCU, then displayed to the user in the graphical interface. These exchanges are stored in the Log file.

When the user must operate the same routine multiple times on the device, for example to automate loading the Mirror registers, as shown in [Figure 48](#), it is possible to record the actions from the Log file then run the routine later as a Script.

In the Script .txt file, it is possible to add:

- A delay between successive commands using DELAY:xx command with xx the delay in milliseconds.
- A pause in the script, for example to have time to change hardware configuration between two commands, using PAUSE command.
- A comment in the script using // at line start.

8 Revision history

Document ID	Release date	Description
UM12292 v.1.0	20 November 2025	Initial release

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <https://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Suitability for use in automotive applications — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Tab. 1.	Configuration Jumpers	7	Tab. 7.	RSTB configuration	10
Tab. 2.	Phoenix Contact/PCB terminal functions	7	Tab. 8.	Output voltage	10
Tab. 3.	Access point functions	8	Tab. 9.	MCU communication I2C selection	10
Tab. 4.	Voltage selection and configuration	9	Tab. 10.	Test points list	12
Tab. 5.	PWRON configuration	9	Tab. 11.	Tool access bar	25
Tab. 6.	FCCUx configuration	10	Tab. 12.	Mode entry hardware conditions	47

Figures

Fig. 1.	Overview diagram of communication between PF09 and NXP GUI	3	Fig. 44.	OTP program details	30
Fig. 2.	Location of key KITPF09FRDMEVB – components	5	Fig. 45.	PROG tool	31
Fig. 3.	Location of key KITPF09FRDMEVB components	6	Fig. 46.	SCRIPT tool	32
Fig. 4.	KITPF09FRDMEVB LED signaling	12	Fig. 47.	Script command window	33
Fig. 5.	KITPF09FRDMEVB -Test points	13	Fig. 48.	Generate an OTP – mirror registers writing script example (OTP-Script)	33
Fig. 6.	GUI folder list	14	Fig. 49.	Script command panel help	34
Fig. 7.	NXP_GUI-version-Setup.exe	14	Fig. 50.	Using the SCRIPT tool	34
Fig. 8.	GUI setup window	14	Fig. 51.	Script commands window	35
Fig. 9.	GUI Licence agreement	15	Fig. 52.	Script results window	35
Fig. 10.	GUI choose components to install	15	Fig. 53.	MIRROR tool	36
Fig. 11.	GUI choose install location	16	Fig. 54.	ACCESS tool	36
Fig. 12.	Complete setup	16	Fig. 55.	Register map menu	37
Fig. 13.	Launch the GUI	17	Fig. 56.	Register content window	38
Fig. 14.	GUI settings	18	Fig. 57.	Accessing one register content using Read and Write buttons	38
Fig. 15.	GUI framework	19	Fig. 58.	Accessing one register content using Bit-Map Dialog	39
Fig. 16.	Framework settings bar	19	Fig. 59.	Read/Write/Reset bar	39
Fig. 17.	Framework settings bars	19	Fig. 60.	SW Regulators tab	40
Fig. 18.	File menu	20	Fig. 61.	SW Regulators tab	40
Fig. 19.	View menu - display	20	Fig. 62.	Sequence Tab	41
Fig. 20.	View menu - show	20	Fig. 63.	Clock tab	42
Fig. 21.	View menu - naming conventions	21	Fig. 64.	PMIC tab	42
Fig. 22.	Import/export menu	21	Fig. 65.	Interrupts tab	43
Fig. 23.	Help menu	22	Fig. 66.	Functional safety tab	43
Fig. 24.	Connection toolbar	22	Fig. 67.	Status tab	44
Fig. 25.	Device connection – Start/stop	22	Fig. 68.	Measurement tab	45
Fig. 26.	Not detected	22	Fig. 69.	PMIC ID	45
Fig. 27.	Disconnected	23	Fig. 70.	IO PINS tool	46
Fig. 28.	Connected	23	Fig. 71.	USB cable plugged in, communication not established yet / USB cable not plugged in.	47
Fig. 29.	Watchdog enablement and configuration	23	Fig. 72.	USB cable plugged in, communication established	47
Fig. 30.	Communication configuration	24	Fig. 73.	Open the GUI and start the connection.	48
Fig. 31.	Watchdog management	24	Fig. 74.	Start GUI in Run mode.	49
Fig. 32.	Enable watchdog refresh unchecked	24	Fig. 75.	GUI in Run mode	49
Fig. 33.	USB and device status bar	25	Fig. 76.	Active Debug mode	50
Fig. 34.	Tool access bar	25	Fig. 77.	Debug mode Activated	50
Fig. 35.	POWER Tool	26	Fig. 78.	Activate Test mode	51
Fig. 36.	OTP tool main panel	27	Fig. 79.	Test mode active	51
Fig. 37.	Power sequence configuration	27	Fig. 80.	Active Emulation Mode	52
Fig. 38.	SW Regulator tab	28	Fig. 81.	Emulation mode active	53
Fig. 39.	SW Regulator tab	28	Fig. 82.	Save folder	53
Fig. 40.	LDO regulators tab	29	Fig. 83.	TBB script	54
Fig. 41.	VMON and VAON tab	29	Fig. 84.	ACCESS tool	55
Fig. 42.	Program ID tab	29			
Fig. 43.	Customer details	30			

Fig. 85.	Device configuration block diagram	55	Fig. 90.	Sector flags status for an empty part	58
Fig. 86.	Save folder	56	Fig. 91.	Sector flags status for VOTP programming	58
Fig. 87.	Script bar: Open	56	Fig. 92.	Sector flags status for OTP programming	59
Fig. 88.	Script bar: Run	56	Fig. 93.	Sector flags status for MTP programming	59
Fig. 89.	MIRROR tool	57			

Contents

1	Introduction	2	6.5.4.4	Script results window	35
2	Finding kit resources and information on the NXP website	2	6.5.5	MIRROR	35
2.1	Collaborate in the NXP community	2	6.5.6	ACCESS	36
3	Getting ready	2	6.5.6.1	Register map	37
3.1	Kit contents	2	6.5.6.2	SW Regulators	40
3.2	Additional hardware	2	6.5.6.3	LDO Regulators	40
3.3	Minimum system requirements	2	6.5.6.4	Sequence	41
3.4	Software	3	6.5.6.5	Clock tab	41
4	Getting to know the hardware	3	6.5.6.6	PMIC Configuration Tab	42
4.1	Kit overview	3	6.5.6.7	Interrupts	43
4.2	Board features	3	6.5.6.8	Functional safety	43
4.3	KITPF09FRDMEVB featured components	4	6.5.6.9	Status tab	44
4.4	KITPF09FRDMEVB evaluation board	5	6.5.6.10	Measurement Tab	44
4.4.1	Voltage selection and configuration	9	6.5.6.11	PMIC ID	45
4.4.2	Power on configuration	9	6.5.7	I/O PINS	45
4.4.3	External power monitoring	10	7	Setting up and running the KITPF09FRDMEVB	46
4.4.4	RSTB pullup	10	7.1	Setting up the KITPF09FRDMEVB	46
4.4.5	Output voltages	10	7.2	Connecting the KITPF09FRDMEVB to the GUI	47
4.4.6	MCU communication I2C selection	10	7.3	Operation modes	47
4.4.7	Debug and OTP configuration	11	7.3.1	Run mode	48
4.4.8	LED signaling	11	7.3.1.1	Run mode definition	48
4.4.9	Test points	12	7.3.1.2	Run mode activation	48
4.4.10	Schematic layout and bill of materials	13	7.3.1.3	With the GUI using mode selection in Connection toolbar (recommended)	48
5	Installing and configuring software tools	13	7.3.1.4	Without the GUI (hardware only)	49
5.1	Flashing KL25Z MCU GUI firmware	13	7.3.2	Debug mode	49
5.2	Installing the PF09 NXP GUI software package	13	7.3.2.1	Debug mode definition	49
5.3	Launching the PF09 NXP GUI	17	7.3.2.2	Debug mode activation	49
6	PF09 NXP GUI	18	7.3.2.3	With the GUI using mode selection in Connection toolbar (recommended)	49
6.1	NXP GUI framework window	18	7.3.2.4	Without the GUI (hardware only)	50
6.2	Framework settings bar	19	7.3.2.5	Debug mode deactivation	50
6.2.1	File menu item	20	7.3.3	Test mode	51
6.2.2	View menu item	20	7.3.3.1	Test mode definition	51
6.2.3	Import/export menu item	21	7.3.3.2	Test mode activation: hardware and software	51
6.2.4	Help menu item	21	7.3.3.3	Test mode deactivation	52
6.3	Connection toolbar	22	7.3.3.4	Test mode operation	52
6.3.1	Device connection	22	7.3.4	Emulation mode	52
6.3.2	I2C communication configuration	23	7.3.4.1	Emulation mode definition	52
6.3.3	Watchdog management	24	7.3.4.2	Test mode activation: hardware and software	52
6.3.3.1	Watchdog enablement and configuration	24	7.3.4.3	Test mode deactivation	53
6.3.3.2	Watchdog configuration on MCU side	24	7.3.4.4	Test mode operation	53
6.4	USB and device status bar	24	7.4	Generate a TBB script	53
6.5	Tools access bar	25	7.5	First-start procedure: configure Watchdog as Infinite Time Out	54
6.5.1	POWER	25	7.6	OTP and Mirror registers	55
6.5.2	OTP	26	7.7	Operate OTP emulation by loading configuration in the Mirror registers	55
6.5.2.1	OTP parameters setting window	26	7.7.1	Modify the Mirror registers with a TBB script ...	56
6.5.2.2	OTP Details window	30	7.7.2	Modify the Mirror registers with the MIRROR tool	56
6.5.3	PROG	31	7.8	Programming an OTP configuration	57
6.5.3.1	Device programming configuration window	31			
6.5.3.2	OTP mode window	31			
6.5.3.3	Fuse Box Status window	31			
6.5.4	SCRIPT	32			
6.5.4.1	Log window	32			
6.5.4.2	Script commands panel	32			
6.5.4.3	Script Commands window	35			

7.9 Save a routine from Log window then Run it
as a Script 59

8 **Revision history** **60**

Legal information **61**

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.