UM12182

KITFS0400A0EVM evaluation board

Rev. 3.0 — 4 June 2026 **User manual**

Document information

Information	Content
Keywords	FS04, KL25Z, NXP GUI, high voltage ASIL D PMIC, S32N processor, S32 automotive platform, central compute, gateway, in-vehicle network, domain controller, telematics
Abstract	The KITFS0400A0EVM evaluation board user manual is intended for engineers involved in the evaluation, design, implementation, and validation of the FS04 high voltage ASIL D PMIC for the S32N processor.

1 Introduction

The KITFS0400A0EVM evaluation board user manual is intended for engineers involved in the evaluation, design, implementation, and validation of the FS04 high-voltage ASIL D PMIC for the S32N processor.

The KITFS0400A0EVM enables development on the FS04 high-voltage ASIL D PMIC for the S32N processor family of devices. This document covers connecting the hardware, installing the software and tools, configuring the environment, and using the kit. The kit can be connected to the NXP GUI software to use the registers, try OTP configurations, and program the device.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on http://www.nxp.com.

The information page for the KITFS0400A0EVM evaluation board is at https://www.nxp.com/KITFS0400A0EVM. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the KITFS0400A0EVM evaluation board, including the downloadable assets referenced in this document.

3 Getting ready

Working with the KITFS0400A0EVM requires the kit contents, additional hardware, and a Windows PC workstation with installed software.

3.1 Kit contents

- Assembled and tested KITFS0400A0EVM evaluation board (soldered rev. D) in an antistatic bag with the following PMIC setup:
  - One soldered down FS04 (U1)
  - One soldered down PF53 (U3) with PPF5300AMMALES OTP configuration
  - One soldered down PF53 (U4) with PPF5300AMMAMES OTP configuration
- Complete assembly of FRDM-KL25Z
- USB-STD A to USB-C cable
- Jumpers required to configure the board
- Nylon spacers and screws

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit:

- One power supply with a range up to 40 V and a current limit initially set to 1.0 A.

3.3 Assumptions

Familiarity with the I^2C-bus is helpful but not required.

3.4 Minimum system requirements

This evaluation kit requires a Windows PC workstation with USB connectivity.

3.5 Software

Before working with this evaluation board, software must be installed. All listed software is available on the evaluation board's information page at https://www.nxp.com/KITFS0400A0EVM

- NXP GUI, latest version

4 Getting to know the hardware

4.1 Kit overview

The KITFS0400A0EVM kit provides an integrated platform for evaluating designs based on NXP's FS04 high voltage ASIL D PMIC for the S32N processor.

The KITFS0400A0EVM kit also accommodates two PF53s to faciliate evaluation of the FS04 at a system level.

The KL25Z freedom board can be connected to the bottom side of the KITFS0400A0EVM. The KL25Z provides the interface between the FS0400 PMIC and the NXP graphical user interface (GUI), using the I²C channel. The KL25Z can also be configured to command and monitor various I/O channels. It can supply 1.8 V or 3.3 V VDDIO and provide 8 V for the VDDOTP pin (after regulators).

The default configuration for the jumpers and switches is provided in Figure 1 of this document.

4.2 Board features

The KITFS0400A0EVM evaluation board allows a user to:

- configure an evaluation environment meeting specific design requirements using the connectors, jumpers and switches on the board
- monitor the performance in real time using the LEDs and test points on the board

4.3 Evaluation board overview

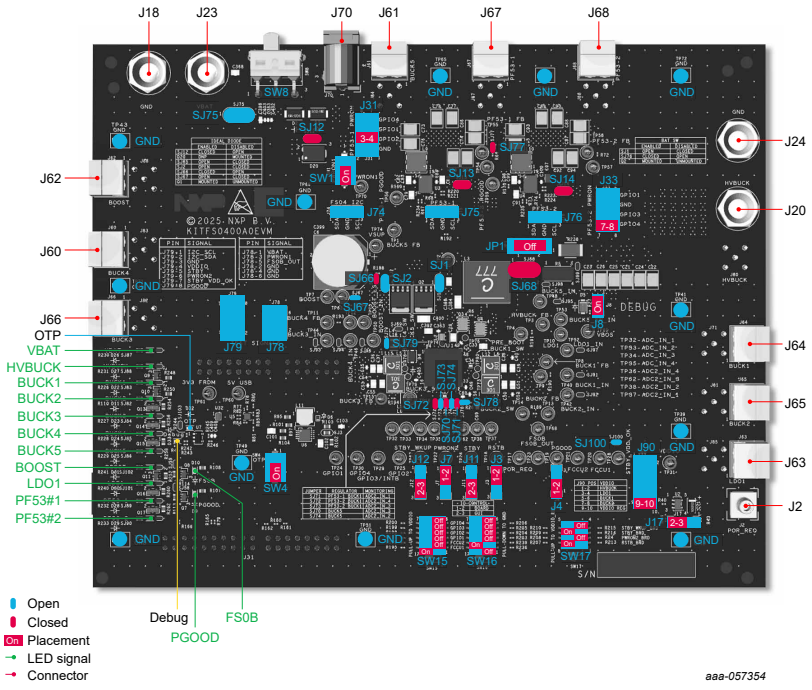

Figure 1. Evaluation board overview with placement of connectors, LEDs, jumpers and switches

4.4 Connectors

Table 1. Description of evaluation board connectors

Label	Signal name	Description
J2	POR_REQ_BRD	Coaxial SMB connector to input POR_REQ from an external GBF
J18	VBAT	Banana jack connector for VBAT input
J20	HVBUCK	Banana jack connector for HVBUCK output
J23	GND	Banana jack connector for VBAT GND
J24	GND	Banana jack connector for HVBUCK GND
J60	BUCK4_OUT / GND	Connector for BUCK4 output (J60-1) and GND (J60-2)
J61	BUCK5_OUT / GND	Connector for BUCK5 output (J61-1) and GND (J61-2)
J62	BOOST_OUT / GND	Connector for BOOST output (J62-1) and GND (J62-2)
J63	LDO1_OUT / GND	Connector for LDO1 output (J63-1) and GND (J63-2)
J64	BUCK1_OUT / GND	Connector for BUCK1 output (J64-1) and GND (J64-2)
J65	BUCK2_OUT / GND	Connector for BUCK2 output (J65-1) and GND (J65-2)
J66	BUCK3_OUT / GND	Connector for BUCK3 output (J66-1) and GND (J66-2)
J67	PF53_1_BUCK1	Connector for PF53_1 output (J67-1) and GND (J67-2)
J68	PF53_2_BUCK1	Connector for PF53_2 output (J68-1) and GND (J68-2)
J70	VBAT	Alternative power jack connector for VBAT input

4.5 LEDs

Table 2. Description of evaluation board LEDs

Label	Color	Indication of lit LED
VBAT	Green	VBAT is supplied
PGOOD	Green	PGOOD is released
FS0B	Green	FS0B is released
OTP	Blue	8 V on VDDOTP pin
Debug	Yellow	5 V on VDDOTP pin
HVBUCK	Green	HVBUCK output is ON
BUCK1	Green	BUCK1 output is ON
BUCK2	Green	BUCK2 output is ON
BUCK3	Green	BUCK3 output is ON
BUCK4	Green	BUCK4 output is ON
BUCK5	Green	BUCK5 output is ON
BOOST	Green	BOOST output is ON
LDO1	Green	LDO1 output is ON
PF53-1	Green	PF53-1 output is ON
PF53-2	Green	PF53-2 output is ON

Note: *If the BUCK3 or BUCK4 output voltage is regulated below 0.7 V, the corresponding LED will not light up even when the output of the regulator is ON.*

4.6 Jumpers

Table 3. Descriptions of evaluation board jumpers

Label	Description	Default position
J3	Input signal for RSTB pin of FS04 • 1-2: controlled manually via SW17 (RSTB_BRD signal) • 2-3: controlled via GUI (RSTB_MCU signal)	1-2
J4	Pullup enablement on open drain PGOOD pin • 1-2: PGOOD pulled up to LDO1 output • 2-3: PGOOD pulled up to VDDIO	1-2
J7	Input/control signal of PWRON2 pin of FS04 • 1-2: controlled manually via SW17 (PWRON2_BRD signal) • 2-3: controlled via GUI (PWRON2_MCU signal)	1-2
J8	VDDOTP supply to FS04 • Open: VDDOTP pulled down to GND • Closed: VDDOTP is supplied by 5V (from VBOS - V(D5)) or 8V if SW4 is closed (from DBG_OTP_8V)	Closed
J11	Input signal to STBY pin of FS04 • 1-2: controlled manually via SW17 (STBY_BRD signal) • 2-3: controlled via GUI (STBY_MCU signal)	2-3
J12	Input signal to STBY_WKUP pin of FS04 • 1-2: controlled manually via SW17 (STBY_WKUP_BRD signal) • 2-3: controlled via GUI (STBY_WKUP_MCU signal)	2-3
J17	Onboard VDDIO voltage selection using MIC5205 (U2) • 1-2: VDDIO_REG = 3.3 V • 2-3: VDDIO_REG = 1.8 V	2-3
J31	Input signal to PWRON pin of PF53 (U3) • 1-2: pulled low to GND • 3-4: controlled by FS04 GPIO2 pin • 5-6: controlled by FS04 GPIO1 pin • 7-8: controlled by FS04 GPIO4 pin	3-4
J33	Input signal to PWRON pin of PF53 (U4) • 1-2: controlled by FS04 GPIO1 pin • 3-4: pulled low to GND • 5-6: controlled by FS04 GPIO3 pin • 7-8: ontrolled by FS04 GPIO4 pin	7-8

Table 3. Descriptions of evaluation board jumpers*...continued*

Label	Description	Default position
J74	FS04 I^2C signals: • 1: SDA • 2: GND • 3: SCL	
J75	PF53-1 I^2C signals: • 1: SDA • 2: GND • 3: SCL	
J76	PF53-1 I^2C signals: • 1: SDA • 2: GND • 3: SCL	
J78	Test signals: • 1: VBAT • 3: PWRON1 • 5: FS0B_OUT • 2,4, 6: GND	
J79	Test signals: • 1: I^2C SCL • 2: I^2C SDA • 3: GND • 4: VDDIO • 5: STBY • 6: PWRON2 • 7: STBY_VDD_OK • 8: PGOOD	
J90	VDDIO external supply selection for logic reference level • 1-2:VDDIO = HVBUCK • 3-4: VDDIO = LDO1 (enabled in STBY) • 5-6: VDDIO = BUCK1 • 7-8: VDDIO = BUCK2 • 9-10: VDDIO = VDDIO_REG (1.8 V or 3.3 V external to PMIC based on J17 settings)	9-10
SJ1	Bypass path for battery switch BAT_SW (Q2) Recommendation: keep open if battery switch (Q2) is used	Open
SJ2	Bypass path for ideal diode (Q1) Recommendation: keep open if ideal diode (Q1) is used.	Open
SJ12	Bypass path for reverse protection diode (D20) Recommendation: • If ideal diode Q1 is installed, D20 is not installed and SJ12 is closed • If ideal diode Q1 is not installed, D20 is installed and SJ12 is open	Closed

Table 3. Descriptions of evaluation board jumpers...*continued*

Label	Description	Default position
SJ13	PF53 PMIC (U3) supply selection • Open : PMIC not supplied • Closed : PMIC supplied by VPRE of FS04	Closed
SJ14	PF53 PMIC (U4) supply selection. • Open : PMIC not supplied • Closed : PMIC supplied by VPRE of FS04	Closed
SJ65 (bottom)	BHS short to VBAT_SENSE Recommendation: BHS should be shorted to VBAT_SENSE when the ideal diode Q1 is not installed	Open
SJ66	VBAT_SENSE pulled up to VBAT through a 500 Ω resistor Recommendation: • If ideal diode Q1 is installed, the VBAT_SENSE pullup is 500 Ω with SJ66 closed and SJ67 open. • If ideal diode Q1 is not installed, the VBAT_SENSE pullup is 5.1 kΩ with SJ67 closed and SJ66 open.	Closed
SJ67	VBAT_SENSE pulled-up to VBAT through a 5.1 kΩ resistor Recommendation: • If ideal diode Q1 is installed, the VBAT_SENSE pullup is 500 Ω with SJ66 closed and SJ67 open. • If ideal diode Q1 is not installed, the VBAT_SENSE pullup is 5.1 kΩ with SJ67 closed and SJ66 open.	Open
SJ68	Bypass for VPRE current measurement jumper JP1	Closed
JP1	Jumper to enable VPRE inductor current measurement • Open : SJ68 must be closed • Closed : enablement to place a current loop for VPRE inductor current measurement	Open
SJ71	PF53-1 output connection to ADC2 input • Closed: PF53-1 monitored by ADC2_IN_1	Closed
SJ72, SJ73	PF53-2 output connection to ADC2 input • SJ72 closed: PF53-2 monitored by ADC2_IN_4 • SJ73 closed: PF53-2 monitored by ADC2_IN_3	SJ72: Closed SJ73: Open
SJ70, SJ74	BUCK5 output connection to ADC2 input • SJ70 closed: BUCK5 monitored by ADC2_IN_3 • SJ74 closed: BUCK5 monitored by ADC2_IN_2	SJ70: Closed SJ74: Open
SJ75	Bypass of SW8 for high-current path supply from J18 VBAT banana connector	Open
SJ76 (bottom)	Open BAT_SW_OUT pin Recommendation: BAT_SW_OUT pin should be left open when the battery switch Q2 is not installed	Closed
SJ77	PF53-1 output connection to BUCK5_SW_IN input	Closed
SJ78	FS0B global filtering option Close to connect the global filtering • Internal FS0B tested on TP68 • Global FS0B tested on TP23	Open

Table 3. Descriptions of evaluation board jumpers...*continued*

Label	Description	Default position
SJ79	BOOST feedback pullup to VPRE when BOOST is not used (only if VPRE output > 3.9 V)	Open
SJ80, SJ81 (bottom)	VPRE compensation network selection • SJ80 closed: fit for 3.3 V VPRE • SJ81 closed: fit for 5.0 V VPRE	SJ80: Closed SJ81: Open
SJ100	STBY_VDD_OK open-drain output pullup to LDO1_OUT through a 200 kΩ resistor Close to connect the pullup circuit	Open

4.7 Switches

Table 4. Description of evaluation board switches

Label	Description	Default position
SW1	FS04 PWRON1 input pin control. • ON: PWRON1 shorted to VBAT or VBAT - V(D20) • OFF (1): PWRON1 node floating	ON
SW4	VDDOTP set to 8 V to start in OTP mode • ON: VDDOTP set to 8 V to power up in OTP mode • OFF (1): If J8 is closed, VDDOTP set to 5 V to power up in Debug mode. If J8 is open, SW4 has no effect on VDDOTP pin of FS04.	ON
SW7 (bottom)	BOOST output discharge button. BOOST discharging when the button is pressed.	OFF
SW8	Battery supply input selection: 1. Supply from J70 connector 2. No supply 3. Supply from J18/J23 banana connectors	2
SW15	I/Os pullup to VDDIO selection (set ON to pullup) 1. FCCU1 (5.1 kΩ) 2. FCCU2 (5.1 kΩ) 3. GPIO1 (5.1 kΩ) 4. GPIO2 (5.1 kΩ) 5. GPIO3/INTB (5.1 kΩ) 6. GPIO4 (5.1 kΩ)	ON-OFF-OFF-OFF-OFF-OFF

Table 4. Description of evaluation board switches...*continued*

Label	Description	Default position
SW16	I/Os pullup to VDDIO_REG selection (set ON to pullup; OFF is 100 kΩ pulldown to GND) 1. RSTB_BRD (5.1 kΩ) 2. PWRON2_BRD (5.1 kΩ) 3. STBY_BRD (5.1 kΩ) 4. STBY_WKUP_BRD (5.1 kΩ)	ON-OFF-ON-OFF
SW17	I/Os pulldown to VDDIO selection (set ON to pulldown) 1. FCCU1 (22 kΩ) 2. FCCU2 (22 kΩ) 3. GPIO1 (5.1 kΩ) 4. GPIO2 (5.1 kΩ) 5. GPIO3/INTB (5.1 kΩ) 6. GPIO4 (5.1 kΩ)	OFF-ON-OFF-OFF-OFF-OFF

4.8 Test points

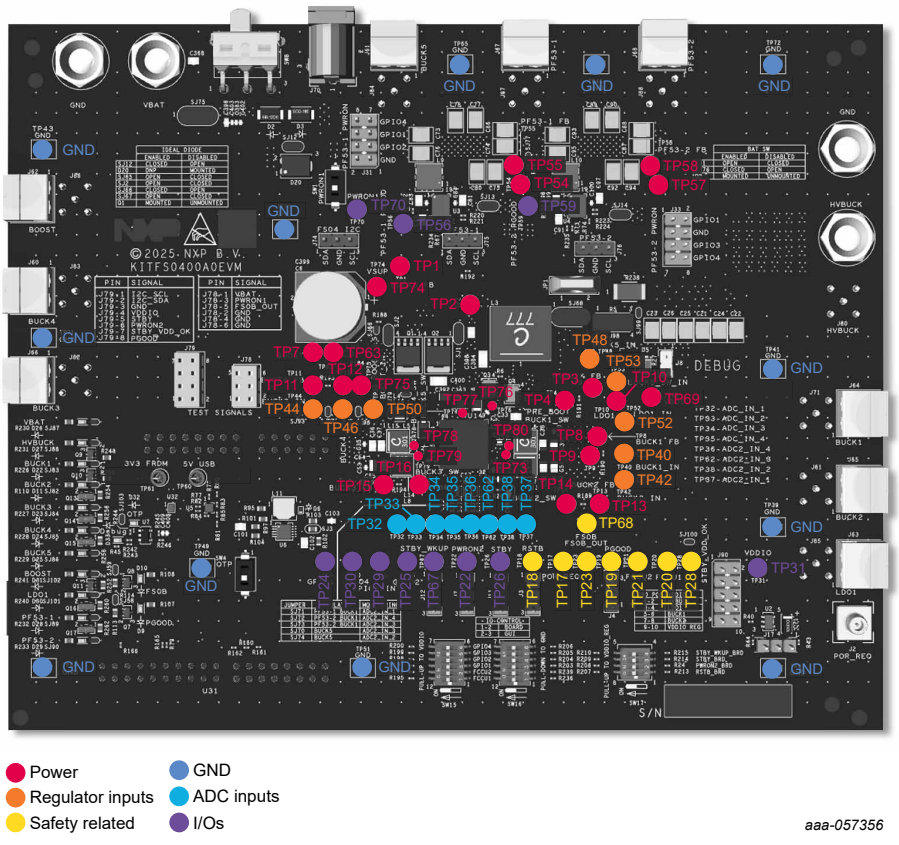

Figure 2. Locations of test points

Table 5. Description of evaluation board test points

Label	Signal name	Description
TP1, TP2	BUCK5_OUT	BUCK5 output

Table 5. Description of evaluation board test points...*continued*

Label	Signal name	Description
TP3, TP4	PRE_FB	HVBUCK output
TP7, TP63	BOOST_OUT	BOOST output
TP8, TP9	BUCK1_OUT	BUCK1 output
TP10	LDO1_OUT	LDO1 output
TP11, TP12	BUCK4_OUT	BUCK4 output
TP13, TP14	BUCK2_OUT	BUCK2 output
TP15, TP16	BUCK3_OUT	BUCK3 output
TP17	POR_REQ	POR_REQ signal
TP18	RSTB	RSTB signal
TP19	PGOOD	PGOOD signal
TP20	FCCU1	FCCU1 signal
TP21	FCCU2	FCCU2 signal
TP22	PWRON2	PWRON2 signal. Input/control signal of PWRON2 pin set with J7.
TP23	FS0B_OUT	FS0B global signal
TP24	GPIO1	GPIO1 signal
TP25	GPIO2	GPIO2 signal
TP26	STBY	Standby request signal
TP28	STBY_VDD_OK	Standby safe transition completed signal
TP29	GPIO3/INTB	GPIO3 or INTB signal
TP30	GPIO4	GPIO4 signal
TP31	VDDIO	IO supply voltage
TP32	ADC_IN_1	ADC1 input 1
TP33	ADC_IN_2	ADC1 input 2
TP34	ADC_IN_3	ADC1 input 3
TP35	ADC_IN_4	ADC1 input 4
TP36	ADC2_IN_4	ADC2 input 4
TP37	ADC2_IN_1	ADC2 input 1
TP38	ADC2_IN_2	ADC2 input 2
TP39, TP41, TP43, TP45, TP47, TP49, TP51, TP64, TP65, TP66, TP71, TP72	GND	GND test point
TP40	BUCK1_IN	BUCK1 input
TP42	BUCK2_IN	BUCK2 input
TP44	BUCK3_IN	BUCK3 input
TP46	BUCK4_IN	BUCK4 input

Table 5. Description of evaluation board test points*...continued*

Label	Signal name	Description
TP48	BUCK5_IN	BUCK5 input
TP50	BOOST_IN	BOOST input
TP52	LDO1_IN	LDO1 input
TP53	BUCK5_SW_IN	BUCK5 load switch mode input.
TP54, TP55	PF53_1_OUT	PF53_1 output
TP56	PF53_1_PGOOD	PGOOD signal of PF53_1
TP57, TP58	PF53_2_OUT	PF53_2 output
TP59	PF53_2_PGOOD	PGOOD signal of PF53_2
TP62	ADC2_IN_3	ADC2 input 3
TP67	STBY_WKUP	Standby wake-up signal
TP68	FS0B	FS0B internal signal
TP69	VBOS	Best of supply voltage
TP70	PWRON1	PWRON1 signal. Input/control signal of PWRON1 pin set with SW1
TP73	BUCK2_SW	BUCK2 switching node
TP74	VSUP	Supply voltage
TP75	BOOST_LS	BOOST low-side drain of the internal MOSFET
TP76	PRE_BOOT	VPRE bootstrap capacitor node
TP77	BUCK5_SW	BUCK5 switching node
TP78	BUCK4_SW	BUCK4 switching node
TP79	BUCK3_SW	BUCK3 switching node
TP80	BUCK1_SW	BUCK1 switching node

4.9 VDDIO selection (J90/J17)

The VDDIO pin can be powered by an external regulator supplied by the KL25Z board 5.0 V rail from USB, using the jumper J90 in 9-10 position. This allows the user to communicate with the FS04 before it powers up. The VDDIO external regulator can be set to 3.3 V or 1.8 V using jumper J17.

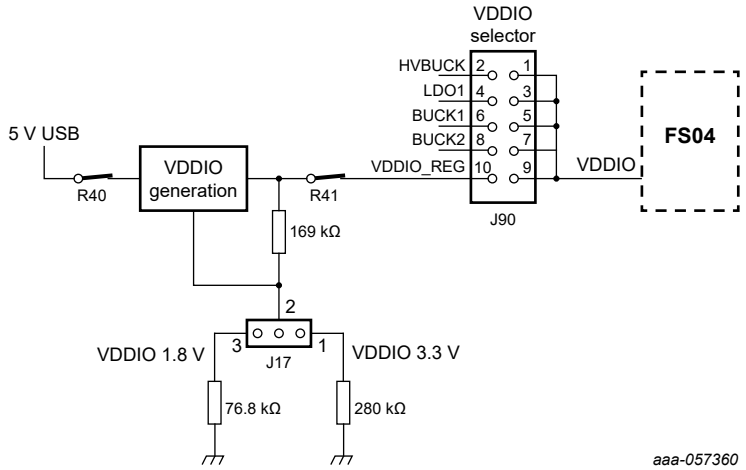

Figure 3. VDDIO selection on board

4.10 VDDOTP selection – Debug circuitry (J8/SW4)

The VDDOTP pin can be set to 5 V to power the device in Debug mode, or to 8 V to power the device in OTP mode. For more information about the operating modes of FS04, see the sections about Debug and OTP modes in the data sheet.

- To set VDDOTP pin to 5 V, close J8 and open SW4.
- To set VDDOTP pin to 8 V, close J8 and close SW4.
- To set VDDOTP to ground, open J8.

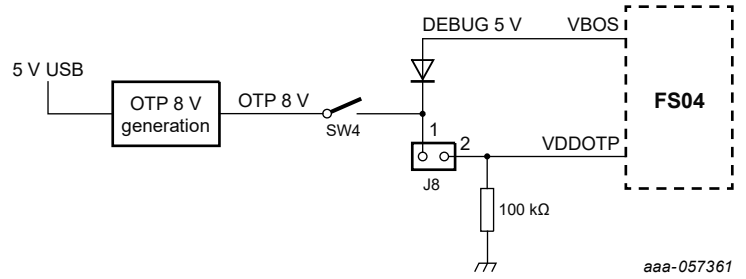

Figure 4. VDDOTP selection on board

4.11 Schematic, board layout, and bill of materials

The schematic, board layout and bill of materials for the KITFS0400A0EVM evaluation board are available at https://www.nxp.com/products/FS04.

5 Installing and configuring software tools

5.1 Getting the NXP GUI software package

During the development phase, the NXP GUI software package for automotive PMIC families will be provided by NXP technical support.

5.2 Flashing the KL25Z firmware

The KL25Z firmware needs to be flashed when the board is used for the first time. Follow the steps below to flash the KL25Z firmware.

1. Connect the USB cable to the USB port of the computer.
2. Press and hold the reset (RST) button on the KL25Z FRDM board.

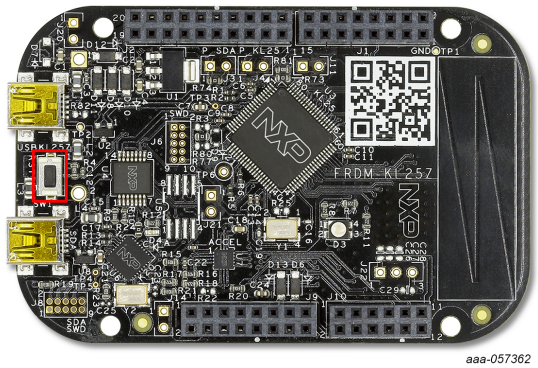

Figure 5. KL25Z board – reset button

3. Connect the USB cable to the SDA port.

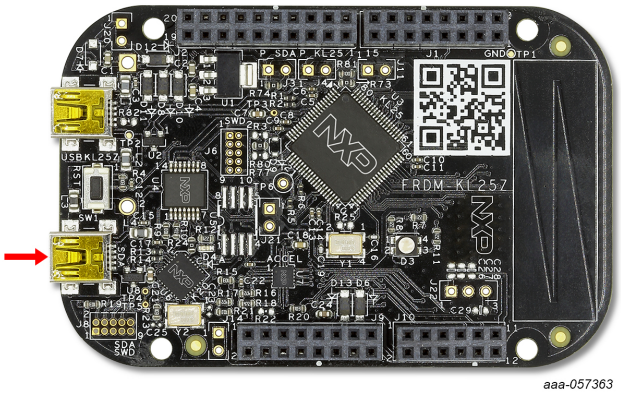

Figure 6. KL25Z board – SDA port

4. From the NXP GUI software package, open the 2 – KL25Z_FW folder.
5. From the Windows File Explorer, open the BOOTLOADER disk.

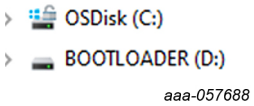

Figure 7. KL25Z board – Disk in file explorer

6. From the 2 – KL25Z_FW folder of the NXP GUI software package, drag **the MSD-DEBUG-FRDM-KL25Z_Pemicro_version.SDA** file and drop it in the BOOTLOADER disk.
   Note: *Make sure to allow enough time for the firmware to be saved in the Bootloader.*

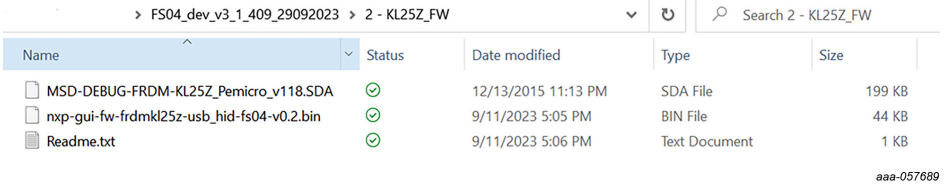

Figure 8. KL25Z board – 2 – KL25Z_FW folder content

7. Disconnect and reconnect the USB cable to the SDA port, this time without pressing the reset button.
8. The FRDM-KL25Z device should appear on the left pane of the File Explorer as pictured below.

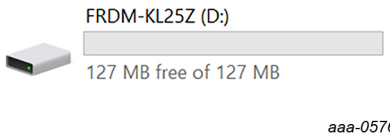

Figure 9. KL25Z board – disk in File Explorer

9. From 2 – KL25Z_FW folder, drag **nxp-gui-fw-frdmkl25z-usb-hid-fs04-version.bin** and drop it in FRDM-KL25Z disk.
   Note: *Make sure to allow enough time for the firmware to be saved to the disk.*
10. The KL25Z board firmware is successfully loaded. Disconnect the USB cable from the SDA port and reconnect it to the USB KL25Z port. The KL25Z should now be recognized by the NXP GUI.

Installing the NXP GUI

1. Open the NXP GUI software package. Unzip and open the 1 – NXP_GUI_Setup folder.

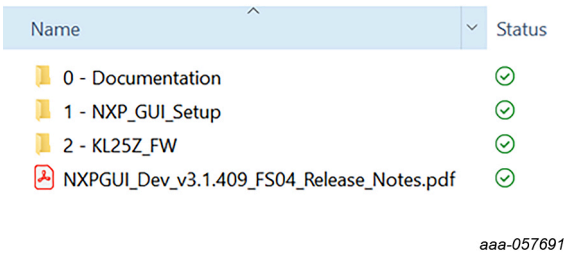

Figure 10. NXP GUI software package content

2. Double click **NXP_GUI-version-Setup.exe** to launch the application and follow the instructions.

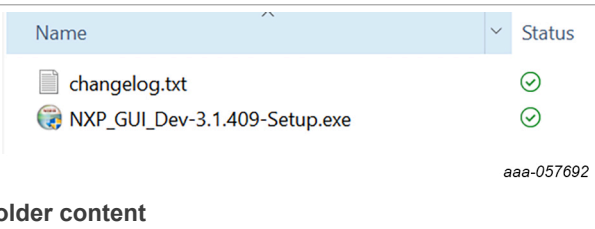

Figure 11. NXP_GUI_Setup folder content

3. Proceed with the following pop-up windows to install the application on the Windows PC.
   Click **Next**, then **I Agree**.

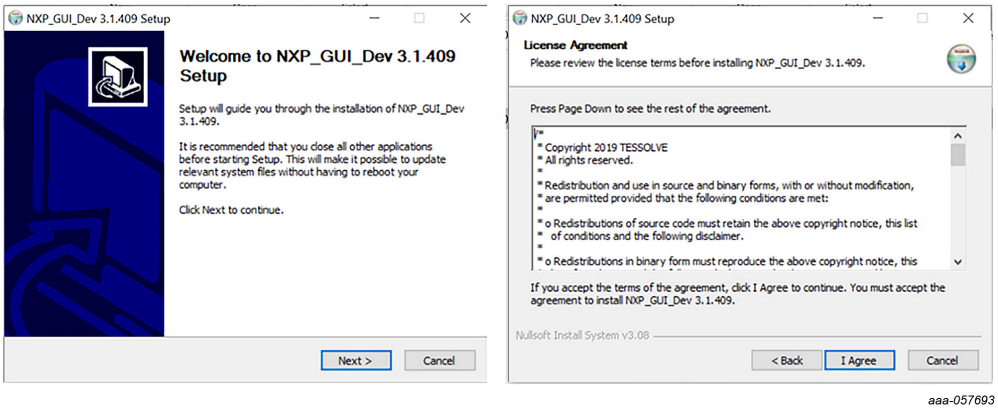

Figure 12. NXP GUI installation tool – license agreement

4. In the **Choose Components** window, select the **MainSection** and **Optional** components, then click **Next**.

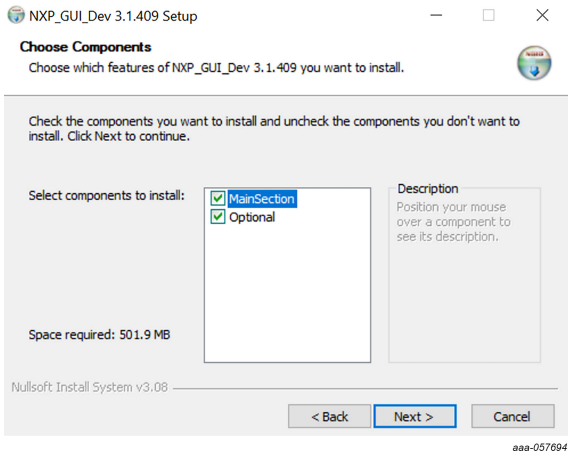

Figure 13. NXP GUI installation tool – Choose Components

5. In the **Choose Install Location** window, select a folder location to install the GUI.

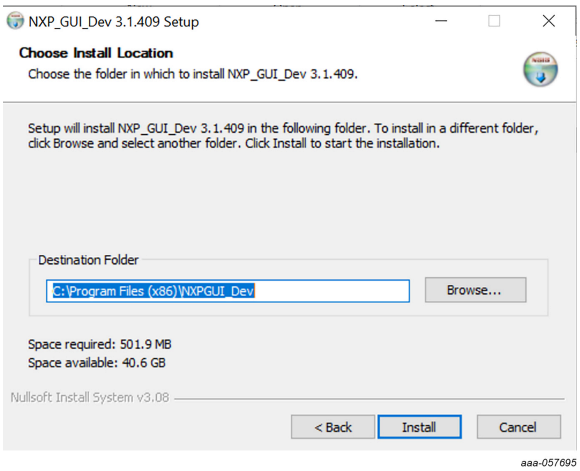

Figure 14. NXP GUI installation tool – Choose Install Location

6. The installation is now complete. Click **Finish** to close the installer.

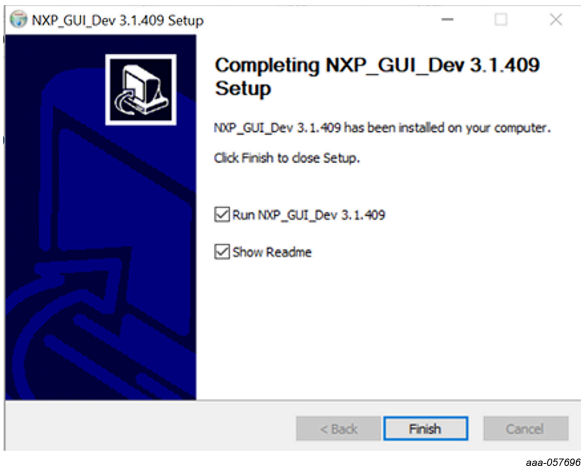

Figure 15. NXP GUI installation tool – Installation complete

5.3 Launching the NXP GUI

When the KITFS0400A0EVM kit is set up and the GUI installed, follow the steps below to launch the GUI:

1. Click on the Windows icon (bottom left corner) and locate the **NXPGUI** in the Windows All Apps bar, then click the **NXPGUI** icon to launch the GUI.

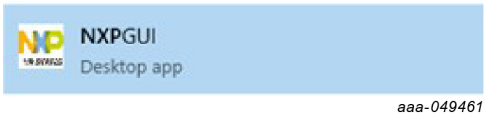

Figure 16. Launch the GUI

2. When the GUI opens, the first window to appear is the **Kit Selection** window. In the **Kit Selection** window, select the settings shown below. When finished selecting the settings, click OK.

Note: *To avoid the* ***Kit Selection*** *window on every launch, check the box* ***Use this configuration and do not ask again****. The* ***Kit Selection*** *window can be enabled/disabled through the* ***File*** *main menu item once the GUI is launched by checking/unchecking the* ***Do not display GUI Kit Selection at Start*** *box.*

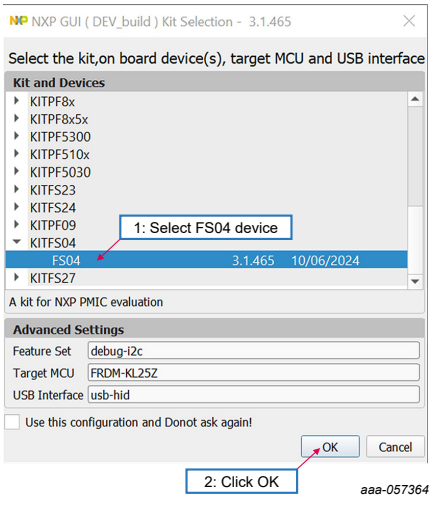

Figure 17. GUI kit selection

6 Configuring the hardware

6.1 Mounting the spacers

Four spacers and screws are delivered with the kit. These spacers and screws are meant to be mounted in each corner of the board in order to serve as a base.

6.2 Setting the jumpers into default configuration

The jumpers required to configure the board are delivered with the kit. Figure 1 shows the default configuration of the jumpers and switches.

6.3 Mounting the KL25Z

Once the KL25Z firmware is flashed, the KL25Z board should be assembled onto the bottom side of the FS04 evaluation board using the corresponding connectors.

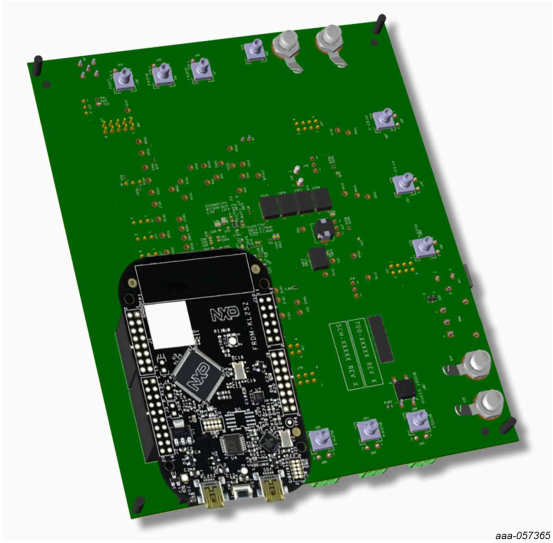

Figure 18. KL25Z assembly on FS04 evaluation board

6.4 Launching the setup

To launch the setup, the typical hardware procedure is:

1. Connect the KL25Z on the development board to the Windows PC workstation.
2. Connect the VBAT connector of the development board to the power supply.

In the initial hardware configuration, the KL25Z is providing:

- I^2C communication and I/O connections
- 5.0 V to generate VDDIO voltage level at 3.3 V or 1.8 V from an external regulator, to generate OTP 8.0 V from an external regulator, and to supply the signaling LEDs
- 3.3 V voltage level for the level shifters between the PMIC and the KL25Z

7 Tool interface (GUI) description

This section gives guidance for use of the NXP GUI.

7.1 NXP GUI framework

The NXP GUI framework consists of the following sections:

• **Framework settings**: to manage file import/export and framework configuration

• **Connection toolbar**: to start the communication with the device, enter or exit Test/OTP modes, select I^2C frequency and addresses, configure and enable the watchdog

• **Tools access bar**: to provide quick access to the evaluation tools and features

• **Log window**: to report communication events

• **Tab content**: toshow the content of each tool. Several tabs may be available inside. These tabs are explained in the following sections of this document.

• **USB and device status**: to indicate whether the device is connected or disconnected, to show the firmware version, and to display the current device mode

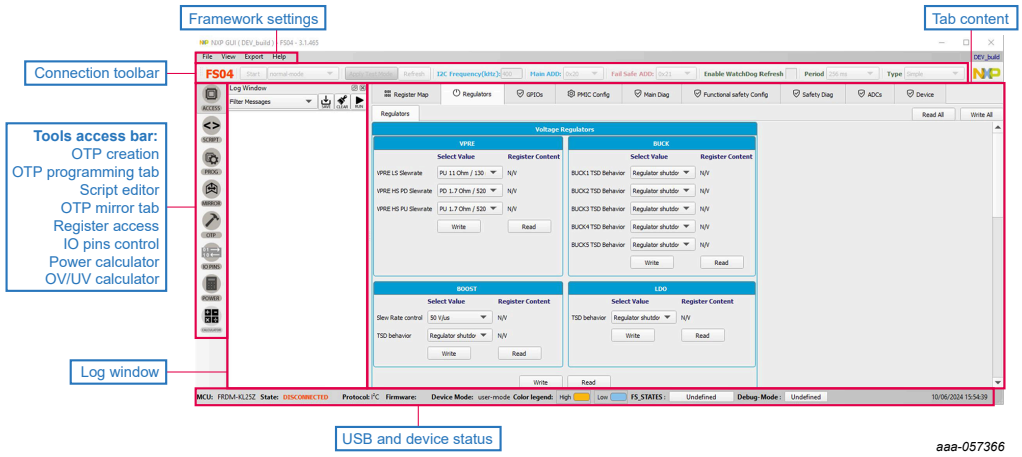

Figure 19. NXP GUI – Framework

7.2 Framework settings

The framework settings menu enables the customization of the display of the NXP GUI and the export of OTP configurations to other file types.

7.2.1 File menu item

The **File** menu item allows customizing the NXP GUI kit selection at application start: box checked to always open NXP GUI as the current GUI version; box unchecked to display the product selection box at application start.

7.2.2 View menu item

The **View** menu item enables:

- Customizing the display of the framework.

- In the **OTP** tool only, adapting the naming convention, allowing the user to select friendly or register name display for the **OTP** tool.

The naming convention options are:

– Friendly: Register names are displayed as user-friendly names in the **OTP** tool.

– Register: Register names are displayed by their technical names in the **OTP** tool.

Example: I2C Main Address ⇔ M_I2CDEVADDR_OTP.

7.2.3 Import/Export menu item

The **Import/Export** menu item allows, in the **OTP** tool only, importing a default OTP configuration file or exporting the configuration to these file types:

- TBB: a TBB file can be used in the **PROG** tool to burn OTP fuses
- HEX: this can be an I-HEX (Intel hex) or S-HEX (simple hex) script file format
- Save, export or load a default CFG config file

7.2.4 Help menu item

The **Help** menu item provides access to documentation and NXP GUI version information.

7.3 USB and device status bar

The USB and device status bar indicates whether the device is connected or disconnected, shows the firmware version, and displays the current device mode and status.

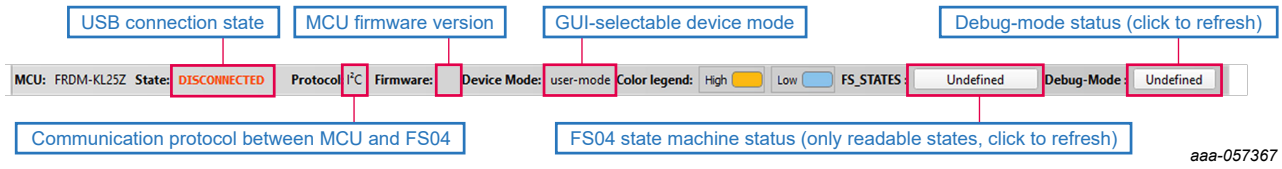

Figure 20. NXP GUI – USB and device status bar

7.4 Connection toolbar

The Connection toolbar enables the connection between the GUI and the device, the I^2C frequency and address configuration, and watchdog management.

Figure 21. Connection toolbar

7.4.1 Device connection and mode menu

The **mode** menu allows the user to connect the GUI and the device, to change between Normal, Debug and Test operating modes of the FS04 device, and to check the current mode of the device.

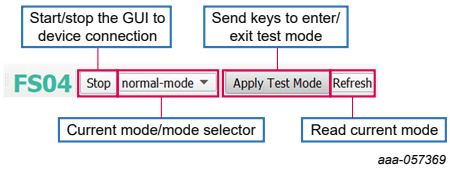

Figure 22. NXP GUI – Device connection and mode menu

7.4.2 How to connect the GUI to the device

When the KL25Z is not connected through the USB port, the state indicator in the USB and Status bar shows **NOT DETECTED**, the **FS04** header text appears red, and the **Start** button is not available.

Figure 23. NXP GUI – Device not detected

After the USB cable is connected, the State indicator displays **DISCONNECTED** and the **Start** button becomes available.

Figure 24. NXP GUI – Device disconnected

Click **Start** to start communication with the FS04.

At this point, the State indicator displays **CONNECTED** and the FS04 header text changes from red to green.

Figure 25. NXP GUI – Device connected

Usually, once connected, the next step is to load an OTP configuration and write it to the Mirror registers.

7.4.3 I^2C configuration menu

The I^2C configuration menu allows the user to configure the I^2C frequency and I^2C addresses for the main and fail-safe registers.

7.4.4 Watchdog management menu

The **watchdog management** menu allows the user to select the watchdog period and type (simple or challenger), and to start sending periodic watchdog refreshes using this configuration.

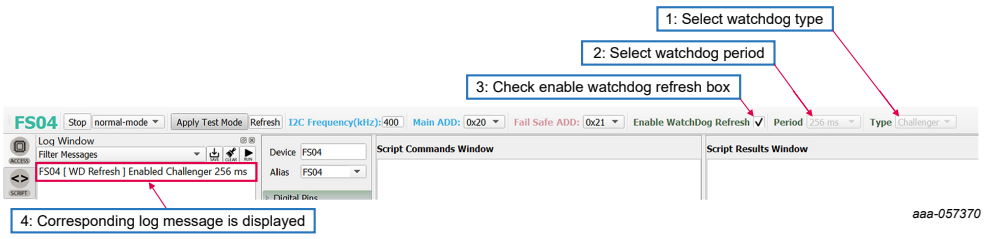

Figure 26. NXP GUI – watchdog management menu

7.5 OTP tool

The **OTP** tool allows the user to build their own OTP configuration for the device, depending on the requirements. Navigation in the OTP registers is possible with the **OTP** tool tabs.

The user can import an existing configuration file (CFG format), modify any parameter and export a new configuration file (CFG format). The **OTP** tool has no direct effect on the device. The CFG file can then be used in the **Mirror** tool or in the script for OTP emulation.

The **OTP** tool displays the bit values in blue for each parameter, to facilitate the use of the OTP map available in the FS04 data sheet.

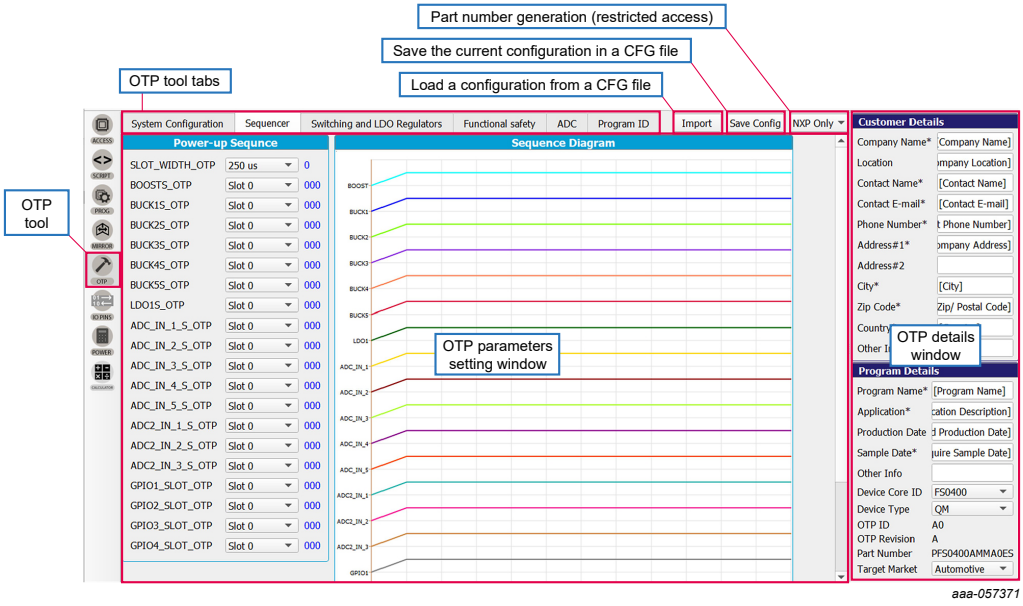

Figure 27. NXP GUI – OTP tool

Note: *A default configuration is available in the **Import/Export** item of the framework settings menu to load a basis configuration of the device in the **OTP** tool.*

Once the OTP configuration is finalized and ready to program, the user can export the TBB file from the **Import/Export** item of the framework settings menu.

7.6 PROG tool

The **PROG** tool allows the user to permanently burn the OTP fuses with the customer's OTP configuration from a TBB file. The TBB file must be exported from the **OTP** tool or provided by NXP.

Device programming can only take place once on the device.

Read the fuse box status to make sure that the device has not been programmed yet before starting the burning process. Only Sector 0 should be fused.

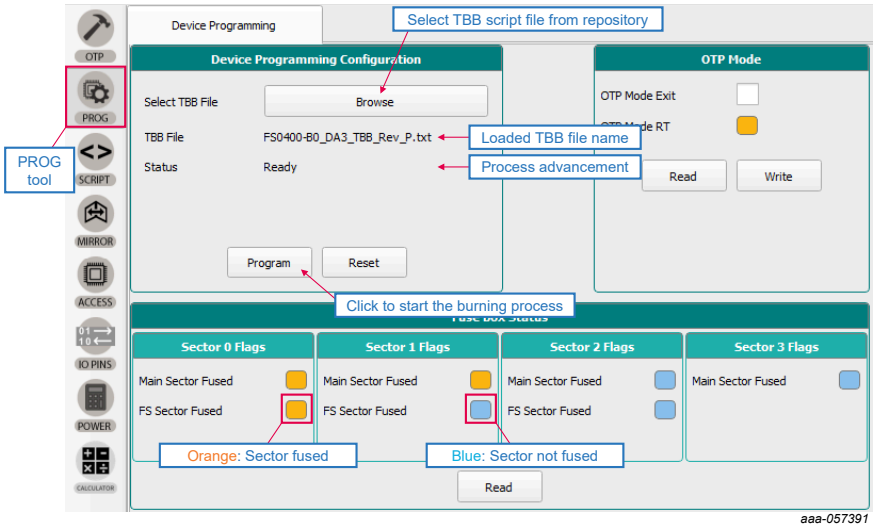

Figure 28. NXP GUI – PROG tool

Warning: *The user can only program parts with the kit during development phase. Customer is not allowed to perform OTP programming for production purposes. Only NXP or a recommended third party are allowed to program the device for production purposes.*

7.7 SCRIPT tool

The **SCRIPT** tool allows the user to create script sequences of commands and to send commands to the device, including reading or writing individually to a register and setting a pin high or low.

The **SCRIPT** tool allows the emulation of an OTP configuration by running a TBB file in the **Script Commands** window.

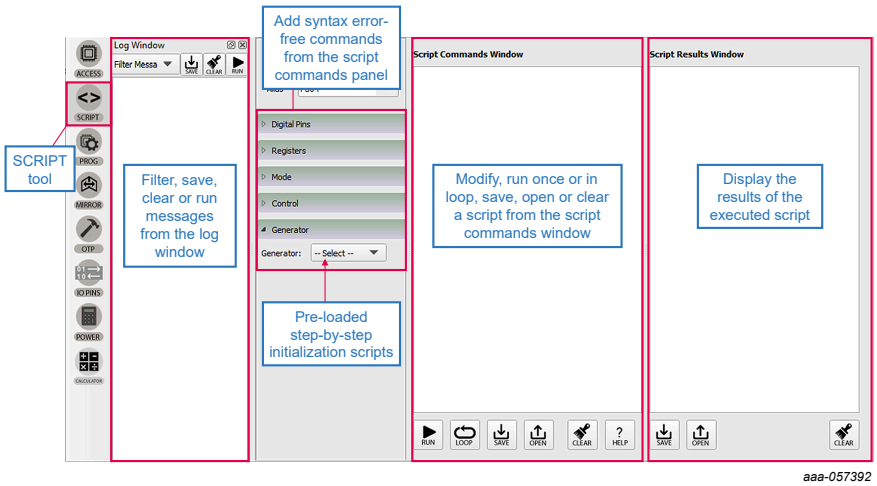

Figure 29. NXP GUI – SCRIPT tool

7.7.1 How to use the script tool

Clicking on any tab from the script command panel brings up the corresponding command parameters. Clicking on the parameter or hitting Enter on the keyboard enters the syntax error-free command in the **Script Commands** window. To execute the commands listed in the **Script Commands** window, click **RUN** in the script

bar. The log window lists events as they occur in real time when the script is executing, and shows the CRC for each sent or received frame. The command results are displayed in the **Script Results** window.

7.8 MIRROR tool

The **MIRROR** tool allows the user to write and read in the mirror registers, assuming the device is in Test mode. The user can define a new OTP configuration, import an already defined OTP configuration, or modify the OTP configuration of an already programmed part after reading the registers first.

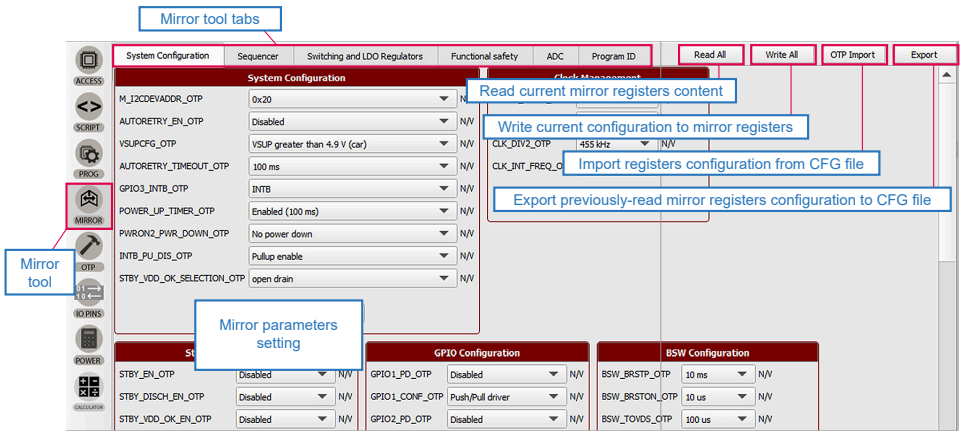

Figure 30. NXP GUI – MIRROR tool

7.9 ACCESS tool

The **ACCESS** tool contains all the functional registers of the device. Two formats are available in this tool with the same content:

- The register map, providing a direct access register per register
- The thematic tabs, providing a thematic order and a more friendly way to operate the registers

In particular, the user can use this tool to write to the functional registers during the initialization phase or during Normal mode. The user can read and check all the main and safety functional configuration and flags.

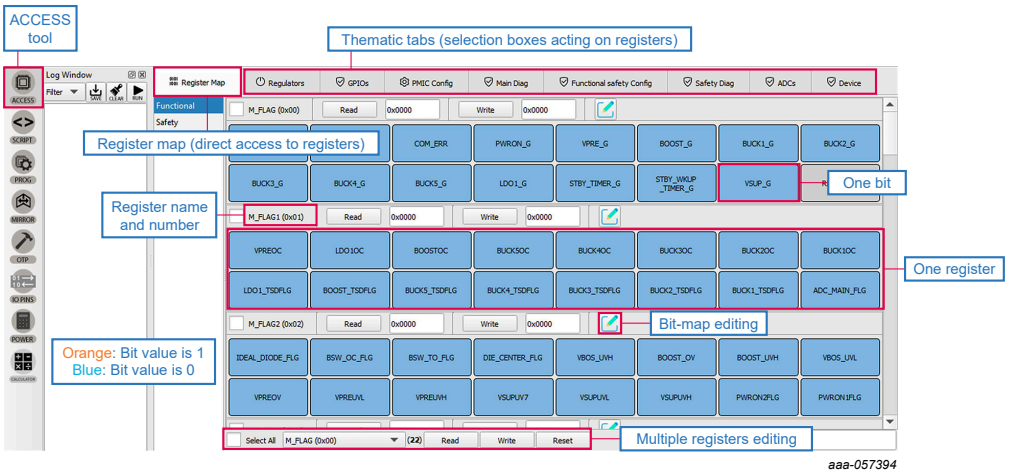

Figure 31. NXP GUI – ACCESS tool

7.10 IO PINS tool

The **IO PINS** tool allows the user to:

- Read the FS04 I/Os
- Control the FS04 I/Os
- Send the safe standby request: the I^2C message + the standby pin toggle
- Generate a standby pulse signal
- Generate a standby wake-up signal

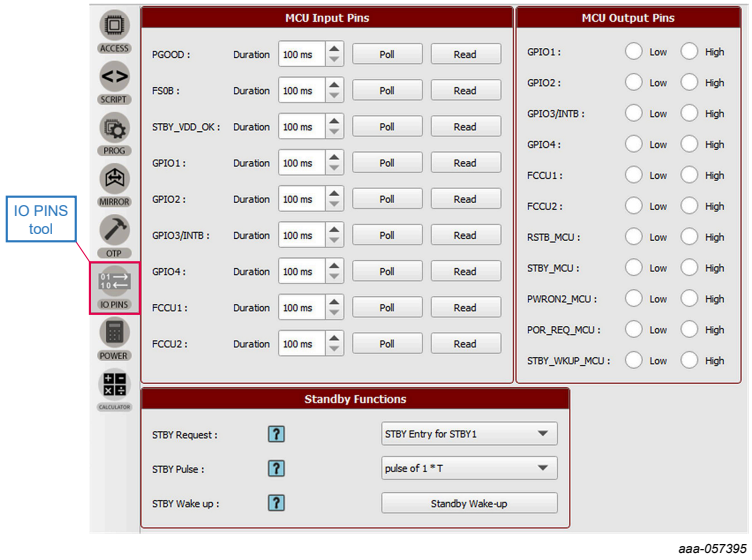

Figure 32. NXP GUI – IO PINS tool

7.11 CALCULATOR tool

The **CALCULATOR** tool allows the user to calculate the overvoltage or undervoltage thresholds for ADC1 and ADC2 monitoring.

From the output voltage and the desired undervoltage and overvoltage thresholds in percentage, the calculator computes the binary or hexadecimal values to be written to the corresponding OV/UV registers.

The calculator also converts the hexadecimal value of the undervoltage or overvoltage thresholds to decimal format.

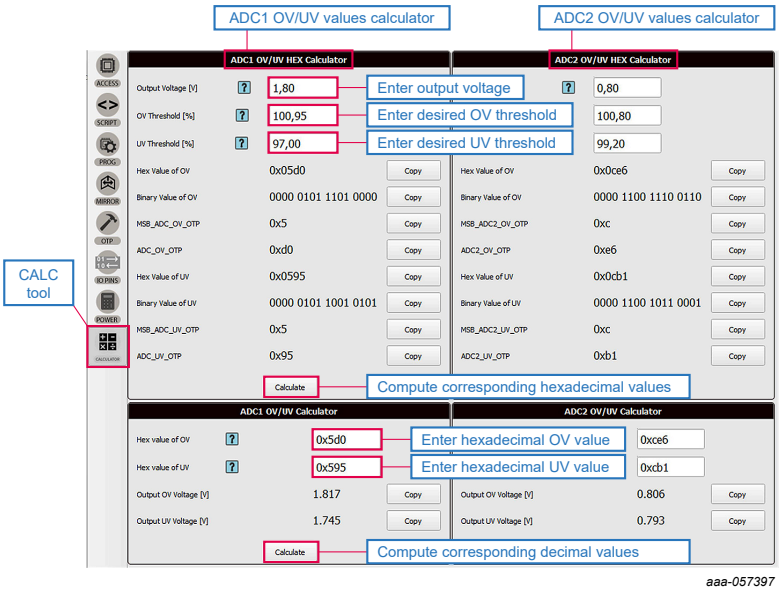

Figure 33. NXP GUI – CALCULATOR tool

Note: *The **Calculate** button must be clicked each time the user changes the input values.*

8 Running the evaluation kit

The flowcharts in this section detail the Power-up sequence in the operation modes offered by the evaluation kit: Normal mode, Debug mode and OTP/Test mode. Debug and OTP/Test modes are provided as means for engineering evaluation of the FS04 device.

8.1 Hardware conditions for operation modes

A certain voltage level on the VDDOTP pin is one condition to enter a given operation mode. Table 6 gives the hardware configuration conditions to enter Normal, Debug or OTP/Test mode.

Table 6. Mode entry hardware conditions

	Switch and jumper configuration		
	Normal mode	**Debug mode entry**	**OPT/Test mode entry**
J8	Open	Closed	Closed
SW4	Open	Open	Closed

8.1.1 Navigating the operation modes

The actions required to navigate the operating modes are summarized in Figure 34.

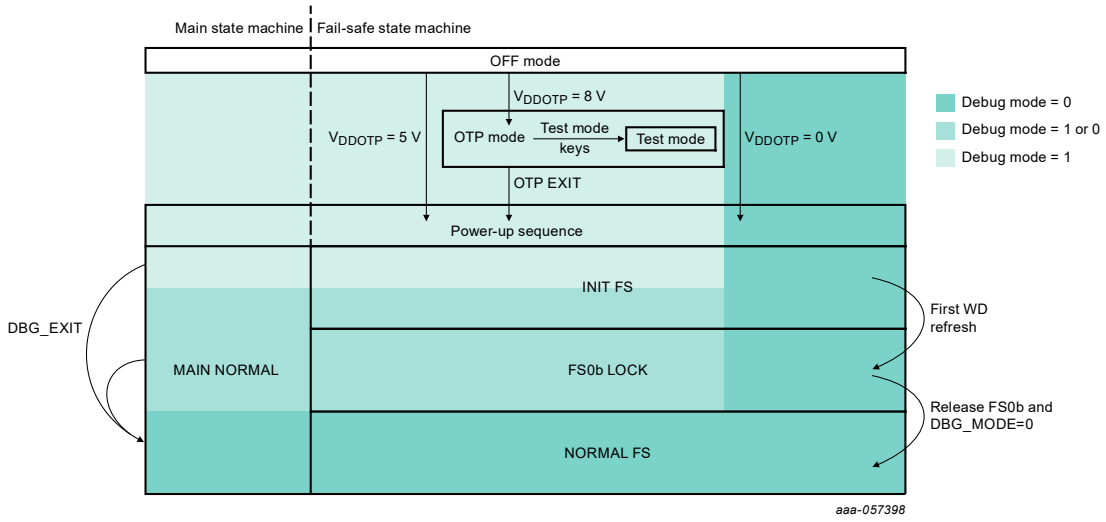

Figure 34. Actions required to change mode

8.1.2 Accessing the configuration layers

There are two layers of configuration on the device:

- OTP configuration, the basis configuration fused in the device
- General device configuration, reprogrammable during the product's operation

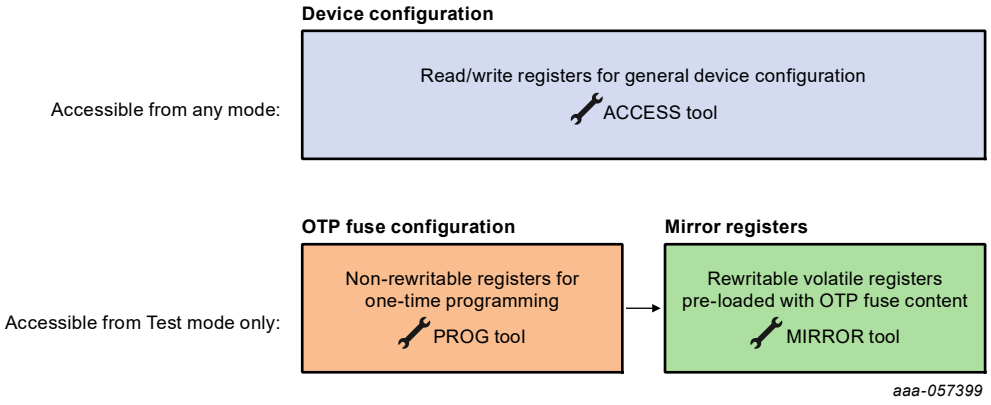

Figure 35. Configuration layers

The OTP configuration is made using the OTP tool. This OTP configuration can then be used as a CFG file to load the Mirror registers using the MIRROR tool, or exported to a TBB file to be fused using the PROG tool.

8.2 Normal mode

In application mode, the VDDOTP pin is connected to GND. The device powers up with full functionality, including all the safety features. When powering up in Normal mode, a first watchdog refresh is required before the watchdog initialization timeout WD_INIT_TIMEOUT is reached. This first watchdog refresh closes the INIT_FS phase.

The user can start directly in Normal mode if the FS04 part soldered on the EVB is programmed.

8.2.1 Normal mode entry procedure

To start the device in Normal mode, follow the steps in Figure 36.

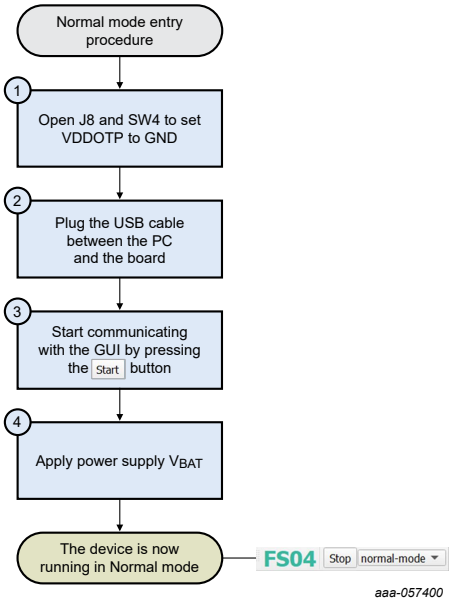

Figure 36. Normal mode entry procedure

As the device is in Normal mode, the I^2C addresses for main and fail-safe registers will be the ones configured in the OTP configuration. These I^2C addresses should be configured in the connection toolbar of the GUI.

During start-up in Normal mode, the device automatically enters the INIT_FS initialization phase. The INIT_FS state is open for an OTP-programmable window of time, and must be closed by the first good watchdog refresh before the window times out.

The user can now write and read in all the functional registers and change or read the IOs values.

8.2.2 Normal mode power-up flowchart

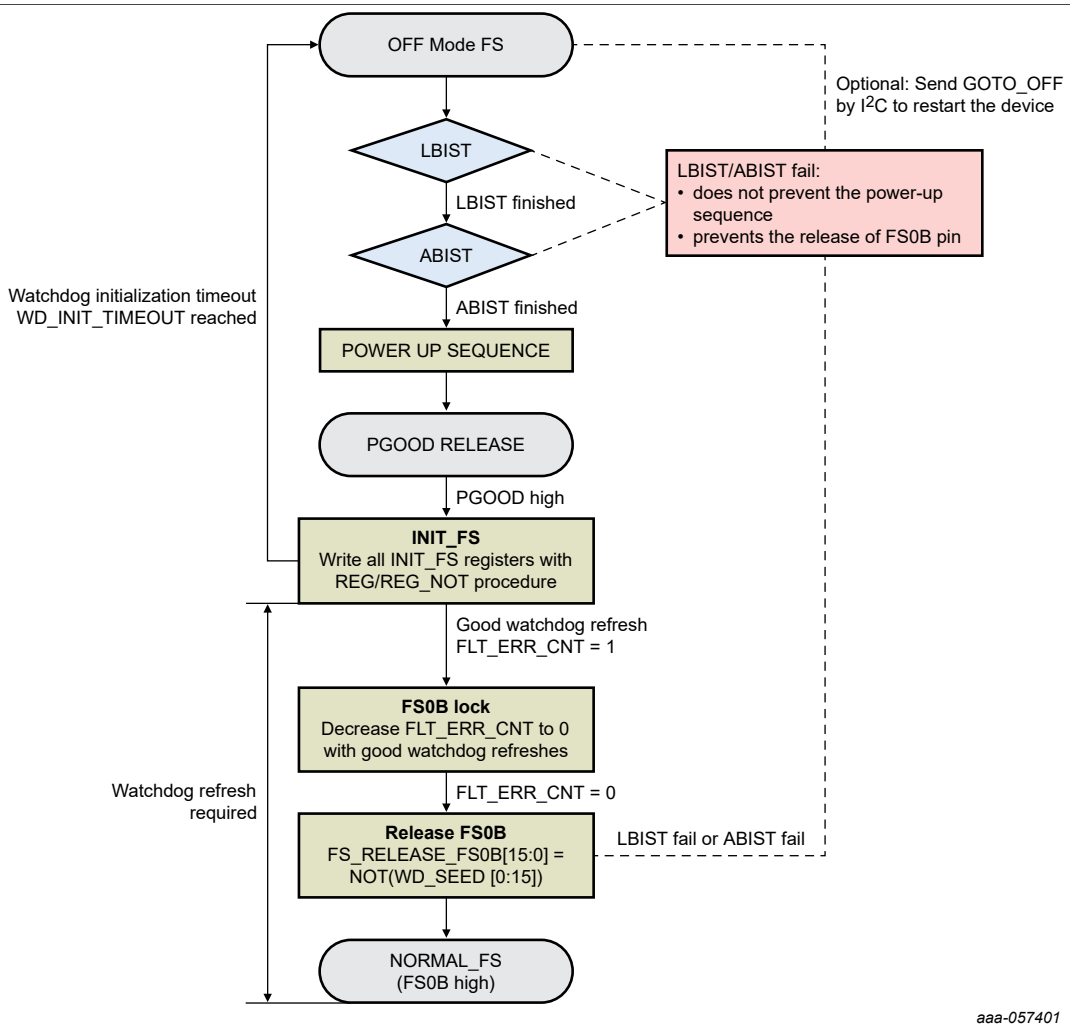

Figure 37. FS04 power-up flowchart in Normal mode

8.3 Debug mode

Debug mode allows the user to power up the device with limited safety functions, as a means for evaluating the device. The following functions are limited when running in Debug mode:

- The watchdog window is fully opened
- The initialization timeout during INIT_FS is disabled
- The Deep Fail-safe (DFS) request from the fail-safe state machine (DFS = 1) is masked
- The eight-second timer monitoring the PGOOD pin is disabled
- The fail-safe output pin FS0B cannot be released
- The FCCU pins are not monitored

- The POR_REQ pin is not monitored

The user can start directly in Debug mode if the FS04 part soldered on the EVB is programmed.

8.3.1 Debug mode entry procedure

To power up the FS04 in Debug mode, follow the steps in Figure 38.

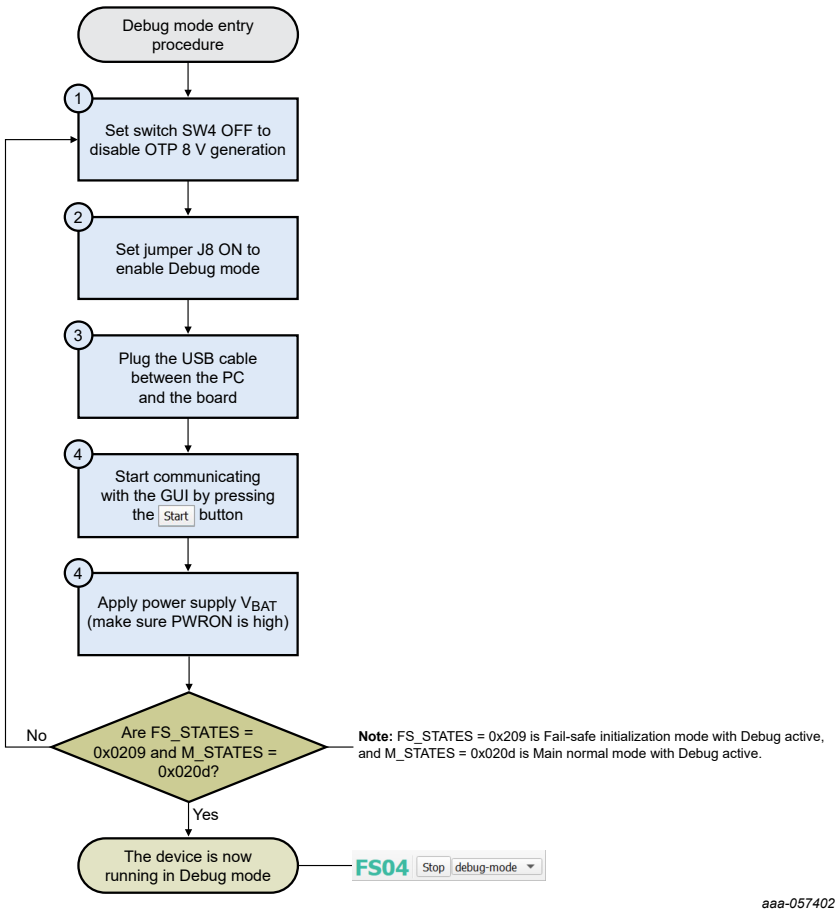

Figure 38. Debug mode entry procedure

The user can now read and write in the functional registers and read or control the IOs of the FS04.

8.3.2 Debug mode exit procedure

To exit the FS04 Debug mode, follow the steps in Figure 39.

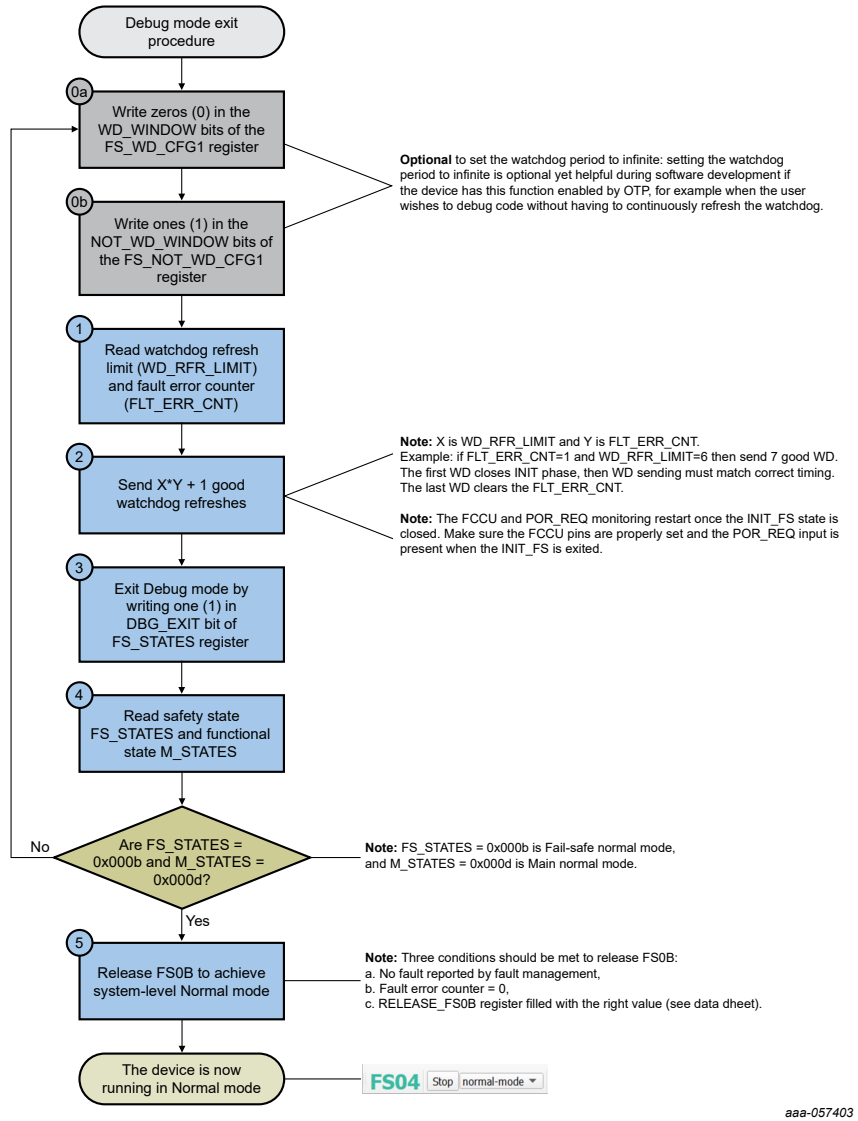

Figure 39. Debug mode exit procedure

Note: *Taking off the Debug Selection jumper J8 will not automatically deactivate Debug mode, as 5 V on the VDDOTP pin is only a condition for Debug mode entry, not a condition to remain in Debug mode.*

8.3.3 Debug mode power-up flowchart

When starting in Debug mode, the INIT_FS timeout window is kept open, and the first good watchdog refresh will close the INIT_FS state.

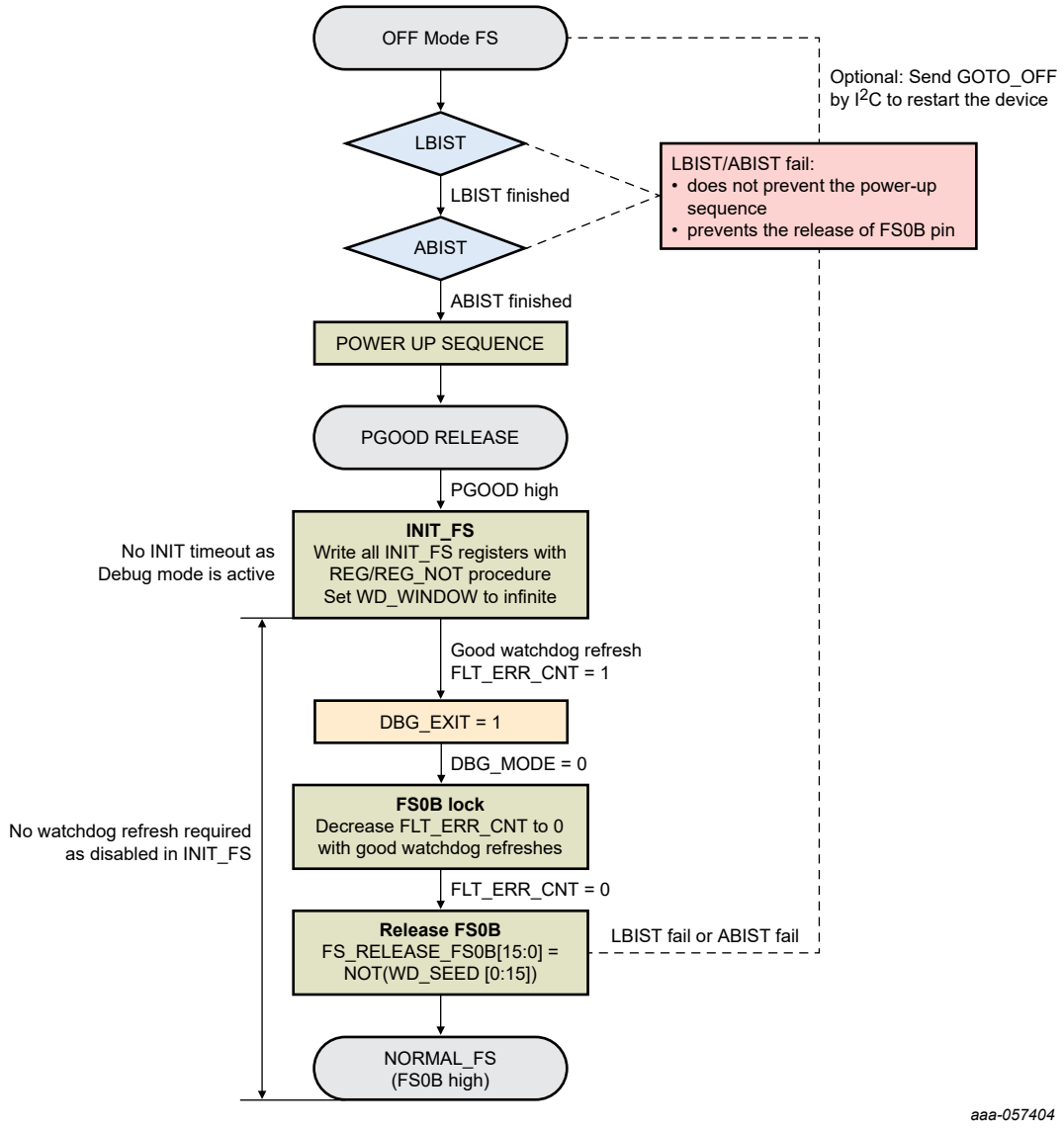

Figure 40. FS04 power-up flowchart in Debug mode

Note: *To allow FS0B to be released from a startup in Debug mode, use I²C to disable the watchdog before INIT_FS closure and Debug mode exit. Otherwise, FS0B remains stuck low in Debug mode.*

8.4 OTP/Test mode

OTP mode is a transition mode to access Test mode. From OTP mode, sending the required I²C keys allows the FS04 to enter Test mode. From Test mode, the user can access the OTP register set, modify the registers to test device functions, and program the OTP configurations.

The user can start in OTP/Test mode whether the FS04 part placed on the EVB is programmed or not. Starting in OTP/Test mode is mandatory if the part is blank.

8.4.1 OTP/Test mode entry procedure

To enter the FS04 Debug mode, follow the steps in Figure 41.

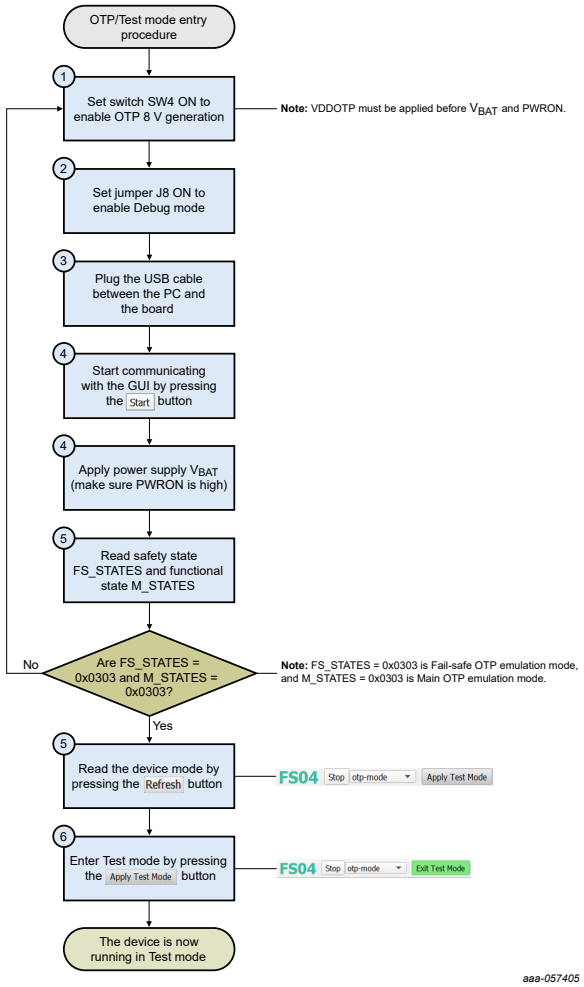

Figure 41. OTP/Test entry procedure

Once Test mode is entered, usually the user will perform OTP emulation. To perform OTP emulation, the next step is to use the **MIRROR** tool in the GUI. Using the **Read All** button on the top right corner, the user can read the currently programmed OTP configuration. If the part is blank, all the registers are set to 0.

The user can load a new OTP configuration in the Mirror registers using the **OTP Import** button on the top right corner, or manually change any of the parameters. Press **Write** or **Write All** to overwrite the parameters in the Mirror registers of the device.

Note: *Use the device guidelines application note or contact the NXP support team to define the OTP configuration.*

8.4.2 OTP/Test mode exit procedure

To power up the device with the newly entered configuration, select Normal mode or Debug mode from the mode menu in the connection toolbar, or switch off SW4 and remove J8 to apply GND to the VDDOTP pin.

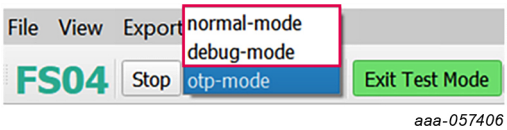

Figure 42. Exit Test mode

The device has now powered up with the newly loaded configuration, and is running in the chosen mode. Press the **Refresh** button in the connection toolbar to check that the device is in the expected mode. If necessary, follow the Section 8.3.2 to enter system-level Normal mode.

Check the FS_STATES and M_STATES in the device status bar.

- In the main registers, the device should be in M_NORMAL
- In the fail-safe registers, the device should be in INIT_FS

The user can now read and write in the functional registers, and read or control the IOs of the FS04. If Debug mode was chosen, refer to the previous section about Debug mode.

8.4.3 OTP/Test mode power-up flowchart

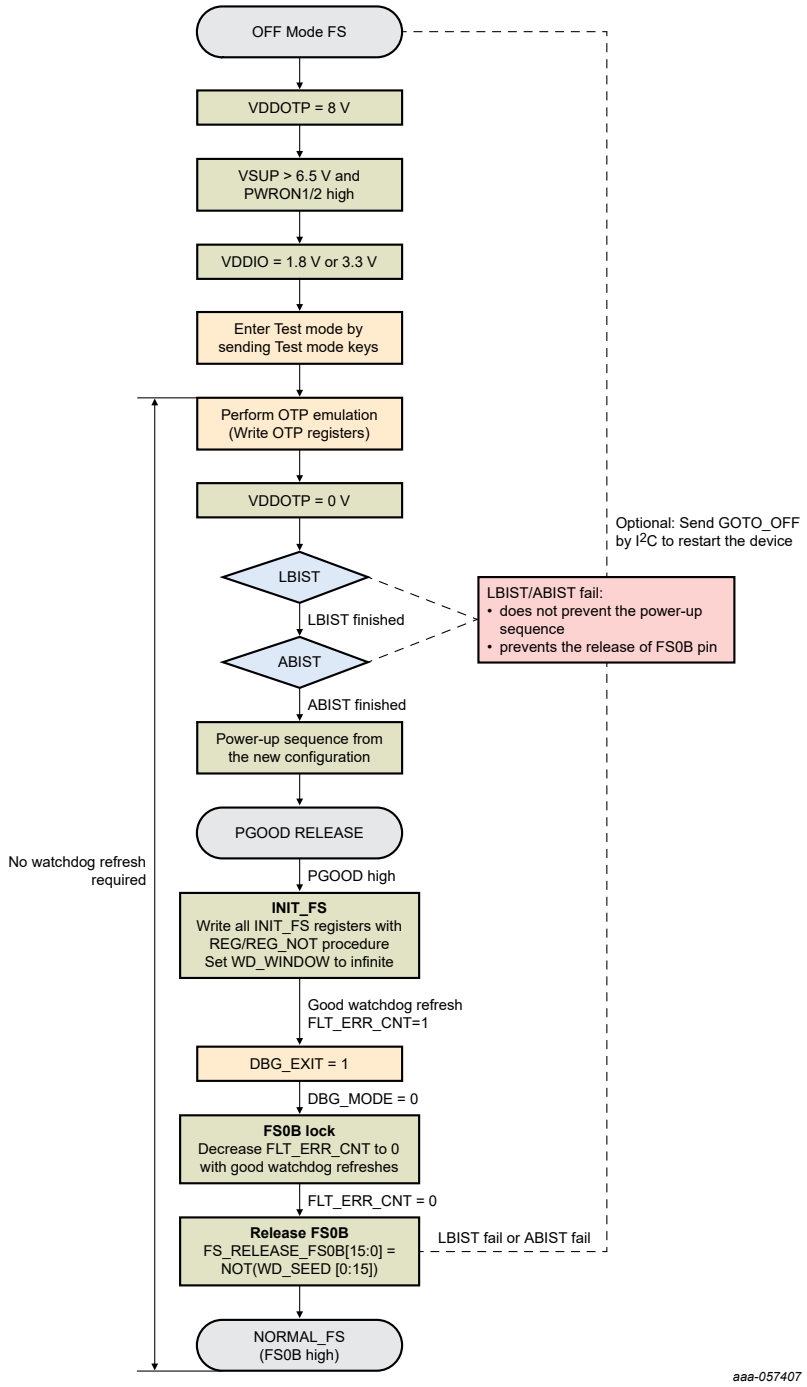

Figure 43. FS04 power-up flowchart in OTP/Test mode

8.5 Programming procedure

Warning: *The user can only program parts with the kit during the development phase. Customer is not allowed to perform OTP programming for production purposes. Only NXP or a recommended third party are allowed to program the device for production purposes.*

Device programming can only take place once on the device.

The programming procedure is done using the **PROG** tool to permanently burn the OTP fuses with the customer's OTP configuration from a TBB file. The TBB file needs to be exported from the OTP tool (Framework settings menu > Import/Export item > TBB) or provided by NXP.

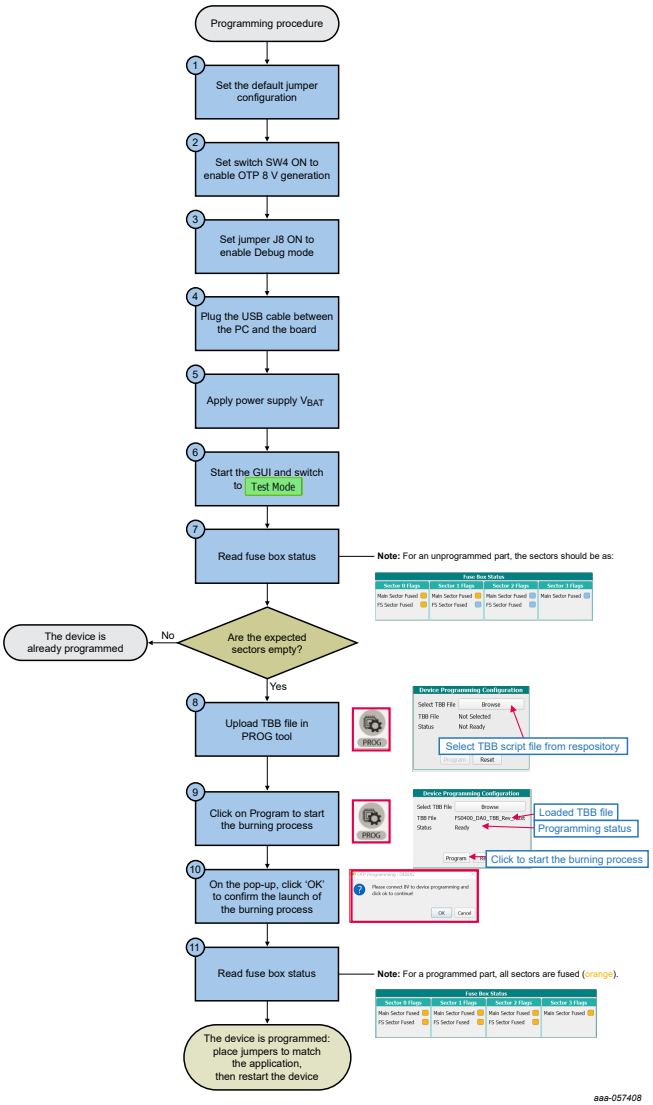

Figure 44. Programming procedure

9 References

1. **KITFS0400A0EVM** — detailed information on this board, including documentation, downloads, and software and tools: https://www.nxp.com/products/FS04
2. **FS04**— detailed information on FS04, high- voltage ASIL D PMIC for the S32N processor: https://www.nxp.com/products/FS04
3. **FS04 data sheet** — detailed information on data sheet: https://www.nxp.com/products/FS04#documentation
4. **FS04 device design guidelines** — detailed information on device design guidelines: https://www.nxp.com/products/FS04#documentation

10 Revision history

Table 7. Revision history

Document ID	Release date	Description
UM12182 v. 3.0	4 June 2026	Corrected title
UM12182 v. 2.0	24 April 2026	• Updating to match rev. D evaluation boards • Changed security level from confidential to public • Revised Section 2 • Revised Kit contents • Revised Section 3.4 • Revised Section 3.5 • Reordered sections under Section 4 • Renamed *Connectors* section to Section 4.3 and removed list of connectors • Revised and renamed figure *Locations of connectors and LEDs* to Figure 1 • Created new Section 4.4 section with list of connectors • Revised Section 4.5 • Revised Figure 2 • Revised Section 4.6, removing figure *Evaluation board jumper and switch locations with default configuration* • Revised Table 3 • Revised Table 4 • Revised and renamed Section 4.9, previously *VDDIO selection (J16/J17)* • Revised Figure 3 • Revised Figure 2 • Revised Table 5 • Revised Section 4.11 • Revised Section 6.1 • Revised Section 6.2 • Revised Figure 18 • Revised Section 7.2.1 • Revised Section 7.2.3 • Removed *POWER tool* section, along with its figure • Revised Figure 37 • Revised Section 8.3.2 • Revised Figure 40 • Corrected name of Figure 41 (it was *Debug mode entry procedure*) • Revised Section 8.4.2 • Revised Figure 43 • Revised Section 8.4.2 • Revised Section 9
UM12182 v 1.0	1 November 2024	• Initial version

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Tables

Figures

Contents