UM12180

NAFEx3352 Evaluation Board User Manual

Rev. 2.0 — 7 November 2025 **User manual**

Document information

Information	Content
Keywords	SPI-bus, NAFEx3352, NAFE33352, NAFE93352, analog front-end, ADC, RTD, TC
Abstract	The NAFEx3352 evaluation board is designed to test NAFE33352 (low power) and NAFE93352 (high speed). NAFEx3352 is a software configurable universal input/output Analog Front End (UIO-AFE) that meets high-precision measurement and control requirements for industrial-grade applications. The NAFEx3352 family offers 14/16/18-bit DAC and a 16/24-bit ADC, low-drift voltage reference, variants integrated with low-offset drift buffers, high-voltage, high-precision amplifiers. This evaluation board, along with the LPC54S018 MCU (with custom firmware) board, provides an easy-to-use evaluation platform for both low power NAFE33352 and high speed NAFE93352.

1 Introduction

The NAFE33352-EVB/NAFE93352-EVB is designed to test the NAFE33352/NAFE93352, which are software-configurable universal Analog Input and Output (AIO) Analog Front-End (AFE) that meets high-precision measurement and control requirements of industrial-grade applications. The EVB hardware design for both the flavor is the same with only the device assembly to be either NAFE33352 or NAFE93352 as the variant ordered. Therefore, we are using the NAFEx3352-EVB term to represent both the EVB flavors throughout this document.

The NAFEx3352 is a highly integrated device, which includes a precision 14/16/18-bit Digital-to-Analog Converter (DAC) and a 16/24-bit Analog-to-Digital Converter (ADC), a low-drift voltage reference, low-offset drift buffers, and high-voltage and high-precision amplifiers with a 70 V input-protection circuit for Electromagnetic Compatibility (EMC) and miswiring scenarios, enabling software-configurable universal analog inputs and outputs. This evaluation board, along with the LPC54S018 MCU (with custom firmware) board, provides an easy-to-use evaluation platform.

A graphical interface allows the user to explore the different functions of the driver. The Integrated Circuit (IC) communicates to the host via the industry-standard SPI bus port. The evaluation software runs under Microsoft Windows 7, 8, and 10 PC platforms.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling. You must use a ground strap or touch the PC case or other grounded source before unpacking or handling the hardware.

2 Finding the kit resources and information on the NXP website

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on http://www.nxp.com.

The information page for the NAFE33352-EVB/NAFE93352-EVB is available at https://www.nxp.com/design/design-center/development-boards-and-designs/NAFE33352-EVB. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a Getting Started tab. The Getting Started tab provides quick-reference information applicable to using the NAFEx3352 evaluation board, including the downloadable assets referenced in this document.

3 Getting ready

This section goes over the prerequisites for EVB bring up.

3.1 Kit contents

The KITNAFEx3352-EVB contents include:

- Assembled and tested the evaluation board in an antistatic bag
- USB cable
- 24 V AC-DC power adapter
- Ferrite block for power adapter
- LPC54S018-EVK with NAFE firmware (included in KIT flavor)

3.2 Assumptions

Familiarity with the SPI-bus is helpful, but not required.

3.3 Minimum system requirements

- PC Pentium processor (or equivalent)
- One USB port (either 3.0 or 2.0 compatible)
- Windows 7, 8, or 10
- LPC54S018-EVK MCU evaluation board (from www.nxp.com)

3.4 Power requirements

For the NAFEx3352 setup, connect the PC to USB port J2 out of the three USB ports J1, J2, and J3 to power up the LPC54S018-EVK MCU evaluation board.

4 Getting to know the hardware

This section gives overview of the KIT with the main components used in the EVB design and how to power it up using AC-DC wall adapter or bench top power supply.

4.1 Kit overview

The NAFEx3352 evaluation kit includes an NAFEx3352 evaluation board, an LPC54S018 evaluation board with custom firmware, and a USB cable.

Use the following steps to set up the hardware:

1. Firmly connect the NAFEx3352-EVK (AIO-AFE) evaluation board to the LPC54S018 (microcontroller) evaluation board using the Arduino connectors.
2. To connect both boards, slide the J200, J202, J204, and J206 male connectors at the bottom side of the NAFEx3352-EVK (AIO-AFE) board into the appropriate female connectors on the LPC54S018 (microcontroller) board.
3. Plug in the supplied 24 V AC-DC power adapter to J308 to power up the device. Install the ferrite block at the end of the AC-DC power cord (where it makes connection to the NAFEx3352EVB) to maintain EMC compliance. Make sure J309, J310, and J311 are jumped for 2-3 position (south).
4. Apply AVDD/DVDD = 3.75 V on J300, HVDD = 15.4 V on J301, and HVSS = -15.4 V on the J302 banana jack connectors and turn on the power supply.
5. Connect the USB to the µUSB cable between the USB port of the computer and the J2 (µUSB) port of the LPC54S018 evaluation board.

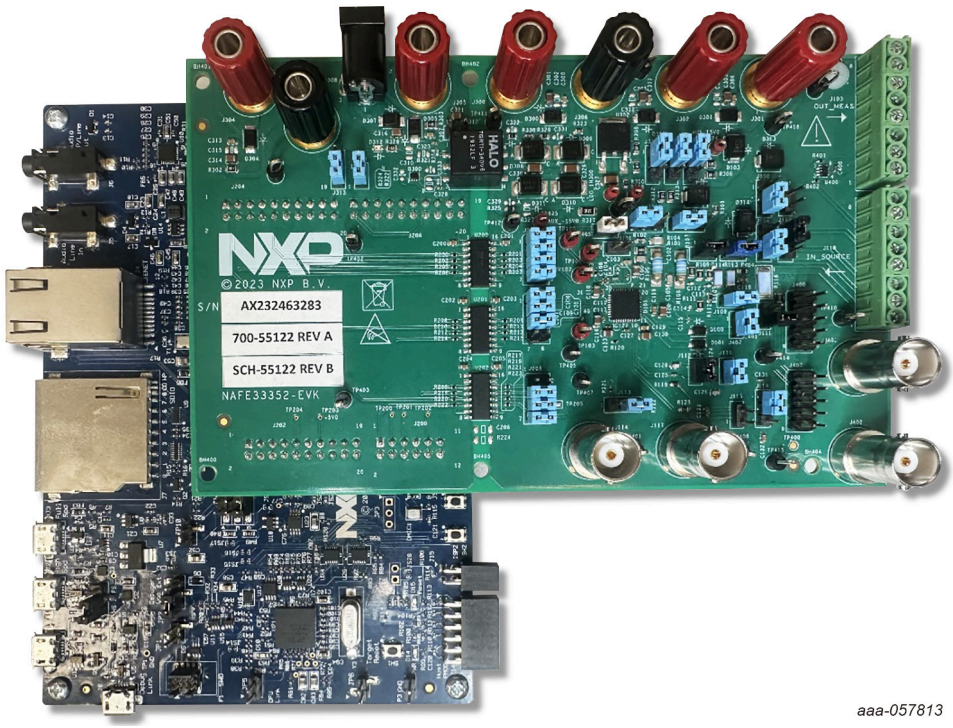

Figure 1. NAFE33352 evaluation board paired with LPC54S018-EVK board

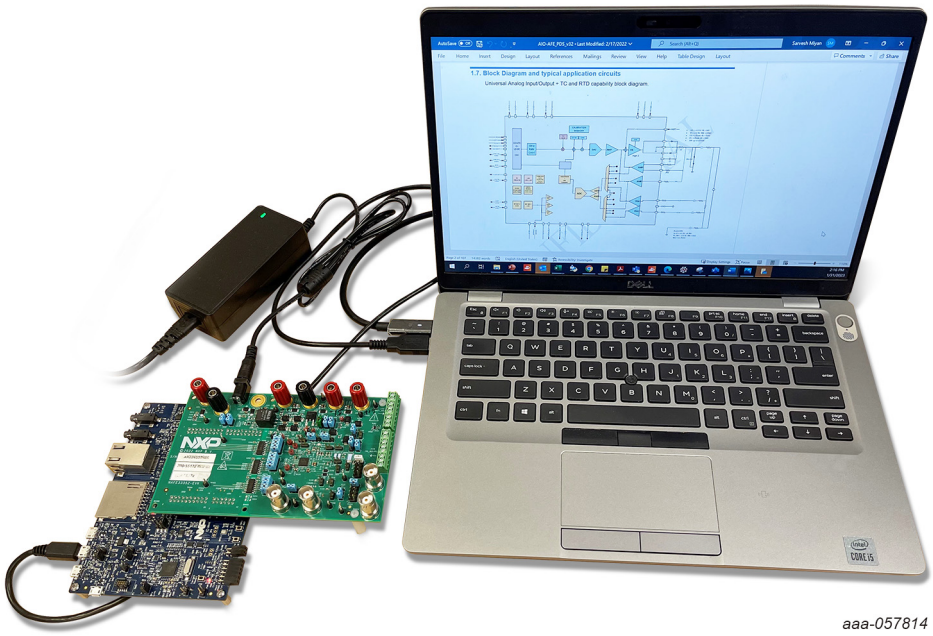

Figure 2. NAFE33352 evaluation board paired with LPC54S018-EVK board

4.2 Kit featured components

Table 1. NAFEx3352 evaluation board main components

Device	Description	Location
NAFE33352/NAFE93352	SW-configurable universal AIO-AFE	U101
MAX13256ATB	Transformer driver	U303
TGMR-340V6LF	Transformer	U301
MAX14930	Four-channel unidirectional digital isolators	U201
MAX14432	Four-channel bidirectional digital isolators	U202
MAX6126	Low-noise voltage reference	U300
CMLDM7002AG	N-channel MOSFET	Q300
LP2950ACDT-3P3RG	3.3 V LDO	U302

4.2.1 Jumpers

Table 2. Jumper settings for external power supply (3.75 V, 15.4 V, -15.4 V)

Setting	Jumper	Comment
EXT_3V3	J310 pin 1 – 2	External 3.3 V power selection
EXT_-15V0	J311 pin 1 – 2	External -15 V power selection
EXT_15V0	J309 pin 1 – 2	External 15 V power selection

Table 3. Jumper settings for AC-DC adapter/transformer power supply (3.75 V, 15.4 V, -15.4 V)

Setting	Jumper	Comment
3V3_LDO	J310 pin 2 – 3	AC-DC adapter/transformer 3.3 V power selection
TX_-15V0	J311 pin 2 – 3	AC-DC adapter/transformer -15 V power selection
TX_15V0	J309 pin 2 – 3	AC-DC adapter/transformer 15 V power selection

5 Tool interface (GUI) description

1. GUI Installation
2. Unzip the NAFEx3352GUI_installer zip file using a compression utility, such as WinZip, WinRAR, or 7z. Two files with type – “Windows Installer Package” and “Application” are shown.

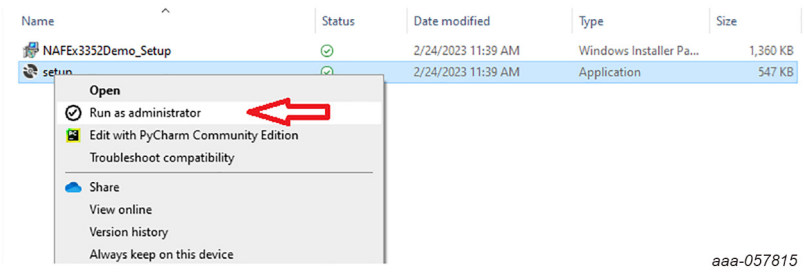

Figure 3. Run as administrator

3. Right click the **setup** application and click **Run as administrator**. Follow the prompts to install the application.
4. Click **Next**.

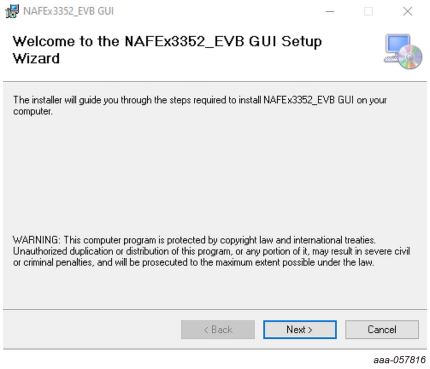

Figure 4. Installation step 1

5. Select **Everyone** and click **Next**.

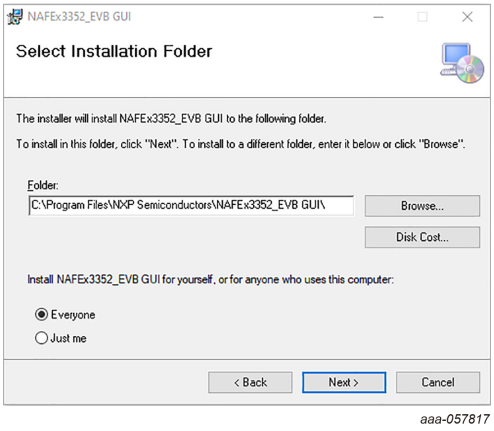

Figure 5. Installation folder selection

6. Click **Close**.

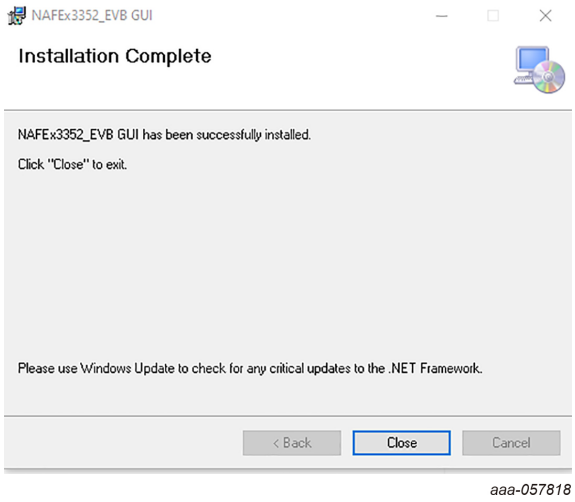

Figure 6. Installation complete

7. On the central command, write NAFE and click the Windows start button at the bottom left. The NAFEx3352Demo application is shown.

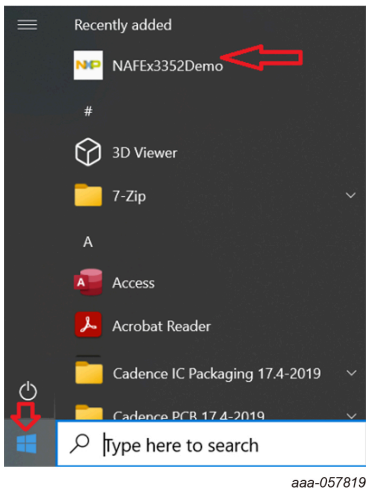

Figure 7. Find the demo GUI

5.1 Connectivity check

1. Click**NAFEx3352 Demo** to open the GUI. If the connection is successful, the user must see on the GUI the MCU board address, the NAFE part number, and type (low-power or high-speed). The below figure shows the part number readback from NAFE33352-EVB:

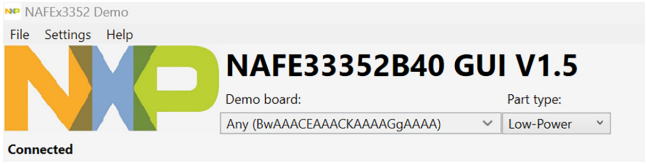

Figure 8. Part readback from NAFE33352-EVB

So, the same GUI used with NAFE933352-EVB reads back the part number from device OTP register as below:

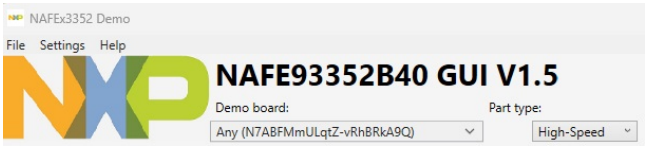

Figure 9. Part readback from NAFE93352-EVB

2. In the absence of proper power to the LPC board or the NAFEx3352 EVB, the GUI is unable to read back the MCU board address or NAFE part number/type. The GUI has a dynamic indicator (marked by a red rectangle below the NXP logo) to show the status of the MCU board connectivity. If it displays **Disconnected**, it means that there is some issue with MCU board connectivity. Check the USB cable connection.

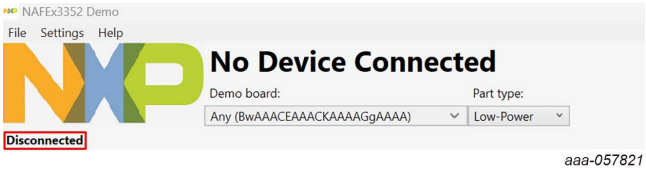

Figure 10. MCU board connection indicator

3. NAFE0000000 means that MCU is not able to read back the part number from EVB. Check the power supply connections of the EVB and if appropriate jumpers are selected as mentioned in Section 4.2.1. The correct NAFE number must be appear as visible in step 1.

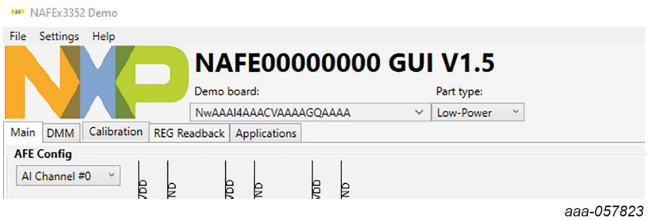

Figure 11. Device read-back error

4. The GUI software sets the SPI clock rate to 8MHz on power up. The SPI clock rate can be changed by clicking **Settings → SPI bitrate → 8 Mbps**.

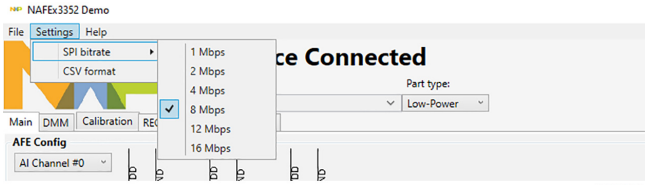

Figure 12. SPI clock rate selector

Note: *The GUI feature and functionality discussed in the following section are applicable to both NAFE33352-EVB and NAFE93352-EVB.*

5.2 Using the tool

Below section describe different section and capabilities of the GUI to evaluate the device functionality and features in all four modes - Voltage Input, Current Input, Voltage Output and Current Output.

5.2.1 GUI

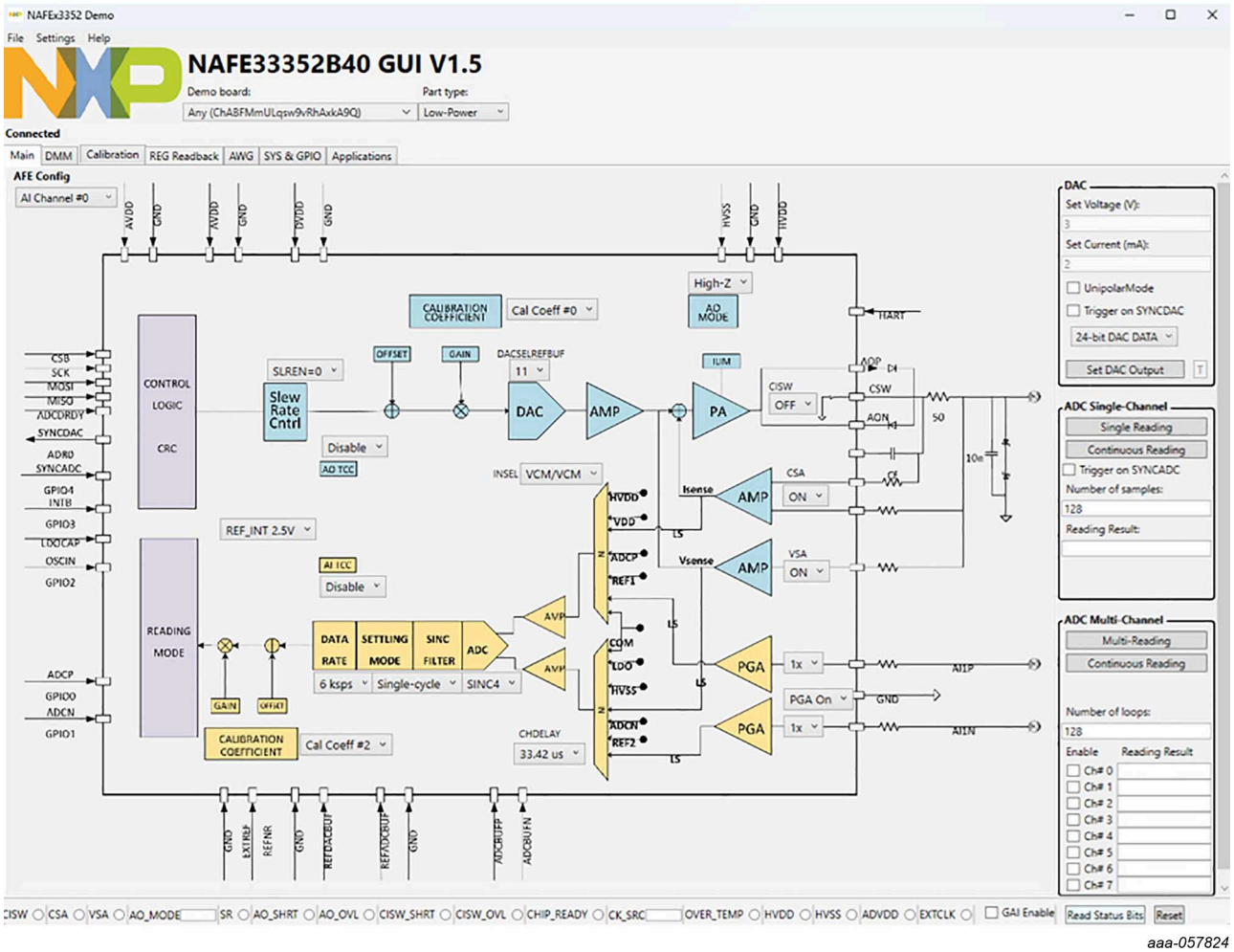

Figure 13. GUI screenshot

Opening the GUI has a default configuration for all parameters.

The main blocks present on the GUI are ADC and DAC.

The ADC block (yellow) allows the user to select analog input settings: PGA gain, input selection, data rate, sinc filter, channel delay, and so on. The actual configuration of the device analog input registers to these selection happens when the user initiates a conversion/reading (single or continuous).

The DAC block (blue) allows the selection of the analog output: slew rate, AIO mode, (Vout/Cout/high-Z), CISW, CSA, and VSA. The user selection is configured and the output is generated at the press of **Set DAC Output**.

5.2.2 Schematic shortcut

It is possible to open the EVKit Schematic directly from the GUI using the menu bar.

Click **Help** → **EVKit Schematic**.

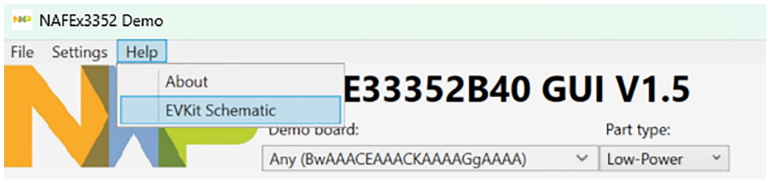

Figure 14. EVB schematic access from GUI

Clicking **EVKit Schematic** opens the schematic in pdf format as shown in Figure 15.

The EVKit schematic provides a detailed blueprint of the electrical components and their interconnections within the evaluation kit. The peripheral and signal-chain components on both Analog Input/Output channels are selected to meet the accuracy/temperature operating requirements of the NAFE33352.

The EVKit schematic is divided into four sections to guide the user through understanding and using the kit.

1. NAFE33352 IC
2. Digital Interface
3. Power supply
4. Measurement Connections and Relay drivers

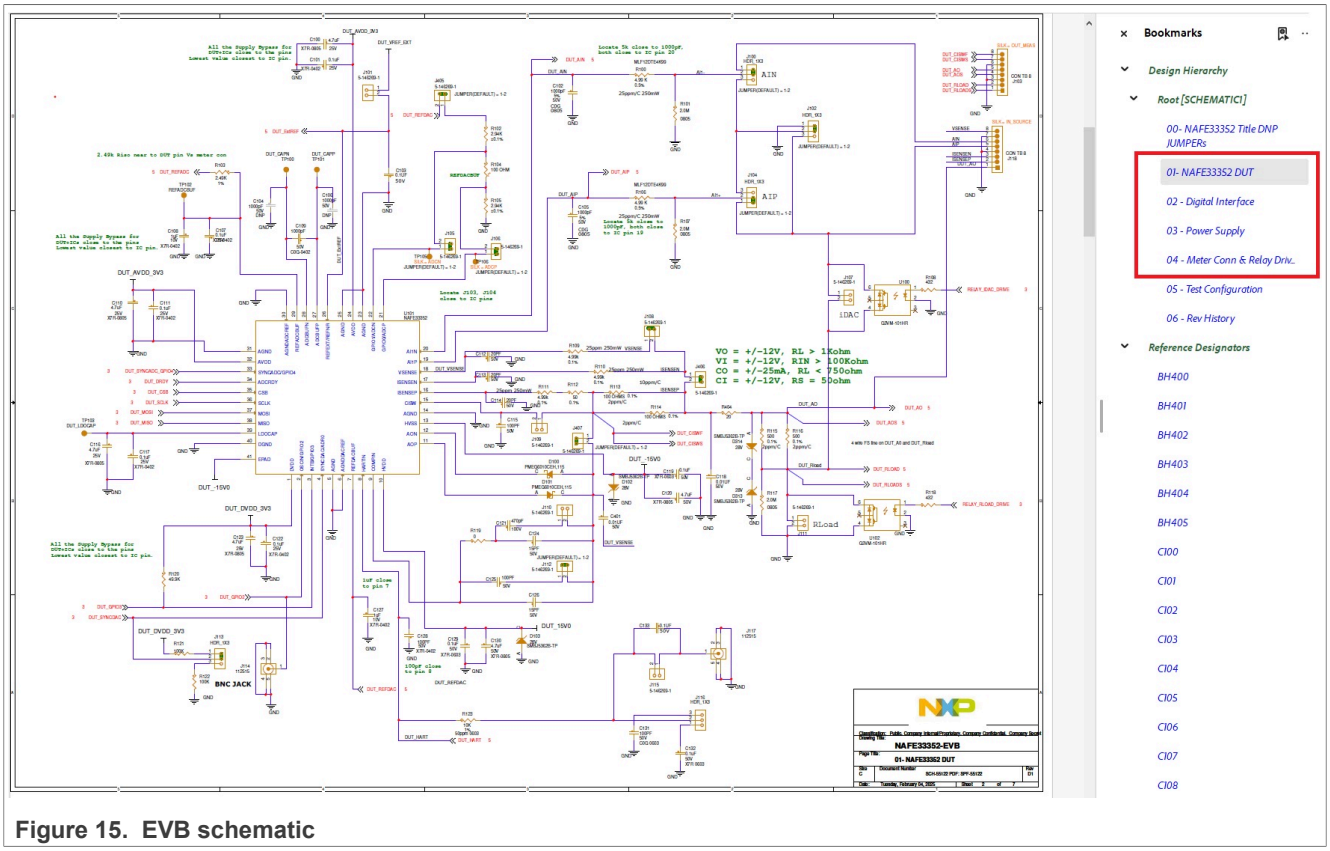

Figure 15. EVB schematic

5.2.3 Channel configuration

1. Select the channel gain using the drop-down menu of the Programmable Gain Amplifier (PGA).

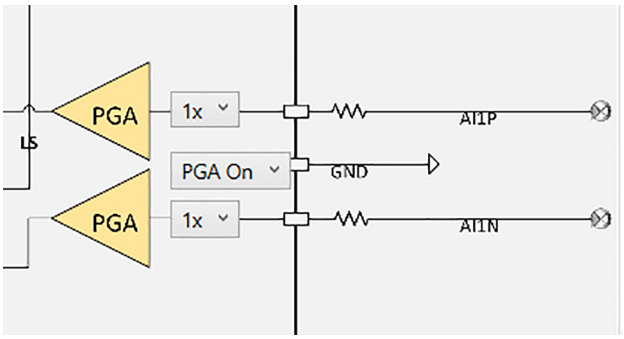

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Figure 16. Analog Input PGA configuration

2. Configure the data rate, SINC filter order, and Settling mode via the corresponding drop-down menu of the ADC.

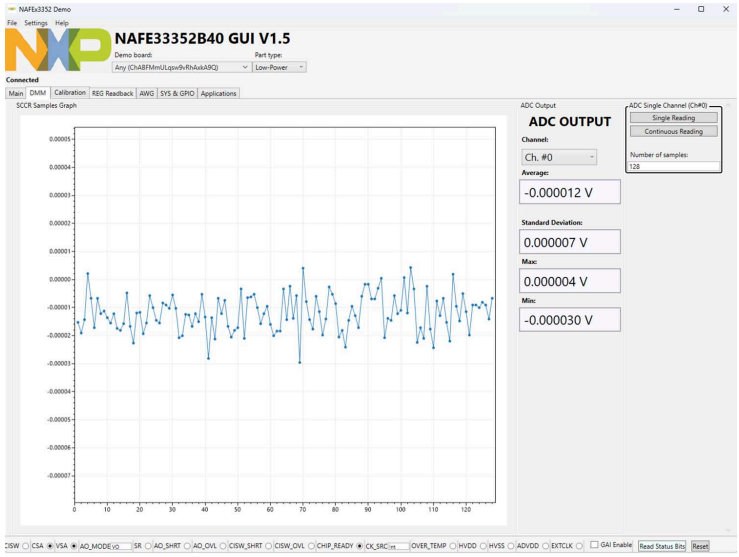

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Figure 17. Analog input data rate, Settling mode, and sinc filter

5.2.4 Conversion modes

Five types of reading (conversion) modes are possible from the device:

1. Single-Channel Single-Reading (CMD_SS)
2. Single-Channel Continuous Reading (CMD_SC)
3. Multichannel Single-Reading (CMD_MS) (available in future revision)
4. Multichannel Multireading (CMD_MM)
5. Multichannel Continuous Reading (CMD_MC)

Refer to the data sheet for more about these conversion modes.

1. Single-Channel Single-Reading
   - Click the **Single Reading** button after picking Inputs to test from the mux drop-down menu.

- Read the input voltage in the Reading Result box.

2. Single-Channel Continuous Reading
   - Enter the number of samples required in the box and click **Continuous Reading**. Once **Continuous Reading** is clicked, a dialog box opens to pick a folder to create a .csv conversion results file on the hard drive with the number of samples requested.
3. Multichannel Multireading
   - Preconfigure the appropriate channels to be sequenced using the AFE configuration drop-down menu and enable those channel numbers accordingly under the Multi-Channel section at the bottom right of the GUI.
   - Click **Multireading**.
   - Read the input voltages in the Reading Result multibox.
4. Multichannel Continuous Reading
   - Preconfigure the appropriate channels to be sequenced using the AFE configuration drop-down menu and enable those channel numbers under the Multichannel section at the bottom right of the GUI.
   - Click **Continuous Reading** and wait for the dialog box to pick the folder to create a .csv conversion results file on the hard drive with the number of samples requested.

5.2.5 Data rate selection

The AI-AFE provides a flexible ADC configuration that enables the user to configure Settling mode, digital SINC filter, and data rate. As reported in the data rate table, the data rate output is a function of the combination of Settling mode, digital SINC filter, and data rate.

The easier way to configure the AI-AFE is:

1. Select the Settling mode (normal or single cycle)
2. Select the digital SINC filter
3. Select the data rate
   For example, to select 9000 sps in Single-Cycle Settling mode and SINC4:

Table 4. ADC data rate (system clock: 4.608 MHz)

		Normal settling					Single-cycle settling				
DRO code	OSR	SINC4	SINC4+ SINC1	SINC4+ SINC2	SINC4+ SINC3	SINC4+ SINC4	SINC4	SINC4+ SINC1	SINC4+ SINC2	SINC4+ SINC3	SINC4+ SINC4
0	8	288000					72000				
1	12	192000					48000				
2	16	144000					36000				
3	24	96000					24000				
4	32	72000					18000				
5	48	48000					12000				
6	64	36000					9000				
7	96	24000					6000				
8	128	18000					4500				
9	192	12000					3000				
10	256	9000					2250				
11	384	6000					1500				
12	512		4500.00	4500.00	4500.00	4500.00		2250.00	1500.00	1125.00	900.00
13	768		3000.00	3000.00	3000.00	3000.00		1500.00	1000.00	750.00	600.00
14	1024		2250.00	2250.00	2250.00	2250.00		1125.00	750.00	562.50	450.00
15	2048		1125.00	1125.00	1125.00	1125.00		562.50	375.00	281.25	225.00
16	4096		562.50	562.50	562.50	562.50		281.25	187.50	140.63	112.50

Table 4. ADC data rate (system clock: 4.608 MHz)*...continued*

17	5760		400.00	400.00	400.00	400.00		200.00	133.33	100.00	80.00
18	7680		300.00	300.00	300.00	300.00		150.00	100.00	75.00	60.00
19	11520		200.00	200.00	200.00	200.00		100.00	66.67	50.00	40.00
20	23040		100.00	100.00	100.00	100.00		50.00	33.33	25.00	20.00
21	38400		60.00	60.00	60.00	60.00		30.00	20.00	15.00	12.00
22	46080		50.00	50.00	50.00	50.00		25.00	16.67	12.50	10.00
23	76800		30.00	30.00	30.00	30.00		15.00	10.00	7.50	6.00
24	92160		25.00	25.00	25.00	25.00		12.50	8.33	6.25	5.00
25	115200		20.00	20.00	20.00	20.00		10.00	6.67	5.00	4.00
26	153600		15.00	15.00	15.00	15.00		7.50	5.00	3.75	3.00
27	230400		10.00	10.00	10.00	10.00		5.00	3.33	2.50	2.00
28	307200		7.50	7.50	7.50	7.50		3.75	2.50	1.88	1.50

4. Select normal settling in the Settling mode drop-down menu.
5. Select SINC 4 in the filter drop-down menu.
6. Select 9000 sps in the data rate drop-down menu.

5.2.6 DMM view tab

DMM tab shows Single-Channel Continuous Read (SCCR) with sample = 128 for selected logical channel. Below, Channel 0 is configured for VCM-VCM.

On DMM, it is possible to analyze the behavior of the signal and report the statistical information as Standard Deviation, max, and min.

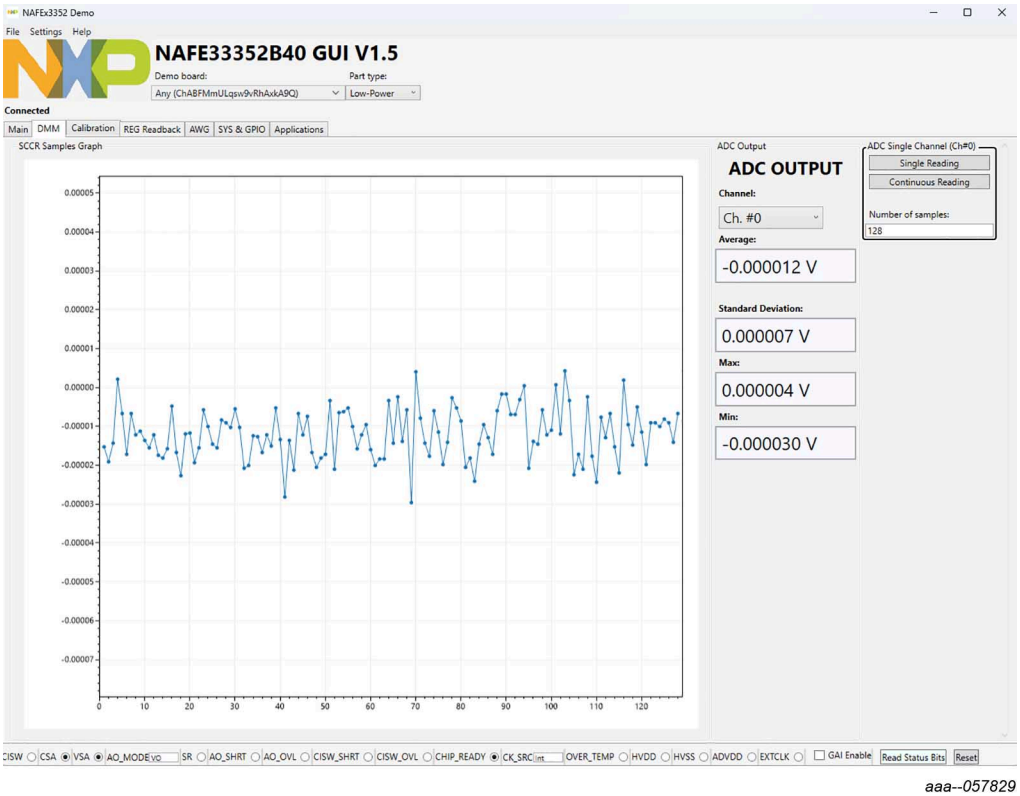

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Figure 18. DMM tab

5.2.7 SYS & GPIO tab

This SYS and GPIO tab provides easy to use blocks to set system level selections like internal vs external reference or clock, General-Purpose Input/Output (GPIO) functionality, and so on. The NAFE33352 includes five GPIOs with dual functionality.

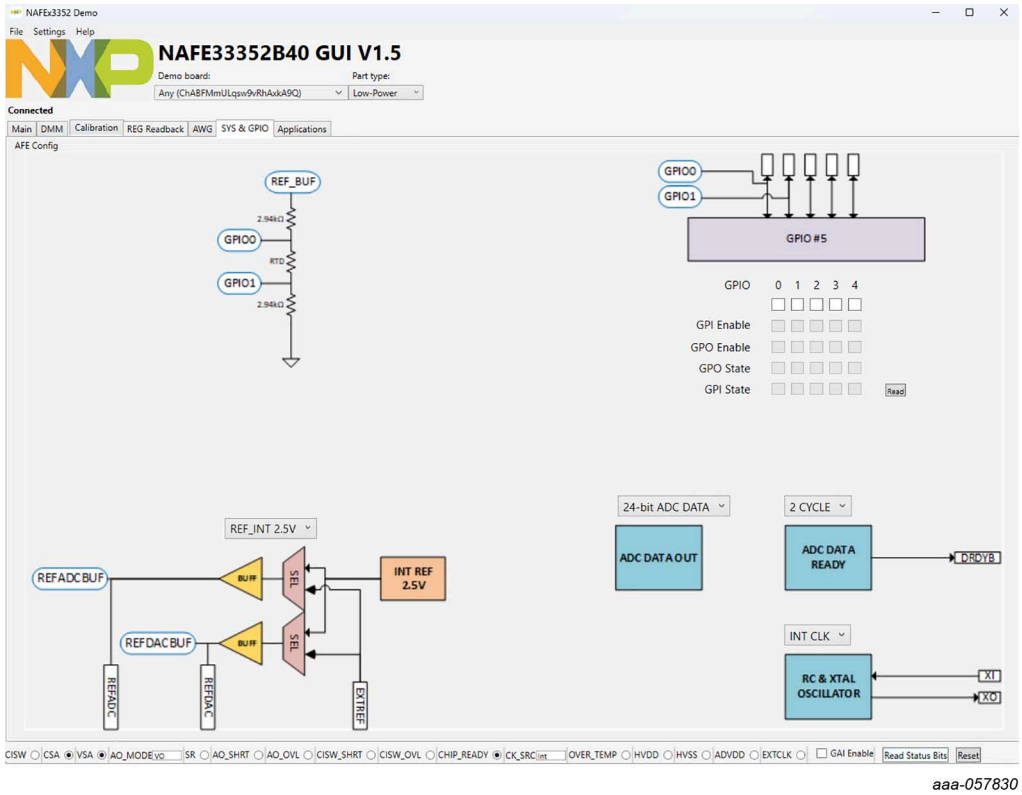

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Figure 19. SYS & GPIO tab

The settings that are possible to change are:

- Reference selection for REF_INT or REF_EXT
- ADC data bit:24 bits or 16 bits
- Clock selection: internal or external
- Data ready signal behavior in 2 cycle or 8 cycle
- GPIO0 and GPIO1 is shared with the ADCP and ADCN that serve as single-ended and differential analog inputs by setting LVMUX. The input common voltage range is from 0.5 V to 2.5 V.

The GPIOs are schematized on the GUI as an array of settings.

The bits that can be accessed from this matrix are:

- **Pin connect:** Should be enabled to use the connected pins as GPIOs.
- **GPI/GPO enable:** Depending on the desired functionality, GPI/GPO must be enabled.
- **GPO state:** Enable or disable this cell to put 1 or 0 on the selected GPIOs.
- **GPI state:** Click **Read** to update the cell states of the GPIOs set as Input.

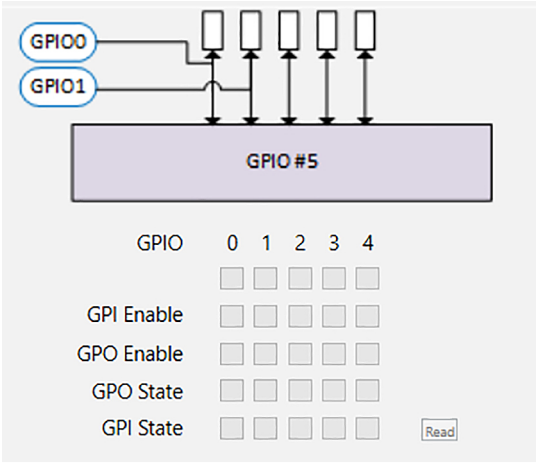


Figure 20. GPIO matrix

5.2.8 AWG tab

The AWG tab provides tools to generate custom waveforms. To create a waveform, adjust the following parameters:

- **AWGAMP_MAX**: This parameter sets the maximum amplitude of the waveform. (Default is 5 V).
- **AWGAMP_MIN**: This parameter sets the minimum amplitude of the waveform. (Default -5 V).
- **STEP AMP**: This parameter defines the amplitude step size for each waveform segment.
- **STEP Freq**: This parameter determines the duration of each waveform segment.
- **HILO TIME**: This parameter specifies the time that the waveform spends at the high and low amplitude levels within a segment.

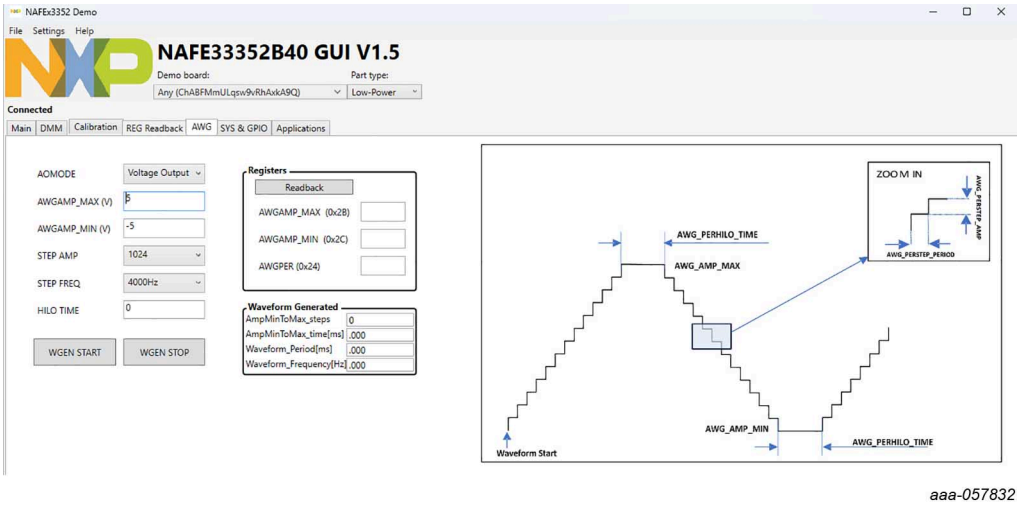


Figure 21. AWG tab

Note: *For some instances with different programming STEP_AMP value, AWG_AMP_MAX, or AWG_AMP_MIN value would not be possible to reach exactly. In these cases, the maximum, minimum code must be clamped to AWG_AMP_MAX, AWG_AMP_MIN value respectively.*

*AMPmintomax_steps = (Amp_max - Amp_min)/(step_size * LSB)*

AMPmintomax_time = (AMPmintomax_steps)/step_freq

Waveform_period = 2(AMPmintomax_time + HILO_time)*

Waveform_freq = 1/Waveform_period

For example:

For 18-bit LSB = (25)/2^18 = 95.367 uV

If Step_size(Code = 0) = 1024, Amp_max = 12.5 V, Amp_min = -12.5 V then AMPmintomax_steps = 256

If step_period(code=0)=4000, then AMPmintomax_time = 0.064 s

If HILO_time = 0, then WF_freq = 7.8125 Hz.

Table 5. Generated waveform frequency with HILO time = 0

Generated waveform frequency (Hz)		STEP_Amp (18-bit)							
		0	1	2	3	4	5	6	7
Code	Step_period (Hz)	1024	2048	4096	8192	16384	32768	65536	131072
0	**4000**	7.8125	15.6250	31.2500	62.5000	125.0000	250.0000	500.0000	1000.0000
1	**6000**	11.7188	23.4375	46.8750	93.7500	187.5000	375.0000	750.0000	1500.0000
2	**9000**	17.5781	35.1563	70.3125	140.6250	281.2500	562.5000	1125.0000	2250.0000
3	**12000**	23.4375	46.8750	93.7500	187.5000	375.0000	750.0000	1500.0000	3000.0000
4	**40000**	78.1250	156.2500	312.5000	625.0000	1250.0000	2500.0000	5000.0000	10000.0000
5	**60000**	117.1875	234.3750	468.7500	937.5000	1875.0000	3750.0000	7500.0000	15000.0000
6	**90000**	175.7813	351.5625	703.1250	1406.2500	2812.5000	5625.0000	11250.0000	22500.0000
7	**150000**	292.9688	585.9375	1171.8750	2343.7500	4687.5000	9375.0000	18750.0000	37500.0000

The main buttons to generate the AWG are **WGEN START** and **WGEN STOP**. To start and stop the waveform generation, use **WGEN START** and **WGEN STOP**, respectively.

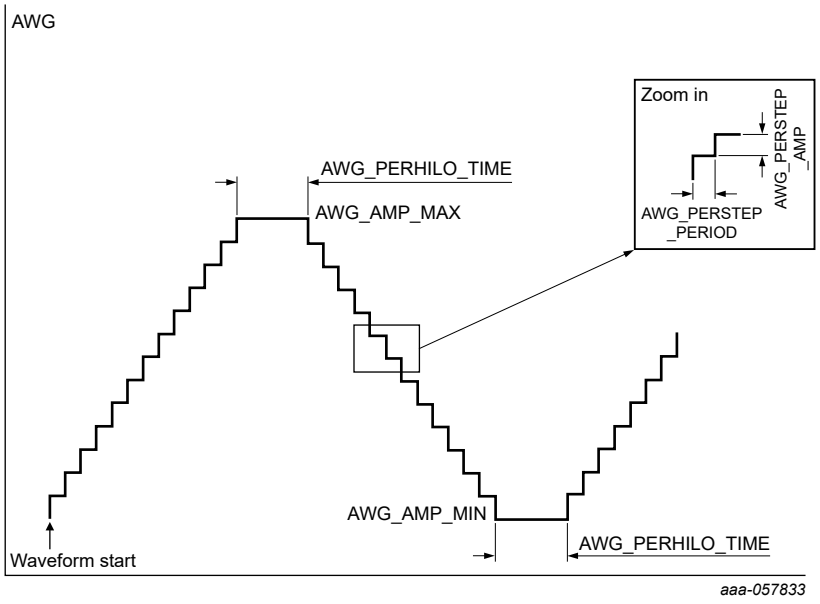


Figure 22. AWG structure

5.2.9 Register reading tab

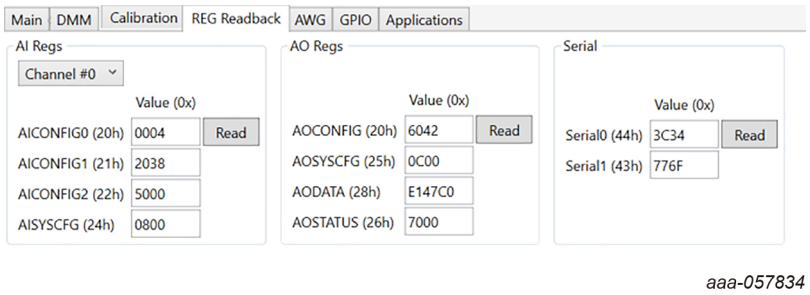


Figure 23. Registers readback

The Register Reading tab enables the user to read main block registers of the device - analog input channels/ system configurations, analog output configuration/status/data, and device serial number for identification. The user can confirm both the AI and AO register configuration completed in the Main tab by clicking **Read** in the REG Readback tab.

5.2.10 Calibration tab

To calibrate the device, follow the instructions provided in the Calibration tab. The selected Gain/Offset registers are written according to the procedure.

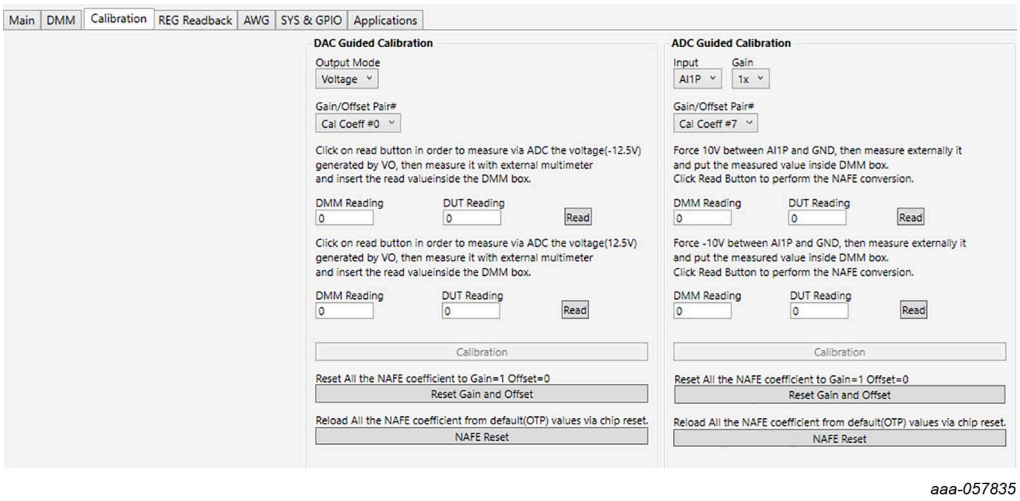


Figure 24. Calibration tab

5.2.11 Check alarm status

The AIO-AFE provides a flexible and configurable global alarm to allow the user to configure it based on the specific application and needs.

Table 6. Alarm and interrupt

Register address	Bit order	Bit name	RW	Default value	Short description
GLOBAL ALARM ENABLE 0x32\h	15	OVER_TEMP_ALRM	RW	0x0	Overtemperature warning at 145 °C.
	14	HVDD_ALRM	RW	0x0	Enable alarm for HVDD supply detect below preset threshold.
	13	HVSS_ALRM	RW	0x0	Enable alarm for HVSS supply detect below preset threshold.
	12	DVDD_ALRM	RW	0x0	Enable alarm for DVDD supply detect below preset threshold.
	11	Reserved	RW	0x0	Unused
	10	GPI_POS_ALRM	RW	0x0	Enable an alarm for rising edge detected at any of the GPI pins.
	9	GPI_NEG_ALRM	RW	0x0	Enable an alarm for falling edge detected at any of the GPI pins.
	8	CONFIG_ERROR_ALRM	RW	0x0	Enable alarm for register configuration error.
	7	OVRRNG_ALRM	RW	0x0	Enable an alarm when one or more data channels are overrange.
	6	UNDRNG_ALRM	RW	0x0	Enable an alarm when one or more data channels are underrange.
	5	OVRLOAD_ALRM	RW	0x0	Enable an alarm when one or more data channels are overloaded or underloaded.
	4	EXTCLK_FREQ_ALRM	RW	0x0	Enable the alarm when the XTAL or EXTCLK frequency varies with internal CLK by XX.
	3	PGA_OV_ALRM	RW	0x0	Enable an alarm when one or more data channels are overvoltage stressing the PGA.
	2	VIEX_OV_ALRM	RW	0x0	Enable an alarm when the excitation voltage source is overloaded.
	1	VIEX_OI_ALRM	RW	0x0	Enable an alarm when excitation current source is overloaded.
	0	TEMP_ALRM	RW	0x0	Enable a programmable temperature alarm, the triggering threshold is set in THRS_TEMP register bits.
GLOBAL ALARM INTERRUPT 0x33\h	15	OVER_TEMP_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	14	HVDD_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	13	HVSS_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	12	DVDD_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	11	Reserved	RW	0x0	Unused
	10	GPI_POS_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	9	GPI_NEG_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	8	CONFIG_ERROR_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	7	OVRRNG_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	6	UNDRNG_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	5	OVRLOAD_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	4	EXTCLK_FREQ_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	3	PGA_OV_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	2	VIEX_OV_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	1	VIEX_OI_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	0	TEMP_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.

For device and input monitoring, various alarms and interrupts are available, including programmable alarm thresholds for (1) temperature alarm, (2) channel-based overrange, and underrange alarms.

The alarm-clearing behavior is determined by GLOBAL_ALRM_STICKY. The ribbon at the bottom of the GUI displays common faults, such as short-circuit, overload, chip status, switch off current input, and the power supply (HVDD, HVSS, ADVVD) for users ease of operation and debug. The status ribbon stays on irrespective of the tab selected by the user. The user can check the latest status by clicking Read Status Bits and can reset the device when needed.

The user must activate GAI Enable to read the alarm status of Over_Temp, HVDD, HVSS, ADVVD, or EXTCLK if there is a fault occurrence.

Figure 25. Alarm status

5.2.12 Reset

The AFE has two types of Reset mode:

- Chip Power-on Reset (POR)
- Command RESET

The button for the Command RESET is available in the Status ribbon and Calibration tabs.

Figure 26. Reset command

When in reset, all HV input pins and GPIO pins are in high-Z Input mode, internal voltage reference is used, ADC digital filters are cleared, all user registers are set to their default values, and all OTP shadow register content is reloaded.

5.2.13 ADC analog input channel configuration and testing

NAFE33352 has eight logical channels, which can be configured to route different internal signals (AVDD, HVDD, HVSS, REF_Byp, and so on) and the external signals at Antenna-in-Package (AIP) and AIN.

Table 7. Analog input selection

Analoginput selection (AI_Config0 at address 0x20\h -> IN_SEL bits 7:3)					
S.No	**IN_SEL**	**Input MUXP**	**Input MUXN**	**Measure type**	**Transfer function**
0	00000	VCM	VCM	DIFF	Vvcm-vcm = adc_code*20*2.5/(12.5*2^24)
1	00001	AI1P	AI1N	DIFF	Vaipn = adc_code*20*2.5/(Gain*2^24)
2	00010	AI1P	VSNS	DIFF	(Vaip-Vsns)* PGA_Gain = adc_code*20*2.5/2^24
3	00011	ADCP/GPIO0	ADCN/GPIO1	DIFF	Vgpio01 = adc_code*20*2.5/(12.5*2^24)
4	00100	AI1P	VCM	SE	Vaip = adc_code*20*2.5/(Gain*2^24)
5	00101	VCM	AI1N	SE	Vain = adc_code*20*2.5/(Gain*2^24)
6	00110	ISNS	VCM	SE	Visns = adc_code*20*2.5/(3.7989*2^24), where CSA gain = 3.7989 with 5 kΩ external resistors.
7	00111	VCM	VSNS	SE	Vvsns = adc_code*20*2.5/2^24, where VSA gain = 1
8	01000	TIA	VCM	SE	Vtia = adc_code*20*2.5/(2.5*2^24)
9	01001	ADCP/GPIO0	VCM	SE	Vgpio0 = adc_code*20*2.5/(12.5*2^24) + 1.5 (VCM voltage)
10	01010	VCM	ADCN/GPIO1	SE	Vgpio1 = adc_code*20*2.5/(12.5*2^24) + 1.5(VCM voltage)
11	01011	REF_BYP	VCM	SE	REF_BYP = adc_code*20*2.5/(12.5*2^24) + 1.5 (VCM voltage) ≥ ~2.5 V
12	01100	VCM	REF_BYP	SE	REF_BYP = (adc_code-2^24)*20*2.5/(12.5*2^24) - 1.5 (VCM voltage) ≥ ~ -2.5 V
13	01101	VCM	BG	SE	BG = (adc_code-2^24)*20*2.5/(12.5*2^24) + 1.5 (VCM voltage) where adc_code > 2^23 ≥ ~1.25 V
14	01110	VADD	VCM	SE	Vavdd = adc_code*20*2.5/(12.5*2^24) + 1.5 (VCM voltage) ≥ ~ AVDD/2
15	01111	VCM	LDO	SE	LDO = adc_code*20*2.5/(12.5*2^24) + 1.5(VCM voltage) ≥ ~1.8 V
16	10000	VHDD	VCM	SE	Vhvdd = adc_code*20*2.5/(12.5*2^24) ≥ ~ HVDD/40
17	10001	VCM	VHSS	SE	Vhvss = adc_code*20*2.5/(12.5*2^24) ≥ ~ HVSS/40
18	10010	DAC_REF	VCM	SE	Vdac_ref = adc_code*20*2.5/(12.5*2^24) + 1.5 (VCM voltage) ≥ ~2.5 V

The AFE Config drop-down menu shows selectable channel configurations (channel #0 - #7 config) to read the converted signal. (Default is AI Channel #0).

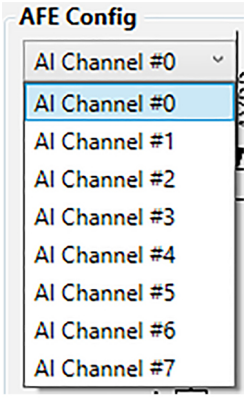


Figure 27. Channel configurations

It's possible to read the internal signal in:

1. ADC Single Channel:
   - Single Reading,
   - Continuous Reading
2. ADC Multichannel:
   - Multireading,
   - Continuous Reading

For more details, see Section 5.2.4.

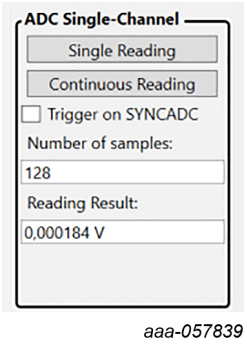


Figure 28. ADC Single-Channel

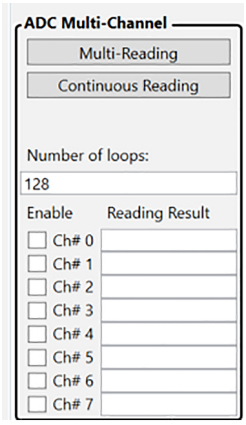


Figure 29. ADC Multi-Channel

5.2.14 Single-Channel Single-Reading (SCSR) example

Example: Channel#0 is configured to read the internal VHDD signal. Figure 30

The steps to follow are:

1. Select the number of channels as AI Channel #0.
2. Select PGA, SINC FILTER, ADC SETTING MODE, ADC DATA RATE, CHANNEL PROGRAM DELAY, and CALIBRATION COEFFICIENT settings in the drop-down menus.
3. Set VHDD/VCM.
4. Set the number of loops as 128 samples.
5. Click the Single Reading.
6. The result is the average of 128 samples.

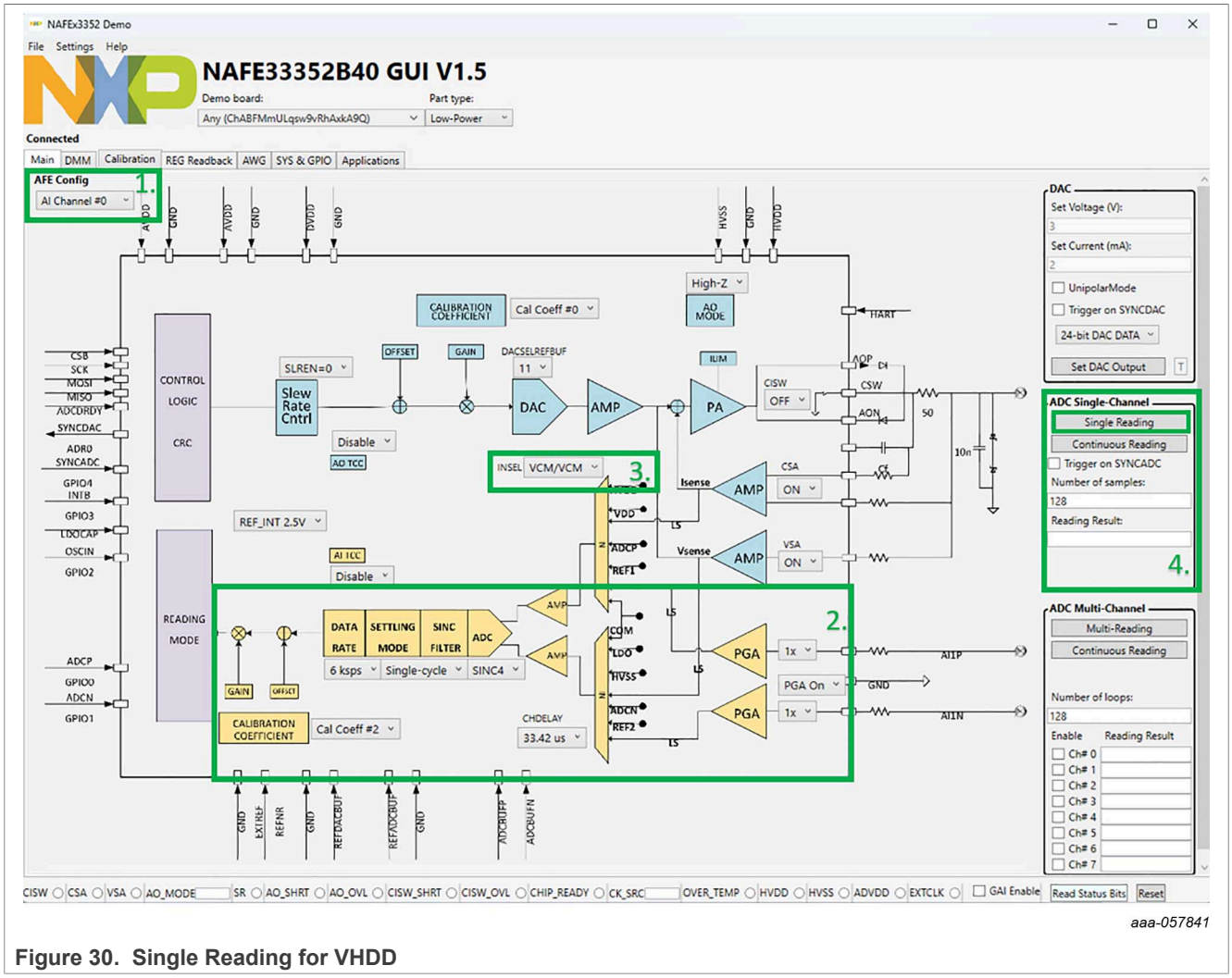


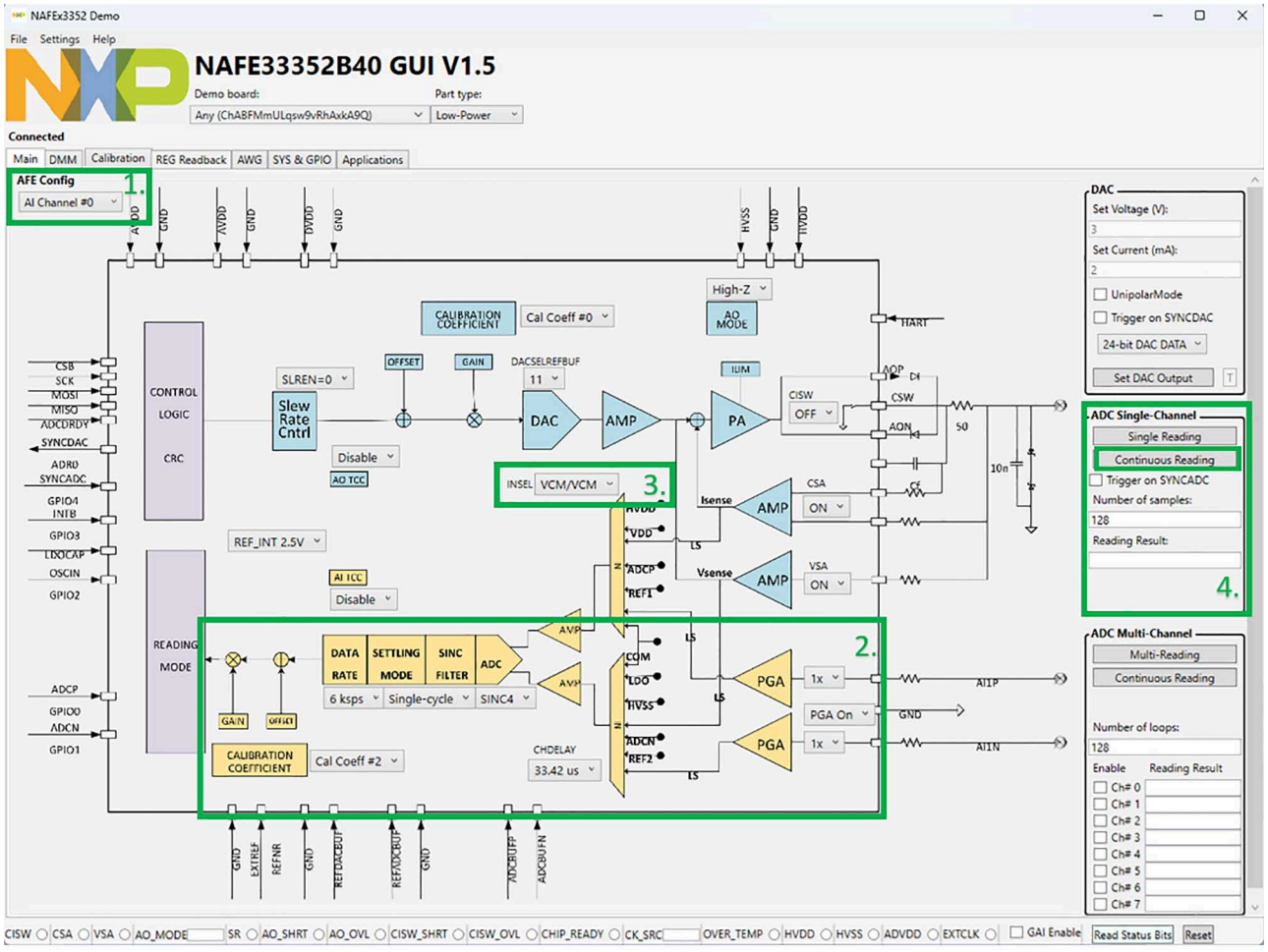
Figure 30. Single Reading for VHDD

5.2.15 Single-Channel Continuous-Reading (SCCR) example

Example: Channel#0 is configured to read the internal VHDD signal. Figure 31

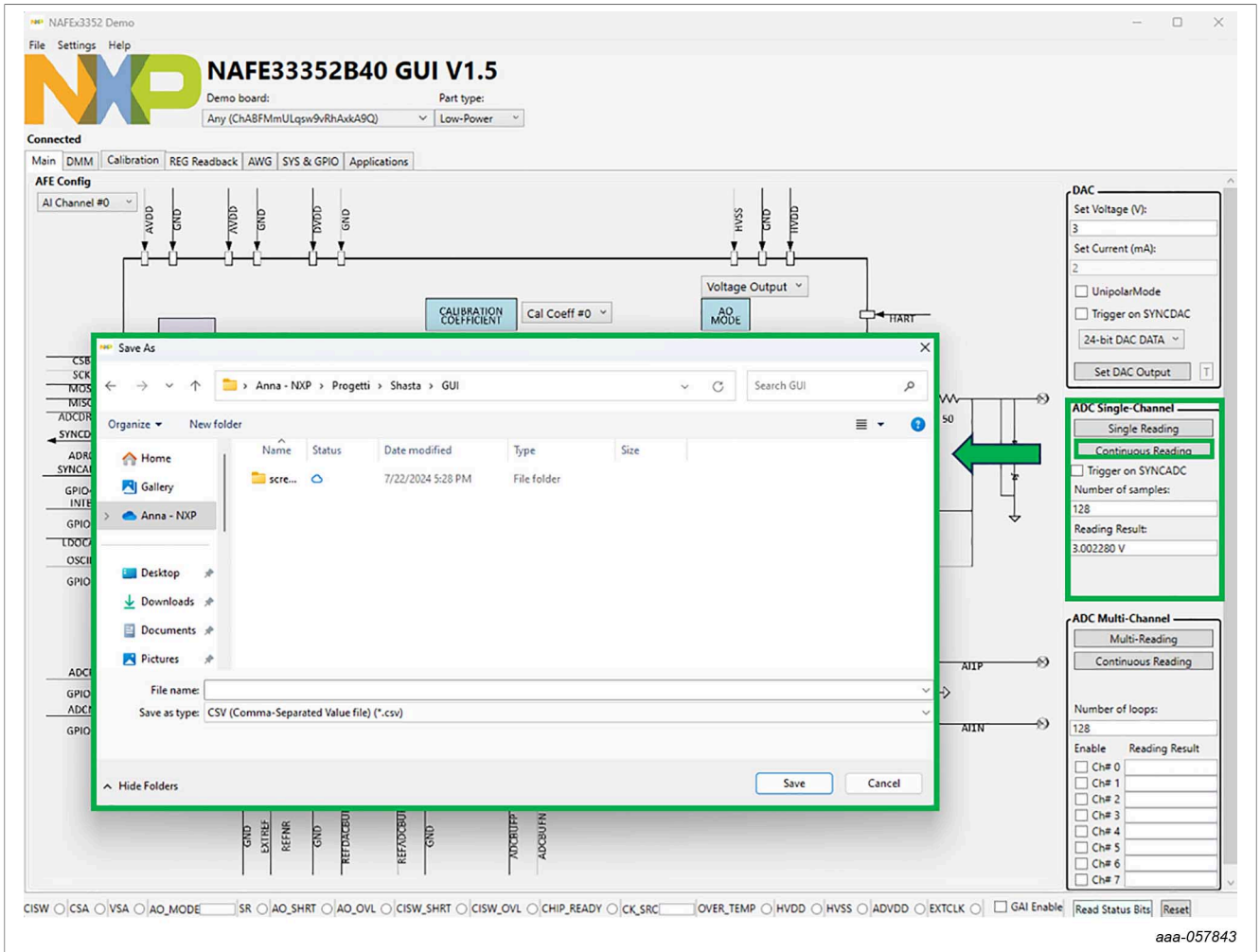
The steps to follow are:

1. Select thenumber of channels as AI Channel #0.
2. Select PGA, SINC FILTER, ADC SETTING MODE, ADC DATA RATE, CHANNEL PROGRAM DELAY, and CALIBRATION COEFFICIENT settings in the drop-down menus.
3. Set VHDD/VCM.
4. Set the number of loops as 128 samples.
5. Click **Continuous Reading** and a box open.
6. Choose where to save the file in *.csv format.
7. The result is 128 samples.



aaa-057842

Figure 31. Continuous Reading for VHDD



aaa-057843

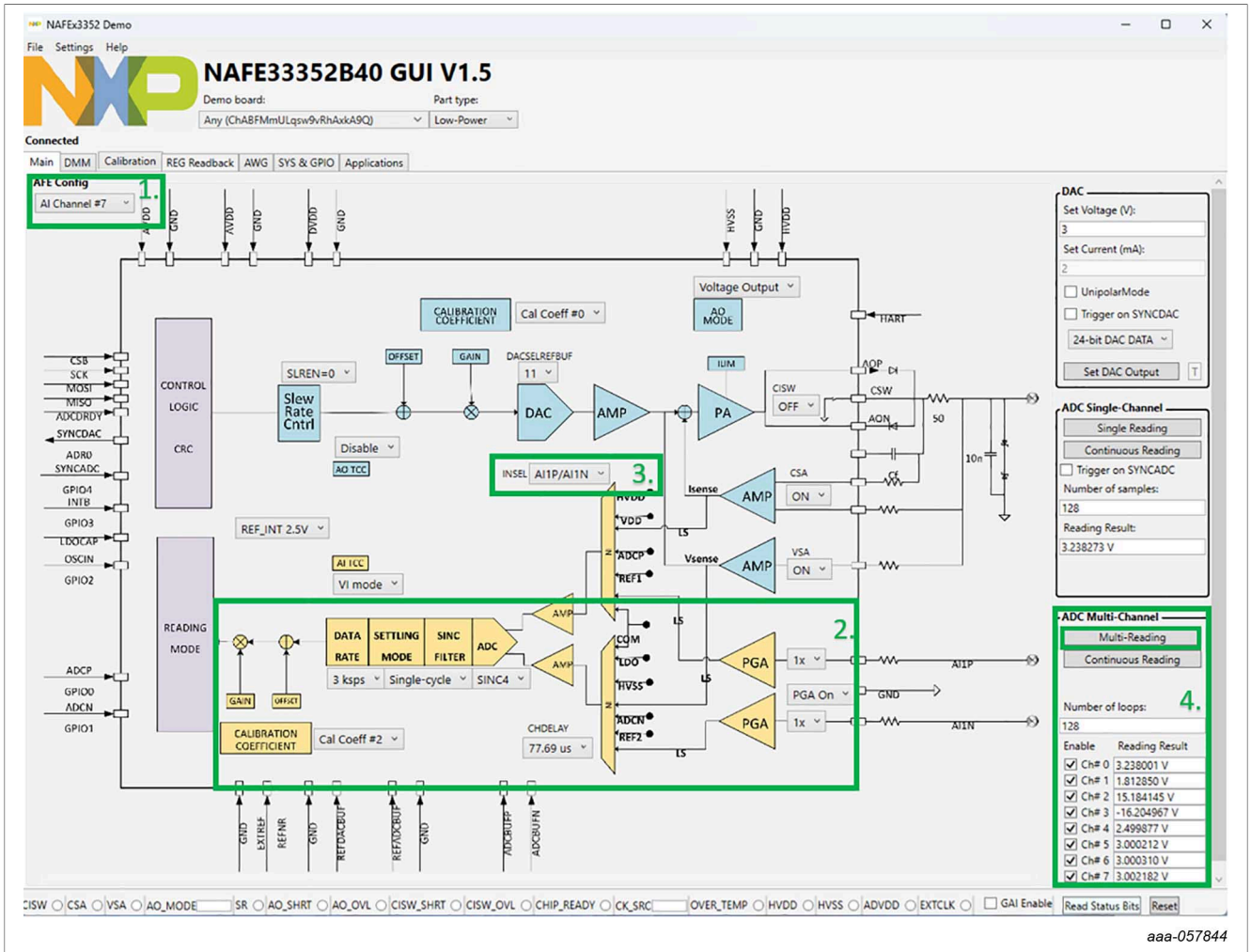
Figure 32. Continuous Reading for VHDD save location

5.2.16 Multichannel Reading (MCR) example

Example: From Channel#0 to Channel#7 are configured to read VADD(ch0), HVDD(ch1), HVSS(ch2), REF_BYP(ch3), GPIO0-1(ch4), AIP-VCM(ch5), VCM-AIN(ch6), LDO(ch7).

The steps to follow are:

1. Select thenumber of channels as AI Channel #0.
2. Select PGA, SINC FILTER, ADC SETTING MODE, ADC DATA RATE, CHANNEL PROGRAM DELAY, and CALIBRATION COEFFICIENT settings in the drop-down menus.
3. Set VADD/VCM.
4. Set the number of loops as 128 samples.
5. Repeat steps 1-3 for the channels that are needed.
6. Click **Multi-Reading**.
7. The result reports for all channels.



aaa-057844

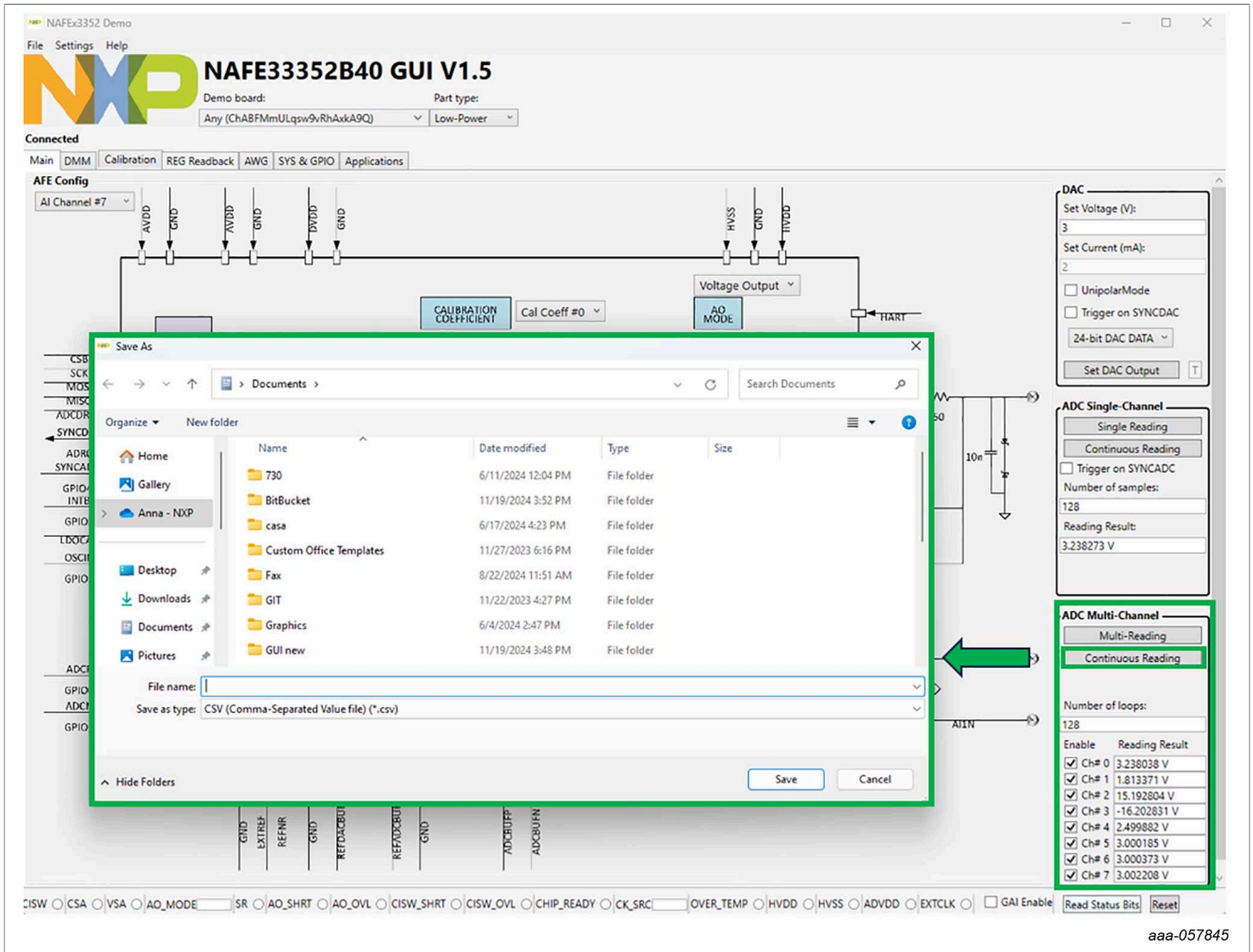
Figure 33. Multi-Reading

5.2.17 Multichannel Continuous-Reading (MCCR) example

Example: From Channel#0 to Channel#7 are configured to read the internal VHDD signal VADD, HVDD, HVSS, REF_BYP, GPIO0-1, AIP-VCM, VCM-AIN, LDO. (Figure 25).

The steps to follow are:

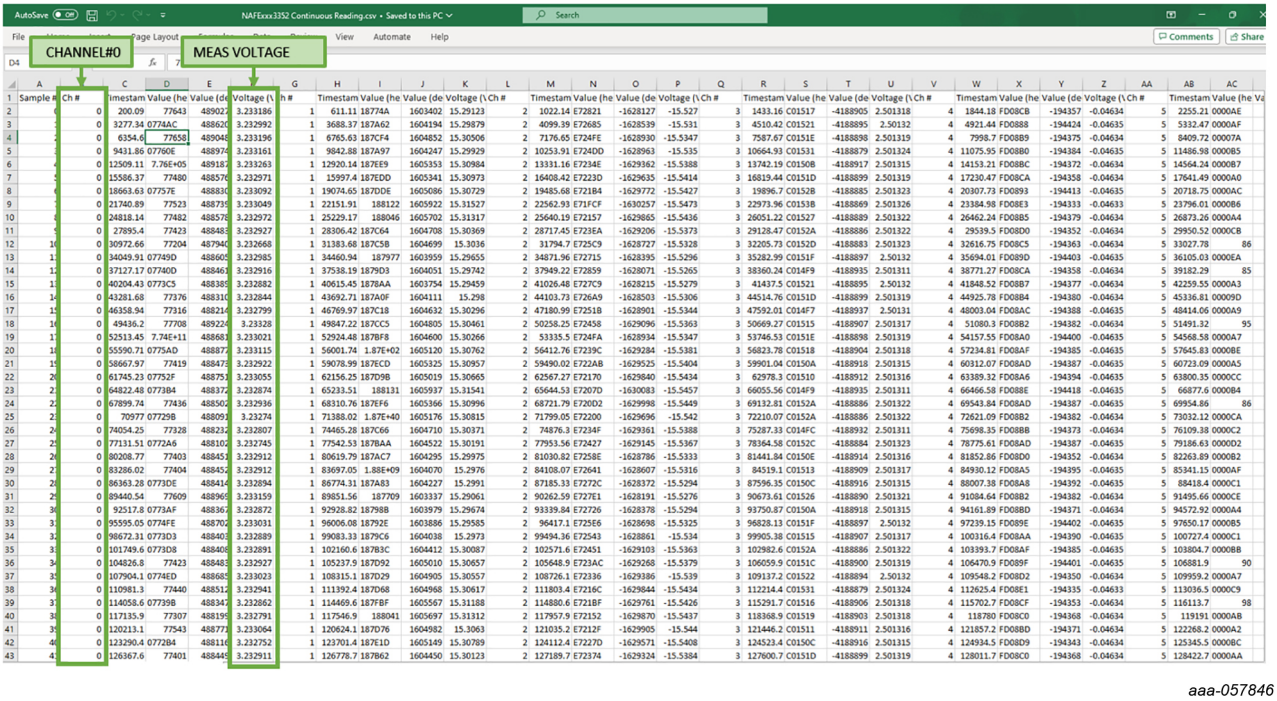
1. Select thenumber of channels as AI Channel #0.
2. Select PGA, SINC FILTER, ADC SETTING MODE, ADC DATA RATE, CHANNEL PROGRAM DELAY, and CALIBRATION COEFFICIENT settings in the drop-down menus.
3. Set VADD/VCM.
4. Set the number of loops as 128 samples.
5. Repeat steps 1-3 for the channels that are needed.
6. Click **Continuous Reading**.
7. Choose where to save the file in *.csv format.
8. The results are 128 samples.



aaa-057845

Figure 34. Multichannel continuous-reading

Figure 35 shows the structure of the csv file, the number of saved channels, and for each channel, the reported voltage measurement with 128 samples (128 rows).



aaa-057846

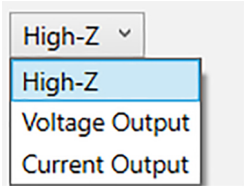
Figure 35. Continuous-reading in .csv format

5.2.18 DAC analog output

The DAC has AIO mode selection.

The user can choose an AIO mode:

- High-Z
- Voltage Output
- Current Output



aaa-057847

Figure 36. AIO mode

When AIO mode is selected high-Z, set Voltage and set Current controls are disabled. The DACSELREFBUF must be 11 to enable Analog Output operation.

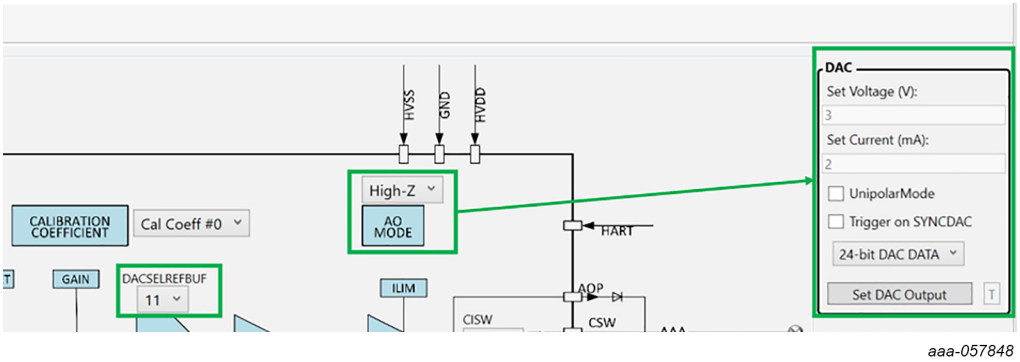
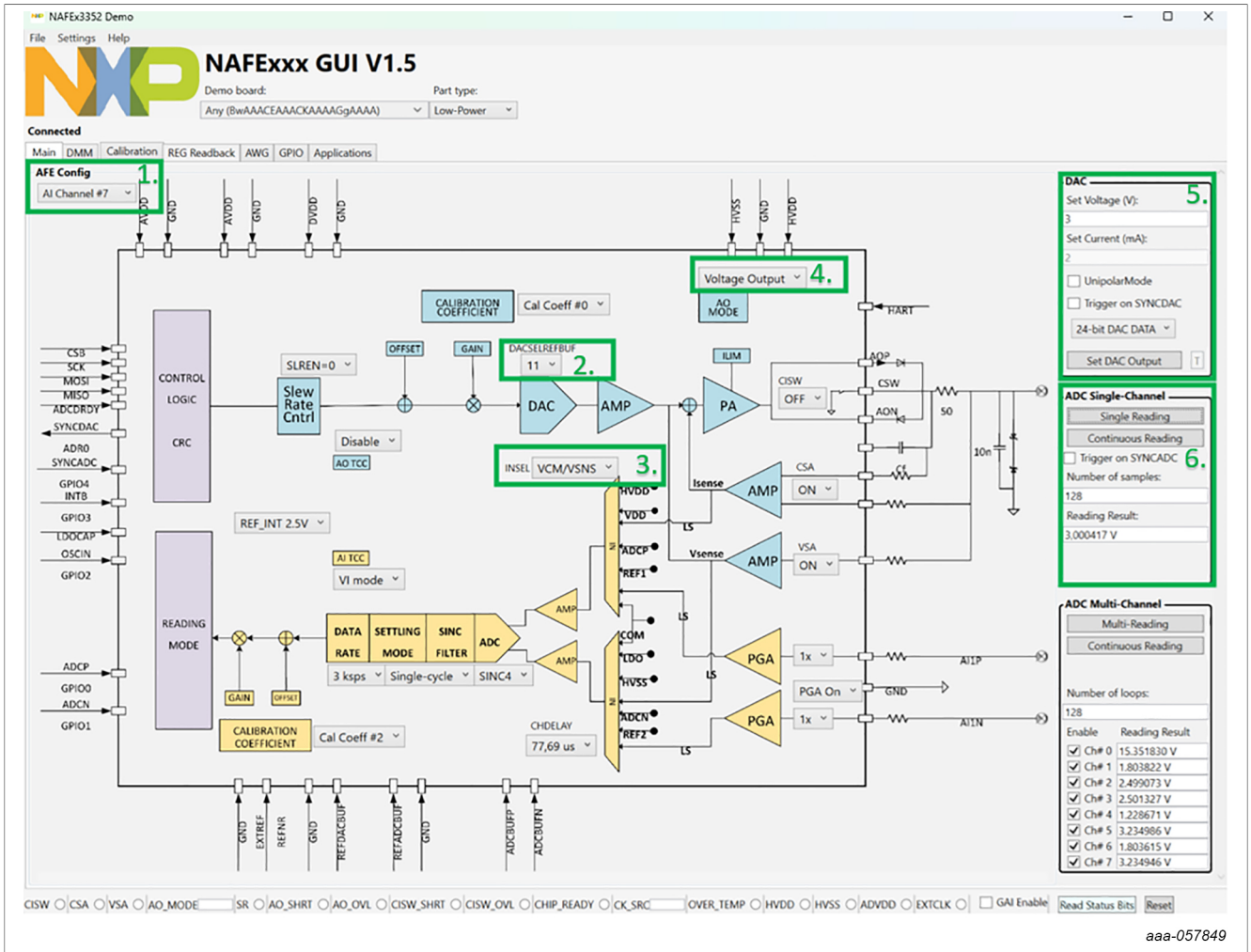


Figure 37. AIO mode in high-Z

5.2.18.1 Voltage output

Figure 38 shows the analog output set for Voltage Output (VO) mode:

1. Set channel.
2. Set the DAC equal to 11.
3. Set as insel VCM/VSNS.
4. Set AIO mode to Voltage Output.
5. Set voltage to 3 V (limit range ±12.5 V).
6. Readback SCSR or SCCR.



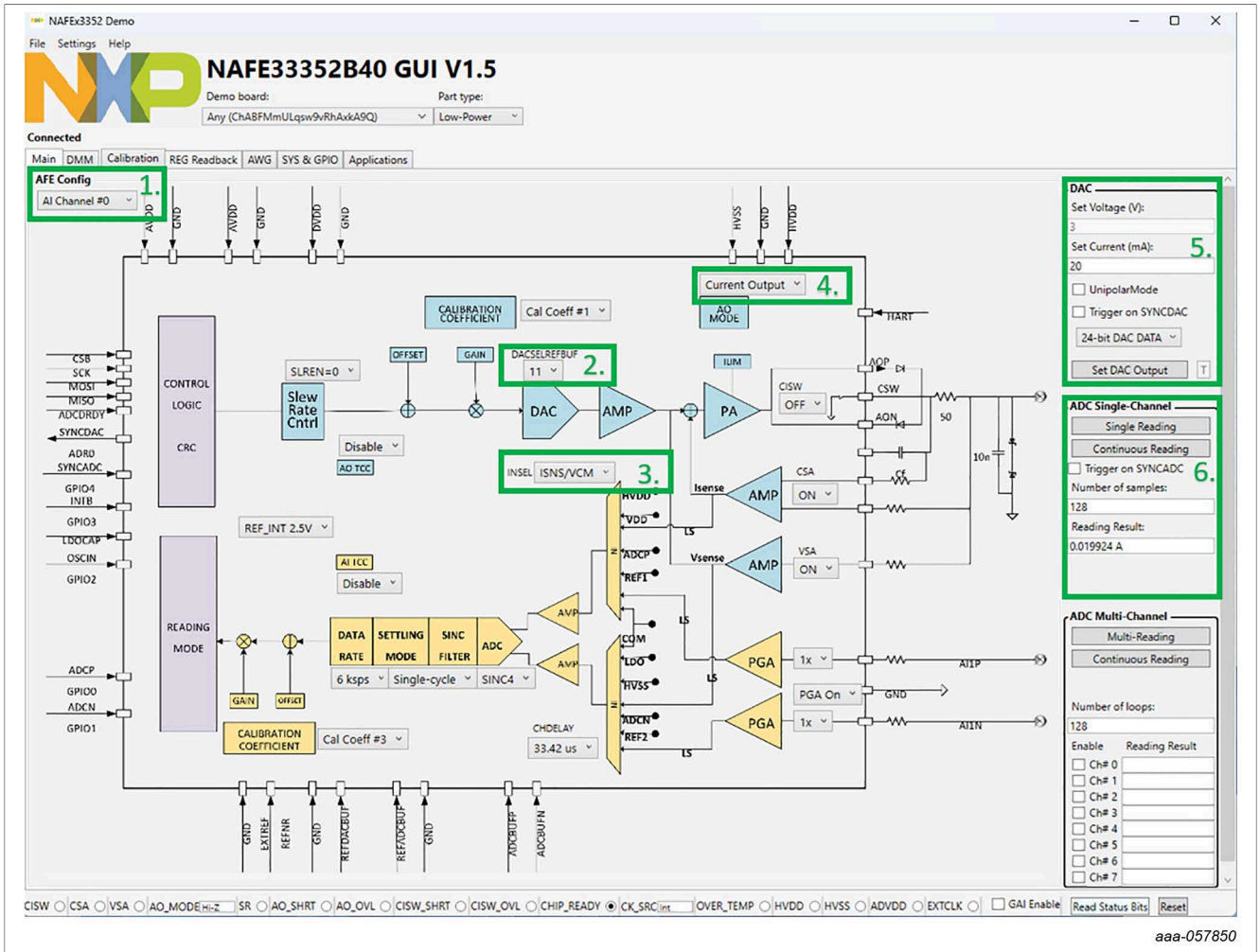
aaa-057849

Figure 38. AIO mode - Voltage Output

5.2.18.2 Current output

Figure 39 shows the analog output set for Current Output (CO) mode:

1. Set thechannel.
2. Put DAC equal to 11.
3. Set as insel INSNS/VCM,
4. Set AIO MODE to Current Output.
5. Set Current to 20 mA (limit range ±25 mA).
6. Readback SCSR or SCCR.



aaa-057850

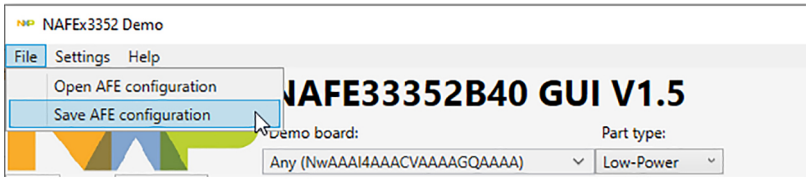
Figure 39. AIO mode in Current Output

5.2.19 Save and load the configuration file

The NAFExx3352 GUI provides a user-friendly save-and-load configuration file function. This function allows the user to save current AFE channel (#0-8) configurations, SCCR number of samples, MCCR enabled channel, and MCCR number of loops in an .acs (AFE configuration settings) file. The user can load a previously saved .acs configuration file to load all configuration settings into the GUI without the need to manually change every setting one by one in the GUI.

5.2.19.1 Save the configuration file

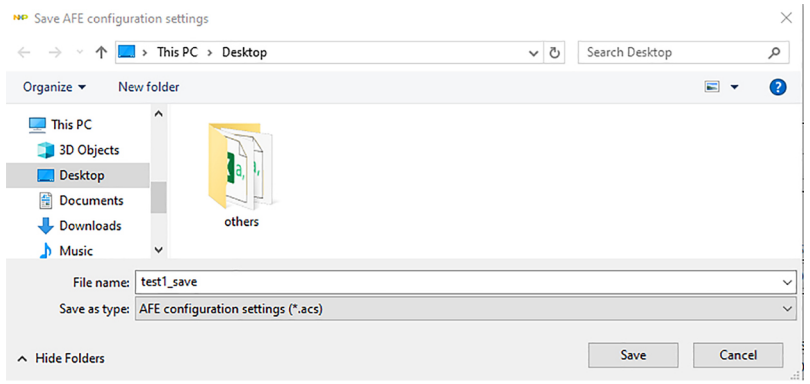
First, launch the NAFExx3352 GUI, select all configuration settings (AFE channel #0-8 configuration settings, SCR/SCCR/MCR/MCCR settings), and proceed to the particular measurement or calibration. If the test result is as expected, the user can select Save AFE configuration in the File tab in the NAFExx3352 GUI as shown in Figure 40.



aaa-057851

Figure 40. Save configuration

Second, key in a filename (such as test1_save.acs) to save the particular measurement configuration settings in an .acs file to be used for future measurement.

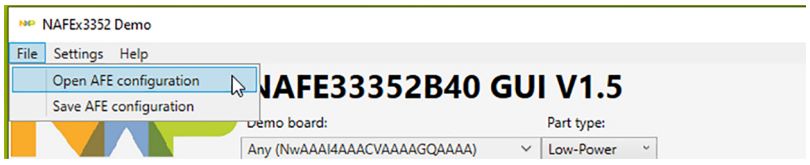


aaa-057852

Figure 41. Example save file

5.2.19.2 Load a configuration file

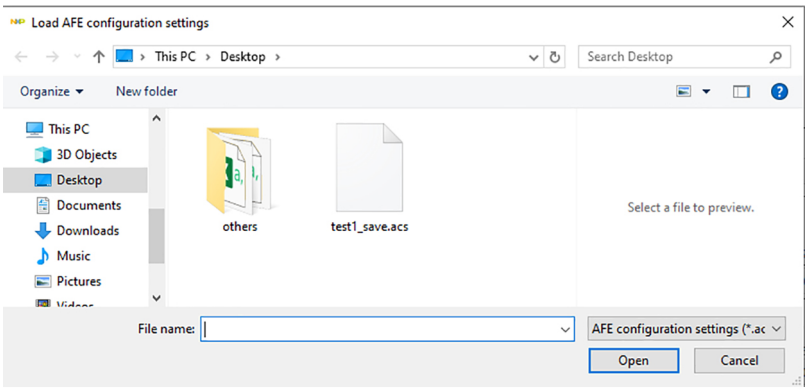
To launch the NAFExx3352 GUI, select **Open AFE configuration** in the File tab.



aaa-057853

Figure 42. Open AFE configuration

Open the saved .acs file to load all configuration settings and proceed, repeating the previous measurement or modifying some settings for a new measurement.



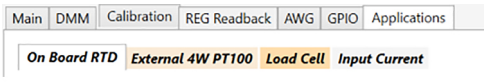
aaa-057854

Figure 43. Load AFE configuration settings

5.3 Application demo

In the GUI, it is possible to try four typical applications of the NAFE, divided into the following subtabs:

- On Board RTD
- External 4W PT100
- Load Cell
- Input Current



aaa-057855

Figure 44. Applications

5.3.1 On Board RTD

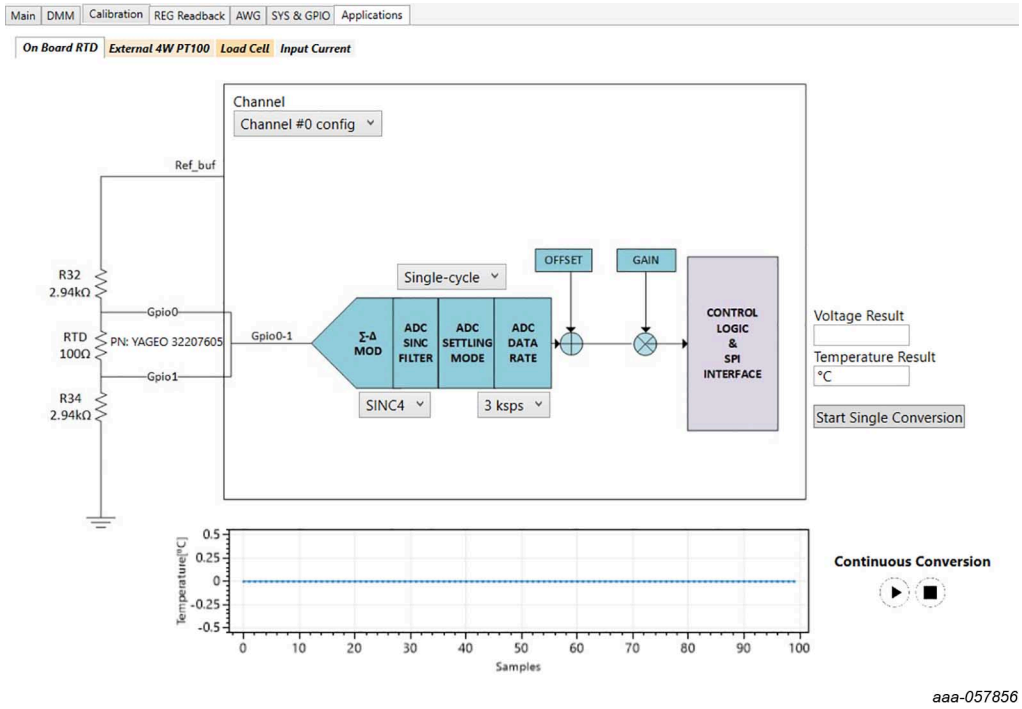


Figure 45. On Board RTD

The EVKit features a voltage divider composed of two resistors and one thermistor. The voltage divider is powered by ref_buf output, as shown in the left portion of Figure 45.

In this section, it is possible to configure only:

- SINC filter
- Single/Normal-cycle
- Data rate

Pressing ▶ (Play) below **Start Single Conversion** executes a single conversion.

Two results are shown:

- Voltage raw result
- Temperature conversion

At the bottom side of the tab, there is a chart and two buttons: ▶ and ■ (Stop). By pressing ▶, a continuous conversion is performed until ■ is pressed. The continuous conversion is configured to make 100 samples at a time. These samples are plotted on the chart.

Figure 46. Continuous conversion warning

It is not possible to set slow rates too slow if Continuous mode is used. A warning message appears below the continuous conversion buttons as shown in Figure 46.

5.3.2 External 4W PT100

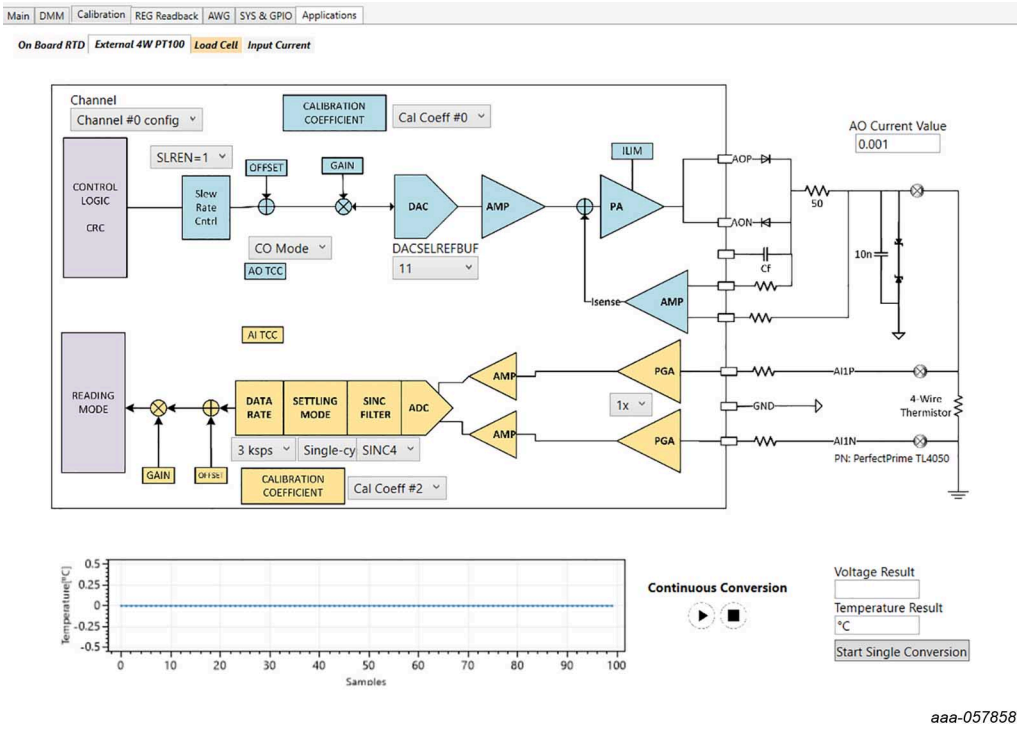


Figure 47. External 4W PT100

PT 100 temperature sensors are the most common type of platinum resistance thermometer. PT indicates that the sensor is made from Platinum (Pt), 100 means, at 0 °C, the sensor has a resistance of 100 ohms (Ω). The four-wire configuration makes it possible to force a current through two wires and read the voltage on the other two wires. This allows the reading of voltage, eliminating the voltage drop because of the current.

In this section, it is possible to configure the following:

- Sinc filter
- Single/Normal-cycle
- Data rate
- Input pin (Sense)
- Output current pin (Force)
- Current magnitude
- Current sign

Pressing ▶ below **Start Single Conversion** executes a single conversion. Two results are shown:

- Voltage raw result
- Temperature conversion

At the bottom of the tab, there are a chart and two buttons: ▶ and ■. By pressing ▶, a continuous conversion is performed until ■ is pressed. The continuous conversion is configured to make 100 samples at a time. These samples are plotted inside the chart.

5.3.3 Load Cell

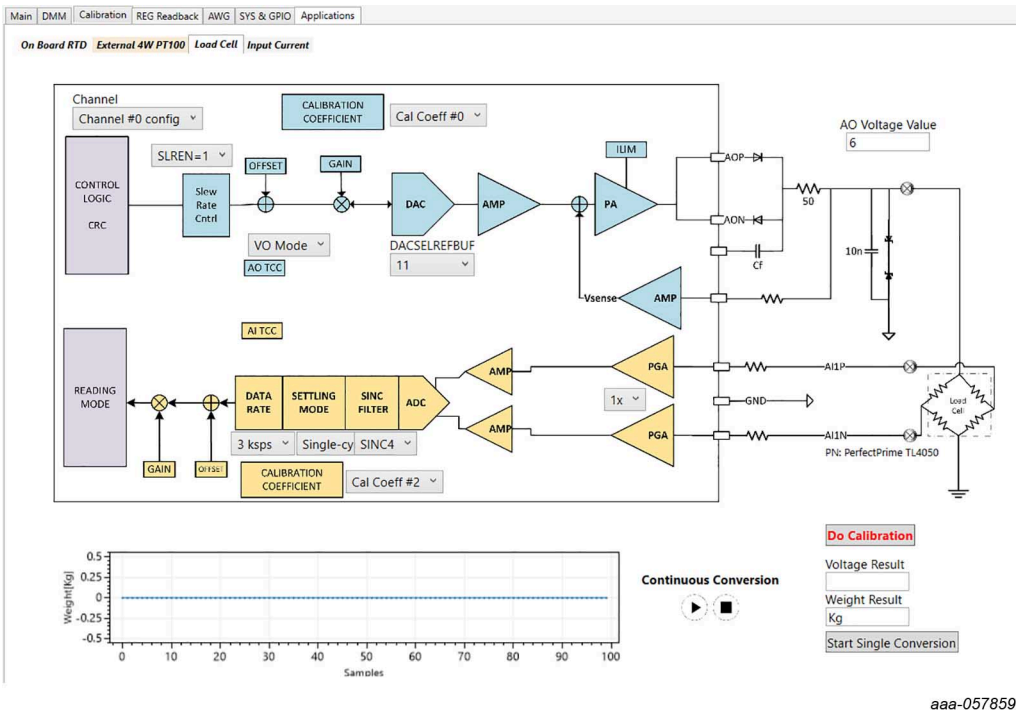


Figure 48. Load Cell

The internal functioning of a load cell differs according to the load cell chosen. There are, for example, hydraulic load cells, pneumatic load cells, and strain-gauge load cells. As shown in Figure 48, a strain-gauge load cell is used as an application example for NAFE33352.

In this section, it is possible to configure:

- Sinc filter
- Single/Normal-cycle
- Data rate
- Input pin (Sense)
- Output voltage pin (Force)
- Voltage magnitude
- Voltage sign

The voltage proportional to the force is small (a few mV), which is why it is recommended to use 16x PGA.

For this kind of conversion, a calibration is needed before starting. This is because the load cell structure transfer function depends on the structure where the load cell is mounted. The **Do Calibration** button, shown in Figure 48, is bold and red each time a calibration is needed. When this button is pressed, a dialog appears, as shown in Figure 49.

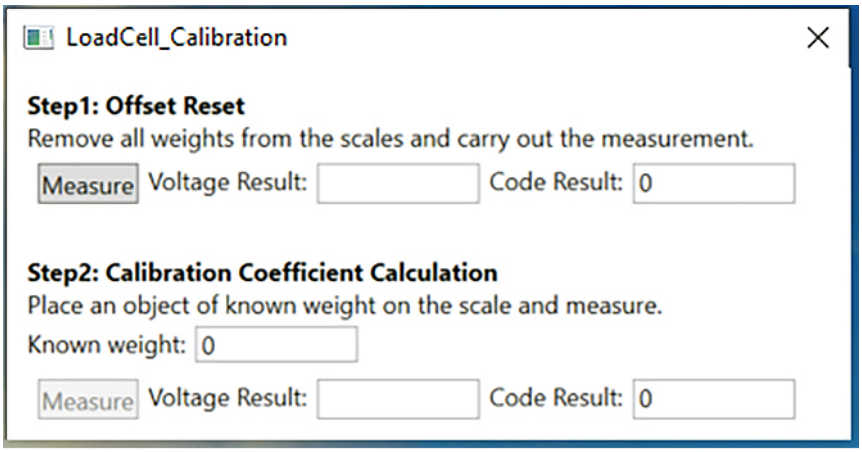


Figure 49. LoadCell_Calibration

The calibration process consists of two steps (as shown in the pop-up dialogue window):

1. **Offset reset:** Remove all weight from the scale and take one measurement. This value is the value at 0 load, therefore the system offset.
2. **Calibration coefficient calculation:** Place an object of known weight on the weight scale, write the known weight (unit kg) in the input box, and take a measurement.

Figure 50. Calibration coefficient calculation

These two measurements take about 4 to 5 seconds.

Pressing ▶ below **Start Single conversion** executes a single conversion. Two results are shown:

- Voltage raw result
- Temperature conversion

At the bottom of the tab, there is a chart and two buttons: ▶ and ■ (Stop). By pressing ▶, a continuous conversion is performed until ■ is pressed. The continuous conversion is configured to make 100 samples at a time. These samples are plotted inside the chart.

5.3.4 Input Current

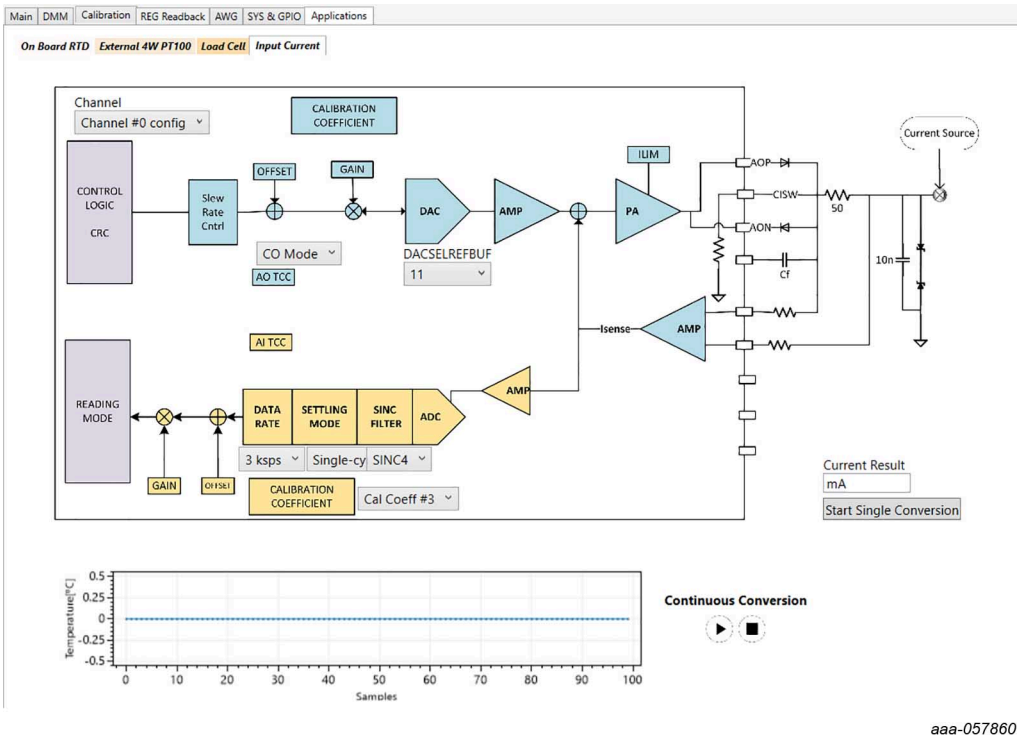


Figure 51. Input Current

In this section, it is possible to configure:

- Sinc filter
- Single/Normal-cycle
- Data rate
- Input pin (Sense)
- Output current pin (Force)

6 Acronyms

A short list of acronyms used in this document is summarized for completeness:

Table 8. Acronyms

Acronym	Description
ADC	Analog-to-Digital Converter
AFE	Analog Front-End
AIP	Analog Input Positive
AWG	Automatic Wave Generator
CSA	Current Sense Amplifier
DAC	Digital-to-Analog Converter
EMC	Electromagnetic Compatibility
EVB	Evaluation Board
EVK	Evaluation Kit
GPIO	General-Purpose Input/Output
HV	High Voltage
LDO	Low Dropout Regulator
LSB	Least Significant Bit
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor.
OTP	One-Time Programmable
PGA	Programmable Gain Amplifier
POR	Power-on Reset
RTD	Resistance Temperature Detector
SE	Single Ended
SPI	Serial Peripheral Interface
VSA	Voltage Sense Amplifier

7 References

This section lists the references used to supplement this document.

1. **NAFE33352 schematic and jumper location** — See NAFE33352_EVB_schematic.pdf.
2. **NAFE33352 data sheet** — Product specification, function, and register map.

8 Revision history

Table 9 summarizes the revisions to this document.

Table 9. Revision history

Document ID	Release date	Description
UM12180 v.2.0	07 November 2025	Updated as per CIN# 202511007I: • Updated the following sections: – Section 1 "Introduction" – Section 2 "Finding the kit resources and information on the NXP website" – Section 5.1 "Connectivity check" • Changed NAFE33352 to NAFEx3352 • Made some editorial changes
UM12180 v.1.0	13 February 2025	Initial version

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