UM12092

Hardware user manual for EVBMA7118DT

Rev. 1.0 — 26 September 2025 User manual

Document information

Information	Content
Keywords	EVBMA7118, BMA7118, BCC, battery cell controller, battery management system
Abstract	This user manual targets the EVBMA7118DT board. The EVBMA7118DT is an evaluation board for the BMA7118 (battery cell controller IC).

1 Introduction

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal, and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost, and improved performance in powering state-of-the-art systems.

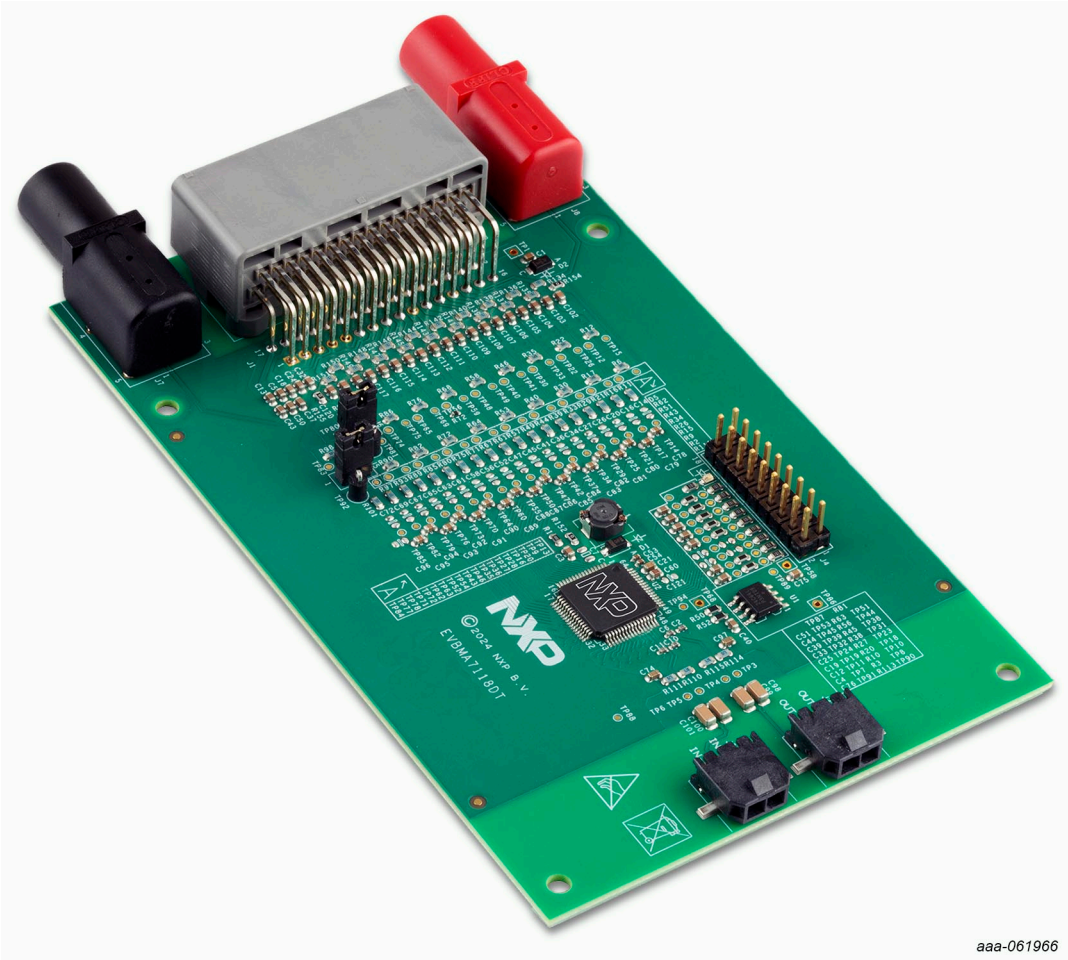

Figure 1. EVBMA7418DT

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2 Getting started

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal, and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost, and improved performance in powering state-of-the-art systems.

The tool summary page for EVBMA7118DT can be found at https://www.nxp.com/EVBMA7118DT. The overview tab provides an overview of the device, product features, a description of the kit contents, a list of (and links to) supported devices, a list of (and links to) any related products, and a **Get Started** section.

The **Get Started** section provides links to everything needed to start using the device and contains the most relevant, current information applicable to the EVBMA7118DT.

1. Go to the NXP secure page for the evaluation board (EVB)
2. On the **Overview** tab, locate the **Jump To** navigation feature on the left side of the window
3. Select the **Get Started** link, review each entry, and download an entry by clicking the title
4. After reviewing the **Overview** tab, visit the other product-related tabs for additional information:
   - **Documentation**: download current documentation
   - **Software & Tools**: download current hardware and software tools
   - **Buy/Parametrics**: purchase the product and view the product parametrics

After downloading files, review each file, including the user guide, which includes setup instructions. If applicable, the bill of materials (BOM) and supporting schematics are also available for download in the **Get Started** section of the **Overview** tab.

2.1 Kit contents/packing list

The EVBMA7118DT contents include:

- Assembled and tested EVBMA7118DT board in an antistatic bag
- Transport protocol link (TPL) cable
- Battery emulator connector cable

3 Getting to know the hardware

3.1 Overview

The EVBMA7118DT is a battery monitor evaluation board populated with one BMA7118. The BMA7118 is an 18 cell analog front-end IC. The board includes the necessary auxiliary components to operate the BMA7118. The EVBMA7118DT can be supplied with a DC laboratory power supply. Alternatively, the board can be connected to the BATT-18EMULATOR or even real battery cells.

3.2 Board features

- The board implements a resistive divider to allow evolution of the analog front-end (AFE) without cell emulators
- Option to connect to the BATT-18EMULATOR or real cells
- Option to connect cell 0 to an external stimulus
- Easy access to general-purpose input/output (GPIO) pins
- Operation mode indicator
- Components assembly only on the top side
- Compact design
- Minimized BOM

3.3 Device features

Table 1. Device features

Device	Description	Features
BMA7118	The BMA7118 is an 18 cells analog front end IC for monitoring of lithium-ion battery cells.	• AEC-Q100 grade 1 qualified: -40 °C to +125 °C ambient temperature range • ISO 26262 ASIL D support for cell voltage and cell temperature measurements from the host microcontroller (MCU) to the cell • Cell voltage measurement – 8 to 18 cells per device – 16-bit resolution and ±0.8 mV typical measurement accuracy with ultra low long-term drift – Clock accurate synchronicity of cell voltage measurements – Integrated configurable digital filter – Redundant comparisons of primary and secondary cell voltages • External temperature and auxiliary voltage measurements – 9 analog inputs configurable as absolute or ratiometric with 5 V input range – 16-bit resolution and 0.1 % measurement accuracy – Integrated configurable digital filter • Internal measurement and monitoring – Two redundant internal temperature sensors – Supply voltages • Operation modes – Active mode (5 mA) resulting in 350 mW power consumption due to integrated DC-to-DC converter – Sleep mode (60 µA) – Deep sleep mode (4.5 µA) – Cyclic wake-up to monitor the pack and the balancing function during sleep – Capability to wake up the host MCU via daisy chain if there is a fault event • Cell voltage balancing – 18 internal balancing field effect transistors (FET), up to 150 mA average with 1.5 Ω R_{DSon} per channel – Support for automatic and simultaneous passive balancing of all channels with automatic odd/even sequence – Global balancing timeout – Timer controlled balancing with individual timers with 10 s resolution and up to 45 h duration – Voltage-controlled balancing with global and individual undervoltage thresholds – Configurable pulse width modulation (PWM) duty cycle balancing – Automatic pausing of balancing during measurement with configurable filter settling time – Configurable delay of the start of balancing after transition to sleep – Automatic discharge of the battery pack (emergency discharge) • Host interface supporting isolated daisy chain communication [transformer physical layer 3 (TPL3)] – 2 Mbit/s data rate for TPL interface – 4 Mbit/s data rate for serial peripheral interface (SPI) • TPL3 daisy chain communication supports – Two wire daisy chain with capacitive or inductive isolation – Synchronization of the monitoring ICs via the communication – Protocol supporting up to six daisy chains and 62 nodes per chain – Unique device ID with dynamic addressing

3.4 Setup description

Figure 2 shows a complete setup. The setup uses the BATT-18EMULATOR to supply and emulate the cell voltages for two EVBMA7118DT. The KIT-PC2TPLEVB enables the communication to a regular PC. The evaluation GUI displays the measured voltages and allows interacting with the BMA7118 devices. Depending on the scope of evaluation, the evaluation system can be altered to use different components (for example, real battery cells or a different TPL communication source).

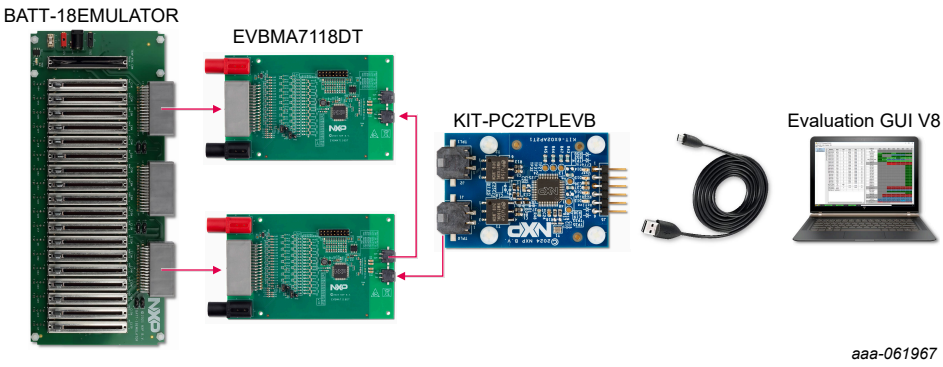


Figure 2. Complete setup using the evaluation GUI and a battery emulator

3.4.1 Supply options

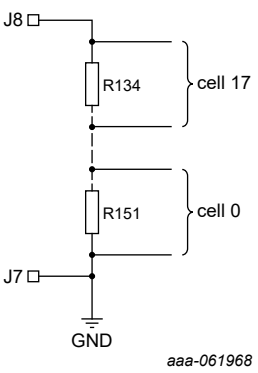
The EVBMA7118DT can be supplied either via a laboratory power supply (J7 and J8), or connected to several battery cells (J1). Table 2 shows the recommended connectors for the connection options.

Table 2. Connectors

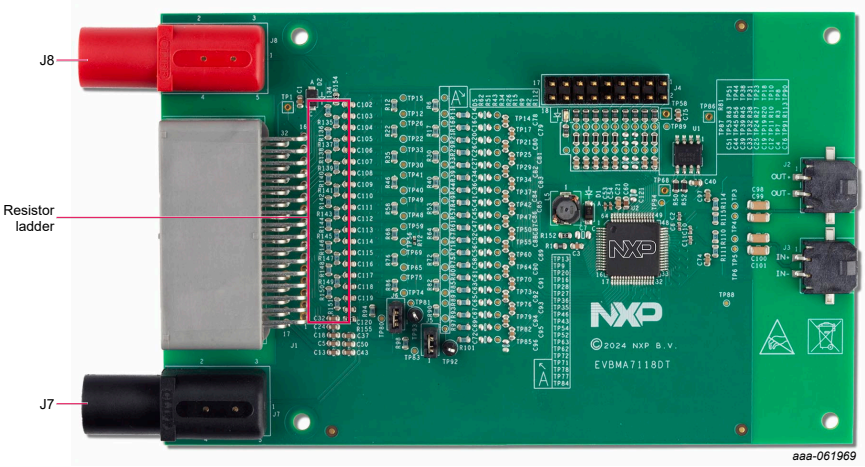
Connector	Recommended mating connector	Manufacturer
J1	MX34032SF1 (with M34S75C4F1 as socket contact)	JAE
J7, J8	default 4 mm banana plug	various

3.4.1.1 Supply via a laboratory power supply

To supply the EVBMA7118DT, the connectors J7 and J8 are connected to the power supply. In this configuration, the resistive divider (R134 to R151) emulates the cells.



Schematic view



Printed-circuit board (PCB) location

Figure 3. Connectors for laboratory power supply

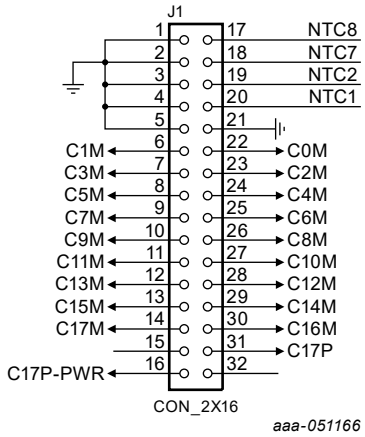
The connectors for the laboratory power supply provide the operation voltage for the BMA7118 and the cell voltage measurement inputs.

The supply via the laboratory supply allows an easy connection and allows exploring all functions of the BMA7118. The drawback of the supply via this approach is:

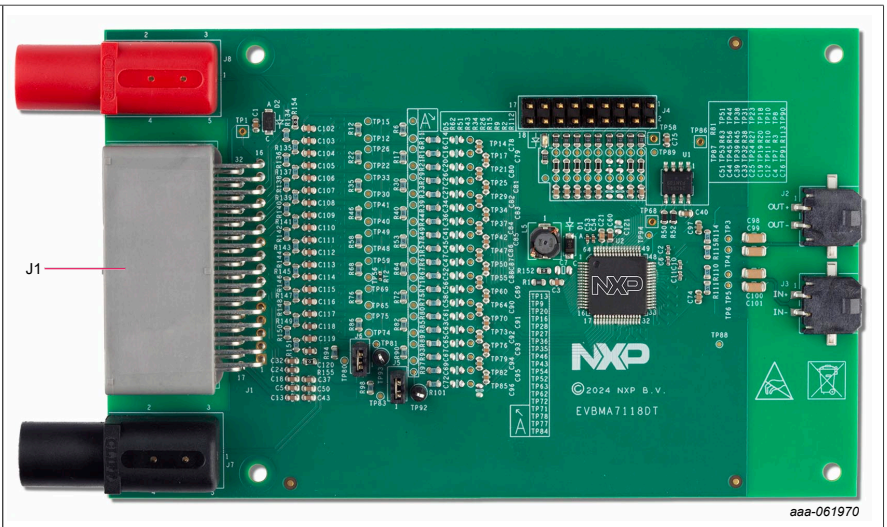
- The tolerances of the resistors influence the actual measured cell voltage. The measured cell voltage is not exactly 1 / 18 of the supply. For accuracy evaluations, the actual cell voltage across the individual resistors (R134 to R151) must be considered.
- When balancing is activated, the balancing current influences the resistive divider. The effective impedance simulated by the resistor changes from 1 kΩ to approximately 120 Ω when balancing at a cell is activated. Due to the impedance change, the voltage for each cell input changes. The cell voltage measurements show fluctuating values. To ensure that each cell input stays within the measurement range, the supply voltage must be limited to approximately 45 V.

3.4.1.2 Connection to battery cells

Alternatively to the laboratory power supply, real cells or a battery emulator (for example, the BATT-18EMULATOR) can be connected via J1. To avoid an influence of leakage currents caused by the resistive divider, desolder the resistors R154, R155, and R134 to R151. The pin assignment of J1 is shown in Figure 4. On J1, the cell 0 is connected between C0M (cell 0 negative) and C1M (cell 1 negative); cell 1 is connected between C1M and C2M. Cell 17 is connected between C17M (cell 17 negative) and C17P (cell 17 positive). C17P-PWR and GND (pin 21) are used to supply the EVBMA7118DT. The supply pins are separated from C17P and C0M respectively to avoid any voltage drop because of the EVB current consumption. Optional external 10 kΩ negative temperature coefficient (NTC) can be connected between each NTCx terminal and one GND terminal.



Schematic view



PCB location

Figure 4. Pin assignment of cell connector

3.4.2 Communication connection

The EVBMA7118DT has two communication connectors (J2 and J3). At the first start after applying power to the BMA7118 only the lower TPL port can wake the IC. Therefore, the lower port (J3) must be connected toward the TPL controller. The higher port (J2) can be used to connect more devices to the daisy chain.

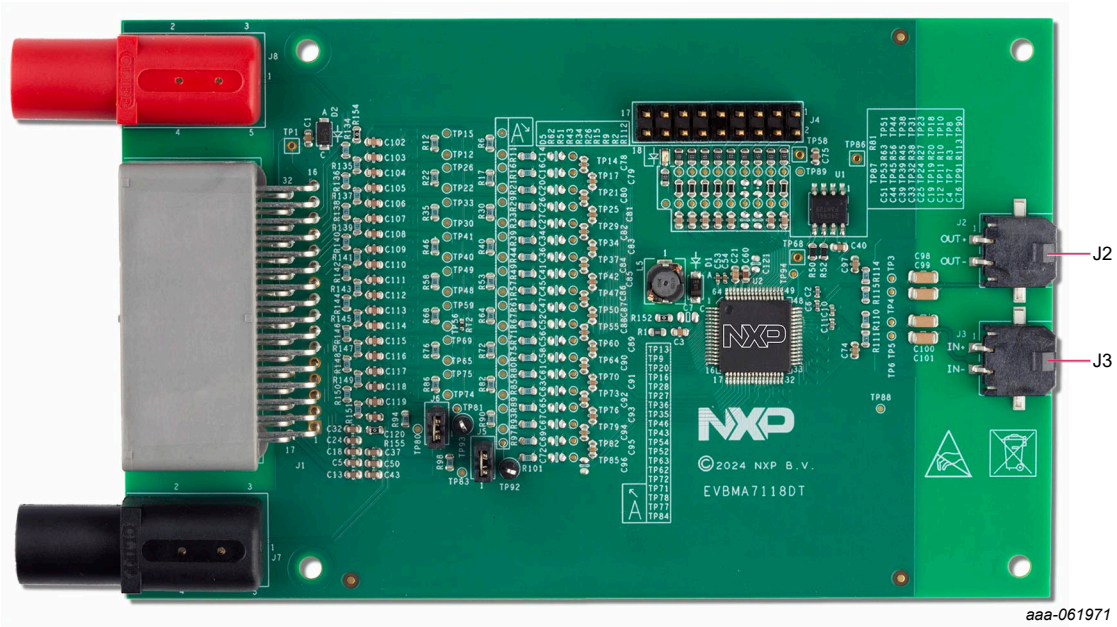


Figure 5. Communication connectors

Table 3. Connectors

Connector	Recommended mating connector	Manufacturer
J2, J3	43645-0200 (with 43030-0001 as terminal)	Molex

Note: *The wake-up capability of the higher TPL port can be configured after power up. The configuration is retained as long as the BMA7118 remains supplied.*

3.4.3 Operation mode indicator

The EVBMA7118DT facilitates an LED (D5) as operation mode indicator. The LED is connected to VAUX of the BMA7118. VAUX is controlled by the BMA7118 and is available in active mode and cyclic mode. In other modes, VAUX is not available.

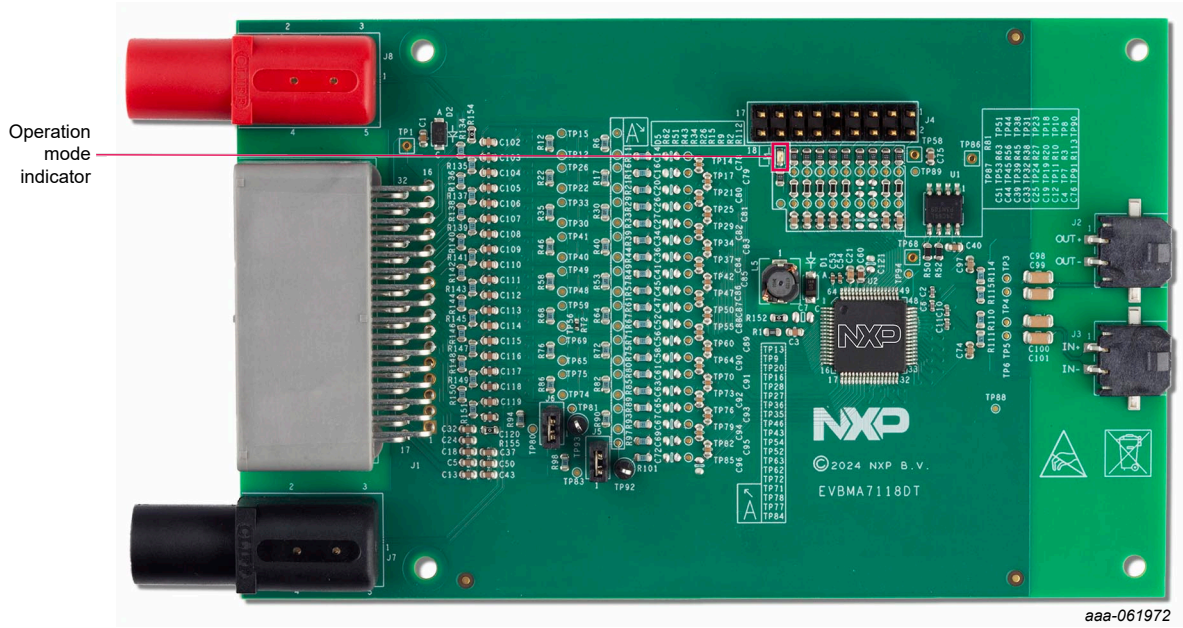
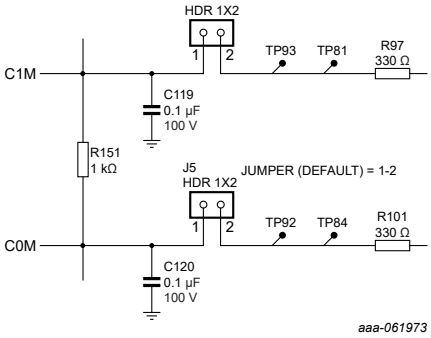


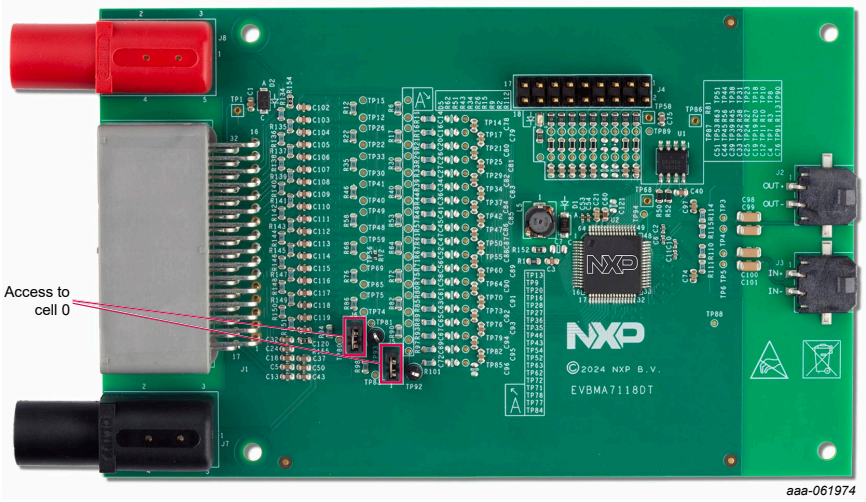
Figure 6. Operation mode indicator

3.4.4 Access to cell 0 inputs

For various evaluation cases, it can be of interest to focus the evaluation on a specific channel only. With jumpers J5 and J6, the input of cell 0 can be disconnected. A customer-specific circuit (for example an external cell simulator) can be attached.



Schematic view



PCB location

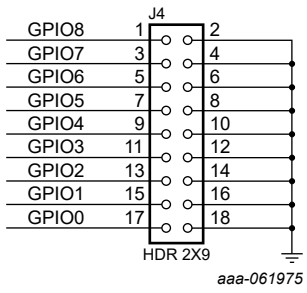
Figure 7. Access points for cell 0

Note: *Applying a voltage at cell 0 also modifies the voltage at cell 1. Ensure the voltage at cell 1 stays within its measurement range.*

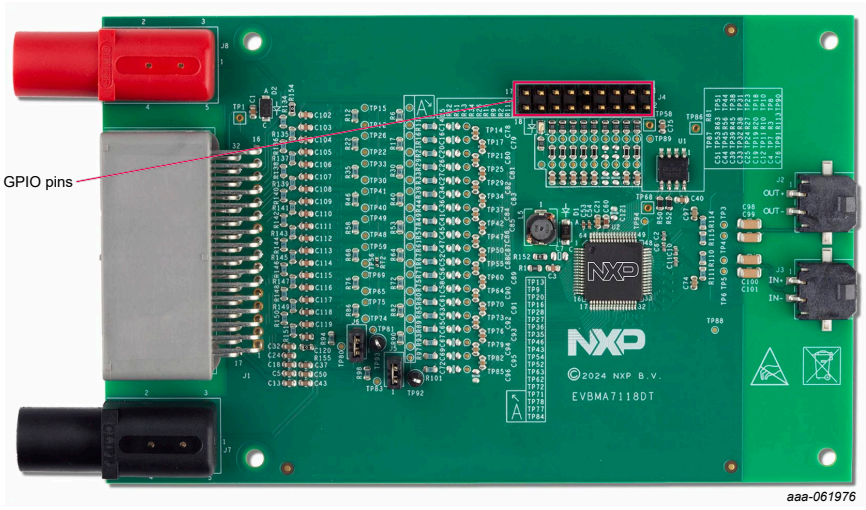
3.4.5 Access to GPIO pins and GND test points

The BMA7118 offers 9 GPIO pins. The GPIO pins offer several functionalities. To allow an easy connection of application-specific circuitry, each GPIO pin is available at connector J4. Connector J4 is also offering several GND pins that can be used for the connection of customer-specific equipment.

Note: *If a specific external circuit is connected, it may be necessary to remove the default circuitry connected at the PCB to this GPIO.*



Schematic view



PCB location

Figure 8. GPIO access

4 Installation and use of software tools

The EVBMA7118DT is not distributed with software. Multiple SW bundles support the EVBMA7118DT. These SW bundles allow a quick evaluation. To select the best evaluation environment, contact the NXP sales support.

5 Troubleshooting

Some common issues and troubleshooting procedures are detailed below. The list below is not an exhaustive list by any means, and additional debug may be needed.

Table 4. Troubleshooting

Problem	Evaluation	Explanation	Corrective action
Unable to establish TPL communication	check TPL connection between the TPL controller and the targets	If there is an interruption in the connection, communication cannot be established.	ensure proper connection
	check supply for all involved components	If the supply for one or more devices in a chain is not present, the devices do not forward communication and communication cannot be established.	Ensure a proper supply connection. Ensure that supplies are turned on with a voltage inside the valid supply range of the ICs. If you use the external supply option, ensure that the needed shorts are present.
	check TPL port connection	After a new power on, the device must be woken via the lower TPL port (J3). If the TPL controller is connected to the higher TPL port (J2), the device does not wake up.	Ensure that the correct TPL port is used for the connection.
Cell 0 is measured as 0 V	check jumpers J5 and J6	With J5 and J6, the connection for the primary measurement on cell 0 can be interrupted to allow the connection of external equipment.	Ensure that J5 and J6 are placed well.
Cell 0 and cell 1 have deviations between primary and secondary measurement.			
Floating cell voltage measurement with supply option lab supply	check if the correct supply option for the board is used	The evaluation board has two supply options. When the laboratory supply option is used, the resistive ladder (R154, R155, and R134 to R151) must be populated.	Ensure that R154, R155, and R134 to R151 are populated.

Table 4. Troubleshooting...*continued*

Problem	Evaluation	Explanation	Corrective action
Cell voltage measurement outside expected accuracy	check the applied voltage at the cell input connection	With the supply option lab supply, the cell voltages are subject to the tolerances of the resistive ladder.	Check applied voltages as a baseline for accuracy estimations.
		With the supply option connection to battery cells, leakage currents caused by the resistive ladder influence the measurement.	Check if the resistive ladder is removed, check applied voltages as baseline for accuracy estimations.
	check markings on the IC	Early evaluation boards are populated with engineering silicon. This silicon may, especially at extreme temperatures, not meet the final accuracy estimations.	Check with your sales representative which accuracy can be expected for the silicon populated on your PCB. Upgrade the IC to a later version or use a later evaluation board.
Cell connection test not working as expected	no open connection is detected even when the connection is open	If the connection to the board is open, the resistive divider (R154, R155, and R134 to R151) still provides a cell voltage to the board.	Ensure that R154, R155, and R134 to R151 are not populated when performing open load tests on the connection to the EVB.
	detection of an open connection for CT0 and CT1, when there should be no open	Jumpers J5 and J6 allow the simulation of a fault for the primary measurement. The secondary measurement remains intact.	Ensure that open load testing is using the primary measurement.

6 Schematics, board layout, and bill of materials

The board schematics, board layout, and bill of materials are available via the tool summary page https://www.nxp.com/EVBMA7118DT.

7 References

[1] Tool summary page for EVBMA7118DT at https://www.nxp.com/EVBMA7118DT.

[2] Product summary page for BMA7118 device at https://www.nxp.com/BMA7118.

8 Revision history

Table 5. Revision history

Document ID	Release date	Description
UM12092 v.1.0	26 September 2025	initial version

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