UG10327

MCX E31x Hardware Design Guide

Rev. 1.0 — 9 October 2025 **User guide**

Document information

Information	Content
Keywords	UG10327, MCX, MCX E31x
Abstract	Hardware design guide for MCX E31x MCU, covering power, decoupling, crystal, and Ethernet

1 Introduction

The MCX E31x microcontroller expands the Arm Cortex MCU portfolio within the MCX family with higher memory options and along side a richer peripheral set, extending capability into various industry applications.

The MCX E31x series devices are well suited to a wide range of applications in electrical harsh environments. This enhancement extends its capabilities to various industry applications, particularly in electrically harsh environments. The MCX E31x series devices are optimized for cost-sensitive applications with low pin-count options.

The purpose of this user guide is to describe possible hardware considerations using the MCX E31x microcontroller in the industry. It covers the most important topics such as the power considerations, bulk/bypass and decoupling capacitors required, reset, crystal, Ethernet, and QSPI configurations. This document also provides PCB Layout recommendations.

2 Power system

The following sections describe different options for power supply configurations, and cover considerations for proper connection of supply and ground pins.

2.1 MCX E31x power domains and configurations

The MCX E31B microcontroller features two flexible and externally supplied power domains: VDD_HV_A, VREFH, and VDD_HV_B. These can be powered at the same or different voltage levels depending on application requirements. Also, it includes a V15 domain to +1.5 V that can be supplied using an external NPN ballast transistor. In contrast, the MCX E315, MCX E316, and MCX E317 variants have a single power domain, VDD_HV_A. This VDD_HV_A reference is the voltage domain for their IOs pins.

Table 1 shows all positive power pins and domains that must be supplied externally along with internal MCU references.

Table 1. Power supply pins and domains

MCU	Package	Power supply pins and domains					
		VDD_HV_A	VREFH	VDD_HV_B	V15	V25	V11
		+3.3 V or +5.0 V	≤ VDD_HV_A	+3.3 V or +5.0 V	+1.5 V	+2.5 V	+1.1 V
MCX E31B	172 HDQFP	Domain and Ref. voltage for I/O pins	ADC high reference voltage	Domain and Ref. voltage for I/O pins	Power supply input	Internal MCU reference	Internal MCU reference
MCX E317 MCX E316 MCX E315	48 LQFP 100 HDQFP 172 HDQFP	Domain and Ref. voltage for I/O pins	ADC high reference voltage	NA	NA	Internal MCU reference	Internal MCU reference

This section covers only an overview of the voltage domains for the different interfaces and I/Os in the MCU. Refer to the latest version of the device *Data sheet* and *Reference Manual* for more details.

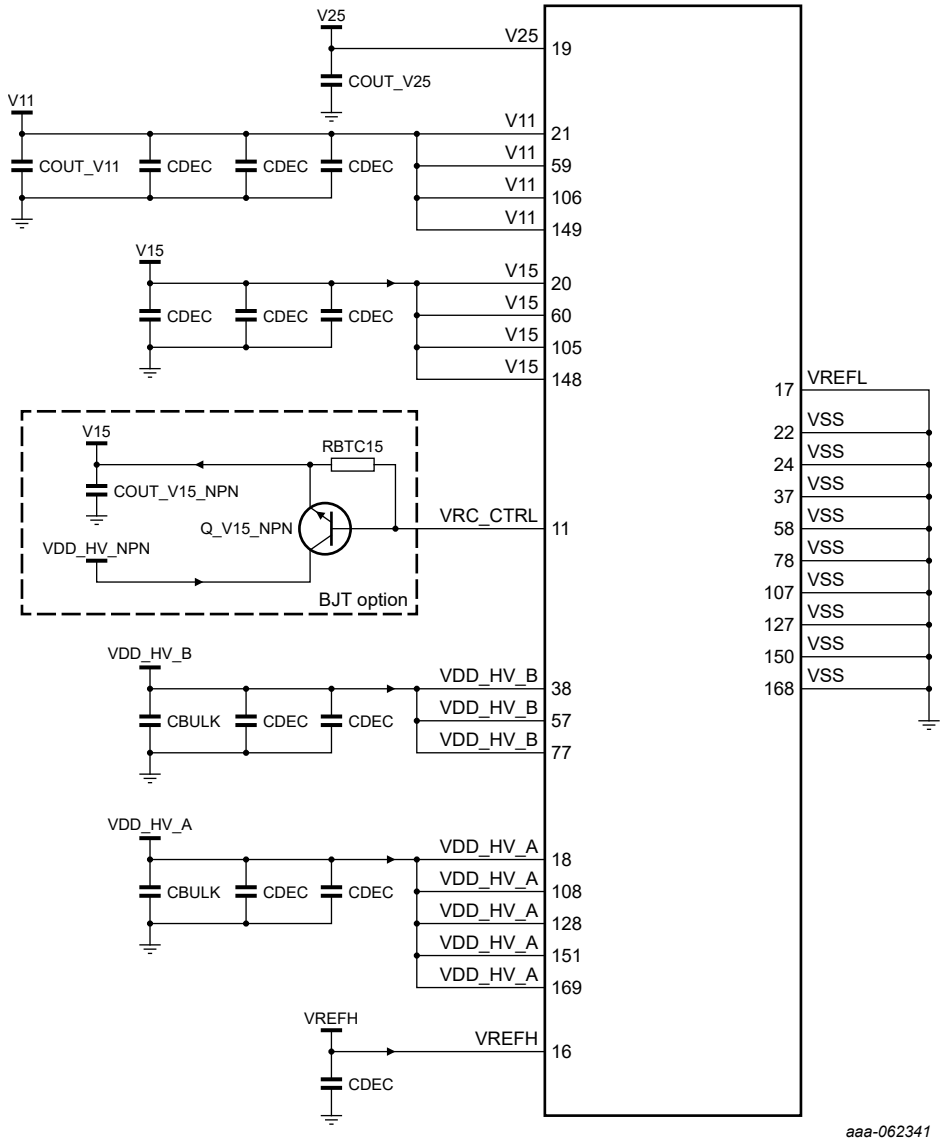


Figure 1. General view of the pinout and power domains for MCX E31B - 172 HDQFP package

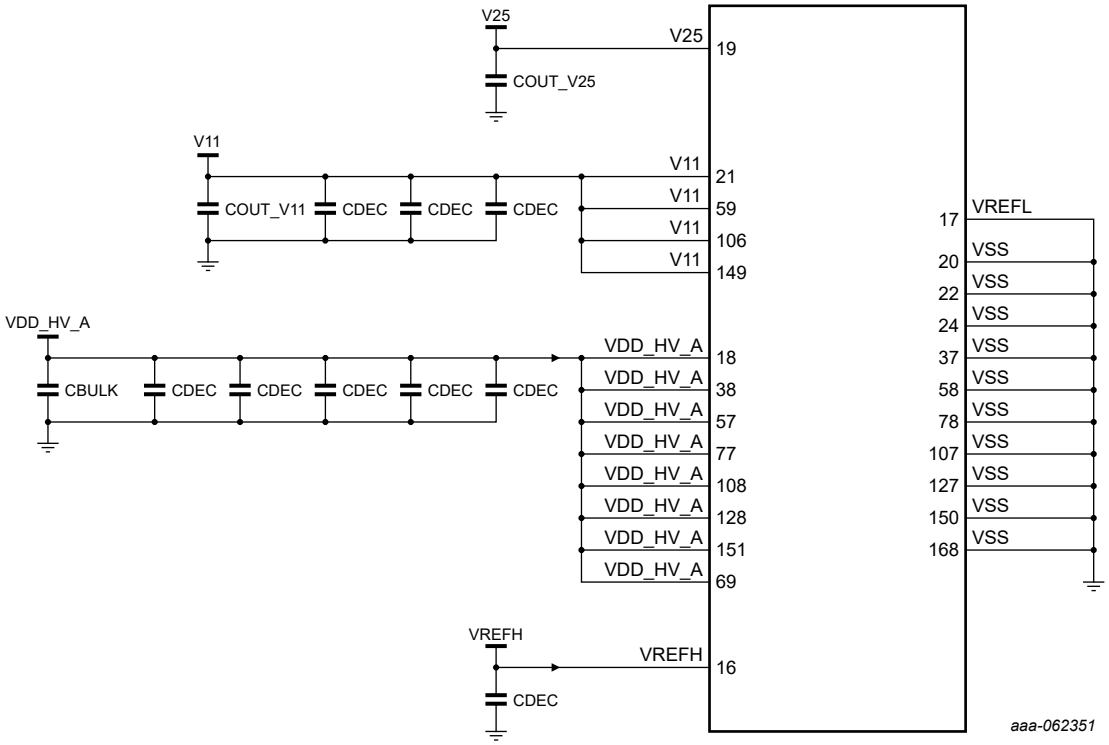


Figure 2. General view of the pinout and power domains for MCX E317 - 172 HDQFP package

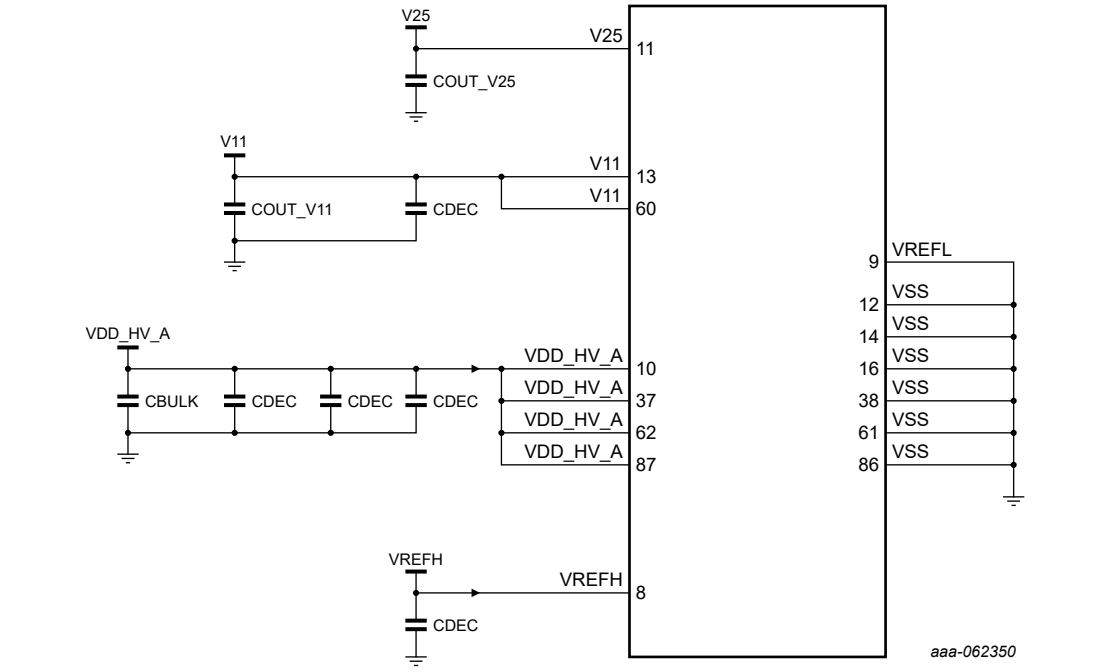


Figure 3. General view of the pinout and power domains for MCX E317, MCX E316 - 100 HDQFP package

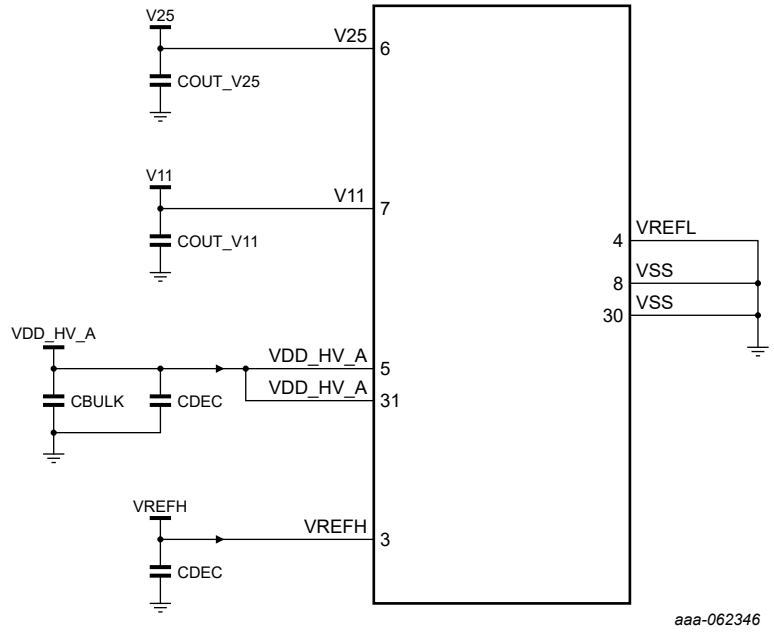


Figure 4. General view of the pinout and power domains for MCX E316, MCX E315 - 48 LQFP package

2.2 VDD_HV_A - main I/O and analog supply voltage

VDD_HV_A is the main I/O and analog supply voltage in the MCX E31x MCU. The VDD_HV_A domain must be connected to an external power supply of +3.3 V or +5.0 V. An off-chip local Bulk/bypass and decoupling capacitors between the VDD_HV_A pins and the VSS reference are required.

Table 2. VDD_HV_A – main I/O and analog supply pins

MCU pin name	Normal operating voltage	MCX E31x MCU package - pin number				Comments
		MCX E315/316 48 LQFP	MCX E315/316/317 100 HDQFP	MCX E31B 172 HDQFP	MCX E317 172 HDQFP	
VDD_HV_A	+3.3 V or +5.0 V	5	10	18	18	All VDD_HV_A pins must be shorted and connected externally to a common reference on the PCB. Use a decoupling capacitor for each supply pin. Add a local bulk/bypass capacitor just for the VDD_HV_A domain, to increase the robustness and decoupling effect on this voltage reference of the MCU.
		31	62	108	108	
		-	87	128	128	
		-	37	151	151	
		-	-	169	169	

2.3 VREFH – ADC high reference voltage

VREFH is the ADC high reference voltage. An off-chip decoupling capacitor between the VREFH pin and the VSS/VREFL reference is required.

The VREFH is the ADC high reference voltage in the MCX E31x MCU. The VREFH pin must be connected to an external power supply or a reference voltage ≤ VDD_HV_A. An off-chip local decoupling capacitor between the VREFH pin and the VSS/VREFL reference is required.

Table 3. VREFH – ADC high reference voltage

MCU pin name	Normal operating voltage	MCX E31x MCU package - pin number				Comments
		MCX E315/316 48 LQFP	MCX E315/316/317 100 HDQFP	MCX E31B 172 HDQFP	MCX E317 172 HDQFP	
VREFH	≤VDD_HV_A	3	8	16	16	A decoupling capacitor must be used on the supply pin.
VREFL	GND	4	9	17	17	

2.4 VDD_HV_B - secondary I/O supply voltage

The VDD_HV_B is the secondary I/O supply voltage in some versions of the MCX E31x MCU family. The VDD_HV_B domain must be connected to an external power supply of +3.3 V or +5.0 V. An off-chip local Bulk/bypass and decoupling capacitors between the VDD_HV_B pins and the VSS reference are required.

Table 4. VDD_HV_B – secondary I/O supply voltage

MCU pin name	Normal operating voltage	MCX E31x MCU package - pin number				Comments
		MCX E315/316 48 LQFP	MCX E315/316/317 100 HDQFP	MCX E31B 172 HDQFP	MCX E317 172 HDQFP	
VDD_HV_B	+3.3 V or +5.0 V	-	-	38	-	All VDD_HV_B pins must be shorted and connected externally to a common reference on the PCB. Use a decoupling capacitor for each supply pin. Add a local bulk/bypass capacitor for the VDD_HV_B domain to increase the robustness and decoupling effect on this voltage reference of the MCU.
		-	-	57	-	
		-	-	77	-	

2.5 V11 - core logic voltage supply (+1.1 V)

V11 is the internally generated core logic voltage supply. An off-chip Bulk/bypass, decoupling and filter capacitors between the V11 pins and the VSS reference is highly recommended. This reference voltage must not be used or connected to other interfaces in the application.

Table 5. V11 – Core logic voltage supply (+1.1 V)

MCU pin name	Normal operating voltage	MCX E31x MCU package - pin number				Comments
		MCX E315/316 48 LQFP	MCX E315/316/317 100 HDQFP	MCX E31B 172 HDQFP	MCX E317 172 HDQFP	
V11	+1.1 V Internal voltage reference	7	13	21	21	All V11 pins must be shorted and connected externally together to a common reference on the PCB. Use a decoupling capacitor for each supply pin. Add a local bulk/ bypass capacitor for the V11 domain to increase the robustness and decoupling effect on this voltage reference of the MCU.
		-	60	59	59	
		-	-	106	106	
		-	-	149	149	

2.6 V25 - flash memory supply (+2.5 V)

V25 is the internally generated flash memory supply. An off-chip filtering and decoupling capacitor between the V25 pin and the VSS reference is required. This reference voltage must not be used or connected to other interfaces in the application.

Table 6. V25 – Flash memory supply (+2.5 V)

MCU pin name	Normal operating voltage	MCX E31x MCU package - pin number				Comments
		MCX E315/316 48 LQFP	MCX E315/316/317 100 HDQFP	MCX E31B 172 HDQFP	MCX E317 172 HDQFP	
V25	+2.5 V Internal voltage reference	6	11	19	19	This internal reference voltage must not be used or connected to other interfaces in the application.

2.7 V15 - high-current logic supply voltage (+1.5 V)

V15 is the high-current logic supply voltage for some MCU versions of the MCX E31x family. The MCX E31x MCU provides the option to supply the voltage reference either using an external NPN ballast transistor and a stability ceramic capacitor or supplying externally by an SBC to +1.5 V. An off-chip bulk/bypass capacitor and a decoupling capacitor between each V15 pin and the VSS reference are required for both configurations. This MCU reference voltage must not be used or connected to other interfaces in the application.

Table 7. V15 – high current logic supply voltage

MCU pin name	Normal operating voltage	MCX E31x MCU package - pin number				Comments
		MCX E315/316 48 LQFP	MCX E315/316/317 100 HDQFP	MCX E31B 172 HDQFP	MCX E317 172 HDQFP	
V15	+1.5 V High-current logic supply voltage	-	-	20	-	All V15 pins must be shorted and connected externally to a common reference on the PCB. Use a decoupling capacitor for each supply pin. Add a local bulk/ bypass capacitor for the V15 domain to increase the robustness and decoupling effect on this voltage reference of the MCU.
		-	-	60	-	
		-	-	105	-	
		-	-	148	-	

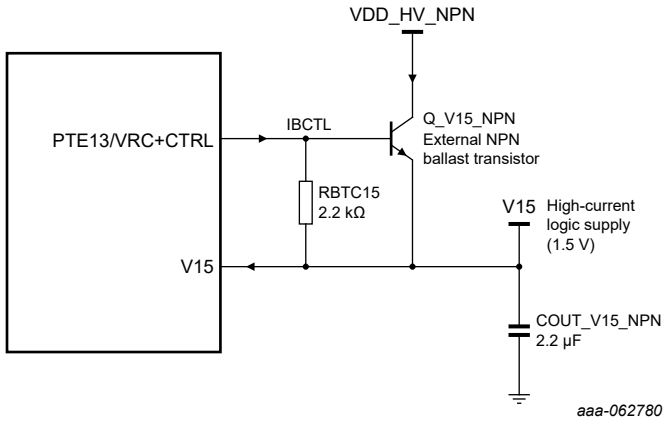


Figure 5. V15 - supplying with the NPN Ballast transistor

Table 8. V15 - component description and values for the external NPN Ballast transistor option

Symbol	Characteristic	Value
Q_V15_NPN	NPN Ballast transistor	-
RBCT15	Metal film resistor	2.2 kΩ
COUT_V15	Stability capacitor. X7R ceramic or tantalum	2.2 µF
CDEC[1]	Decoupling capacitor	100 nF – 220 nF
1.		

[1] A decoupling capacitor can be used per each supply pin and a local Bulk/bypass capacitor just for the V15 domain, to increase the robustness and decoupling effect on this voltage reference of the MCU.

2.8 VSS and VREFL – Ground and ADC reference low

All VSS pins and VREFL pin of the MCU must be externally connected in a continuous and single solid GND plane.

Table 9. VSS pins – MCU Ground reference

MCU pin name	Normal operating voltage	MCX E31x MCU package - pin number				Comments
		MCX E315/316 48 LQFP	MCX E315/316/317 100 HDQFP	MCX E31B 172 HDQFP	MCX E317 172 HDQFP	
VSS	0 V-GND	8	12	22	20	All VSSx pins and the VREFL pin of the MCU must be externally connected in a continuous and single solid GND plane as mandatory.
		30	14	24	22	
		-	16	37	24	
		-	38	58	37	
		-	61	78	58	
		-	86	107	78	
		-	-	127	107	
		-	-	150	127	
		-	-	168	150	
		-	-	-	168	
VREF	VSS	4	9	17	17	

2.9 Bulk and decoupling capacitors

The effectiveness of the bulk/bypass and the decoupling capacitors depends on the optimal placement and connection type. The bulk capacitor acts as a local power supply for the power pin. It should be placed near the decoupling capacitors and as close as possible to the assigned reference voltage pin. Decoupling capacitors make the current loop between supply, MCU, and ground reference as short as possible for high-frequency transients and noise. Therefore, each decoupling capacitor should be placed as close as possible to each of its respective power supply pin. The ground side of the decoupling capacitor should have a via to the pad, which goes directly down to the ground plane.

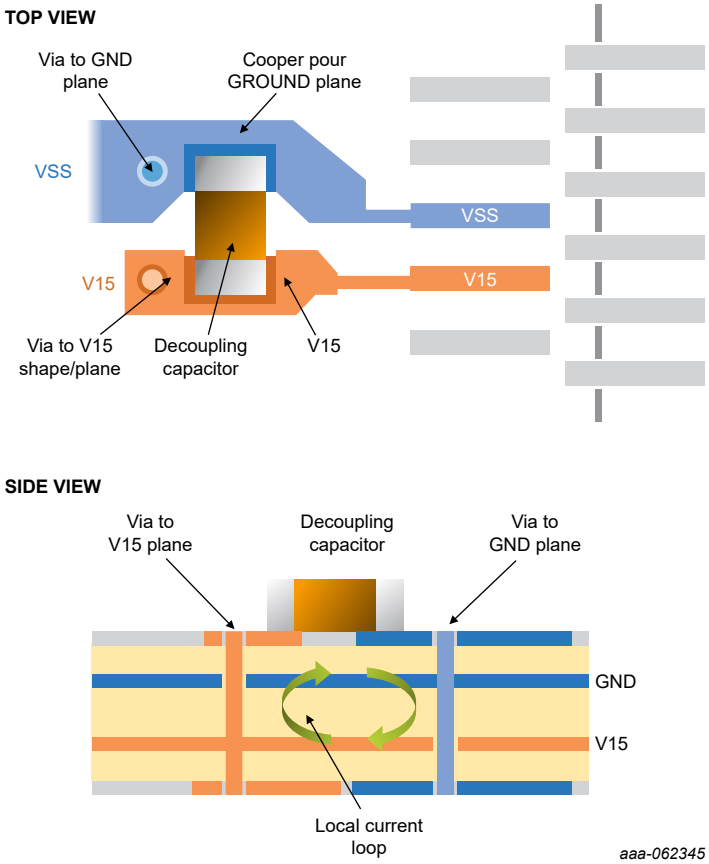


Figure 6. Bulk and decoupling capacitor connections

2.10 Power considerations

The MCX E31x MCU has great versatility in its power supply because in some models (MCX E31B) it integrates three external power domains (VDD_HV_A, VDD_HV_B, and V15), and can generate other voltages using some special pins such as VRC_CTRL (only available in some models). These special pins can be activated or deactivated. However, Domain A and Domain B cannot be deactivated by any Software command.

If power to Domain B is removed externally, the microprocessor resets due to built-in voltage sensors and indicator flags that detect power issues, protecting the microcontroller. However, if power to Domain A is removed externally, the entire MCX E31x shuts down.

2.10.1 MCU power supply ramp rate

During power-on of the MCU, the power supply must assure a ramp-rate within this range from VDD_OFF (= 0.1 V) to the voltage operating level of VDD_HV_A, VDD_HV_B, and V15. The outcome of violating the specification causes unexpected behavior, stuck operation or damage in the MCU.

Note: *For detail on the maximum and minimum limit of MCU supply ramp rate, refer to the MCX E31x device data sheet.*

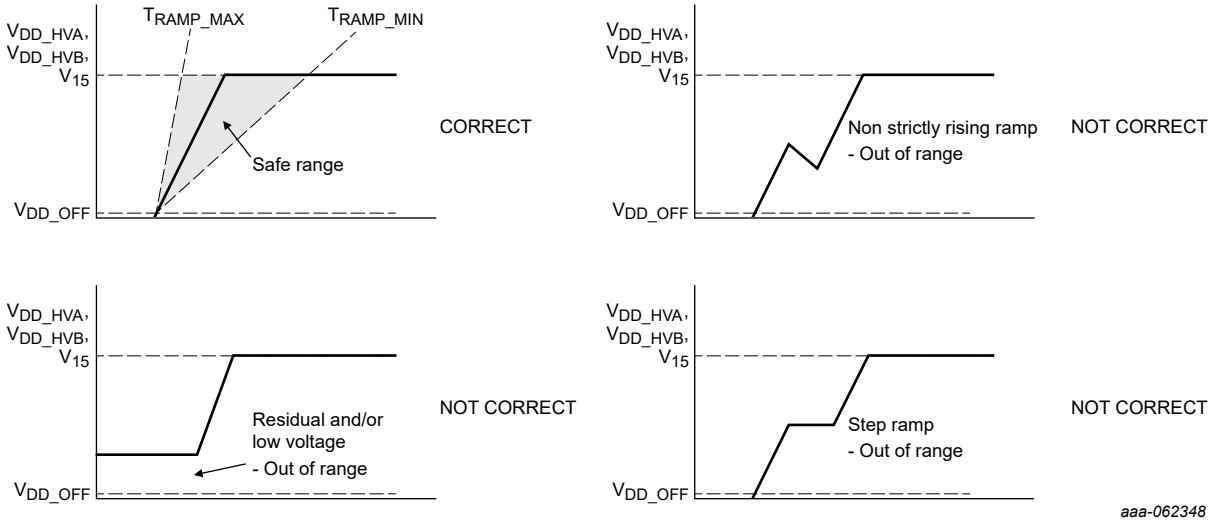


Figure 7. MCU power supply ramp rate

2.11 Pinout differences between MCX E31B - 172 HDQFP and MCX E317 - 172 HDQFP

Table 10 describes the pinout differences between MCX E31B - 172 HDQFP and MCX E317 - 172 HDQFP.

Table 10. Pinout differences between MCX E31B - 172 HDQFP and MCX E317 - 172 HDQFP

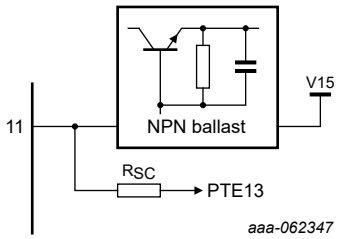
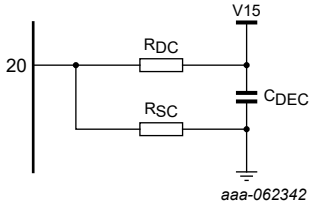
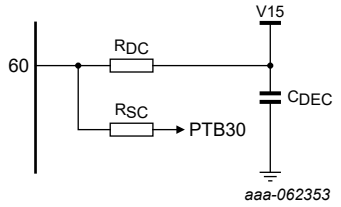
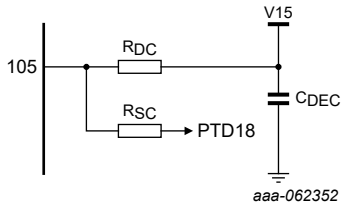
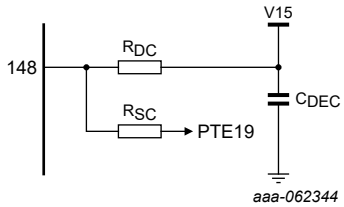
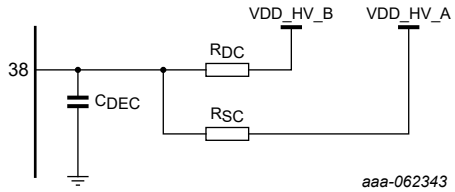
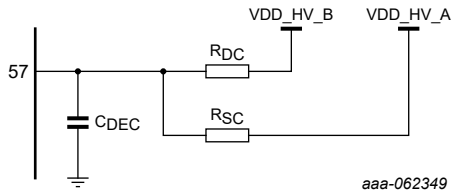
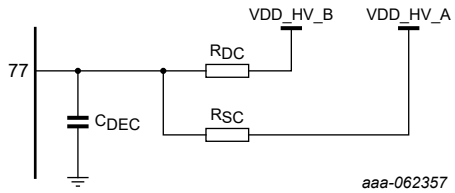
172 HDQFP MCU pin number	MCX E317			MCX E31B		Topology recommended for a drop-in replacement between an MCX E317 and an MCX E31B on a 172 HDQFP package
	Pin name	Pin function	I/O power domain	Pin name	Pin function	
11	PTE13	IO	VDD_HV_A	PTE13	VRC_CTRL - PMC voltage regulator control output [4]	 See [1], [2], [3], [4]
20	VSS	Supply GND	-	V15	+1.5 V - High-current logic supply voltage	 See [1], [2], [3], [4]
60	PTB30	IO	VDD_HV_A	V15	+1.5 V - High-current logic supply voltage	

Table 10. Pinout differences between MCX E31B - 172 HDQFP and MCX E317 - 172 HDQFP*...continued*

172 HDQFP MCU pin number	MCX E317			MCX E31B		Topology recommended for a drop-in replacement between an MCX E317 and an MCX E31B on a 172 HDQFP package
	Pin name	Pin function	I/O power domain	Pin name	Pin function	
						See [1], [2], [3], [4]
105	PTD18	IO	VDD_HV_A	V15	+1.5 V - High-current logic supply voltage	 See [1], [2], [3], [4]
148	PTE19	IO	VDD_HV_A	V15	+1.5 V - High-current logic supply voltage	 See [1], [2], [3], [4]
38	VDD_HV_A	VDD_HV_A - main I/O and analog supply voltage	-	VDD_HV_B	VDD_HV_B - secondary I/O supply voltage	 See [1], [2], [3], [5], [6]
57	VDD_HV_A	VDD_HV_A - main I/O and analog supply voltage	-	VDD_HV_B	VDD_HV_B - secondary I/O supply voltage	 See [1], [2], [3], [5], [6]
77	VDD_HV_A	VDD_HV_A - main I/O and analog supply voltage	-	VDD_HV_B	VDD_HV_B - secondary I/O supply voltage	 See [1], [2], [3], [5], [6]

[1] $R_{DC} = R_{SC} = 0\ \Omega$.
[2] R_{DC} must be used just for MCX E31B and R_{SC} should be removed.
[3] R_{SC} must be used just for MCX E317, and R_{DC} should be removed.
[4] The V15 reference for the MCX E31B should have all considerations mentioned in Section 2.7.
[5] The VDD_HV_A reference for the MCX E317 should have all considerations mentioned in Section 2.2.
[6] The VDD_HV_B reference for the MCX E31B should have all considerations mentioned in Section 2.4.

3 Clock circuitry

The MCX E31x MCU has the following clock sources:

- 8 MHz - 40 MHz fast external oscillator (FXOSC)
- 48 MHz fast internal reference clock oscillator (FIRC)
- 32 kHz low-power oscillator (SIRC)
- 32 kHz slow external oscillator (SXOSC)
- Up to 320 MHz system phased lock loop (SPLL)

FIRC and SIRC are internal and do not have to be considered from the hardware design perspective. The external oscillator works with a range from 8 MHz to 40 MHz. It provides an output clock that can be provided to the PLL or used as a clock source for some peripherals. When using the external oscillator as the input source for the PLL, the frequency range of the external oscillator should be 8 MHz to 40 MHz.

3.1 EXTAL and XTAL pins

These pins provide the interface for a crystal to control the internal clock generator circuitry. EXTAL is the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier. The Pierce oscillator provides a robust, low-noise, and low-power external clock source. It is designed for optimal startup margin with typical crystal oscillators. The MCX E31x MCU supports crystals or resonators ranging from 8 MHz to 40 MHz. The input capacitance of the EXTAL and XTAL pins is 7 pF.

Table 11. EXTAL and XTAL pins

MCU pin name	Normal operating voltage	MCX E31x MCU package - pin number				Comments
		MCX E315/316 48 LQFP	MCX E315/316/317 100 HDQFP	MCX E31B 172 HDQFP	MCX E317 172 HDQFP	
XTAL	External crystal output	10	17	25	25	
EXTAL	External crystal input	9	15	23	23	

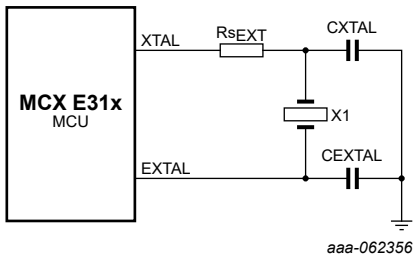


Figure 8. Reference oscillator circuit

Table 12. Components of the oscillator circuit

Symbol	Description
RsEXT	Series resistor for current limitation
X1	Quartz crystal / ceramic resonator
CXTAL	External load capacitor on XTAL pin
CEXTAL	External load capacitor on EXTAL pin

Table 12. Components of the oscillator circuit*...continued*

Symbol	Description
The Rs and load capacitors values depend on the specifications of the crystal and on the board capacitance. It is recommended to develop evaluation and characterization of the crystal on the PCB in collaboration with the part manufacturer.	

4 Debug and programming interface

This section explains best practices for debugging and programming the MCX E31x MCU, including reset mechanisms, external reset pin considerations, and JTAG/TRACE connectivity.

4.1 RESET system

Resetting the MCU provides a way to start processing from a known set of initial conditions. System reset begins with the on-chip regulator in full regulation and system clocking generation from an internal reference.

4.2 External pin RESET

For all reset sources, the RESET_B pin is driven low by the MCU for at least 128 bus clock cycles and until flash memory initialization has completed. After flash memory initialization has completed, the RESET_B pin is released and the internal chip reset deasserts. Keeping the RESET_B pin asserted externally delays the negation of the internal chip reset. The RESET pin is the same as the standard SIUL2_GPIO/eMIOS_GPIO. It can operate as a pseudo-open-drain output because there is also a PMOS device in the output stage.

The reset pin, similar to some other GPIO has a weak internal pullup. If the environment and the customer application are noisy, an external pullup resistor to VDD_HV_A must be added directly to the reset pin to avoid a sporadic or unintended reset occurs. Refer to the device data sheet for the levels of voltage and current allowed in the pin. A capacitor in the reset line is not directly required for the MCU. However, an external capacitor can be added between the RESET pin and the ground for additional ESD protection. If used, this capacitor should be placed as close as possible to the debug interface or connector. The values of the pullup resistor and the capacitor must be selected according to the design requirements of the application. Refer to the device data sheet for the minimum RESET pulse value that can be detected for the MCU.

4.3 JTAG and TRACE interface

A number of commonly used debug connectors are shown here. Most of the Arm development tools use one of these pins. When developing your Arm circuit board, it is recommended to use a standard debug signal arrangement to make connection to the debugger easier:

Table 13. JTAG signal description

Signal name	Description	MCU pin name	MCX E31x MCU package - pin number				Recommend	I/O power domain
			MCX E315/316 48 LQFP	MCX E315/316/31 100 HDQFP	MCX E31B 172 HDQFP	MCX E317 172 HDQFP		
JTAG_TDO	JTAG test data output	PTA10	44	92	161	161	Pullup	VDD_HV_A
JTAG_TDI	JTAG test data input	PTC5	45	95	165	165	Pullup	
JTAG_TCK/ SWD_CLK	Clock into the core	PTC4	46	96	166	166	Pulldown	

Table 13. JTAG signal description*...continued*

Signal name	Description	MCU pin name	MCX E31x MCU package - pin number				Recommend	I/O power domain
			MCX E315/316 48 LQFP	MCX E315/316/317 100 HDQFP	MCX E31B 172 HDQFP	MCX E317 172 HDQFP		
JTAG_TMS/ SWD_DIO	JTAG test mode select	PTA4	48	98	170	170	Pullup	
RESET	Reset MCU	PTA5	47	97	167	167	Pullup	
External pullup/down resistors for the JTAG signals can be added to increase debugger connection robustness.								

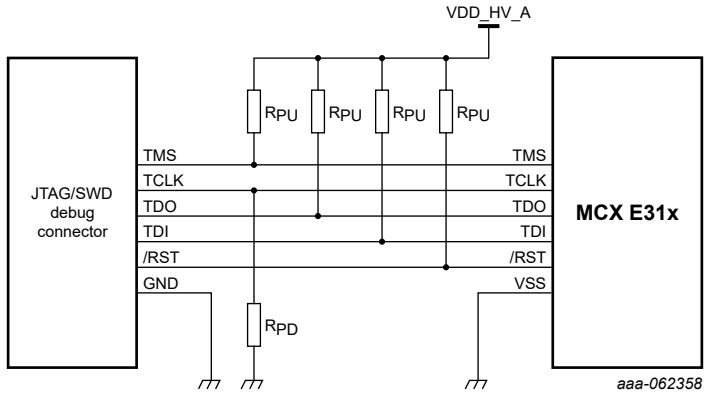


Figure 9. JTAG pin connections

Table 14. JTAG connector – Component description

Symbol	Parameter	Typ value range	Units
R_{PU}	Pullup resistor	4.7 k-10 k	Ω
R_{PD}	Pulldown resistor	4.7 k-10 k	Ω

5 Communication modules

When in an application, different voltage levels in the MCU domains are used (for example VDD_HV_A = +5.0 V and VDD_HV_B = +3.3 V), ensure that the following communication interfaces are configured to use the same voltage domain (VDD_HV_A or VDD_HV_B).

- FlexCAN
- LPUART
- LPI2C
- LPSPI
- QSPI
- Ethernet MAC
- SAI

Also, verify that the data lines are within the voltage range allowed for that communication. For example, VDD_HV_B = +3.3 V in the case of Ethernet MAC, SAI, and QSPI.

A cross-combination of voltage domains for communication interfaces is not allowed (for example, the TX data line with VDD_HV_A and the RX data line with VDD_HV_B).

5.1 CAN interface

The physical layer characteristics for CAN are specified in ISO-11898-2. This standard specifies the use of cable comprising parallel wires with an impedance of nominally 120 Ω (95 Ω as minimum and 140 Ω as maximum). The use of shielded twisted pair cables is necessary for electromagnetic compatibility (EMC) reasons, although ISO-11898-2 also allows for unshielded cable. A maximum line length of 40 meters is specified for CAN at a data rate of 1 Mb. However, at lower data rates, potentially much longer lines are possible. ISO-11898-2 specifies a line topology, with individual nodes connected using short stubs.

Though not exclusively intended for automotive applications, the CAN protocol is designed to meet the specific requirements of a vehicle serial data bus: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth. Each CAN station is connected physically to the CAN bus lines through a transceiver device. The transceiver can drive the large current needed for the CAN bus and has current protection against defective CAN or defective stations. A typical CAN system with an MCX E31x microcontroller is shown in Figure 10.

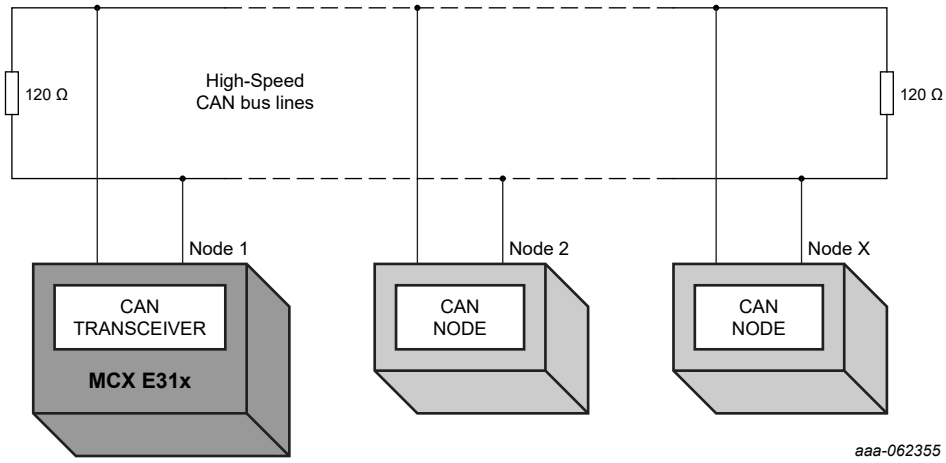


Figure 10. CAN system

The CAN module is a full implementation of the CAN protocol specification, the CAN with flexible data rate (CAN FD) protocol and the CAN 2.0 version B protocol, which supports both standard and extended message frames and long payloads up to 64 bytes transferred at faster rates up to 8 Mbit/s. The message buffers are stored in an embedded RAM dedicated to the CAN module. See the chip configuration details in the Device Reference Manual for the number of message buffers configured in the chip.

Like most other CAN physical transceivers, the CANH, CANL, and SPLIT pins are available for the designer to terminate bus depending on the application. Figure 11 shows examples of the CAN node terminations.

Note:

When operating with different voltage levels in MCU domains (for example, VDD_HV_A = +5.0 V and VDD_HV_B = +3.3 V), ensure that the CANx_TX/RX data lines meet the following requirements:

1. *The CANx_TX/RX data lines must operate within the same voltage domain (VDD_HV_A or VDD_HV_B).*
2. *The data lines must be within the voltage range allowed for communication with the CAN Physical layer.*

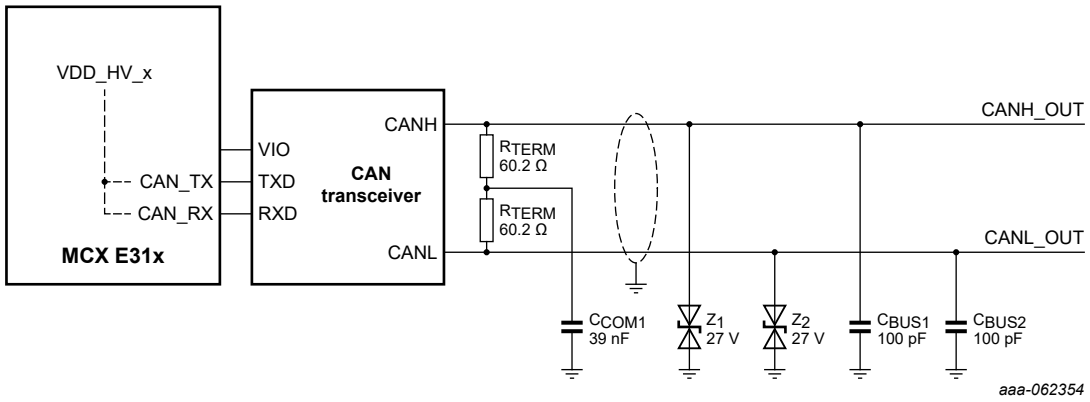


Figure 11. CAN physical transceiver circuit

CAN components data

Table 15. CAN components

Reference	Description
CBUS1 and CBUS2	The Capacitors CBUS1 and CBUS2 are not required. They may be added for EMC reasons, in which case the maximum capacitance from either bus wire to ground must not exceed 300 pF total. If Zener stacks are also needed, the parasitic capacitance of the Zener stacks must also be included in the total capacitance budget.
Z1 and Z2	The Zener stacks Z1 and Z2 could be required to satisfy Automotive EMC requirements (ESD in particular). These devices should be placed close to the connector.
RTERM1, RTERM2, and CCOM1	Depending on the position of the node within the CAN network it might need a specific termination. RTERM1, RTERM2, and CCOM1 must be that they assist in having an overall cable impedance. On a bus implementation of a CAN network only the two nodes on the two ends of the bus have terminator resistors. The nodes not placed on the end of the CAN bus do not have termination. A thorough analysis is required to maintain this requirement of the CAN networks. The SPLIT pin on the transceiver is optional and the designer might choose not to use it. This pin helps stabilize the recessive state of the CAN bus and can be enabled or disabled by software when required.
LBUS1–Common mode choke	A common mode choke on the CANH and CANL lines can help reduce coupled electromagnetic interference and needed to satisfy Automotive EMC requirements. This choke, together with transient suppressors on the transceiver pins, can greatly reduce coupled electromagnetic compatibility noise, and high frequency transients. LBUS1 is not required.

CAN termination:

In a transmission line, there are two current paths, one to carry the currents from the driver to the receiver and another to provide the return path back to the driver. The CAN transmission lines are complex because there are two signals that are sharing a common termination and a ground return path. For reliable CAN communications, it is essential that the reflections in the transmission line be kept as small as possible. This can only be done by proper cable termination.

Reflections happen quickly during and just after signal transitions. On a long line, the reflections are more likely to continue long enough to cause the receiver to misread logic levels. On short lines, the reflections occur sooner and have no effect on the received logic levels.

5.2 Ethernet MAC interface

The MII/RMII interface signal can be directly routed to the MAC-NET interface. However, series termination resistors may be considered on RXCLK, TXCLK, and all RX/TX signals for EMI suppression. These resistors should be placed within 100 mils of the Ethernet physical interface and routed to an uninterrupted reference plane. Series termination resistors with value between 33 Ω and 50 Ω are commonly recommended to improve electromagnetic interference (EMI) performance.

Although RMII and MII are synchronous bus architectures, various factors limit signal trace lengths. With a longer trace, the signal becomes more attenuated at the destination and therefore more susceptible to noise interference. Longer traces also act as antennas, and if run on the surface layer, can increase EMI radiation. If a long trace is running near and adjacent to a noisy signal, the unwanted signals could be coupled in as crosstalk. It is recommended to keep the signal trace lengths as short as possible. Ideally, keep the traces under 6 inches. Trace length matching to within 2.0 inches on the MII or RMII bus is also recommended. Significant differences in the trace lengths can cause data timing issues. Minimize the use of vias throughout the design. Vias add capacitance to signal traces. As with any high-speed data signal, good design practices dictate that impedance should be maintained and stubs should be avoided throughout the entire data path.

Because the TX and RX data signals are triggered by the rising edge of the clock, communication in MII and RMII is synchronous. Therefore, the length of the EMAC data lines and the clock line between the K3 microcontroller and the PHY must be matched. The allowed deviation in length matching depends on the rise/fall time for digital signals between these two elements, although it is recommended that any deviation be less than 10 mm as MII and RMII.

MII signaling: Figure 12 shows the PHY-MAC and MAC-MAC connections in an MII interface. Data is exchanged via 4-bit wide data nibbles TXD[3:0] and RXD[3:0]. Data transmission is synchronous with the transmit (TX_CLK) and receive (RX_CLK) clocks. For the PHY-MAC interface, both clock signals are provided by the PHY and are typically derived from an external crystal running at a nominal 25 MHz or from the CLK_OUT signal on the switch. When the Ethernet Switch is configured for MAC-MAC communication, the switch provides the clocks and acts like a PHY.

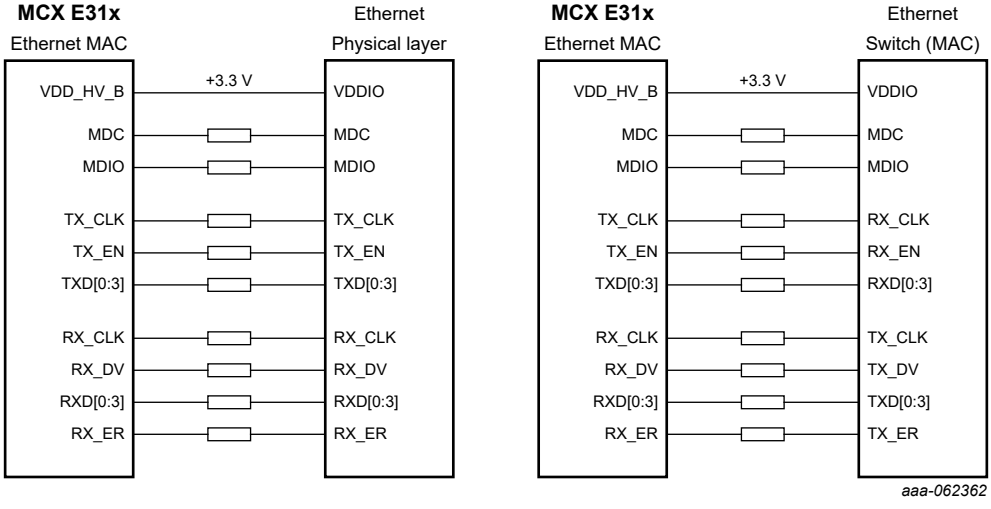


Figure 12. MII interface connections – block diagram

RMII signaling: RMII data is exchanged via 2-bit data signals TXD[1:0] and RXD[1:0] as shown in Figure 13. Transmit and receive signals are synchronous with the shared reference clock, REF_CLK.

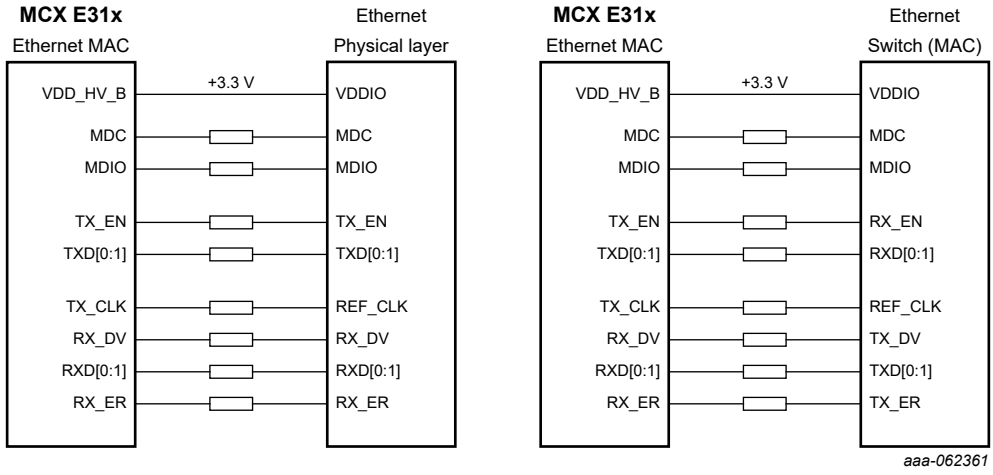


Figure 13. RMII interface connections – block diagram

Note:

All signals of the Ethernet MAC module of the MCX E31x microcontroller are in the VDD_HV_B domain. A method for voltage level translation is not required in the Ethernet Physical layer or MAC interface since the VDD_HV_B domain should be connected to +3.3 V.

6 Quad serial peripheral interface

The MCX E31x MCU has one instance of QuadSPI. The quad serial peripheral interface (QuadSPI) block acts as an interface to an external serial flash device. It supports SDR mode up to 4 bidirectional data lines respectively. The QuadSPI supports an A-side. The following external memory option can be supported:

Single Quad Flash on the A-side

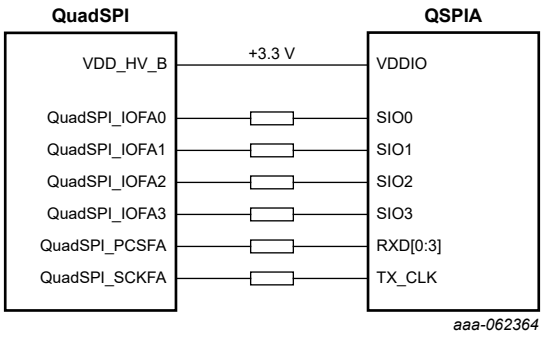


Figure 14. Block diagram - single quad serial Flash

Note: *All signals of the QSPI module of the MCX E31x microcontroller are in the VDD_HV_B domain. A method for voltage level translation is not required in the QSPI memory interface since the VDD_HV_B domain should be connected to +3.3 V.*

Table 16. QSPI signal description

Signal name	MCU pin name	MCX E31x MCU package - pin number				I/O power domain
		MCX E315/316 48 LQFP	MCX E315/316/317 100 HDQFP	MCX E31B 172 HDQFP	MCX E317 172 HDQFP	
QuadSPI_PCSFA	PTC3	-	-	49	-	VDD_HV_B

Table 16. QSPI signal description*...continued*

Signal name	MCU pin name	MCX E31x MCU package - pin number				I/O power domain
		MCX E315/316 48 LQFP	MCX E315/316/317 100 HDQFP	MCX E31B 172 HDQFP	MCX E317 172 HDQFP	
QuadSPI_IOFA3	PTC2	-	-	50	-	VDD_HV_B
QuadSPI_IOFA2	PTD12	-	-	54	-	VDD_HV_B
QuadSPI_IOFA1	PTD7	-	-	51	-	VDD_HV_B
QuadSPI_IOFA0	PTD11	-	-	55	-	VDD_HV_B
QuadSPI_SCKFA	PTD10	-	-	56	-	VDD_HV_B

Data and clock signal termination: Clock generation and distribution become more difficult as the speed and performance of microprocessors increase to higher limits. Controlled and precise clocking distribution techniques are needed to maintain a synchronous system. Clock signal quality and skew are the two major problems with distributing clock signals. With higher frequencies, and the associated fast edge rates, long traces behave like transmission lines. Ring back, overshoot, and undershoot occur as a result of poor termination of transmission lines. They contribute to bad signal quality, false switching, and they can cause damage in extreme cases.

Given the effective output driver strength of 22 Ω to 33 Ω and the transmission line characteristic impedance of 50 Ω, you should add the termination resistor close to the output driver, to minimize the reflection as shown in Figure 15.

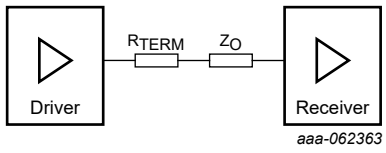


Figure 15. Point-to-point transmission line

Data signal routing: To keep the correct timing for the data transfer from the microcontroller to the IC memory, the PCB data traces should be the same length and time delay as the clock trace from the microcontroller to the IC memory. Data signals should be routed with controlled impedance traces to reduce signal reflections. Avoid routing traces with 90 ° angle corners. The recommendation is to cut the corner and smooth the trace when a trace route must change direction. To improve the signal integrity further, avoid using multiple signal layers for data signal routing. All signal traces should have a continuous and solid GND reference plane.

Clock signal routing: In high-speed synchronous data transfer, good signal integrity in a PCB design is of critical importance, especially for the clock signals, SCLK and DQS. When routing the clock signal, special care should be taken. The following practices are recommended.

- Run the clock signal at least 3W of the trace width away from all other signal traces. This helps keep the clock signal clean from crosstalk noise.
- Use as few via(s) as possible for the whole signal path, each signal via should have a ground transition via next to them; without this, the signal routing could have an impedance change and to cause a signal reflection.
- All signal traces should go with a solid GND reference plane.
- Run the clock trace as straight as possible and avoid using serpentine routing.
- Keep a continuous ground in the next layer as a reference plane.
- Keep as much space between high-speed routing (differential pairs, clock routing, and so on) and other routing. The general principle here is that by spacing out traces at three times their line width, measured center to center, 70 % of their electrical field can be stopped from mutual interference.

7 Unused pins

Table 17 describes the options and configurations for the unused pins and the considerations for other modules and sections of the MCU.

Table 17. Unused pins configuration

Module	Pin name	Function	Recommendation
GPIO	PTx	ENETx	The unused GPIO should be left unconnected or externally connected to VSS/GND reference.
		FTMx	
		FlexIOx	
		CANx	
		LPUARTx	
		LPI2Cx	
		ADCx	
		CMPx	
		Others	
External Clock	XTAL	XTAL	The pins with the XTAL and EXTAL functions must be left unconnected if not in use.
	EXTAL	EXTAL	
JTAG	PTA4	JTAG_TMS	Since these pins have either internal weak pullups (TDI, TDO and TMS) or pulldown (TCK) it is ok to add external pull resistors in parallel to the internal ones to increase debugger connection robustness.
	PTA10	JTAG_TDO	
	PTC5	JTAG_TDI	
	PTC4	JTAG_TCK	
RESET	PTA5	PTA5/TCLK1/ RESET_b	The reset pin cannot be left unconnected. It must be pulled up to VDD_HV_A with an external resistor directly to the RESET pin. Refer to the chapter of RESET system.
Power	VDD_HV_A	Main I/O and Analog Supply Voltage	No VDD_HV_A, VREFH, and VDD_HV_B power pin should be left unconnected or unpowered. All power pins must be shorted together externally on their voltage domain. Appropriate bulk/bypass and decoupling capacitors should be used.
	VDD_HV_B	Secondary I/O Supply Voltage	
	VREFH	ADC High Reference Voltage	
	V15	High-current logic supply voltage (+1.5 V)	No V15 power pin should be left unconnected or unpowered. All V15 power pins must be shorted together externally on their voltage domain. Appropriate bulk/bypass and decoupling capacitors should be used to filter noise on the supply. Refer to the chapter in this document.
	V11	Core logic voltage supply (+1.1 V)	No V11 power pin should be left unconnected. All V11 power pins must be shorted together externally on their voltage domain. Appropriate bulk/bypass and decoupling capacitors should be used to filter noise on the supply. Refer to the chapter in this document. The V11 domain must not be used or connected to other interfaces in the application.
	V25	Flash memory supply (+2.5 V)	The V25 power pin should not be left unconnected; the decoupling capacitor should be used to filter noise on the supply. Refer to the chapter in this document. The V25 domain must not be used or connected to other interfaces in the application.

Table 17. Unused pins configuration*...continued*

Module	Pin name	Function	Recommendation
Ground	VSSx	VSSx	No VSSx/VREFL pin should be left unconnected. All VSSx/VSS_DCDC and VREFL must be shorted together externally to GND.
	VREFL	ADC Low Reference Voltage	

8 References

For more detail on MCX E31x devices, refer to the following documents.

- MCXE315/316/317/31B - Robust 5V Arm Cortex M7 MCU, SIL2 compliant (MCXEP172M160FB0)
- MCXE31x Reference Manual (MCXE31XRM)

9 Acronyms

Table 18. Acronyms

Term	Description
EMAC	Ethernet media access controller
EMC	Electromagnetic compatibility
ESD	Electrostatic discharge
ESD	Electrostatic discharge
FIRC	Fast internal reference clock
FlexCAN	Flexible controller area network interface
GPIO	General-purpose input/output
HDQFP	High-density quad flat package
JTAG	Joint test action group
LPI2C	Low-power inter-integrated circuit
LPSPI	Low-power serial peripheral interface
LPUART	Low-power universal asynchronous receiver/transmitter
MAC	Media access controller
MII	Media-independent interface
NPN	Negative-positive-negative
PCB	Printed-circuit board
PCB	Printed-circuit board
PMOS	P-channel metal-oxide semiconductor
QSPI	Quad serial peripheral interface
RMII	Reduced media-independent interface
SAI	Serial audio interface
SIRC	Slow internal reference clock

10 Revision history

Table 19 summarizes revisions to this document.

Table 19. Revision history

Document ID	Release date	Description
UG10327 v.1.0	9 October 2025	Initial public release

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