UG10272

S32Z280-400EVB Evaluation Board Solution for S32Z2 User Guide

Rev. 1.0 — 10 July 2025 **User guide**

Document information

Information	Content
Keywords	S32Z280, 400EVB, Evaluation Board Solution
Abstract	The primary objective of this document is to highlight the functionality of the S32Z280-400EVB Evaluation Board (EVB) for use by software and hardware developers.

1 Overview

The primary objective of this document is to highlight the functionality of the S32Z280-400EVB Evaluation Board (EVB) for use by software and hardware developers.

The EVBs provide a platform for evaluation and development of S32Z2 automotive products – facilitating hardware & software development and providing robust debug capabilities.

See the board schematics in conjunction to viewing this document.

1. SCH-89955 (S32Z280-400EVB)
2. SCH-54935 (S32X-MB)

Note: *As revisions change, some of the images may show slight differences from delivered boards. Schematics contain full change lists.*

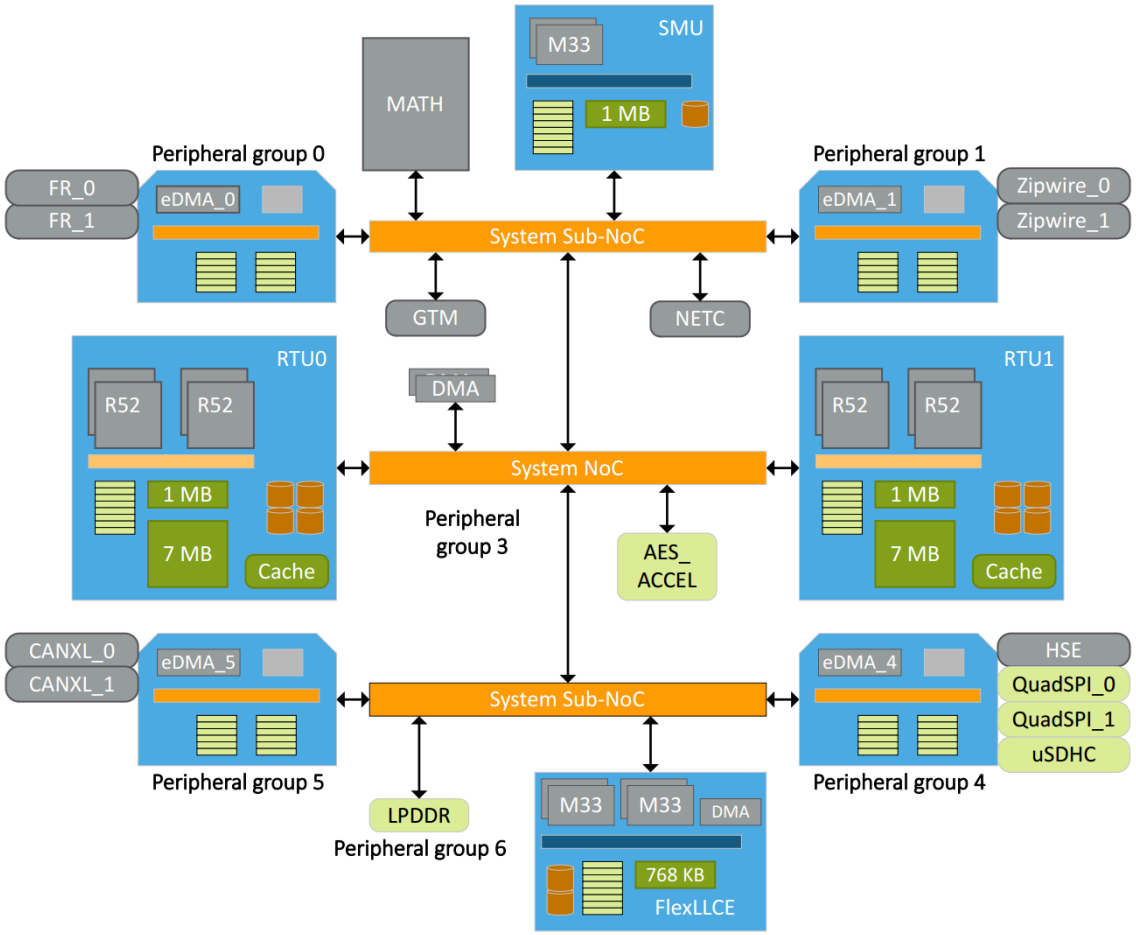


Figure 1. Detailed S32Z2 system diagram

Figure 1 shows a system overview of the S32Z2 device. It is a high-end, 32-bit, Arm-based Microcontroller (MCUs), targeting applications related to safety, vehicle dynamics, domain control & HEV/EV systems. It has a wide feature set, requiring an extensive development platform for evaluating the functions available to a user.

This EVB solution was designed by NXP to allow silicon samples to be evaluated, with as much functionality pinned-out and available to the user as possible. In some cases, pins have been dedicated to a particular purpose on these EVBs and may not be available for alternate functions. Where possible, jumper configuration and on-board multiplexing allows for alternate functions to be evaluated.

The EVB system comprises a common motherboard (S32X-MB) and a daughtercard (S32Z280-400EVB). In this manual, the daughtercard used is the S32Z280-400EVB which is designed to support the S32Z2 which is one of the three unique package options for S32Z2/E2 family MCUs.

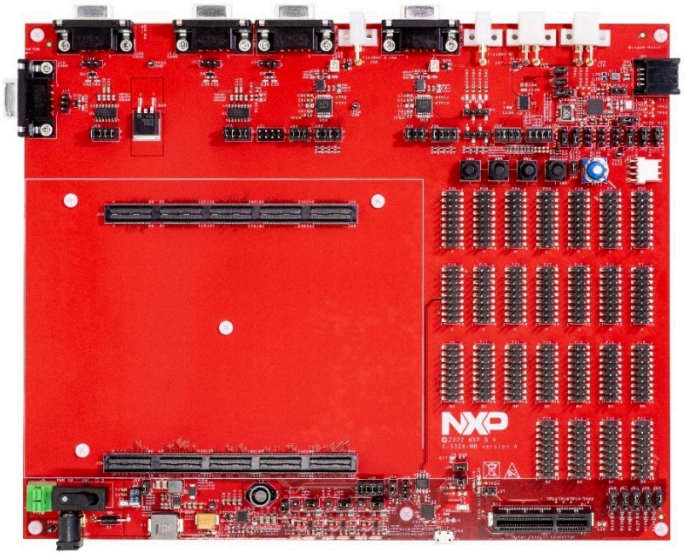


Figure 2. S32X-MB

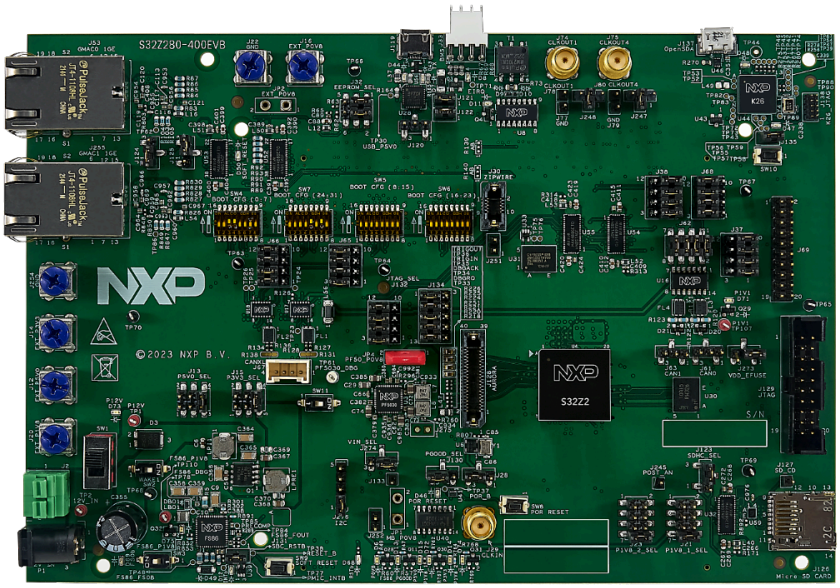


Figure 3. S32Z280-400EVB daughtercard

The daughtercard attaches to the motherboard via long interconnectors on the bottom side of the S32Z280-400EVB daughtercard.

The following figure shows the placement of the board on top of the motherboard. The daughtercard extends past the left side of the motherboard. Support posts have been included in the daughtercard kit to support the weight of the overhanging edge of the daughtercard.

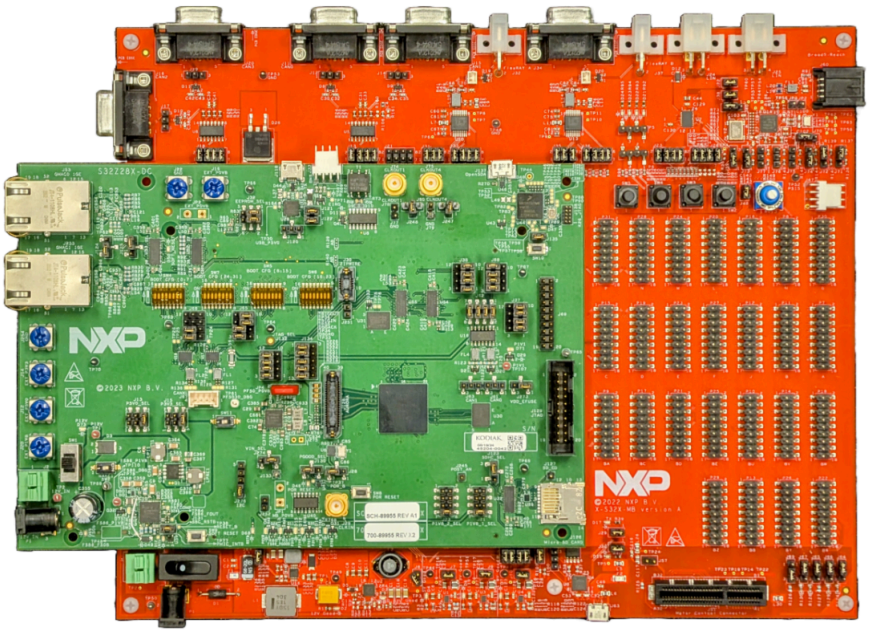


Figure 4. MB and S32Z280-400EVB daughtercard

2 Boot modes

2.1 Introduction

This chapter provides details about different boot options available. This chip supports two boot modes:

1. Serial Boot mode from UART (LINFlexD) and CAN(FlexCAN)
2. Boot from external flash memory (from QuadSPI flash or SD**)**

Combinations of the following inputs control the boot mode:

- Boot mode pins (BOOTMOD _0 and BOOTMOD_1)
- RCON switch Settings

2.2 Serial boot mode

Serial Boot mode is entered via the BOOTMOD input pins. Serial download can also be initiated if the Functional Reset Counter (FREC register in the MC_RGM module) reaches a value ≥ 8.

In Serial Boot mode, BootROM programs the HSE_H SWT (Watchdog timer) for a 60 s timeout, then continuously polls for activity on any of the available interfaces:

- CAN
- UART

If no activity is detected, the timer expires, and the core is reset. BootROM sequentially checks for activity on all available interfaces and selects the first serial interface that it identifies as active as the download interface.

Jumpers J124 and J125 are BOOTMOD _0 / BOOTMOD_1.

BOOTMOD[1:2] = b01 to select serial boot mode.

To select the Serial Boot Mode:

- Switch OFF the power supply
- Set the jumpers as shown in the figure 5:

J124 : Position (2-3)

J125 : Position (1-2)

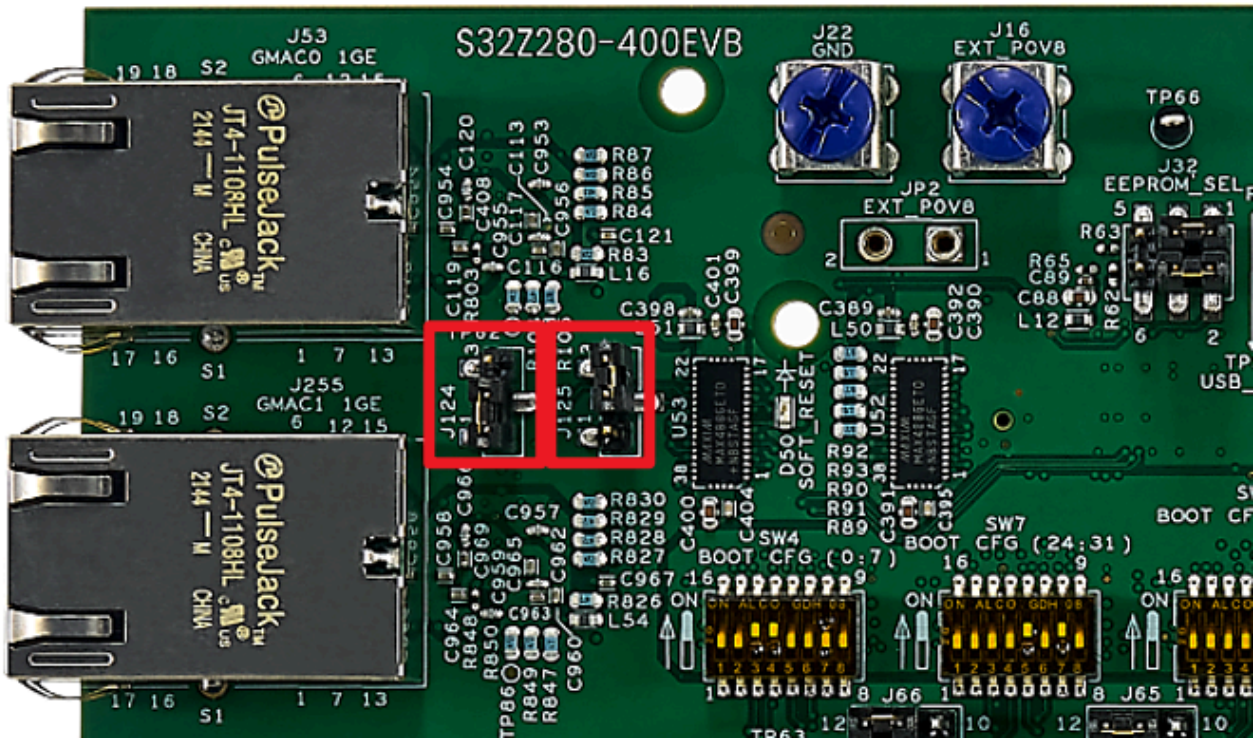


Figure 5. Jumpers J124 and J125 for boot mode selection

2.2.1 FlexCAN

BootROM supports serial download from the FlexCAN module. Communication between the chip and the host (transmitting utility) is done by exchange of data using CAN packets. BootROM supports transfer of data only in non-FD mode.

2.2.2 UART (LINFlexD)

BootROM supports boot from the LINFlexD_9 module, configured in UART mode. The communication between the MCU and the host (transmitting utility) is done by exchange of data through UART packets. LINFlexD_9 is configured to communicate in 8-bit mode with even parity configuration.

To select LINFlexD_9 for the UART:

- Switch off the power supply

- Set the Jumper J247 to position 1-2. As shown in the figure (LIN_SEL).

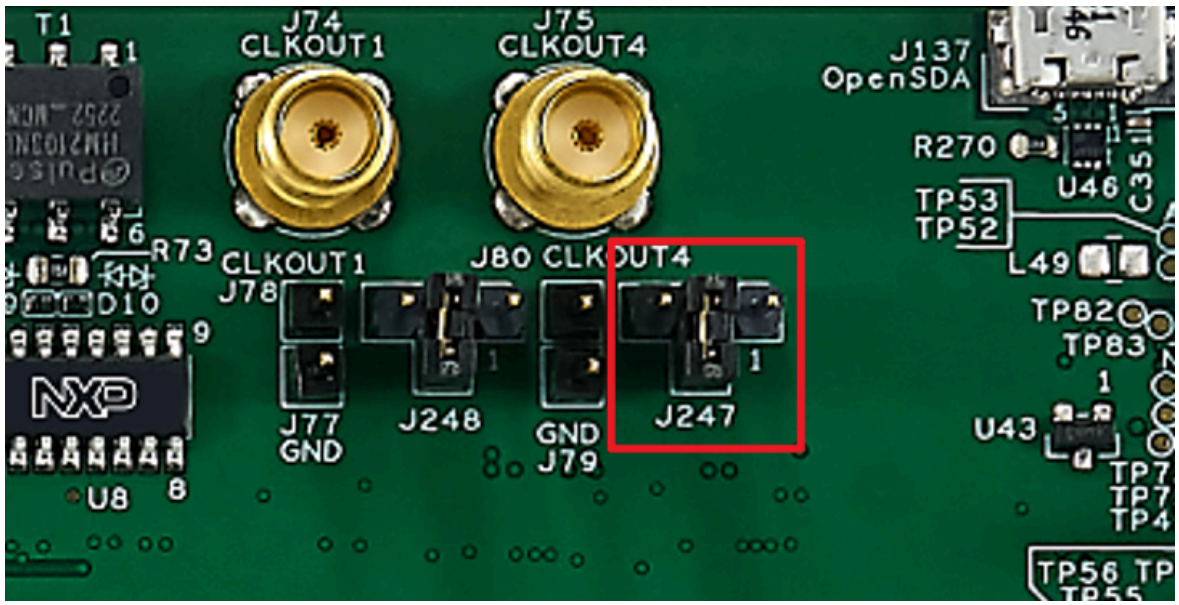


Figure 6. Jumper J247

Note: *If doing parallel RCON boot, set the jumper to 2-3 position. By default, the jumper is placed at the 2-4 position, which the LIN_SEL is software controlled.*

2.3 Boot from external flash memory

BootROM supports boot from external flash memory devices over the following interfaces:

- QuadSPI – Hyper Flash
- SD via uSDHC interface

In order to boot from the External Flash memory devices, following selections need to be made:

1. Enable Parallel RCON Boot
2. Select the QSPI/SD Boot modes

To enable boot form Parallel RCON:

- Switch off the power supply
- Set the jumpers as shown in the above figure- Boot Mode selection Reference:

J124 : Position (1-2)

J125 : Position (2-3)

2.3.1 QSPI boot mode

To Enable QSPI boot mode:

- Switch OFF the power supply
- Enable the parallel RCON Boot
- Change the below RCON settings to select the corresponding flash memory:

QuadSPI_Mode	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]
HyperFlash	**0**	**0**	**1**
Octal Flash	**0**	**1**	**1**

There are 32 dip switches for selecting the RCON configuration shown in the figure. BOOT_CFG(0:31) Corresponds to RCON Switches 1 to 32.

1 – Switch ON

0 – Switch OFF

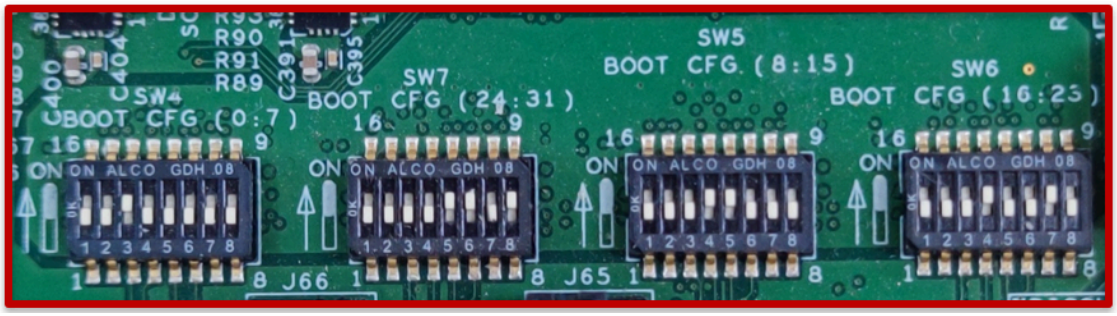


Figure 7. RCON Switches

2.3.2 SD boot via uSDHC interface

SD Boot device selection is controlled by BOOT_CFG1[7:5] as shown in the following table. To change from QSPI boot mode to SD Mode -

- Switch OFF the power supply
- Enable the parallel RCON Boot.
- Change the below RCON settings to select the corresponding SD/MMC boot:

Table 1. SD boot via uSDHC interface

Boot Options	BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]
SD Boot	**0**	**1**	**0**
Reserved	**1**	**1**	**1**

2.3.3 Additional RCON settings for clock/speed/phase for different boot configurations

For detailed RCON settings, see S32Z2_Fuse_map in the reference manual.

The following RCON settings summarize the switch configuration.

Table 2. RCON settings for switch configuration

BOOT_ CFG[14]	BOOT_ CFG[13]	BOOT_ CFG[12]	BOOT_ CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_ CFG[8]
QuadSPI CAS (only valid for HyperFlash Mode) 0000-1111:Quad SPI_SFACR[CAS] Value				CK2 0 : CK2 Clock not required 1: CK2 Clock required	Reserved	Serial RCON Detection 1 : I2C connected as Serial RCON 0: Parallel RCON

Table 2. RCON settings for switch configuration...*continued*

BOOT_CFG[20]	BOOT_CFG[19]		BOOT_CFG[18]	BOOT_CFG[17]	BOOT_CFG[16]	BOOT_CFG[15]
LPDDR4_FLASH_BNKAV_CFG 0 : No BNKAV config will be done 1: BNKAV config will be done	CKN 0 : Differential Clock not required 1: Differential Clock required	SD Speed 0 Default Speed 1 - High Speed	QuadSPI POR Delay 000: 300usec 001: 600usec 010: 1000usec 011: 2000usec 100: 5000usec 101: 50000usec 110: 100000usec 111: 300000usec	Wait Period 000: No Wait 74 Clock Cycles 001: 5ms 010:10ms 011:20ms 100:35ms 101:Reserved 101: Reserved 111:50ms (max) (only for SD/MMC/e MMC Configuration)		XOSC BYPASS MODE SEL ECTION : Selects XOSC Mode if XOSC Configuration Fuse is not blown. 0 : Reserved 1 : Crystal Mode

MMC Boot Modes	BOOT_CFG[19]	BOOT_CFG[20]	BOOT_CFG[21]	BOOT_CFG[22]
	MMC Boot Modes 0000- 1-bit Normal Speed 0001 - 4-bit Normal Speed 0010 - 8-bit Normal Speed 0011- 1-bit HIGH Speed 0100 - 4-bit HIGH Speed 0101 - 8-bit HIGH Speed 0110 - 4-bit DDR HIGH Speed 0111 - 8-bit DDR HIGH Speed			

BOOT_CFG[23]	BOOT_CFG[22]	BOOT_CFG[21]
TDH : Time Hold Delay 00: Data aligned at PosEdge of Internal reference clock 01: Data aligned with 2X serial flash		Reserved

BOOT_CFG[30]	BOOT_CFG[29]	BOOT_CFG[28]	BOOT_CFG[27]	BOOT_CFG[26]	BOOT_CFG[25]	BOOT_CFG[24]
DQS_SEL : 00: Reserved 01: Pad loopback 10: Reserved 11: External DQS		DLLFSMPF : Selects the Nth tap provided by slave delay-chain. N can vary from 0 to 7. See SMPR[DLLFSMPF] in QuadSPI chapter.			FSDLY: Full Speed Delay selection. See SMPR[FSDLY] in QuadSPI chapter.	FSPHS: Full Speed Phase selection. See SMPR[FSPHS] in QuadSPI chapter.

3 Daughtercard

The daughtercard (DC) is fully capable of operating stand-alone (that is, completely disconnected from the motherboard) by means of on-board power management ICs and included 12V AC adapter, or by using external bench power supplies.

3.1 Default Jumper Settings (DC)

Figure 8 shows the default placement of jumpers across the entire board, with each red box highlighting the key jumpers for power supply selection and Boot mode selection. This is how the S32Z280-400EVB board should look when initially removed from packaging.

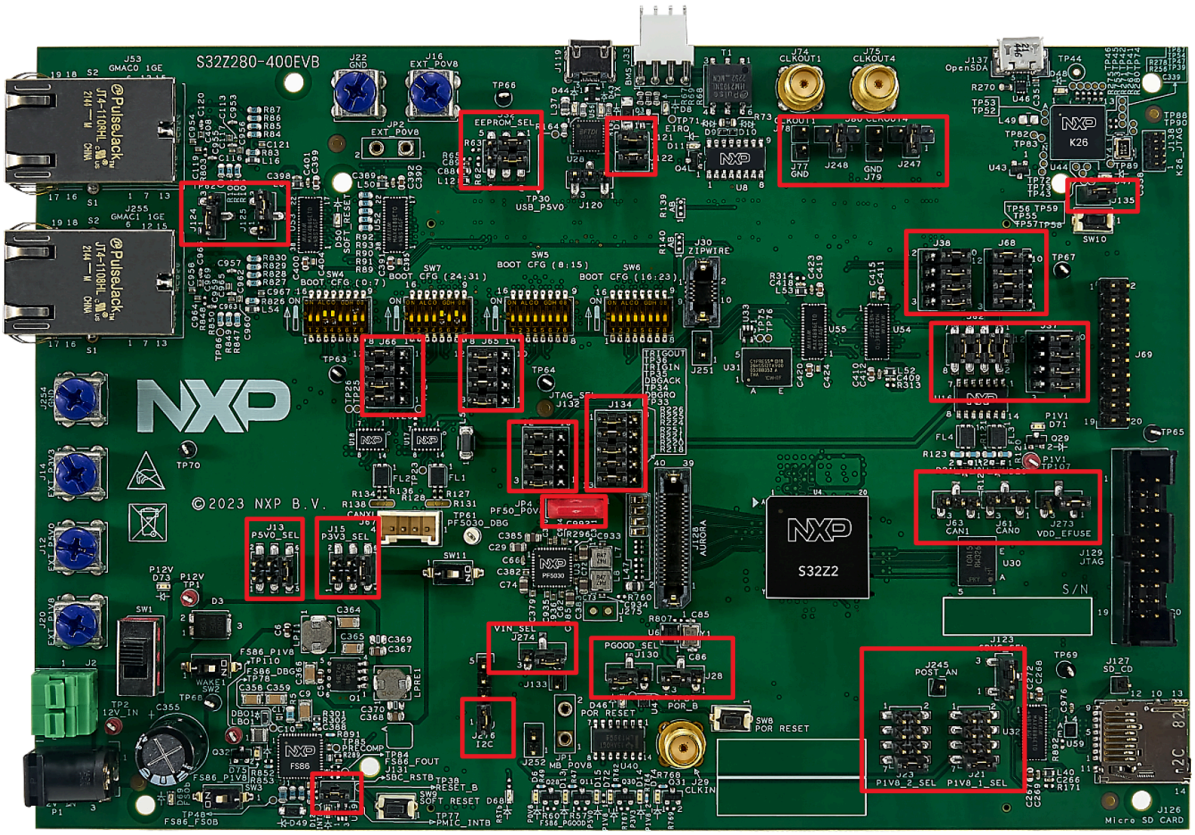


Figure 8. Highlighted default jumper settings

The following table provides an overview of all the jumpers available including their default position as well as the functionality of each jumper position.

Table 3. List of jumpers

Label from Schematic	Overall Function	Default Configuration	Pins	Pin description	Link to extended description
P1	12 Volt Power Connector	-	-	-	3.2.3
J2	12 Volt Terminal Block	-	-	-	3.2.3
JPx	0.8V power supply jumper	Dependent on System Basis Chip on board	JP1	MB Supply	3.2
			JP2	External Supply	
			JP4	PF5030 Supply	
J12	External 5.0V power plug	-	-	-	3.2.2

Table 3. List of jumpers*...continued*

Label from Schematic	Overall Function	Default Configuration	Pins	Pin description	Link to extended description
J13	5.0V power supply jumper	Pins 5-6	1-2	MB Supply	3.2
			3-4	External Supply	
			5-6	SBC Supply	
J14	External 3.3V power plug	-	-	-	3.2.2
J15	3.3V power supply jumper	Pins 5-6	1-2	MB Supply	3.2
			3-4	External Supply	
			5-6	SBC Supply	
J16	External 0.8V power plug	-	-	-	3.2.2
J20	External 1.8V power plug	-	-	-	3.2.2
J21	1.8V power supply jumper	Pins 7-8	1-2	MB Supply	3.2
			3-4	External Supply	
			5-6	N/A	
			7-8	PF5030	
J22	External GND	-	-	-	3.2.2
J23	1.8V power supply jumper	Pins 7-8	1-2	MB Supply	3.2
			3-4	External Supply	
			5-6	N/A	
			7-8	PF5030	
J28	Clock In	Pins 2-3	1-2	Enabled	3.3
			2-3	Disabled	
J29	CLOCKIN SMA	-	-	-	3.3
J32	EEPROM Select	1-2	1-2	To MB	3.9
		3-4	3-4	To MB	
			5-6	EEPROM_SCL EEPROM_SDA	
J33	Battery Management System Interface	-	-	-	-
J53	GMAC0 1GE	-	-	-	3.10
J61	CAN0	Open	1	CAN0_P	3.6
			2	-	
			3	CAN0_N	
J63	CAN1	Open	1	CAN1_P	3.6
			2	-	
			3	CAN1_N	

Table 3. List of jumpers*...continued*

Label from Schematic	Overall Function	Default Configuration	Pins		Pin description		Link to extended description
J67	CANXL	Open	1		CAN0XL_P		3.7
			2		CAN0XL_N		
			3		CAN1XL_P		
			4		CAN1XL_N		
J74	CLKOUT1 SMA	-	-		-		3.3
J75	CLKOUT4 SMA	-	-		-		3.3
J77	GND	-	-		-		-
J78	CLKOUT1 header	Open	1		CLKOUT0		3.3
J79	GND	-	-		-		-
J80	CLKOUT4 header	Open	1		CLKOUT1		3.3
J119	USB Micro B	-	-		-		3.5
J121	Enable TX LED	Pins 1-2 (On)	1		USB_TXLED		3.5
			2		CBUS0		
J122	Enable RX LED	Pins 1-2 (On)	1		USB_RXLED		3.5
			2		CBUS1		
J123	SDHC Select	Pins 2-3	1-2		SDHC to MB		3.8
			2-3		SDHC to SD Socket		
J124	BOOT_MODE0	Pins 1-2	1-2		High		3.4
			2-3		Low		
J125	BOOT_MODE1	Pins 2-3	1-2		High		3.4
			2-3		Low		
J127	SD_CD_B	Open	1		SD_DC		3.8
J130	MB PGOOD_SEL	Pins 1-2	1-2		MB Power Good		3.1
			2-3		SBC Power Good		
			Open		External Power		
J131	SBC_RSTB	Pins 1-2	1		RESET_B		3.3.3
			2		SBC_RSTB		
J132	JTAG_SEL	Pins 2-3	1	2-3	To MB	J_TDI	3.11.2
		Pins 5-6	4	5-6	To MB	J_TDO	
		Pins 8-9	7	8-9	To MB	J_TCK	
		Pins 11-12	10	11-12	To MB	J_TMS	
J134	JTAG or OpenSDA	Pins 1-2	3	1-2	To OpenSDA *OpenSDA is for Future Use	To 20-pin JTAG	3.11
		Pins 4-5	6	4-5			
		Pins 7-8	9	7-8			
		Pins 10-11	12	10-11			

Table 3. List of jumpers...*continued*

Label from Schematic	Overall Function	Default Configuration	Pins	Pin description	Link to extended description
		Pins 13-14	15 13-14		
J247	LIN Select	Pins 2-4	1-2	LIN6-9	3.5
			2-3	RCON4, PSI5	
			2-4	SOFT_RESET	
J248	RCON Select	Pins 2-4	1-2	MISC	3.4
			2-3	RCON4, OpenSDA	
			2-4	SOFT_RESET	
J252	PF Power On	Open	1-2	-	-
J254	External GND	-	-	-	3.2.2
J255	GMAC1 1GE	-	-	-	3.10

3.2 Power supply

The EVB has five distinct power rails. They are: 5V, 3.3V, 1.8V(1), 1.8V(2), and 0.8V. The purpose of each rail is shown by their connections in the diagram below . Each rail has an associated LED to signal when the power rails are working as intended, these will illuminate when power is successfully applied regardless of option used.

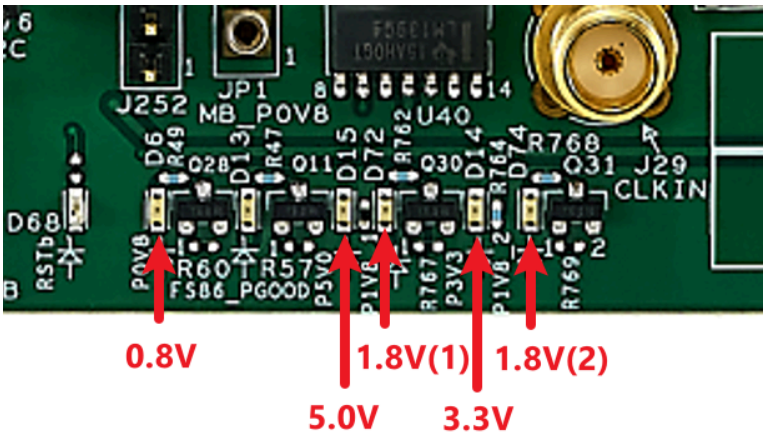


Figure 9. LED power indicators

By default, the S32Z280-400EVB is powered by the on-board power management ICs.

The S32Z280-400EVB features one System Basis Chip, the NXP FS86 series SBC, and the NXP PF5030 PMIC. The following figure shows the power-tree connections.

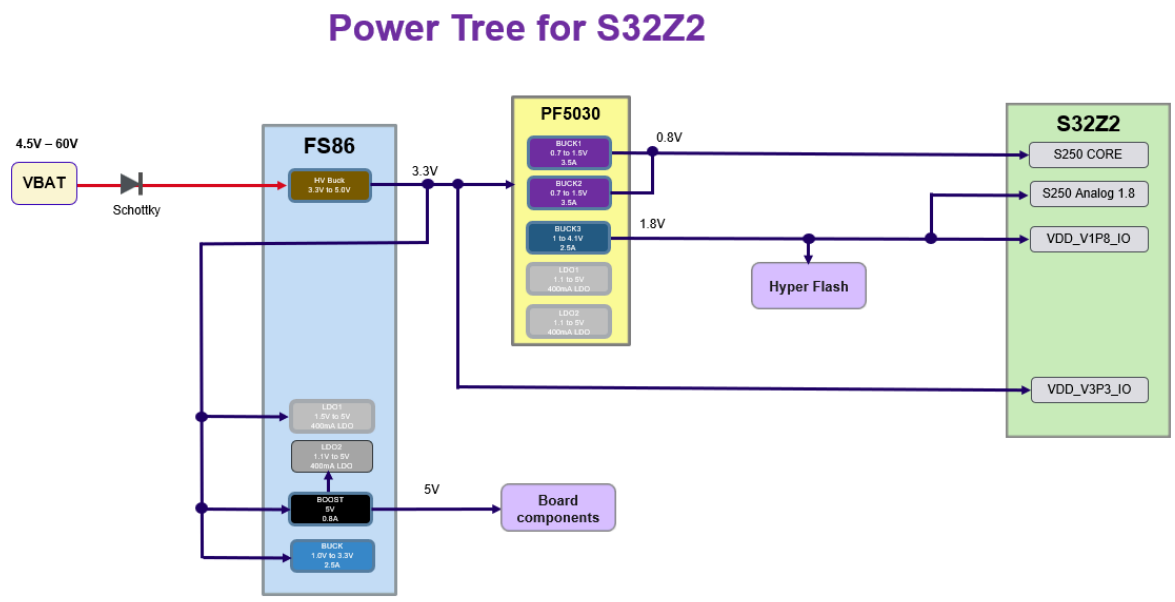


Figure 10. Daughtercard power trees for PF5030 PMICs

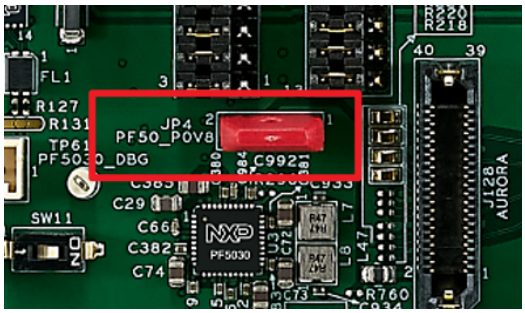


Figure 11. JPx jumper

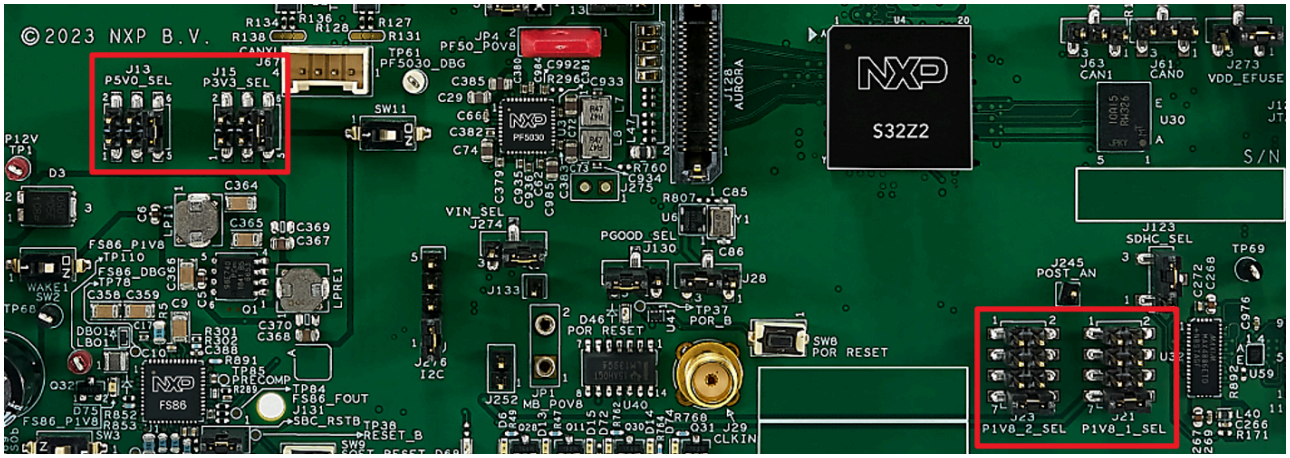


Figure 12. Physical power supply selection jumpers

Figure 12 shows possible supply options for each power rai. For the 0.8V power rail, the big red jumper (Figure 11) can be moved to switch between the motherboard, external supply, or PF5030.

Table 4. 0.8V Power supply options

Jumper Placement	Voltage Supply Source
JP1	Motherboard
JP2	External Supply
JP4	PF5030

Next, J13 corresponds to the supply options for 5.0V. The table below demonstrates the possible placement of the jumper in order to receive the desired supply of 5.0V.

Table 5. 5.0V Power supply options

Jumper Placement (J13)	Voltage Supply Source
Pins 1-2	Motherboard
Pins 3-4	External Supply
Pins 5-6	System Basis Chip

Additionally, J15 corresponds to the supply options for 3.3V. The table below demonstrates the possible placement of the jumper in order to receive the desired supply of 3.3V.

Table 6. 3.3V Power supply options

Jumper Placement (J15)	Voltage Supply Source
Pins 1-2	Motherboard
Pins 3-4	External Supply
Pins 5-6	System Basis Chip

J21 and J23 correspond to the supply option for 1.8V. Two separate jumpers are needed in order to deliver the proper 1.8V power supply. It is important to note that pins 5-6 and pins 7-8 correspond the two different options of possible PMICs on the S32Z280-400EVB daughtercard. The board will only have one PMIC, so place the jumper on the pins that correspond to the PMIC on the daughtercard if supplying from the PMIC is desired. The tables below demonstrate the possible placement of the jumpers in order to receive the desired supply of 1.8V.

Table 7. 1.8V Power supply options

Jumper Placement(J21)	Voltage Supply Source
Pins 1-2	Motherboard
Pins 3-4	External Supply
Pins 5-6	N/A
Pins 7-8	PF5030

Table 8. 1.8V Power supply options

Jumper Placement(J23)	Voltage Supply Source
Pins 1-2	Motherboard
Pins 3-4	External Supply
Pins 5-6	N/A
Pins 7-8	PF5030

The green highlight in Figure 13 represents the default configuration of the board.

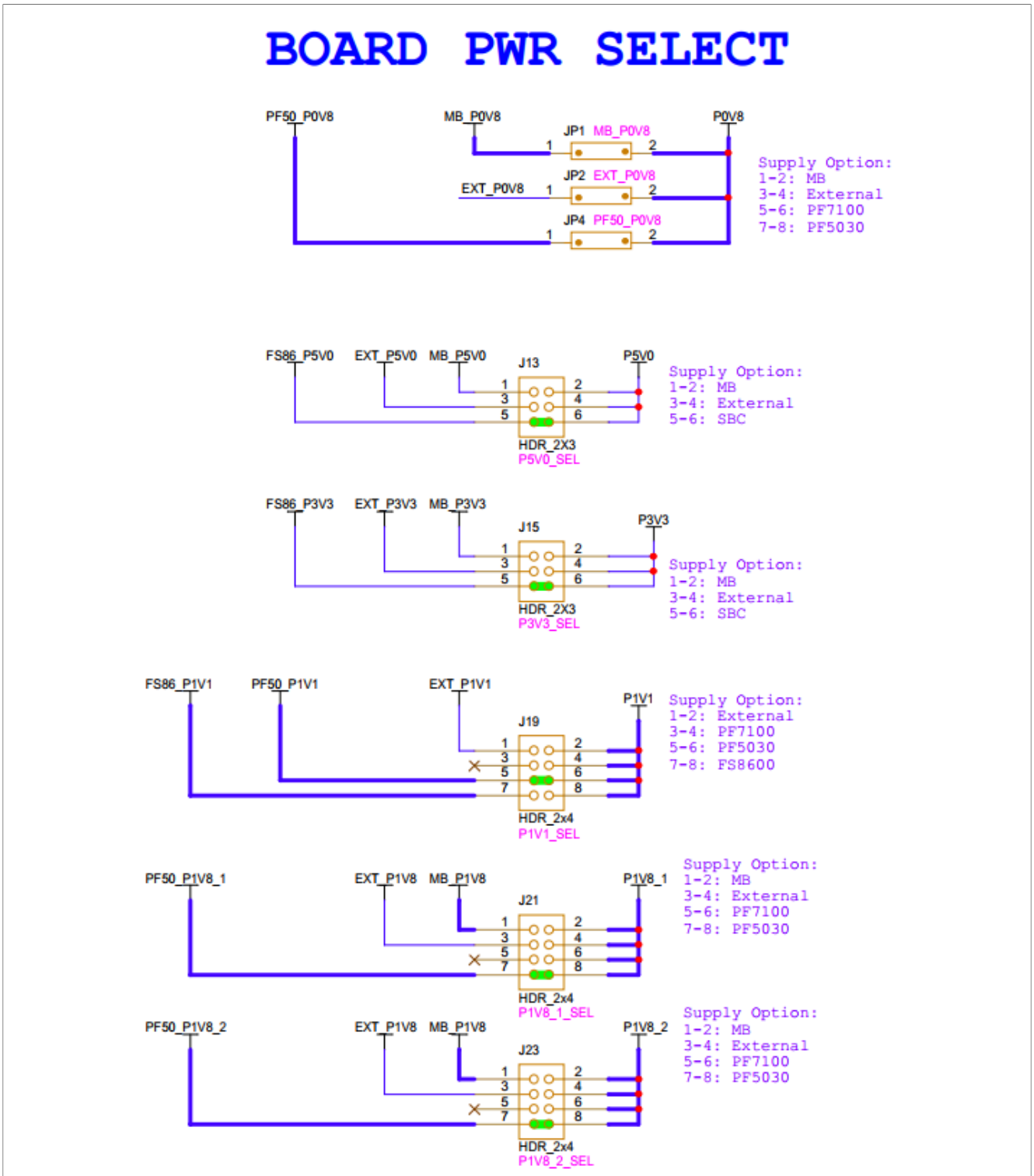


Figure 13. Example of daughtercard supply selection jumper

3.2.1 Power from motherboard

The primary purpose of the motherboard when used with the daughtercard is to provide additional IO pin-out and communication transceivers, however, it is also capable of supplying 5V, 3.3V, 1.8V, and 0.8V from its own regulators.

For best use of the S32Z280-400EVB daughtercard, it is recommended to use the daughtercard power supplies since the daughtercard can ensure all proper power segments. However, as shown in the tables above, it is possible to select power supplies from the motherboard or externally.

3.2.2 Power from multiple external supplies

To power the daughtercard from individual external supplies, e.g., a bench supply unit, each rail must be plugged into its corresponding screw terminal. Use the schematic in Figure 13 or table 2-6 to use the proper pins for each power selection jumpers in order to configure the board for external power supply.

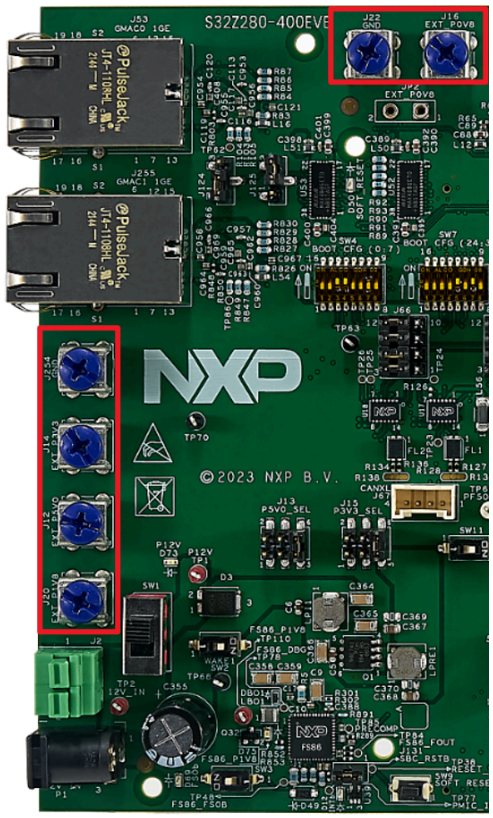


Figure 14. DC banana sockets for individual external supplies

3.2.3 Power from SBC/PMIC

On the EVB the NXP FS86 is used in conjunction with the PF5030 PMIC.

To receive all power rails from a single external supply, a 12V source must be plugged into the daughtercard via barrel jack P1 or terminal block J2. The 12V supply is used to power the SBC which, together with the PMIC, generates all the required voltages.

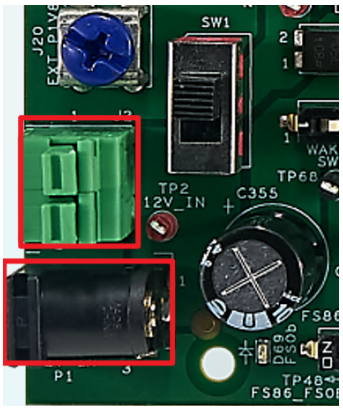


Figure 15. 12V Connections into FS86 SBC

The SBC and PMIC are pre-programmed via fuses to provide the required voltages and correct power sequence.

3.2.4 SBC/PMIC debug mode

The SBC/PMIC solution includes hardware watchdogs that can reset the board and MCU if not serviced by application software. Normally, during development, it is desirable to disable this feature to allow application debug without interference from the watchdogs. This is accomplished by setting SW3 and SW11 to the “ON” position.

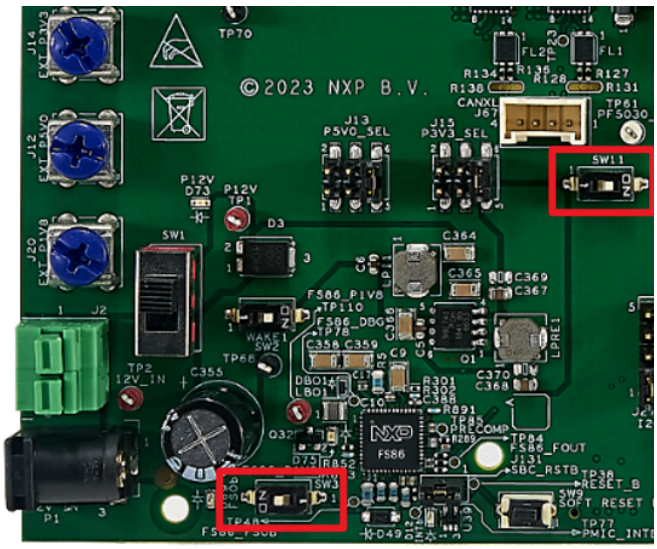


Figure 16. SBC and PMIC debug jumpers

3.3 Clock and reset

3.3.1 Clocking

There are three clocking options on the daughtercard, configured by R59 and R807. R59 has two configurable positions, connect 1-2 or connect 3-2, or can be left unpopulated (this is the default configuration). R807 is initially installed but can be removed to use external clock options.

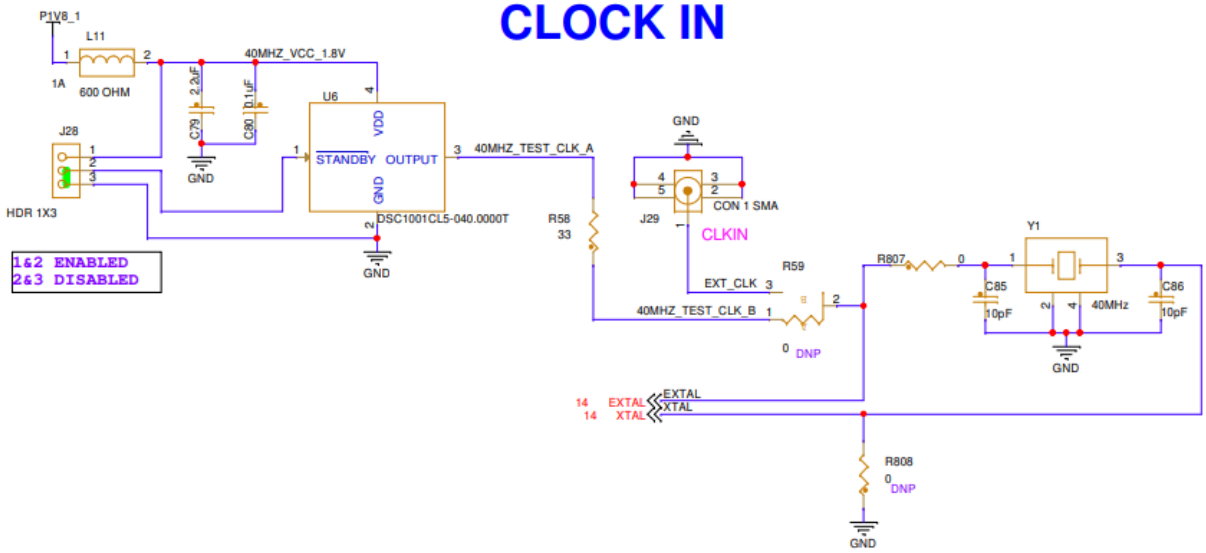


Figure 17. DC clocking configuration schematic

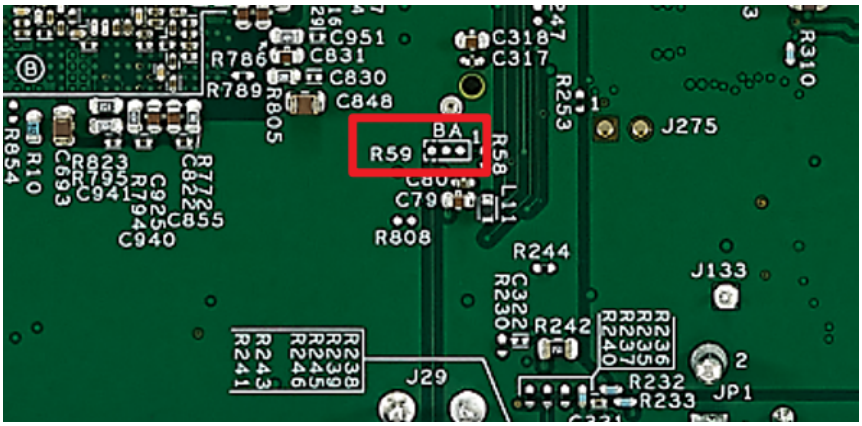


Figure 18. Clocking option

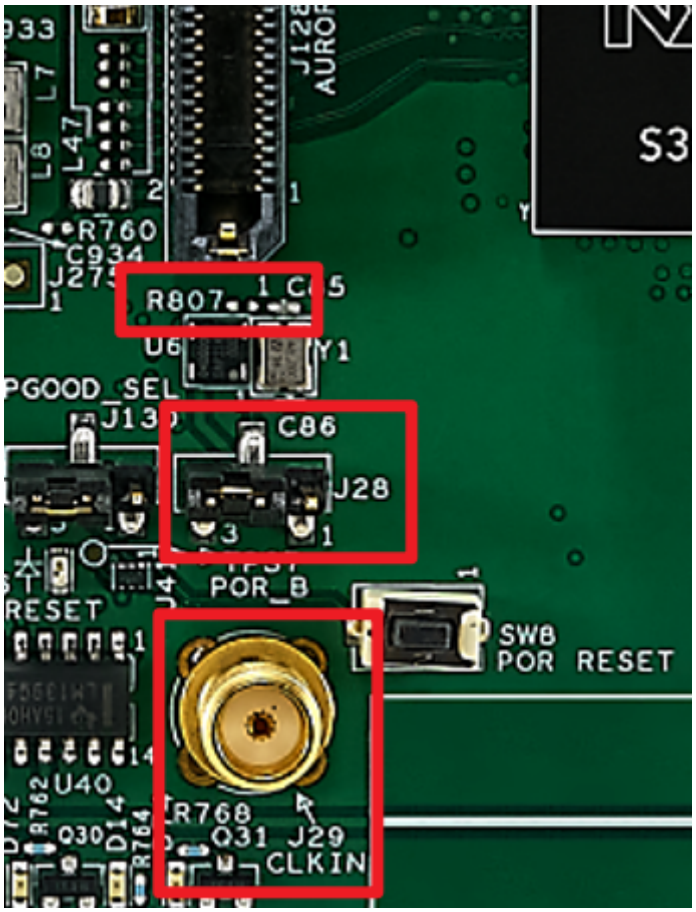


Figure 19. Physical DC clocking configuration

The clocking options on the EVB are as follows:

3.3.1.1 40MHz crystal

To use the 40MHz clock from the crystal, R59 must be left unpopulated, and R807 must be installed. This is the default configuration.

3.3.1.2 40MHz OSC

To use the 40MHz clock from the oscillator chip, R59 must be configured in position 1-2, and R807 must be removed. Header J28 can then be used to enable the chip, by connecting pins 1&2.

3.3.1.3 External SMA

To use an external clock with a custom frequency, R59 must be configured in position 3-2, and R807 must be removed. The external clock is connected to the SMA connector J29.

Table 9. Summary of resistor positions for different clocks

Clock Source	R59	R807
40MHz Crystal	Removed	Installed
40MHz OSC	1-2	Removed

Table 9. Summary of resistor positions for different clocks*...continued*

Clock Source	R59	R807
External SMA	3-2	Removed

3.3.2 Reset

The daughtercard contains two reset switches: POR RESET and SOFT RESET.

3.3.2.1 POR RESET

The open-drain POR_B pin on the S32Z280-400EVB daughtercard is a device reset source which can be externally triggered using the POR RESET switch on the daughtercard (Figure 19), or driven low by the SBC if it is determined that the device requires a reset, due to a low-voltage condition for example.

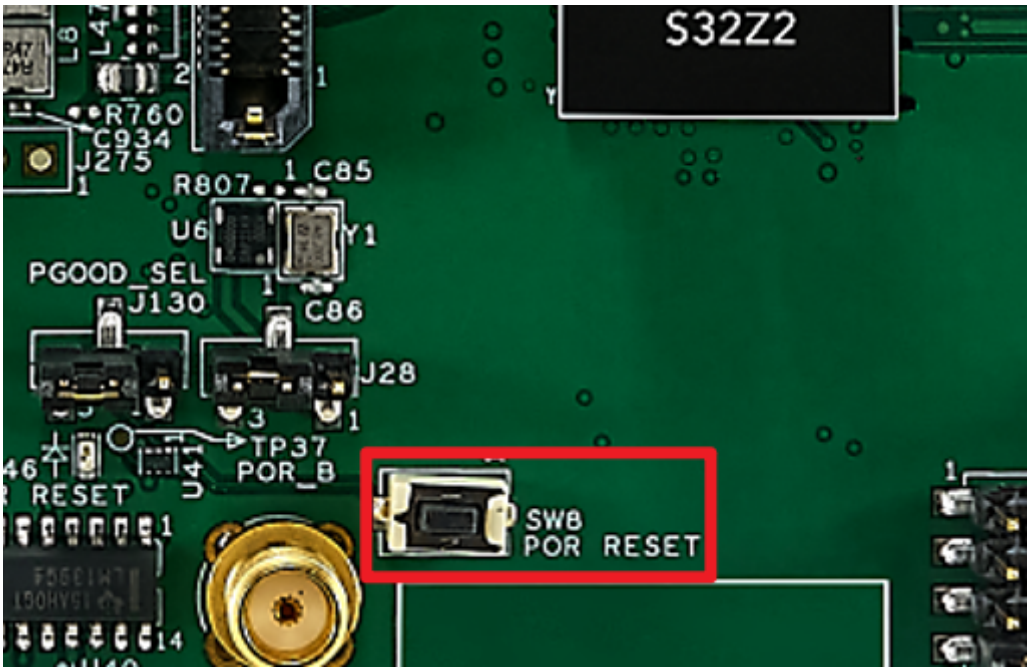


Figure 20. POR RESET switch on DC

When operating from an external power supply, header J130 must be opened for correct operation of the POR RESET switch.

3.3.2.2 Functional reset

To trigger a functional reset, the SOFT_RESET switch on the daughtercard is used. This triggers a signal to SOFT_RESET and RESET_B. When operating from an external power supply, header J131 must be opened for correct operation of the SOFT_RESET switch.

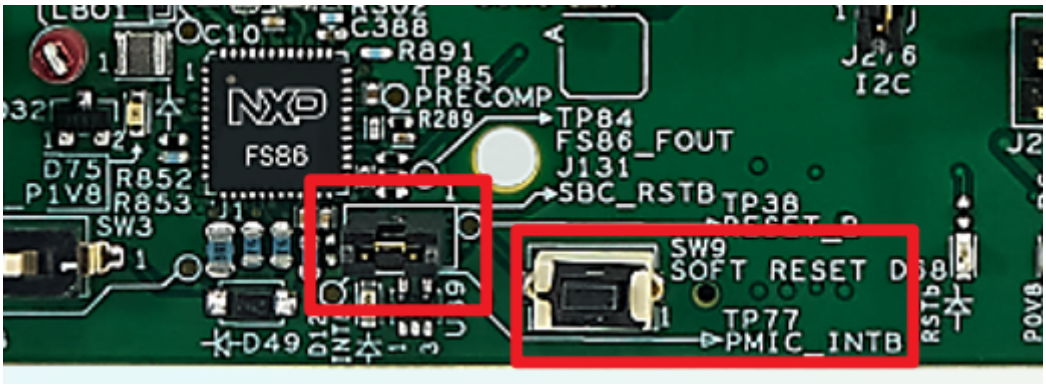


Figure 21. Functional reset switch and J131 on S32Z280-400EVB daughtercard

3.4 RCON switches

There are four banks of dip switches on the S32Z280-400EVB daughtercard, each with eight switches, giving a total of 32 switches. These switches are used for configuring the boot options of the S32Z2 device. To boot from Flash and allow for debug connection the switches should be placed in the correct positions as described in the boot modes section:

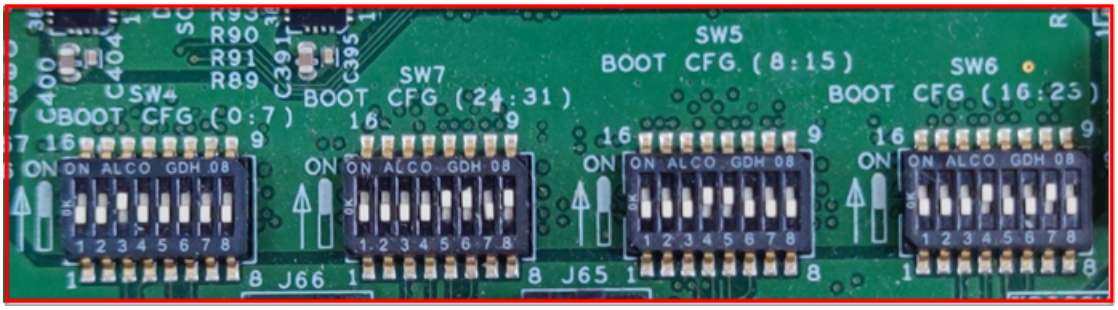


Figure 22. Default RCON switch positions for flash boot

Users should only change these default values if they are familiar with the boot processes of the device and wish to alter these booting source/conditions.

3.5 LIN

The S32Z2's LIN9 interface is dedicated to the daughtercard USB-UART. This interface may also be used as a serial boot source.

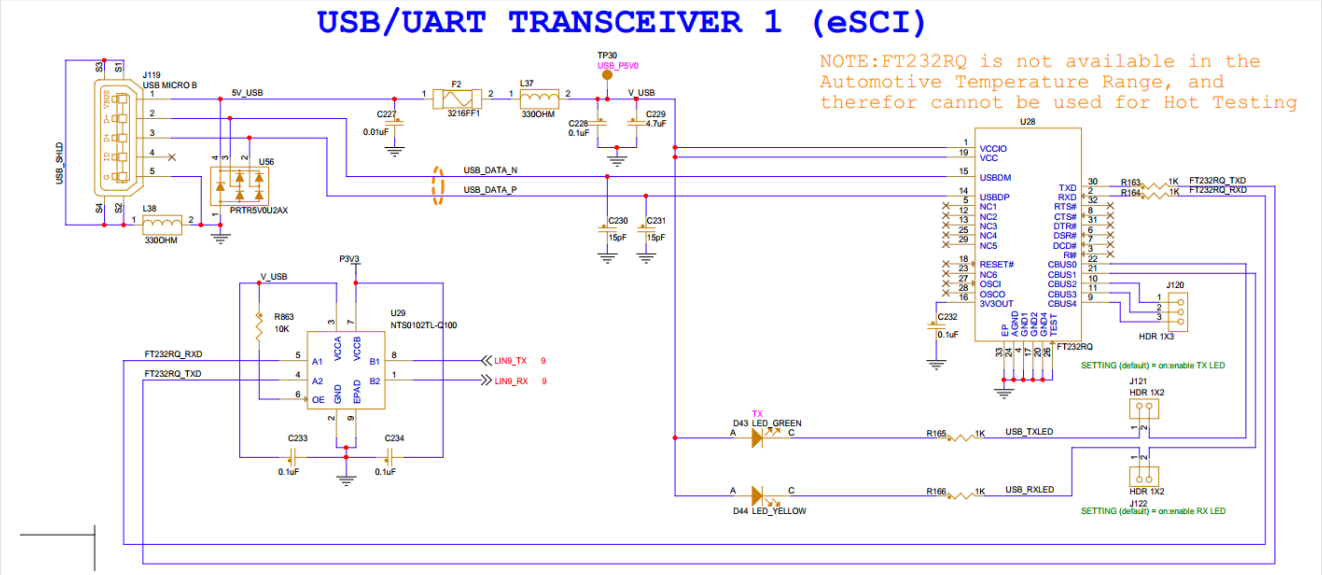


Figure 23. USB-UART LIN9

The S32Z2's remaining LIN interfaces are multiplexed with alternate functions. Routing of LIN signals is accomplished via several on-board multiplexers and jumper blocks.

Component U54 provides selecting between LIN signals and a combination of RCON and PSI-5 signals. This is controlled by jumper J247.

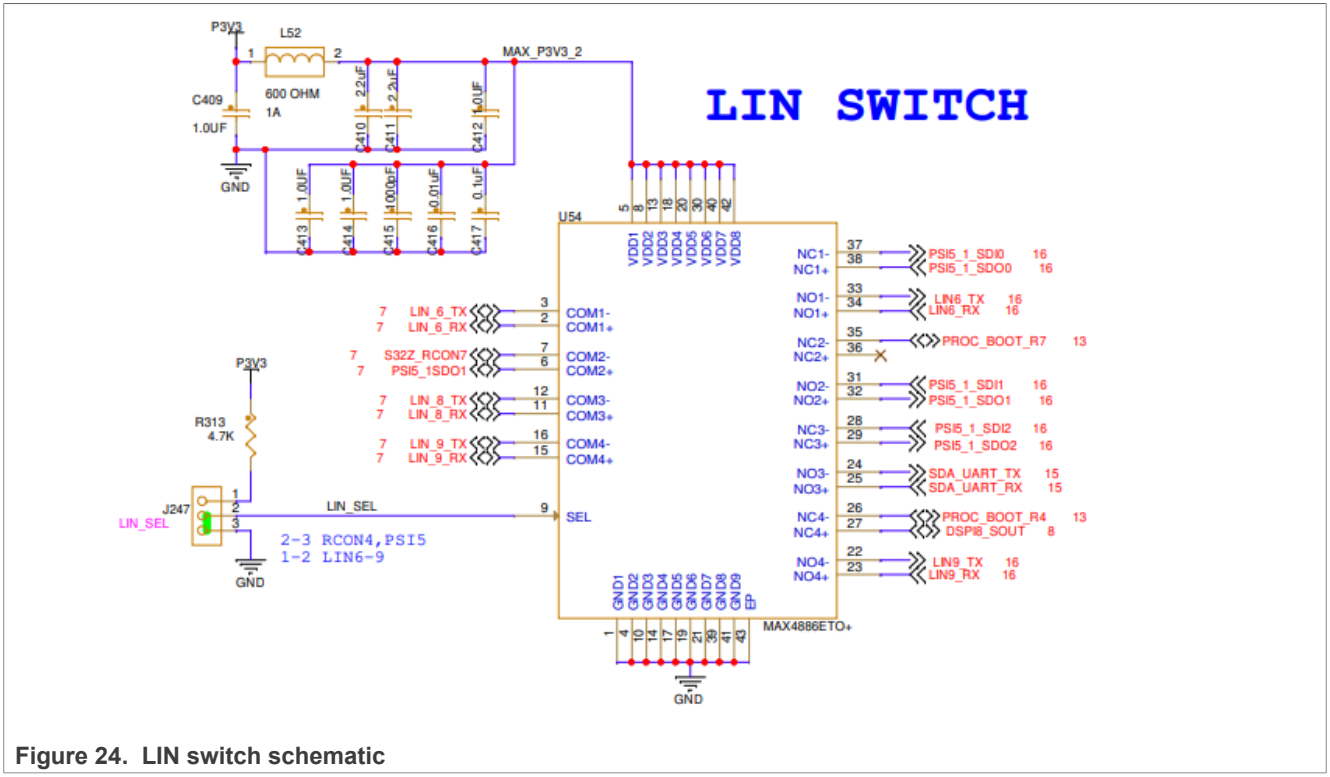


Figure 24. LIN switch schematic

Component U55 includes among several other signals, routing for LIN11.

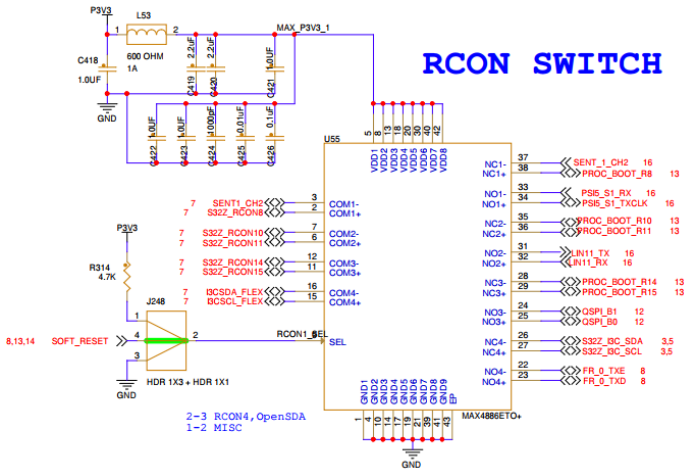


Figure 25. RCON switch schematic

3.6 CAN

Header J62 is used to connect CAN0 and CAN1 instances to CAN-FD transceivers on the daughter-card. CAN bus-level signals are then available on pin headers J61 and J63 for these two CAN instances.

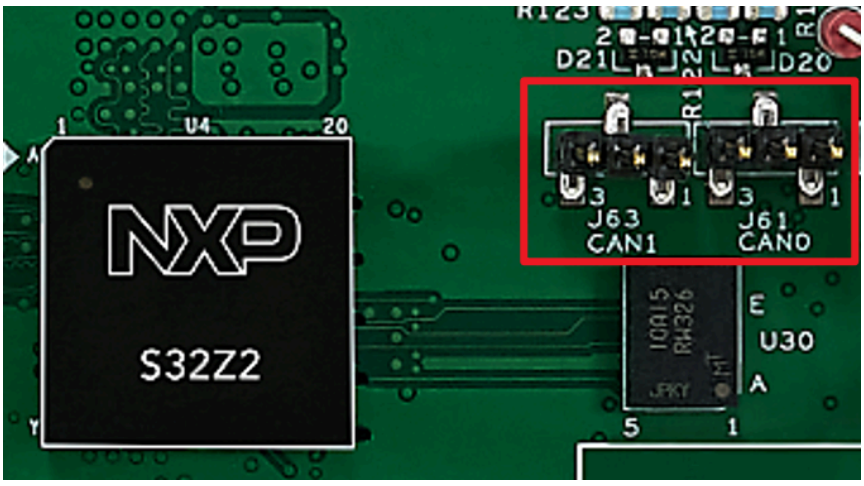


Figure 26. Daughtercard CAN0 and CAN1 connector

The CAN0 interface also allows the user to perform a serial boot even when using the daughtercard stand-alone (disconnected from the motherboard).

Remaining CAN interfaces not dedicated to other functions on the daughtercard, are routed to the motherboard connectors.

3.7 CAN-XL

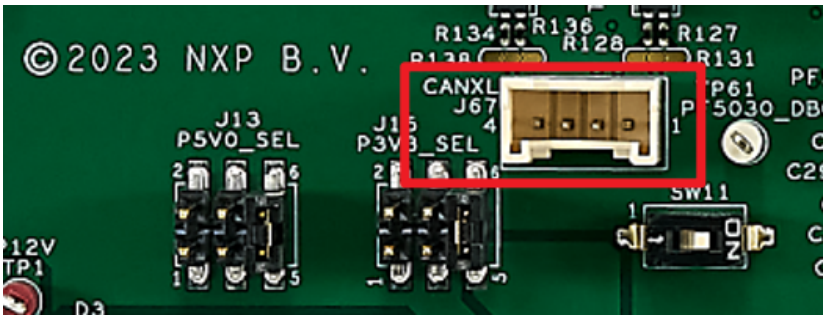


Figure 27. CANXL connector

S32Z280-400EVB includes two CAN modules supporting the upcoming CAN-XL standard. The daughtercard has reserved space for two NXP CAN-XL transceivers to be released soon. Signals CANXL_RX0/TX and CANXL_RX1/TX are routed to CANXLSIC_SO14 package footprints with CAN bus physical signals available on jumper J67.

3.8 SDHC

An alternative solution for booting is to use an SD card. For this use, the daughtercard contains a micro SD card socket. J123 is used to switch the device's SDHC connection to either this micro SD card socket (connect pins 2&3), or the GPIO headers on the motherboard (connect pins 1&2).

Table 10. MCU GPIO PIN numbers for SDHC signals

SDHC Signal	MCU GPIO Pin
SD_CLK	GPIO111
SD_CMD	GPIO106
SD_DATA0	GPIO107
SD_DATA1	GPIO108
SD_DATA2	GPIO109
SD_DATA3	GPIO110

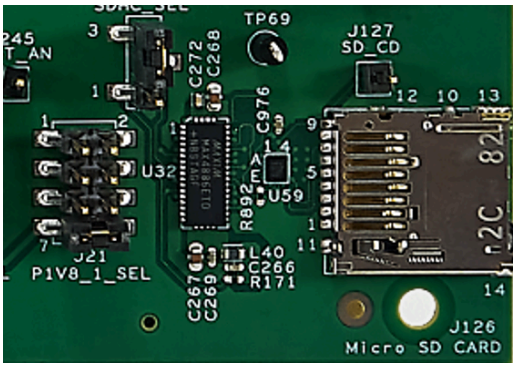


Figure 28. Micro SD socket

This is an alternate solution for booting where this interface can be used to perform a boot from the SD card.

3.9 EEPROM

Header J32 is used to connect MCU GPIO pins to either the motherboard (default configuration), or to SDA and SCL of the daughtercard's EEPROM chip, allowing I2C access to the 8192 bits of serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) located in chip U7. This provides support for Serial RCON, allowing the user to store boot configuration and load with Serial RCON via I2C, an alternative that uses fewer pins than the parallel RCON option.

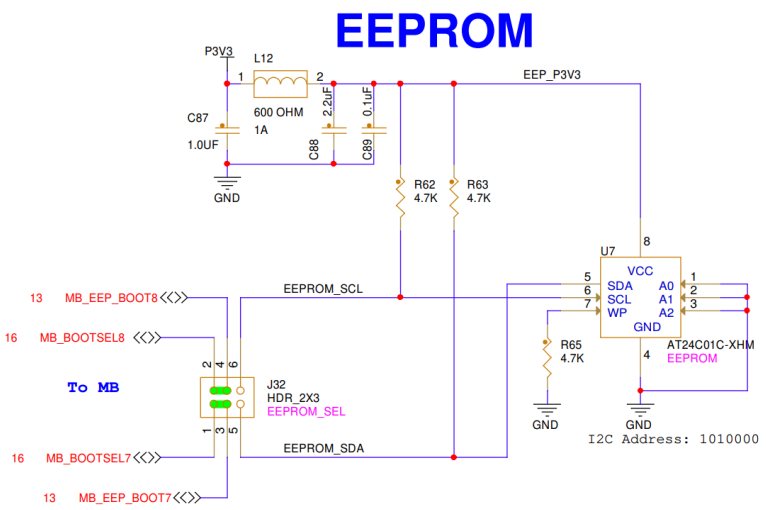


Figure 29. S32Z280-400EVB daughtercard EEPROM schematic

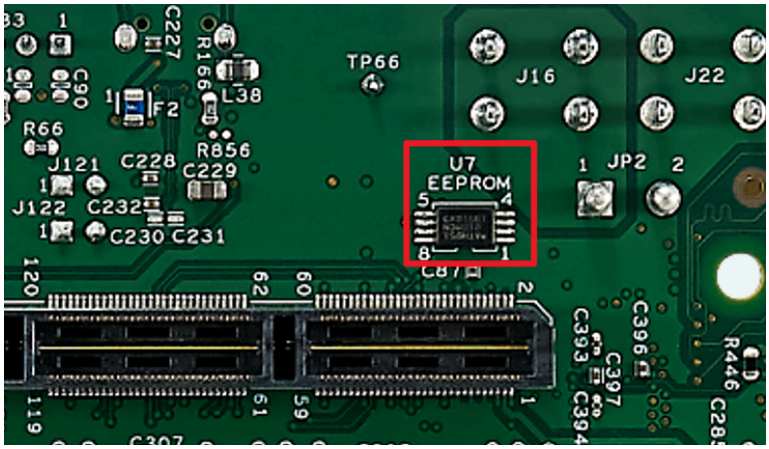


Figure 30. Physical EEPROM

3.10 Ethernet

The daughtercard includes two 1Gbps RGMII Ethernet PHY (U12 and U58) connected to ETH0 and ETH1 respectively interfaced on the MCU:

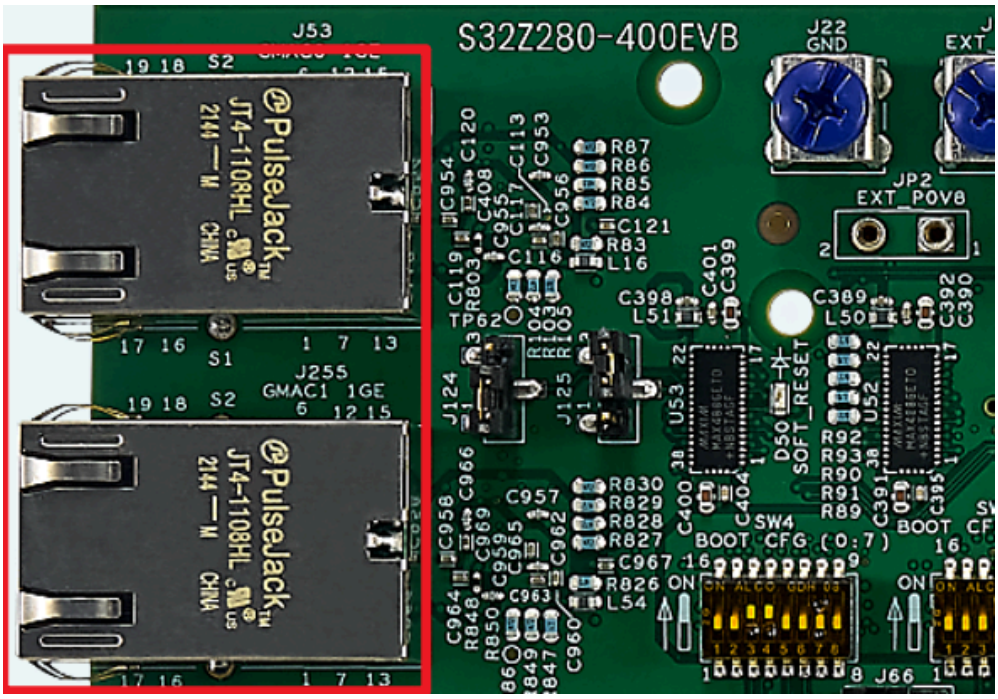


Figure 31. RGMII ethernet PHYs

3.11 Debug

3.11.1 Aurora

The daughtercard contains a connector (J128) for the Aurora Trace Port, allowing debug information to be sent over a high-speed serial link. The five differential pairs from the connector (four TX and one Clock) are connected directly to the MCU.

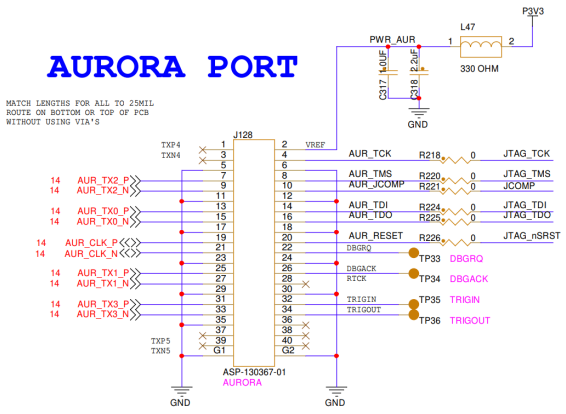
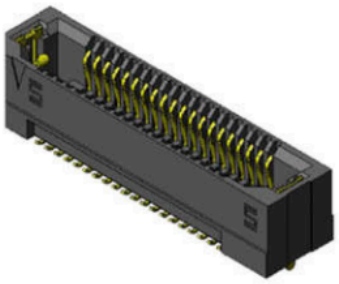


Figure 32. S32Z280-400EVB daughtercard aurora schematic

Figure 32 shows the definition of Aurora trace connections with the recommended connector currently included on the EVB.

Position	Connector Signal	Recommended Connection	Pin Number	Pin Number	Recommended Connection	Connector Signal
	GND		Latch			GND
1	(TXP[4]) (+)	N/C	1	2	VDD_IO_AUR 3.3V	VREF
2	(TXN[4]) (-)	N/C	3	4	N/C	TCK*
3	GND	GND	5	6	GND	GND
4	TXP[2] (+)	TXP[2]	7	8	N/C	TMS*
5	TXN[2] (-)	TXN[2]	9	10	N/C	TDO*
6	GND	GND	11	12	N/C	JCOMP (nTRST) *
7	TXP[0] (+)	TXP[0]	13	14	N/C	TDI*
8	TXN[0] (-)	TXN[0]	15	16	N/C	TDO*
9	GND	GND	17	18	GND	GND
10	CLKP (+)	CLKP	19	20		RESET-
11	CLKN (-)	CLKN	21	22	N/C	DBGRQ
12	GND	GND	23	24	GND	GND
13	TXP[1] (+)	TXP[1]	25	26	N/C	DBGACK
14	TXN[1] (-)	TXN[1]	27	28	N/C	RTCLK
15	GND	GND	29	30	GND	GND
16	TXP[3] (+)	TXP[3]	31	32	N/C	TRIGIN
17	TXN[3] (-)	TXN[3]	33	34	N/C	TRIGOUT
18	GND	GND	35	36	N/C	RESERVED
19	(TXP[5]) (+)	N/C	37	38	N/C	RESERVED
20	(TXN[5]) (-)	N/C	39	40	N/C	RESERVED
	GND		Latch			GND



Samtec ASP-130367-01

Figure 33. Aurora trace connector definition

3.11.2 JTAG

A JTAG debug port is included on the S32Z280-400EVB daughtercard (J129). The standard 20-pin 2.54mm (0.10”) JTAG connector is used here.

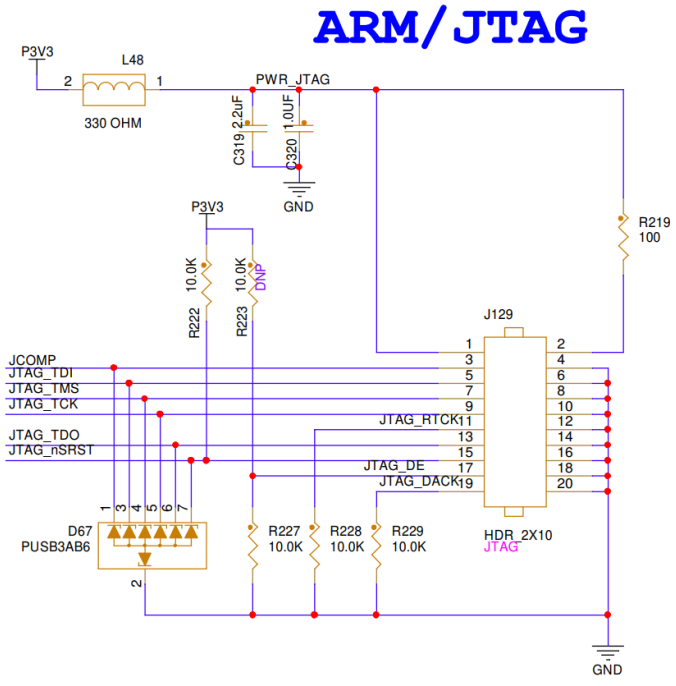


Figure 34. JTAG connector schematic

3.11.3 Lauterbach debuggers

The Lauterbach debug hardware for Aurora and JTAG setup for use with S32Z devices is as follows:

- LA-3520 + LA-3521 + LA3505 + LA3000
  1. Up to 6 lanes (LA-3522 supports 8)
  2. Up to 12.5 Gbps/lane

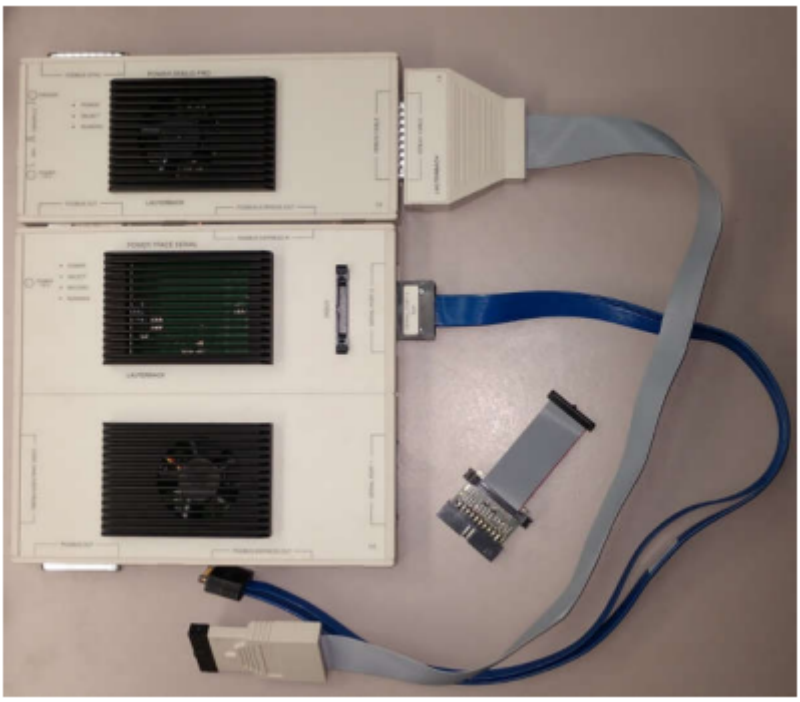


Figure 35. Lauterbach hardware setup

3.11.4 OpenSDA

There is an OpenSDA interface included on the board. NXP does not provide software support for OpenSDA interface on the EVB at the moment.

3.11.5 Other

Aurora trace tools are also available from other vendors, such as Green Hills and PLS. JTAG only tools are available from multiple vendors, including NXP and Green Hills.

3.12 SPI

DSPI10 is available on the S32Z280-400EVB daughtercard on J69. The remaining DSPI instances are routed to pins on the motherboard.

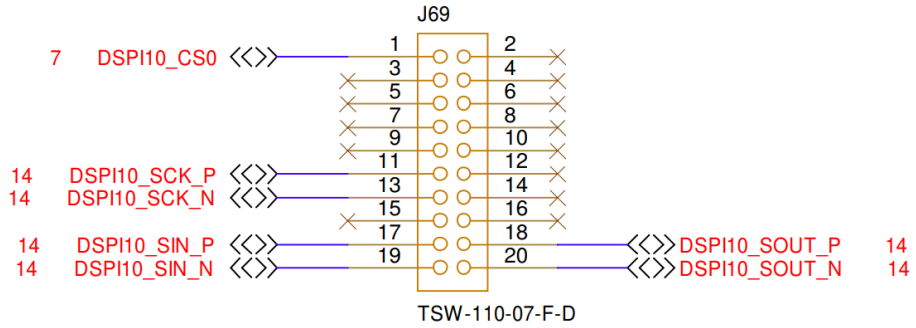


Figure 36. DSPI header schematic

3.13 Flash

The QSPI0 interface is connected to an on-board serial Flash device which may be used as a boot interface.

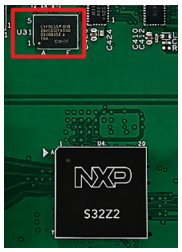


Figure 37. On-board serial flash

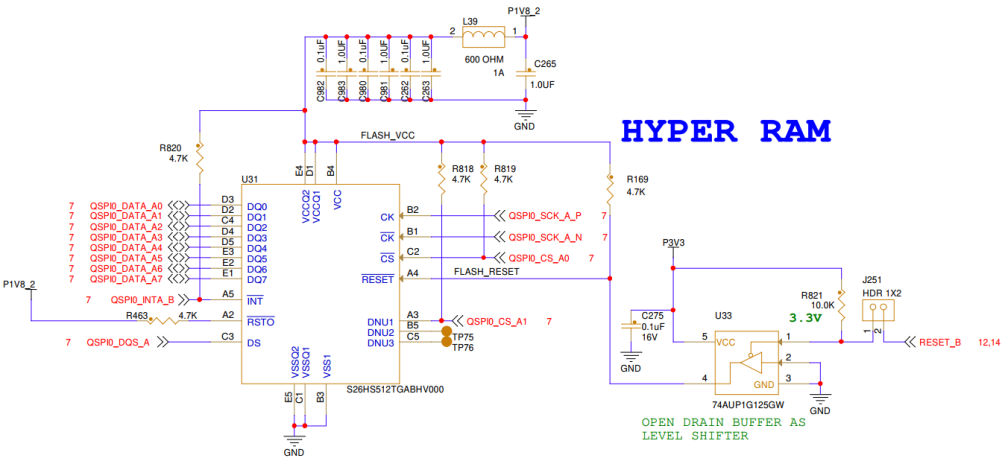


Figure 38. Serial flash schematic

Note: *The schematics incorrectly identify the part as "Hyper RAM" whereas it is a serial Hyperflash device.*

4 Motherboard

Figure 38 shows the general placement of components of the motherboard. See Appendix B at the bottom of this document for a full overview.

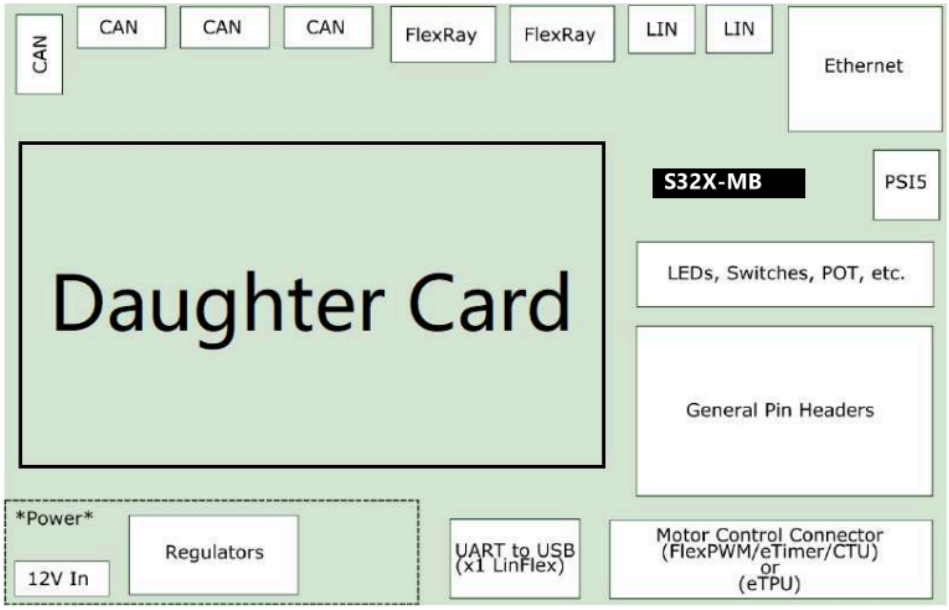


Figure 39. Overview of component placement on EVB

Default Jumper Settings (MB)

Figure 39 shows the default placement of jumpers for the entire motherboard, with each red box notating the placement of each jumper. This is how the motherboard should look once removed from the packaging. Note that there may slight differences between new boards, since some of the jumper placements are done by hand at manufacture.

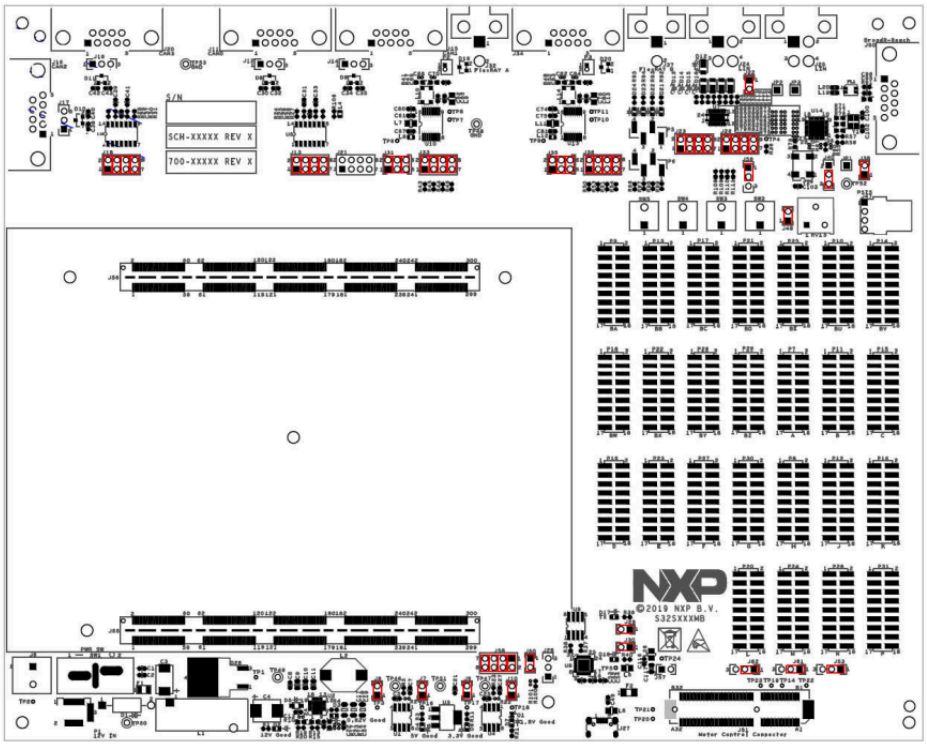


Figure 40. Default configurations of motherboard

4.1 Power supply

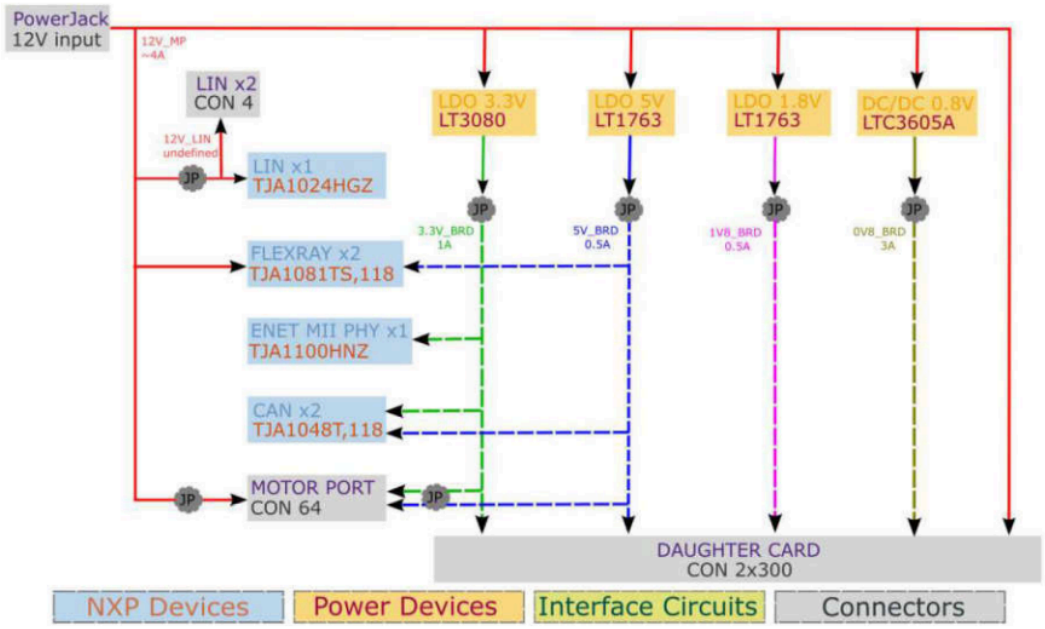


Figure 41. Motherboard power supply diagram

The motherboard is powered from a 12V supply, via either the barrel jack connector P1 or the terminal block J6). The 12V supply is used to supply regulators for power rails: 5V, 3.3V, 1.8V and 0.8V, each with a corresponding status LED to show that the rail is working properly.

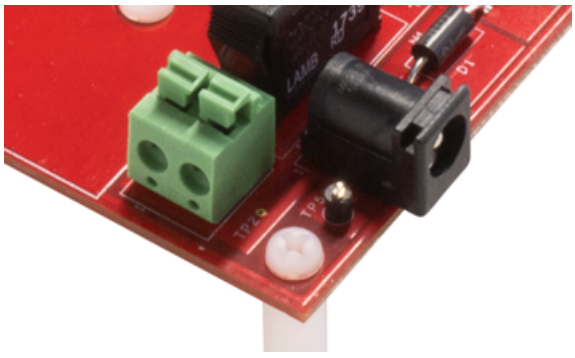


Figure 42. Physical motherboard power connectors

Headers J7-J10 are set by default to enable the distribution of power from each regulator – removing the jumper isolates the rail from the motherboard.

Table 11. Enable/disable headers for MB power rails

Power Rail	Enable/Disable Header
5V	J7
0.8V	J8
3.3V	J9
1.8V	J10

4.2 CAN

The S32Z2 device has 24 FlexCAN modules implementing the CAN 2.0B and FD CAN protocols.

4.2.1 CAN 0-3

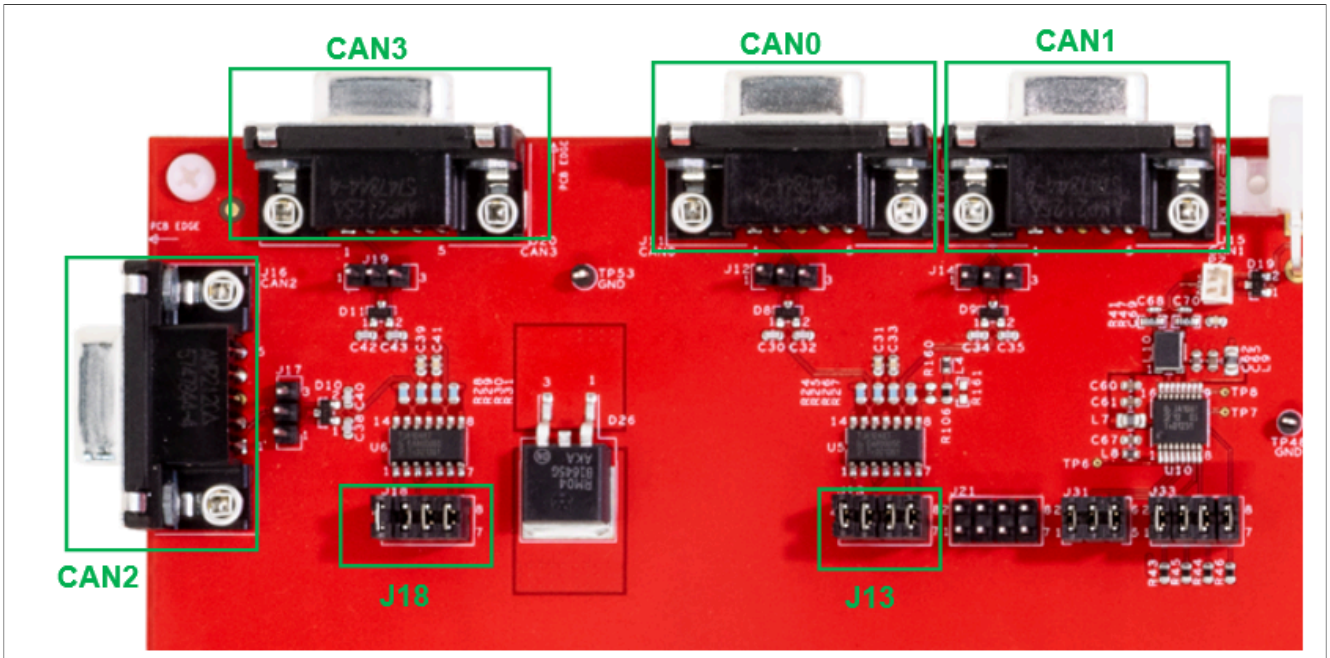


Figure 43. Physical CAN connectors (default configuration labelling)

The EVB motherboard contains four CAN connectors and two TJA1048 transceiver modules – each module providing a dual high-speed interface between the physical two-wire CAN buses and the protocol controller of the MCU. TJA1048 supports CAN FD up to 5Mbps for the data phase.

The TX/RX outputs of the TJA1048 modules are connected by default via J13 and J18 to CAN ports 2 and 6 of the MCU, also available as the following GPIO pins, both available on the general access headers on the motherboard, and connected to the daughtercard. The Motherboard schematic lists these CAN interfaces as CAN0 through CAN3, however they are connected to CAN instances 2 and 6 on the S32Z280-400EVB daughtercard. Note that CAN instances 1 and 3 are not connected to the daughtercard. The following table shows this mapping and also the MCU GPIO pin number for each signal.

Table 12. Default DC CAN mapping and MCU GPIO PIN numbers for MB CAN instances 0-3

MB CAN Signal	DC CAN Signal	MCU GPIO Pin
CAN0_TX	CAN6_TX	GPIO[138]
CAN0_RX	CAN6_RX	GPIO[139]
CAN1_TX	Not Connected	
CAN1_RX	Not Connected	
CAN2_TX	CAN2_TX	GPIO[166]
CAN2_RX	CAN2_RX	GPIO[167]
CAN3_TX	Not Connected	
CAN3_RX	Not Connected	

4.2.2 CAN 4-7

Header J21 provides direct access to CAN ports 7, 9, and 10 of the MCU, with no transceiver module. However, jumper wires can be used to connect any of these ports to the inputs/outputs of the TJA1048 modules as described in Section 5.2.1 via headers J13 and/or J18.

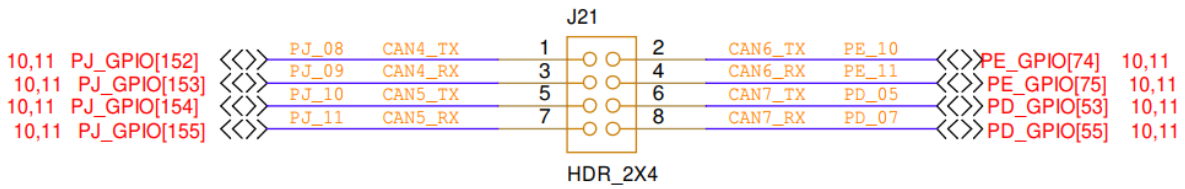


Figure 44. J21 CAN 4-7 MCU access

The motherboard schematic maps CAN 4-7 signals to the MCU GPIO pins as shown in Table 11.

Table 13. MCU CAN instance and GPIO pin numbers for MB CAN instances 4-7

CAN Signal	MCU GPIO Pin	MCU GPIO Pin
CAN4_TX	Not Connected	
CAN4_RX	Not Connected	
CAN5_TX	CAN7_TX	GPIO[118]
CAN5_RX	CAN7_RX	GPIO[119]
CAN6_TX	CAN10_TX	GPIO[146]
CAN6_RX	CAN10_RX	GPIO[147]
CAN7_TX	CAN9_TX	GPIO[159]
CAN7_RX	CAN9_RX	GPIO[160]

4.3 LIN

S32Z2 contains 13 LINFlexD modules, LIN0-11 and MSC_0_LIN. The EVB contains connections to four of these modules as well as a TJA1024 quad LIN transceiver module, interfacing between the physical LIN buses and the protocol controller of the MCU.

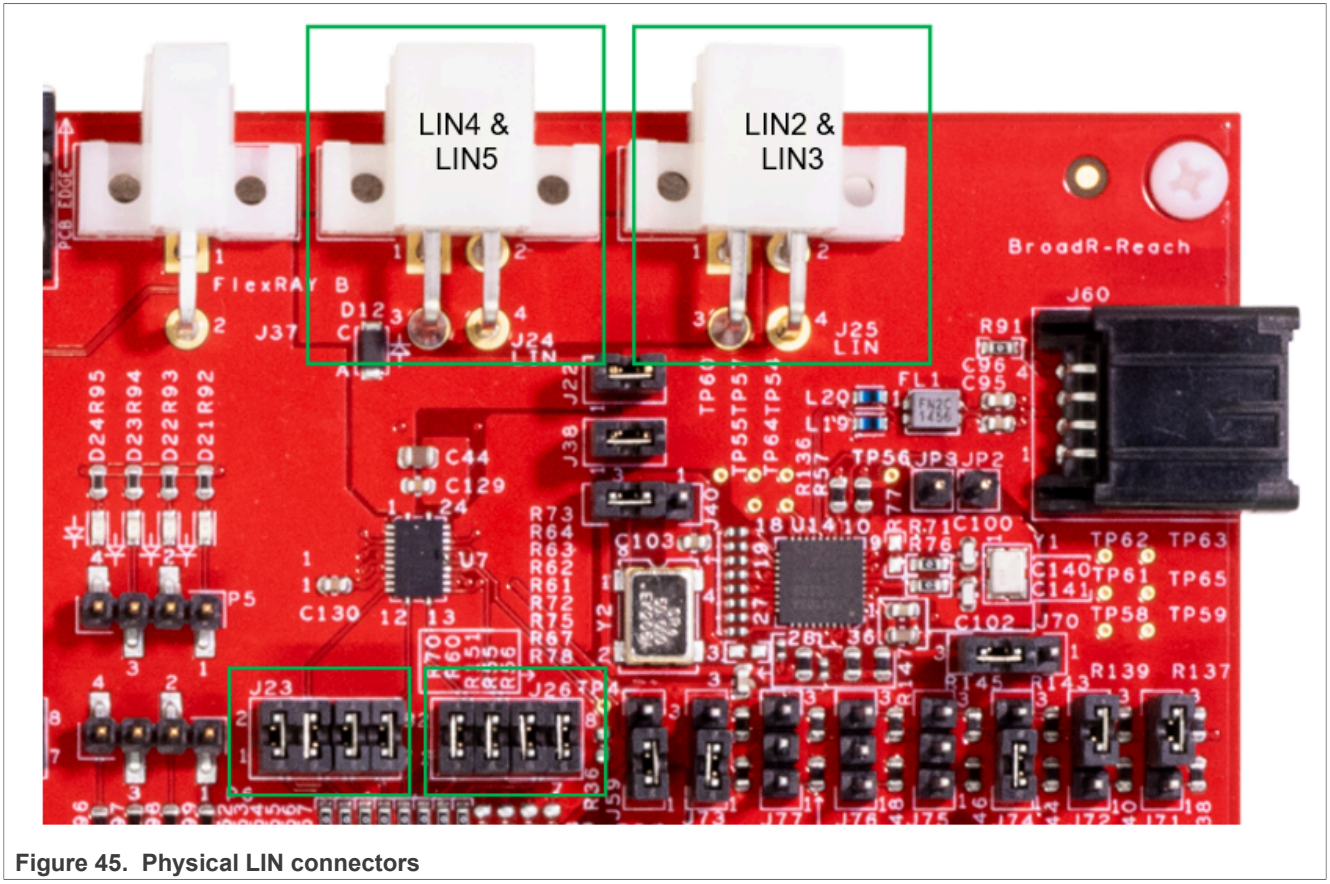


Figure 45. Physical LIN connectors

The four LIN ports are connected by default via J24 & J25 to LIN instances and GPIO pins on the MCU, both available on the general access headers on the motherboard and connected to the daughtercard. In the motherboard schematic, these four LIN ports are referred to as LIN2-5. Table 12 maps the motherboard LIN ports to the MCU.

Note: *Motherboard LIN3 is not directly connected to the daughter-card due to routing constraints. However, it is possible to connect to the general access headers with J26.*

Table 14. MCU LIN module and GPIO pin numbers for MB LIN signals

Motherboard LIN	MCU LIN Signals	MCU GPIO Pin
LIN2_TX	Not Connected	Not Connected
LIN2_RX	Not Connected	Not Connected
LIN3_TX	Not Connected	Not Connected
LIN3_RX	Not Connected	Not Connected
LIN4_TX	LIN11_TX	GPIO[157]
LIN4_RX	LIN11_RX	GPIO[158]
LIN5_TX	LIN9_TX	GPIO[150]
LIN5_RX	LIN9_RX	GPIO[151]

4.4 USB/UART

The USB/UART section of the motherboard allows the user to connect to the board and start up a serial terminal with just a USB cable, avoiding the need for any RS232 to USB converters (USB types may change between board revisions).

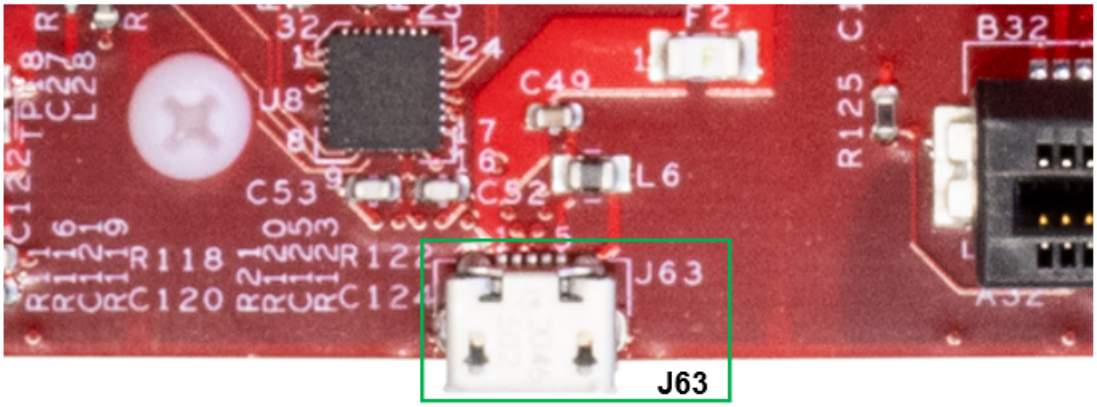


Figure 46. J63 UART Connector

4.5 FlexRay

S32Z2 contains two FlexRay communication controller modules that implement FlexRay Protocol Specification 2.1A. The connectors available on the EVB are J32 for FlexRay_A, J37 for FlexRay_B, and J34 for a joint connection. The EVB contains a TJA1081 transceiver module for each FlexRay, providing an advanced interface between the physical buses in the network and the protocol controller of the MCU.

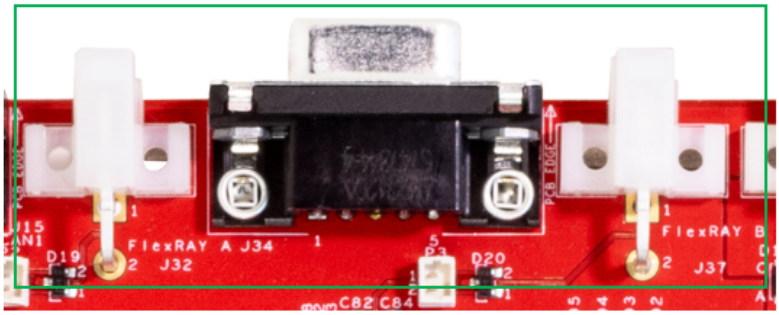


Figure 47. Physical FlexRay connectors

Header J31 for FlexRay_A and J35 for FlexRay_B are used to enable and route the FlexRay signals from the transceiver modules to the following GPIO pins, both available on the general access headers on the motherboard and connected to the daughtercard. Table 13 maps motherboard FlexRay signals to MCU FlexRay instances and GPIO pins.

Table 15. MCU GPIO PIN numbers for FlexRay signals

MB FlexRay Signal	MCU FlexRay Signal	MCU GPIO Pin
FLXR0A_TXEN	FR_0_TXE_A_B	GPIO[6]
FLXR0A_TXD	FR_0_TXD_A	GPIO[7]
FLXR0A_RXD	FR_0_RXD_A	GPIO[8]
FLXR0B_TXEN	FR_0_TXE_B_B	GPIO[6]

Table 15. MCU GPIO PIN numbers for FlexRay signals...*continued*

MB FlexRay Signal	MCU FlexRay Signal	MCU GPIO Pin
FLXR0B-TXD	FR_0_TXD_B	GPIO[1]
FLXR0B-RXD	FR_0_RXD_B	GPIO[2]

Header J33 for FlexRay A and J36 for FlexRay B are used to configure the operating mode of the transceiver modules by setting pins STBN and EN. By default, both pins are high, so the module is operating in Normal mode. Using jumper wires, the following table shows the other possible configurations.

Table 16. TJA1081 FlexRay transceiver module mode select

Mode	STBN	EN
Normal	1	1
Receive Only	1	0
Go to Sleep	0	1
Sleep	0	0

Note that both pins have internal pull-down resistors, so if the jumpers are left floating, the module will enter Sleep mode.

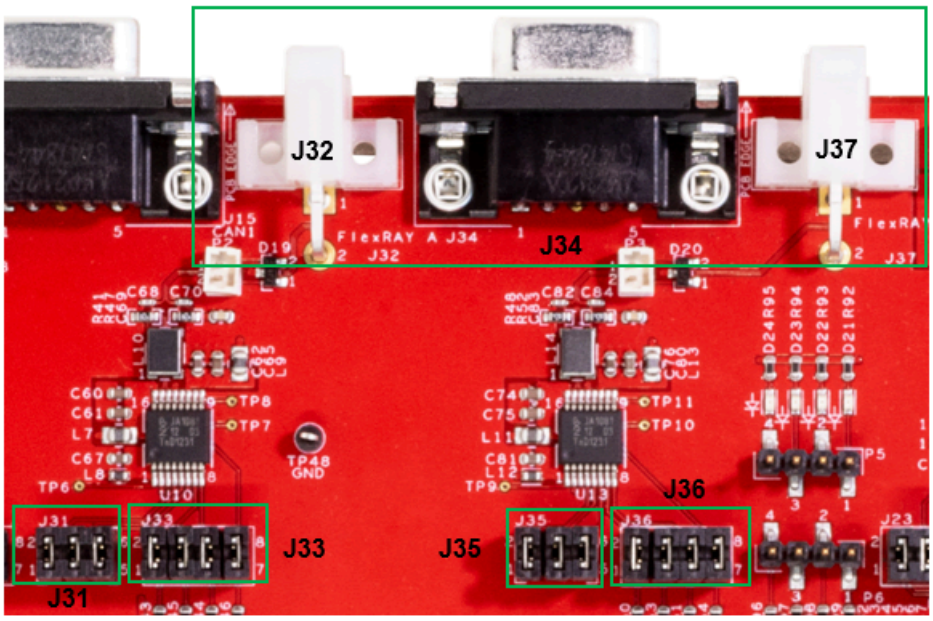


Figure 48. FlexRay connectors, enable, and mode select jumpers

4.6 Ethernet

S32Z2 contains two NET Controller (NETC) dual Ethernet module. It is capable of 10/100/1000 Mbps MII/RMII/RGMII.

The S32Z2 daughtercard provides two Gigabit Ethernet PHY connected to ETH0 and ETH1 interface on the MCU. All Ethernet capabilities are on the S32Z280-400EVB daughtercard. There are no Ethernet connections to the motherboard.

4.7 PSI5

There is one PSI5 instance from the S32Z2 accessible on the motherboard. To connect to the PSI5 instance, connector J47 is used.

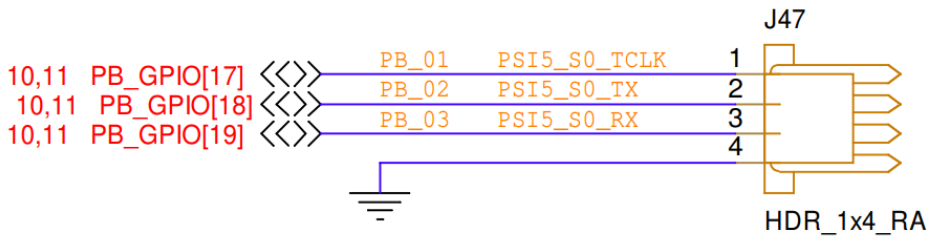


Figure 49. PSI5 interface schematic

PSI5 signals can be accessed from the motherboard J47. Set Daughter card jumper J68 positions 4-5 and 7-8 to route MCU signals to J47.

Table 17. MCU GPIO PIN numbers for PSI5 signals

PSI5 Signal	MCU GPIO Pin
PSI5_S_0_TCLK	GPIO[5]
PSI5_S_0_TX	GPIO[23]
PSI5_S_0_RX	GPIO[3]

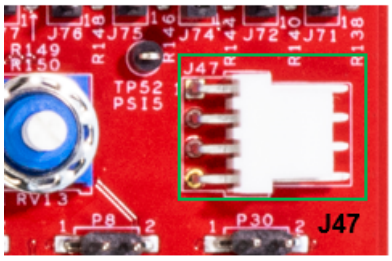


Figure 50. Physical PSI5 connector

4.8 User LEDs

There are four yellow user LEDs on the motherboard, connected via header P5. Each LED will turn ON when its corresponding header pin is pulled to ground.

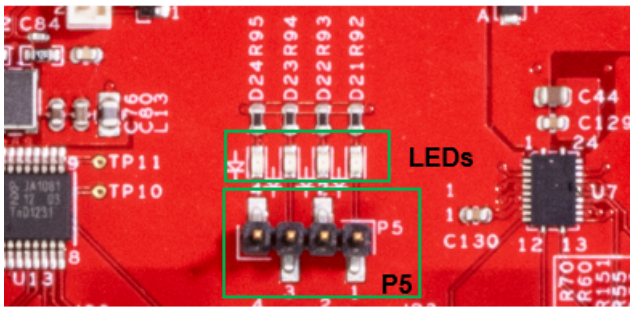


Figure 51. Motherboard user LEDs

4.9 User inputs

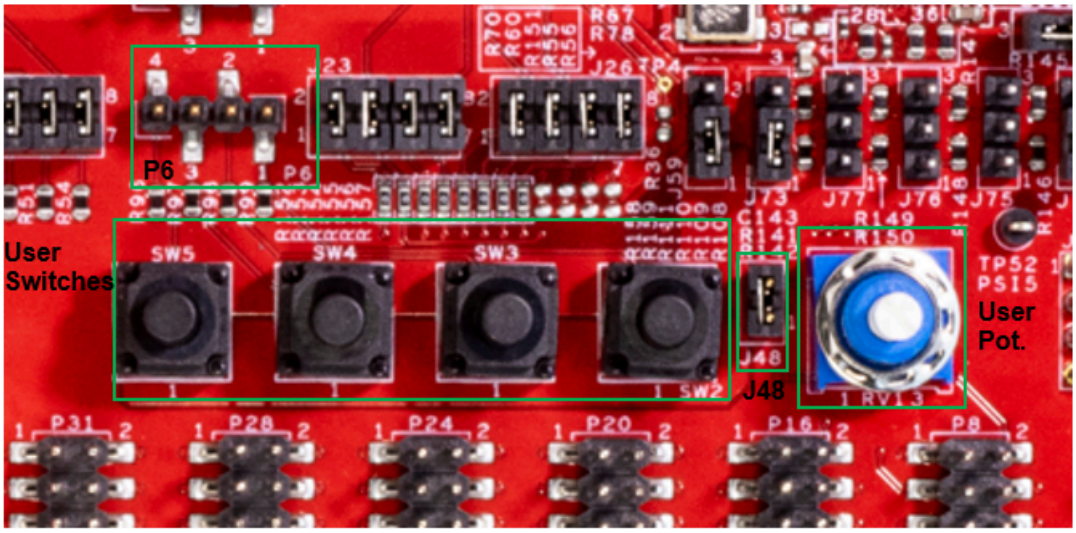


Figure 52. Motherboard user inputs

4.9.1 Switches

There are four user pushbutton switches on the motherboard, each connected via header P6. User can connect any GPIO from the headers to P6 using jumper wires. When a switch is pressed the header pin is high (3.3V), and when released, the pin is low.

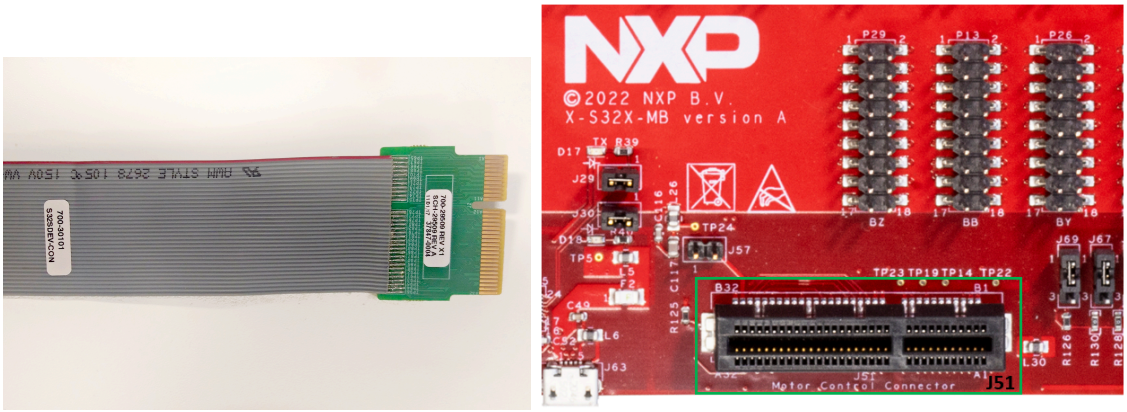
4.9.2 Potentiometer

There is a 2K potentiometer on the motherboard, connected to header J48. This is not connected to any MCU pin on the daughtercard but is available on the general access headers on the motherboard. This is connected to analog ground for isolation.

4.10 Motor control

There is a separate motor control connector available on the motherboard, located in the bottom right of the board.

Note: *This connector is not used with S32Z2 Family MCUs. A separate daughter-card, S32SE288-975EVB, includes two motor-control connectors for use with NXP motor kits.*



S32SDEV-CON motor control connector cable and socket

4.11 Other connectors

There are general access connectors available that allow easy access to MCU GPIO pins that are not dedicated to other purposes on the daughter-card.

This boiler plate is not ready for publication until the steps found in the Freescale Trademark Attribution Worksheet have been completed. You can access it here: http://compass.freescale.net/go/ 215485375

Note also that the ARM attribution must be updated from “ARMnnn” to reflect the correct product name.

5 Revision history

Table 18. Revision history

Document ID	Release date	Description
UG10272 v.1.0	10 July 2025	• Initial release

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