UG10246

NXP 48V Motor Control Development Platform User Guide

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Document information

Information	Content
Keywords	Motor control, 48V, PMSM
Abstract	This user guide introduces NXP 48 V Motor Control Development Platform for high power automotive motor control applications.

1 Introduction

This user guide introduces NXP 48 V Motor Control Development Platform for high power automotive motor control applications. This development platform is built up of three standalone boards called Power Stage board, Adapter board and Controller board. These boards are mechanically and electrically connected to each other and cannot operate independently. Power Stage board primarily controls energy flow from power supply source to the motor load. Adapter board processes and adjusts analog, digital and power supply signals, which are routed in between Power Stage board and Controller board. Controller board contains microcontroller, system basis chip, and communication layers, which ensure proper control of power elements, supply of processing circuitry and communication with external systems. This platform is formed to drive two 3-phase BLDC/PMSM or one 6-phase motors in power range up to 5.6 kW. Moreover, it offers several advanced features for complex, high-end motor control application development in 48 V automotive or non-automotive segments.

1.1 MC development platform features

NXP 48 V MC development platform provides following functionalities:

- **System parameters:**
  - Two independent 48 V 3-phase half-bridge arrangements with standalone DC-link circuits
    - Standalone DC-link pre-charging for each DC-link circuit in two steps
  - Extended low voltage operation starting from 24 V
  - Phase current capability up to 80 $A_{(RMS)}$ and 120 $A_{(MAX)}$ for each 3-phase half-bridge
  - Power supply converters for internal digital and analog subsystems:
    - 48 V/15 V Non-Isolated DC/DC Buck-Boost converter
    - 12 V/12 V Isolated DC/DC Flyback converter
- **Analog quantities measurement:**
  - Phase current sensing using triple-shunt configuration
    - Parallel connection of two shunts in each leg of inverter
    - Various hardware (HW) configurations allow to change maximum current sensing range
  - Measurement of following voltages:
    - BEMF voltage sensing by voltage divider
    - Phase voltage reconstruction realized by external comparators and dedicated microcontroller (MCU) peripherals with software (SW) routine
    - DC-link voltage measurement
    - Forward voltage measurement
    - Battery voltage measurement
  - Temperature measurement on different positions of Power Stage board
    - Measurement of temperature in each leg of inverter
    - Temperature measurement of pre-charge MOSFETs
    - Multiplexing of temperature signals
- **Motor speed and position sensors support:**
  - Resolver sensor signal generation and signal processing support
  - Encoder/HALL signal processing support
- **Fault detection and safe mechanisms:**
  - Fault protection mechanisms
    - Over-voltage protection using single comparator
    - Over-current protection using window comparators
    - Over-temperature protection
    - Pre-charge desaturation protection

  - Monitor of Buck power supply malfunction
- Independent safe mechanisms for PWM signals:
  - Safe open mechanism turns-off all power MOSFETs in 3-phase half-bridge
  - Safe short mechanism turns-on only low side power MOSFETs in 3-phase half-bridge
- Power supply redundancy:
  - Main Non-Isolated Buck-Boost converter is backed up Isolated Flyback converter in case of Buck-Boost malfunction
- Galvanically isolated control and wake-up signals

- **General system information:**
  - S32K344 Arm® Cortex®-M7-based microcontroller in lockstep core configuration linked with FS2613 SBC (System Basis Chips)
  - Short protection realized by fuse
  - Robust high current screw terminals
  - Massive aluminum heatsink, supported by active cooling
    - MCU independent/dependent control of dual fans (not included)
  - Automotive connectivity interfaces LIN, CAN, and Ethernet
    - Galvanically isolated and non-isolated CAN transceivers
  - Application buttons and switches
  - Headers for MCU pin accessibility
  - On-board debugger and JTAG debug interfaces
  - LED indicators and debugging headers

1.2 Operation conditions of NXP 48 V MC development platform

*The platform was not evaluated in whole operation range, values in the table above are based on design specification.

Table 1. Electrical specification of NXP 48 V MC development platform

Parameter	Min		Typical	Max
Designed Power Stage electrical specifications				
Supply voltage	20 V		48 V	60 V
Phase current	-		80 A	120 A
Ambient temperature	0°C		20°C	40°C
Board temperature (with passive heatsink)	-		-	150°C
Electrical conditions of Power Stage applied for EMC evaluation				
Supply voltage	-		-	48 V
Phase current	-		2 A	5 A
Ambient temperature	-		25°C	-
Board temperature (with passive heatsink)	-		-	-
Adapter board specifications				
Flyback	Input supply voltage	8 V	12 V	16 V
	Output current	-	500 mA	1 A
Input digital ports	Input supply voltage	-	5 V	5.5 V

Table 1. Electrical specification of NXP 48 V MC development platform*...continued*

Parameter	Min		Typical	Max
Fan control	Output supply voltage	-	12 V	15 V
	Output current	-	100 mA	500 mA
Encoder	Output supply voltage	-	5 V	5.1 V
	Output current	-	-	10 mA
Controller board specification				
Input supply voltage of SBC	3.2 V		12 V	15 V

Note: *NXP does not guarantee compliance with EMC standards within or out of the conditions specified in the section "Designed Power Stage electrical specifications" of Table 1.*

1.3 NXP 48 V MC development platform architecture

The simplified block diagram of NXP 48 V MC development platform is depicted in Figure 1. This hardware platform consists of three different boards, which contains different subsystems reasonably distributed on each board. The boards are mechanically and electrically connected to each other by means of different type of connectors i.e., header connectors or PCIe connector. For the sake of clear clarity, the architecture of complete platform is decomposed on board architectures. Figure 2 shows block diagram of Power Stage board, Figure 3, Figure 4, Figure 5, Figure 6 and Figure 7 show block diagrams of Adapter board and Figure 8 shows block diagram of Controller board.

Block diagram of complete NXP 48 V MC development platform demonstrates connection of individual boards to each other and way of system interaction with environment through different interfaces. Power Stage board is in charge to transform DC voltage and current provided by supply source on the input terminals to 3-phase AC voltage and current on the output terminals for the motor load. Two 3-phase half-bridges with output terminals are capable of independent controlling of two 3-phase BLDC/PMSM motors or single 6-phase motor. The electrical and mechanical connection of Power Stage board and Adapter board is arranged by two header connectors, where each of the two supports signal transfer just for particular 3-phase half-bridge.

The main purpose of Adapter board is to adjust and process analog, digital and power supply signals, which are transmitted between Power Stage board and Controller board. There are several subsystems, which support proper operation of platform. Platform communication with superior system is carried out through galvanically isolated CAN (Controller Area Network) transceiver. In addition, superior system is capable to control and wake the system up through wake-up control signals. The connection of Controller board and Adapter board is arranged by means of PCI-Express connector. It contains a huge number of pins for analog, digital and power supply signals, therefore can easily fulfill requirements for control of two 3-phase motors or one 6-phase motor. Moreover, it provides sufficient mechanical robustness of Controller and Adapter boards connection.

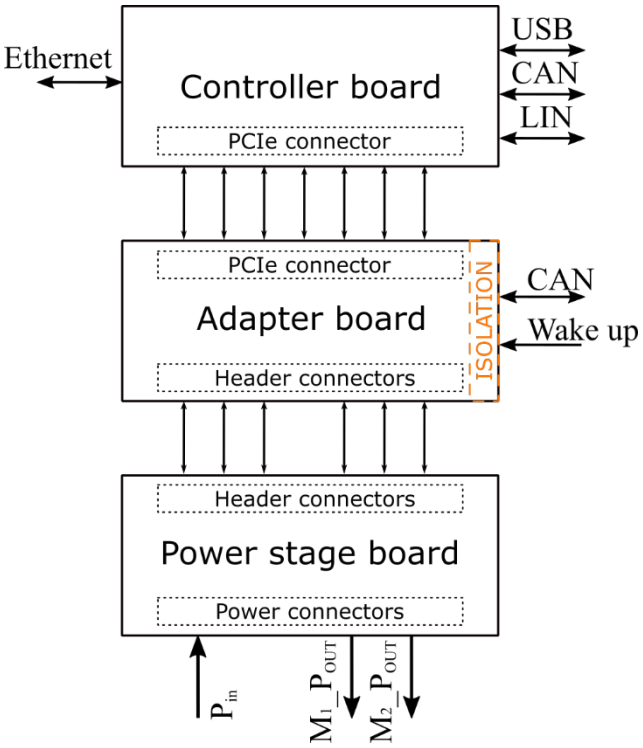


Figure 1. Block diagram of NXP 48 V MC development platform

NXP 48 V MC development platform introduces benefit of modularity to be able to scale output power with less or more powerful Power stage boards or boost computational performance with more powerful microcontrollers being a part of the Controller board.

The following sections provide detailed explanation of Power stage board, Adapter board and Controller board architectures.

1.3.1 Power stage board architecture

Various block colour differentiate a block functionality:

- Green – Motor control related hardware + 3-phase half-bridge
- Gray – Interfaces and terminals
- Orange – Other functions of the system
- Red – Board power supply functionality

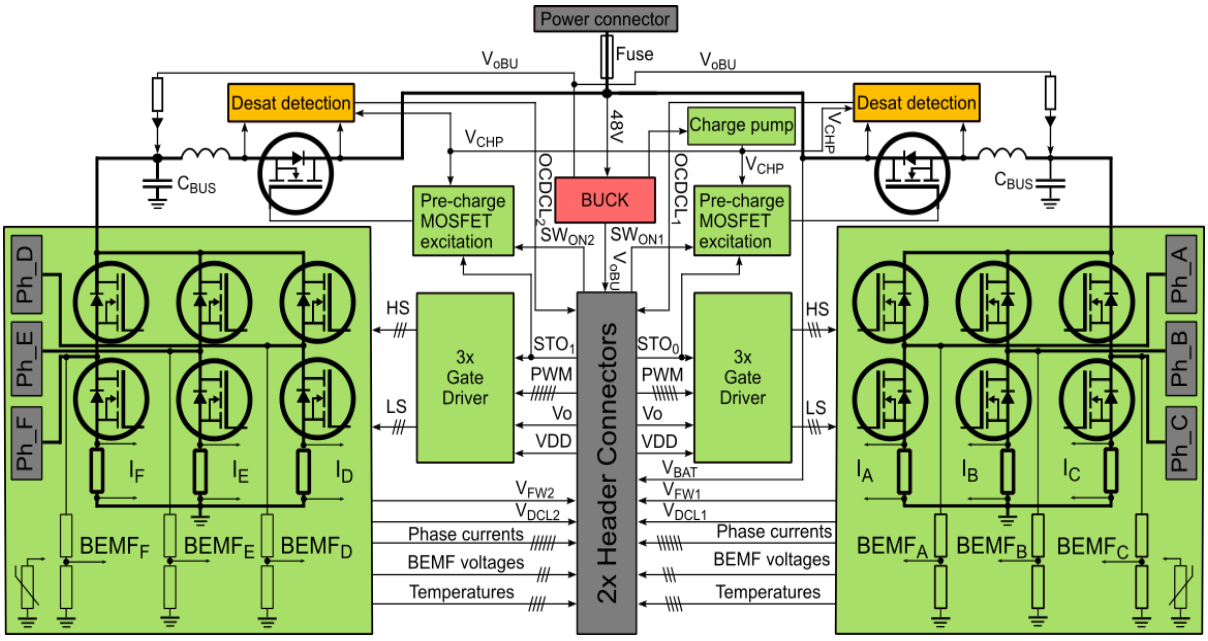


Figure 2. Block diagram of Power Stage board

Power Stage board is constructed to be fully functional and be reliably operated in wide range of input voltage from 24 V up to 60 V. Figure 2 shows block diagram of Power Stage board. The board primarily contains two 3-phase MOSFET half-bridges. The phase outputs of both 3-phase half-bridges are connected to the robust power terminals. Each 3-phase MOSFET half-bridge is powered from standalone DC-link circuit, which is pre-charged by own pre-charge circuit built up on power MOSFETs. The power MOSFETs of 3-phase half-bridges and power MOSFETs of pre-charge circuits are duplicated due to high power. Parallel connection of components is highlighted by bold outlines i.e., power MOSFETs or shunt resistors. Simple analog logic supporting high side MOSFET switching is used for pre-charge MOSFETs. Three single phase gate drivers are used to excite one 3-phase MOSFET half-bridge. Those gate drivers provides enough energy for all power MOSFETs. They are activate by default, however can be disabled by shutdown signals STO_0 for first 3-phase MOSFET half-bridge or STO_1 for second 3-phase MOSFET half-bridge. Those control signals can be generated by microcontroller or supervisor system over galvanic isolated layer. Single 3-phase MOSFET half-bridge with three standalone gate drivers utilizes one control signal shared for those three gate drivers and particular pre-charge circuit.

The sensors of phase currents and BEMF voltages are also implemented in Power Stage board. Two parallelly connected shunt resistors are placed in each leg of inverter below low side MOSFETs. Differential signals of phase current are directly connected to the particular header connector and transmitted to Adapter board. The BEMF voltages, DC-link, forward and battery voltages are scaled by voltage dividers, which adjust analog signals to fit the ADC input range of 0-5 V. Such scaled analog signals are subsequently connected to particular header connector. Additionally to phase current and BEMF voltage measurement, the Power Stage board support temperature measurement by NTC sensors. The NTC sensors are placed close to each phase of inverter and close to pre-charge MOSFETs, because fully operated power MOSFETs are sources of the greatest heat. All analog and digital signals of Power stage board are subsequently transferred through two header connectors to the Adapter board.

Input 48 V voltage is used to be converted by step-down Buck converter. The converter configuration enables to operate in wide range of input voltage, from 20 V up to 60 V, while output voltage is always constantly set to 15 V. This output voltage is connected to header connectors and transmitted to Adapter board to power supply redundancy circuit.

The pre-charge circuit contains power MOSFETs, which allow to connect DC-link circuit with input terminals and transfer energy from input to the output through 3-phase MOSFET half-bridge and excitation circuit, which

controls turn-on/off process of power MOSFETs. The process of DC-link capacitors pre-charging is an essential function in high voltage and especially high-power systems due to limitation of inrush current. The DC-link circuit is pre-charged in two steps. In the first step, limited DC current is injected through diode and resistor from Buck converter to the DC-link capacitors. DC-link capacitors are going to be pre-charged on 15 V. In the second step, pre-charge MOSFET excitation circuit turns on pre-charge power MOSFETs, which allows to connect input terminals with DC-link capacitors. Those capacitors are subsequently charged on the level of voltage of input power supply source. Turn-on action of pre-charge MOSFETs is conditional by followings requirements.

1. Digital control signals STO_0 or for first 3-phase MOSFET half-bridge or STO_1 for second 3-phase MOSFET half-bridge have to be inactive, which means logic zero has to appear on these ports. However this condition is bypassed in current HW configuration, so logic state of STO0 of for first 3-phase MOSFET half-bridge or STO1 for second 3-phase MOSFET half-bridge doesn't influence of pre-charge functionality.
2. Digital control signals SW_{ON1} or for first 3-phase MOSFET half-bridge or SW_{ON2} for second 3-phase MOSFET half-bridge have to be activated at the same time.
3. High side position of pre-charge MOSFETs requires boosting of excitation voltage over the DC-link voltage. This role is covered by charge pump circuit, which utilizes switching voltage of Buck converter.

Monitoring of desaturation fault of pre-charge MOSFETs is an additional feature and also utilizes boosted voltage from charge pump circuit. Reverse polarity protection of input source is handled by fuse, which is irreversible damaged if such event happened. Heat dissipation and cooling of system is handled by aluminum heatsink and active cooling system.

1.3.2 Adapter board architecture

Various block colour differentiate a block functionality:

- Green – Motor control related hardware + 3-phase half-bridge
- Pink – Application control
- Gray – Interfaces and terminals
- Orange – Other functions of the system
- Red – Board power supply functionality
- Violet – Communication interface

Figure 3, Figure 4, Figure 5, Figure 6 and Figure 7 show individual block diagrams of Adapter board. The Adapter board is responsible for signal processing of all signals, which are transferred in between Power Stage board and Controller board. In addition, the board provides communication interface with superior system through galvanically isolated layer. Mechanical and electrical connection with Power Stage board is arranged by header connectors, while mechanical and electrical connection with Controller board is arranged by PCIe connector. Overall architecture of Adapter board is divided on several block diagrams.

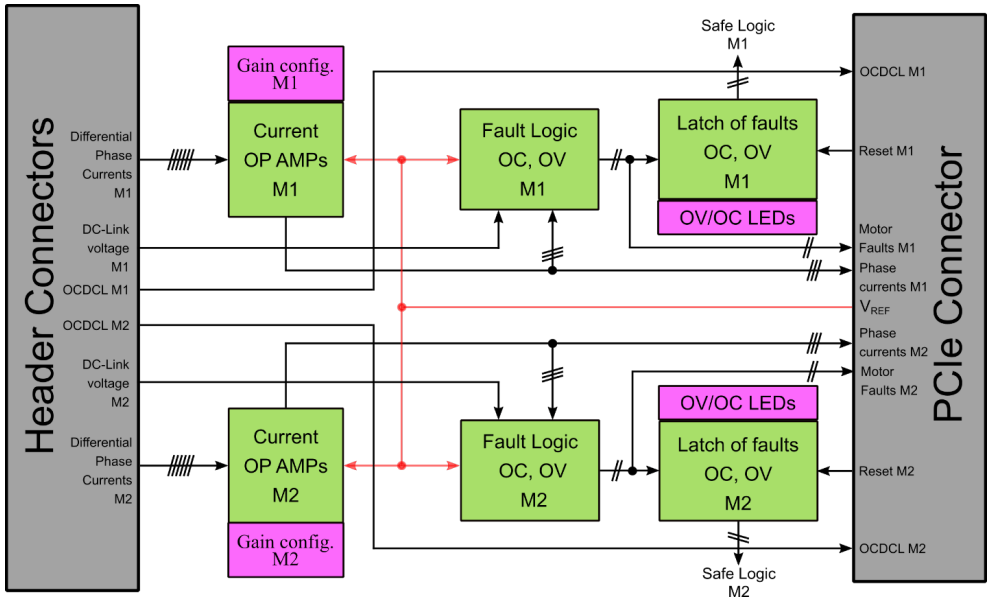


Figure 3. Block diagram of Adapter board - current sensing and fault logic

Figure 3 shows simplified block diagram of current sensing circuit and fault logic of Adapter board. Differential signals phase currents are routed to conditional circuitry with operational amplifiers. Conditional circuitry amplifies those differential signals and adds voltage offset in order to fit ADC input range of 0-5 V. The range of current measurement can be modified by gain configuration headers, which are a part of conditional circuitry with operational amplifiers. Amplified signals of current are directly routed to the PCIe connector and are also used for fault monitoring purpose. Fault logic is monitoring phase currents and DC-link voltage in order to detect over-current state and over-voltage state. There is only one, common fault signal of overcurrent for all 3-phase currents. The output signals of fault logic are routed to the PCIe connector and are also routed to the latch logic. The signal of desaturation fault of pre-charge MOSFETs is routed from header connector directly to PCIe connector without additional signal processing. This logic is latching the fault state of over-current or over-voltage or both and in addition, it indicates latched fault status by LEDs. Reset of the latched faults is carried out by reset signal, which is provided by microcontroller and routed over PCIe connector. Outputs of latch logic are subsequently routed to the safe logic. The conditional circuitry with operational amplifier and fault logic require voltage reference due to bidirectional flow of phase current. This voltage reference is provided by Controller board and transmitted over PCIe connector. Each 3-phase MOSFET half bridge utilizes standalone conditional circuitry with operational amplifiers and fault logic.

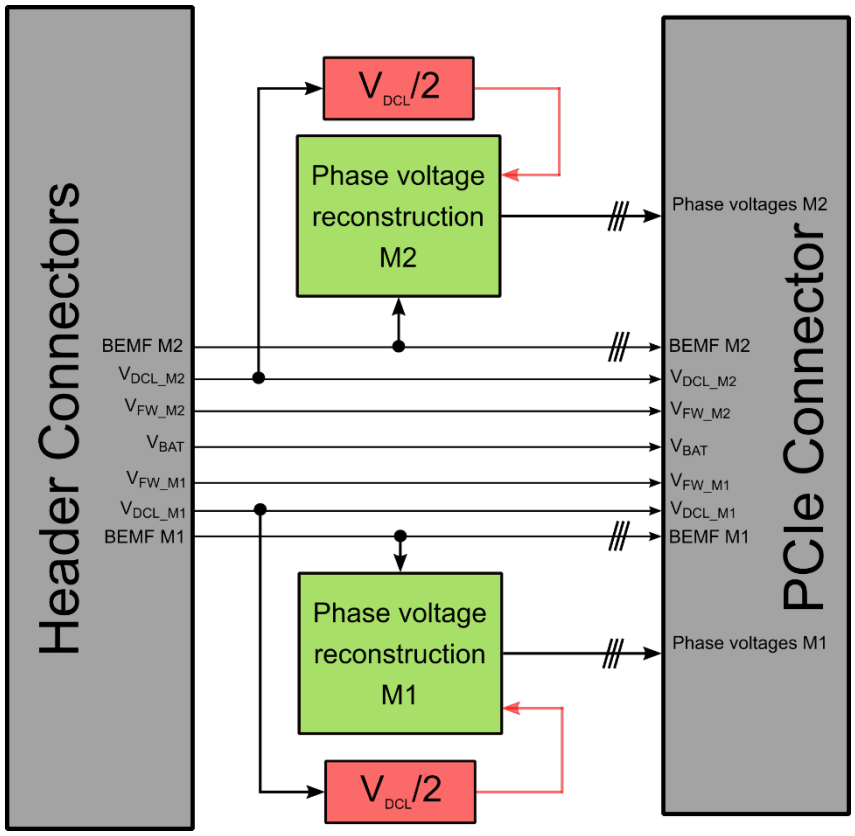


Figure 4. Block diagram of Adapter board - Phase voltage reconstruction and analog signals transfer

Figure 4 shows block diagram of Adapter board - phase voltage reconstruction and analog signals transfer. Analog signals of forward voltage, DC-link voltage, BEMF voltages for both 3-phase MOSFET half bridges and battery voltage are directly routed from header connectors to PCIe connector. However, DC-link voltages of both 3-phase MOSFET half-bridges as well as BEMF signals are used for phase voltages reconstruction purpose. This hardware circuit supports signal processing, but final reconstruction of phase voltage is carried out by means of appropriate timer module of microcontroller and software routine. The outputs of phase voltage reconstruction module are routed to PCIe connector. Each 3-phase MOSFET half-bridge uses standalone phase voltage reconstruction module.

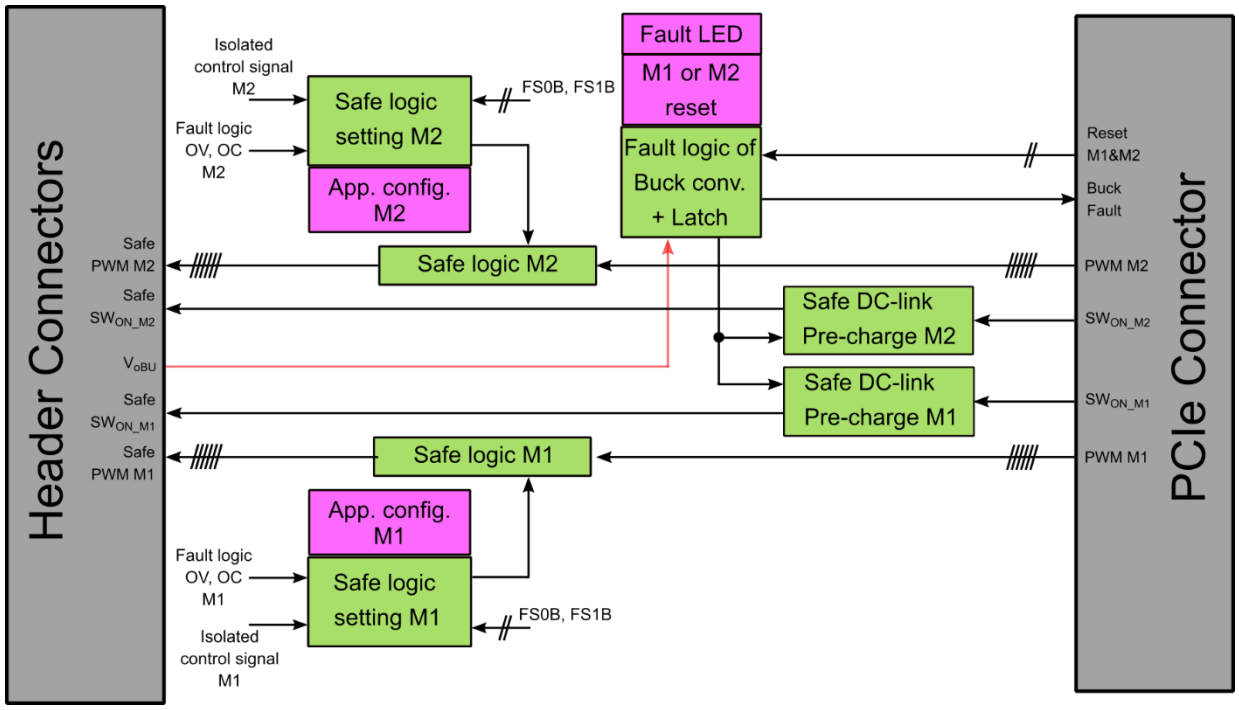


Figure 5. Block diagram of Adapter board - Safe logic

Figure 5 shows block diagram of Adapter board safe logic circuitry. This circuitry is composed of several parts, which process generated PWM signals, pre-charging control signals, latched fault signals and external control signals. In addition, monitoring of proper operation of Buck converter is a part of this safe logic. Latched fault signals of over-current and over-voltage together with external control signal and fault-safe signals FS0B or FS1B are processed in Safe logic setting block. This block enables to configure safe state of system in accordance with application requirements by means of App. Config block. The NXP 48 V MC development platform supports two safe states:

- Safe open state – All MOSFETs are turned off
- Safe short state – Low side MOSFETs are turned on and high side MOSFETs are turned off

The safe state can be activated on behalf of fault logic behavior, interaction of superior system or interaction of system basis chip (SBC).

The block of Safe logic processes PWM signals generated by microcontroller depending on operation of system. There are three typical operation states:

1. Normal operation: Behavior of PWM outputs of safe logic copies behavior of the inputs. Generated PWM signals are transmitted through safe logic without change of behavior, only symmetrical propagation delay is inserted.
2. Fault operation: Safe open state – The PWM outputs of safe logic are deactivated, input PWM signals are not propagated through safe logic.
3. Fault operation: Safe short state – The outputs of safe logic are modified and do not follow input behavior. PWM channels of safe logic for low side MOSFETs are activated and PWM channels of safe logic for high side MOSFETs are deactivated.

The fault logic of Buck converter monitors output voltage of Buck converter and detect fault in case of under-voltage state. This fault is subsequently latched and signalized by Fault LED. Latched fault of Buck undervoltage disable digital control signal of pre-charge MOSFETs. Activation of pre-charge MOSFETs is conditioned to proper functionality of Buck converter.

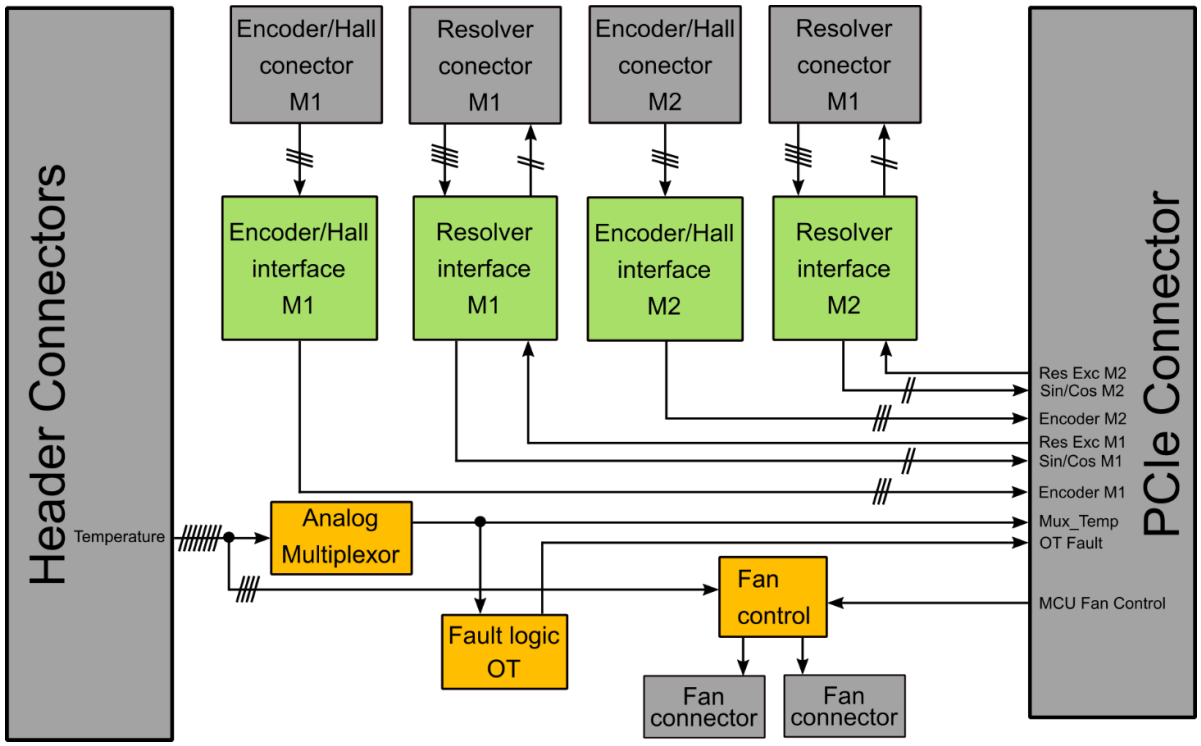


Figure 6. Block diagram of Adapter board - Rotor position signals processing and temperature processing

Figure 6 shows block diagram of Adapter board - Rotor position signals processing and temperature processing. Adapter board supports resolver and encoder/hall signal processing for sensor-based motor control applications. Resolver signal processing circuit deals with resolver excitation, and sine-cosine signal processing. Those two functions are part of one block in figure above. Resolver sensor is connected to the system over resolver connector and microcontroller signals connection is managed over PCIe connector.

Signal processing of encoder/hall is carried out over different module. Encoder sensor or three Hall sensor can be connected over Encoder/Hall connector. An output signals of Encoder/Hall interface module are routed to the PCIe connector, where can be processed by appropriate peripheral of microcontroller. Both rotor position signal processing interfaces are duplicated in Adapter board, which allows to execute independent control of two 3-phase PMSM or BLDC motors with resolver or encoder/hall sensors.

Eight analog signals of temperature are routed from header connectors to Analog multiplexer. Single output of multiplexer is routed to PCIe connector, but it is also used for over-temperature fault logic. An output of this fault logic is subsequently routed to the PCIe connector. Selection of input analog channels is managed by three GPIO pins of microcontroller routed from PCIe connector. Four specific analog signals of temperature and digital control signal from microcontroller are used for control of active cooling realized by fan control block. This block mainly processes signals of temperature and controls two fans either by four analog signals of temperature or by digital signal provided by microcontroller. Those two fans can be connected over fan connectors.

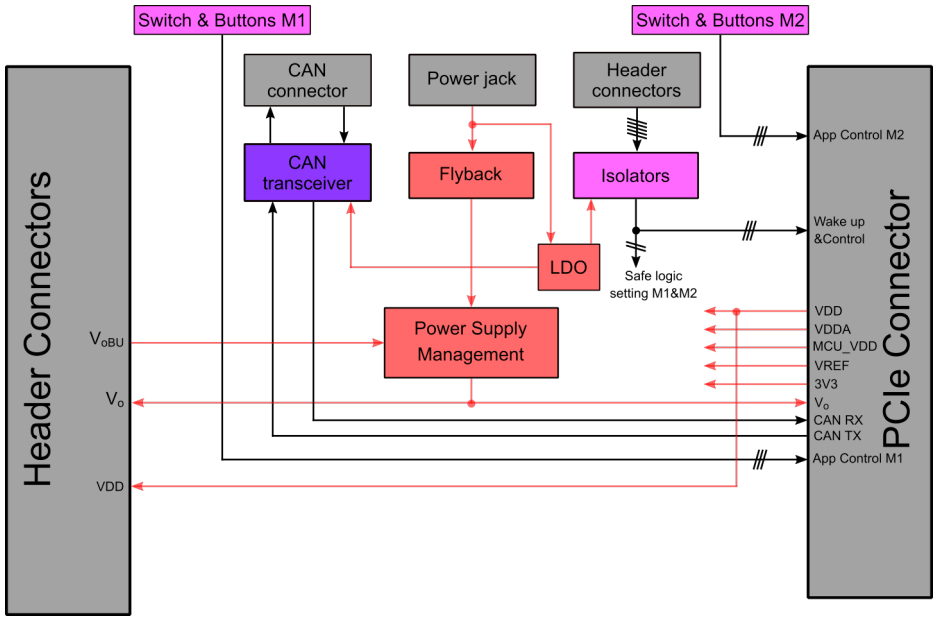


Figure 7. Block diagram of Adapter board - Isolated layer, Power supply management and Application control buttons

Figure 7 shows block diagram of Adapter board Isolated layer, Power supply management and Application control buttons. The Adapter board contains galvanically isolated circuitry with CAN transceiver, Flyback converter and Isolators for digital control and wake-up functionalities. This galvanically isolated layer allows to supply, control and communicate with NXP 48 V MC development platform from superior system. Digital signals of superior system can be connected over Header connector to the Isolator and can control or wake the system up. The control signal of superior system can only invoke pre-defined safe state i.e., if the system is not responding. The galvanically isolated CAN transceiver is responsible for communication of the superior system with NXP 48 V MC development platform. The Flyback converter represents redundant power supply source to the Buck converter. This isolated converter is in charge of overtaking the supply task in case of malfunction of Buck converter and it is powered from standalone 12 V battery. The output of Flyback converter is connected to Power Supply Management block. Additional LDO regulator provides power supply for circuitry of galvanically isolated layer. The Power Supply Management block connects the output voltage of Buck converter and output voltage of Flyback converter and provide output voltage V_o, which is routed to the header connector and PCIe connector. During normal operation of Buck converter, the output voltage V_o is equal to the Buck output voltage. If Buck converter operation is interrupted or faulty and do not provide sufficient voltage at output, the output voltage V_o is equal to the Flyback output voltage. Main purpose of this Power Supply Management block is to keep the system alive in case that main power supply source failed. The power supply signals VDD, VDDA, MCU_VDD, VREF and 3V3 are provided by Controller board and used for supplying of all circuitries of Adapter board. The VDD power supply signal is also transmitted to the Power stage board over header connector.

The Adapter board also contains buttons and switches which are dedicated for application control. Those application control signals are routed to the PCIe connector.

1.3.3 Controller board architecture

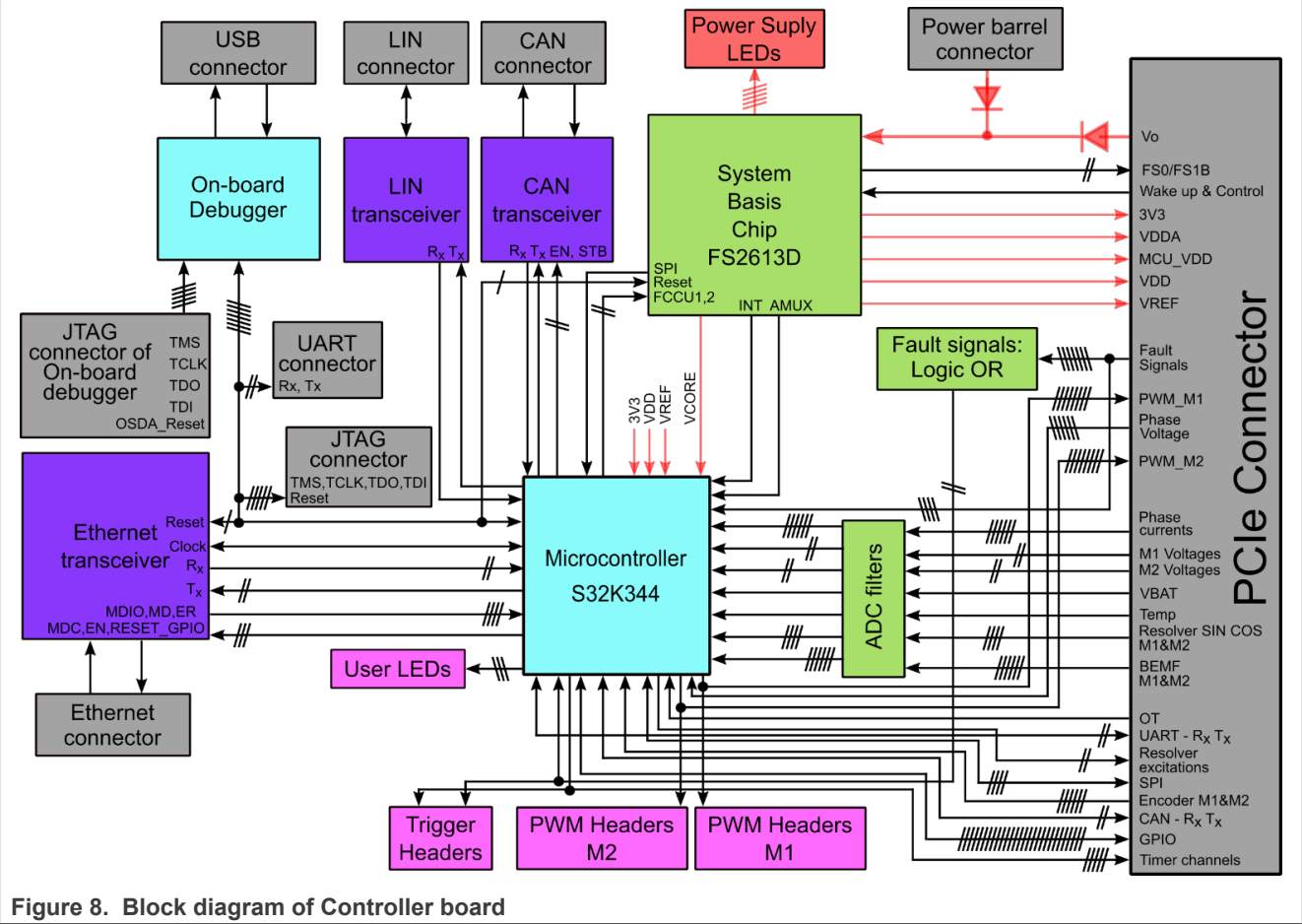


Figure 8. Block diagram of Controller board

Various block colour differentiate a block functionality:

- Green – Motor control related hardware + 3-phase half-bridge
- Pink – Application control
- Gray – Interfaces and terminals
- Red – Board power supply functionality
- Violet – Communication interface
- Turquoise – Microcontroller and application software download, and debug interface

Figure 8 shows simplified block diagram of Controller board. This board is in charge of controlling energy transformation process and establishes communication with environment. The main role of the board components is played by microcontroller S32K344, which is tightly linked with SBC FS2613D.

The SBC part provides power supply outputs for analog, digital, communication circuitry and microcontroller itself. Functionality of power supply outputs of SBC is signalized by Power supply LEDs. The System basis chip is powered by V_o input voltage from PCIe connector. This input voltage is provided by Power supply management block situated in Adapter board. The SBC can be optionally powered through barrel connector, however the Controller board cannot be connected to the NXP 48 V MC development platform. The System basis chip offers also functional and safety features which supervise microcontroller operation or interact with external systems and allow to do pre-development of safety application. Fail-safe outputs (FS0/FS1B) of system basis chip are routed to the safe logic through PCIe connector. The wake-up and control signals routed from galvanically isolated layer through PCIe connector are connected to the input ports of SBC. The

FCCU0/1 signals are routed from SBC to the microcontroller and are responsible for HW failure monitoring of microcontroller. Communication of SBC with microcontroller is managed over SPI interface.

Automotive non-isolated communication interfaces CAN, LIN and Ethernet are a part of board circuit enablement. Those interfaces are connected to the microcontroller and output terminals are placed solely on Controller board. Software upload and its debugging can be carried out through JTAG interface or On-board debugger. This On-board debugger is capable to create virtual serial port for communication with FreeMASTER, which is useful tool for debugging and visualization. Trigger and PWM header connectors, user LEDs support application debugging. ADC filters are used for analog signals filtering. The motor fault signals of over-current, over-voltage Buck monitoring malfunction and desaturation fault of pre-charge MOSFETs are processed by logic OR function in order to create common and standalone fault signals for first motor configurations and second motor configuration.

2 NXP 48V MC Development platform PCB description

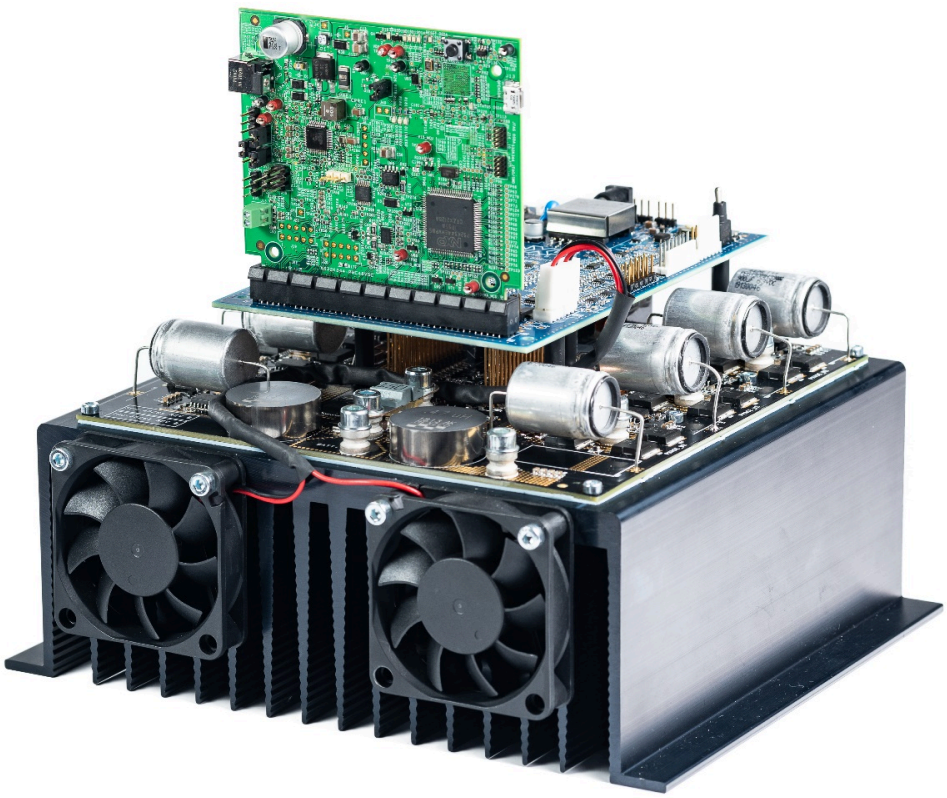


Figure 9. NXP 48V MC development platform

2.1 Power Stage board PCB description

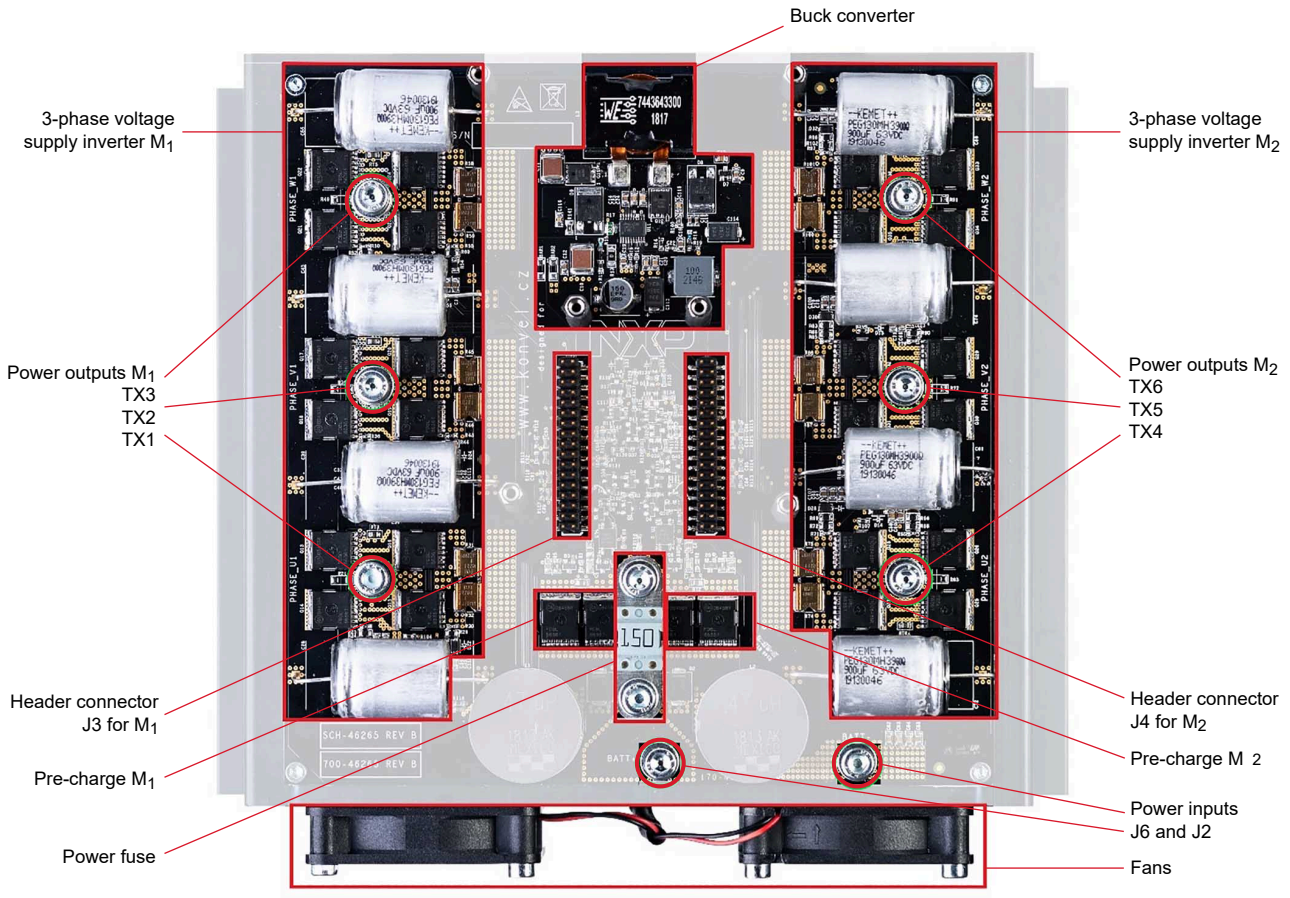


Figure 10. Power Stage board: block locations on PCB

The Power Stage board does not contain any jumper configuration for flexible change of circuit configuration or any test point due to direct and close connection of adapter board. The following sections summarize the on-board headers, connectors and their pinouts and signal meanings.

2.1.1 Power supply, power outputs and fuse holder

The Power Stage board input and output terminals are populated by power bolts, which reduce power losses during energy transfer. These power bolts have threaded metric hole M3 for wiring ring-eye terminals. Beside of input and output terminals, those power bolts are also used for fuse connection, which is placed between positive input terminal and both pre-charge circuits. Use appropriate wires and high conductivity terminals to connect your power source and motor load. In the following table, there is summary of power bolt connectors placed on Power Stage board.

Figure 11. Power Bolt

TE Connectivity part no. 225858-E

Table 2. Power input, output, and fuse terminals

Terminals	Signal name	Description
J1	P48V	Power supply (+) pin
J2	-VIN	Power supply (-) pin
J5	P48V	Fuse terminal A
J6	+VIN	Fuse terminal B
TX1	U1	Power Output Phase A
TX2	V1	Power Output Phase B
TX3	W1	Power Output Phase C
TX4	U2	Power Output Phase D
TX5	V2	Power Output Phase E
TX6	W2	Power Output Phase F

2.1.2 Header connector

The Power Stage board is populated by two header connectors in order to transfer signals between Adapter board and Power Stage board. In addition, header connectors provide robust connection of those two boards. The connectors pinout description is summarized in the following table.

Figure 12. Header connector for first and second MOSFET half-bridg

Matting connector: part no. SSW-117-01-S-D Fischer Electronic SL16 SMD 247

Table 3. Pinout description of header J3 for first 3-phase MOSFET half-bridge

Terminals	Signal name	Description
1	D_PWM1	Safe PWM signal phase A top
2	D_PWM2	Safe PWM signal phase A bottom
3	D_PWM3	Safe PWM signal phase B top
4	D_PWM4	Safe PWM signal phase B bottom
5	D_PWM5	Safe PWM signal phase C top
6	D_PWM6	Safe PWM signal phase C bottom
7	OVCI_1	Desaturation fault of pre-charge MOSFETs for first DC-link
8	/STO_0	Shutdown for first 3-phase MOSFET half-bridge
9	VDD	Digital power supply
10	ON_1	Enable of pre-charge for first 3-phase MOSFET half-bridge
11	U1_SENSE	BEMF_A
12	U1_NTC	Temperature of Phase A
13	V1_SENSE	BEMF_B
14	V1_NTC	Temperature of Phase B
15	W1_SENSE	BEMF_C
16	W1_NTC	Temperature of Phase C
17	VBAT_SENSE	Battery voltage
18	PRECHARGE1_NTC	Temperature of pre-charge MOSFETs for first 3-phase MOSFET half-bridge
19	VFW1_SENSE	Forward voltage of first 3-phase MOSFET half-bridge
20	VDCL1_SENSE	DC-link voltage of first 3-phase MOSFET half-bridge
21	IU1_P	Phase A current (+) positive
22	IU1_N	Phase A current (-) negative
23	IV1_P	Phase B current (+) positive
24	IV1_N	Phase B current (-) negative
25	IW1_P	Phase C current (+) positive
26	IW1_N	Phase C current (-) negative
27	GNDA	Analog ground
28	GNDA	Analog ground
29	GND	Digital ground
30	GND	Digital ground
31	VoBU	Buck converter output voltage
32	Vo	Output voltage of Buck or Flyback converter
33	VoBU	Buck converter output voltage
34	Vo	Output voltage of Buck or Flyback converter

Table 4. . Pinout description of header J4 for second 3-phase MOSFET half-bridge

Terminals	Signal name	Description
1	D_PWM6	Safe PWM signal phase D top
2	D_PWM7	Safe PWM signal phase D bottom
3	D_PWM8	Safe PWM signal phase E top
4	D_PWM9	Safe PWM signal phase E bottom
5	D_PWM10	Safe PWM signal phase F top
6	D_PWM11	Safe PWM signal phase F bottom
7	OVCI_2	Desaturation fault of pre-charge MOSFETs for second DC-link
8	/STO_1	Shutdown for second 3-phase MOSFET half-bridge
9	VDD	Digital power supply
10	ON_2	Enable of pre-charge for second 3-phase MOSFET half-bridge
11	U2_SENSE	BEMF_D
12	U2_NTC	Temperature of Phase D
13	V2_SENSE	BEMF_E
14	V2_NTC	Temperature of Phase E
15	W2_SENSE	BEMF_F
16	W2_NTC	Temperature of Phase F
17	VBAT_SENSE	Battery voltage
18	PRECHARGE2_NTC	Temperature of pre-charge MOSFETs for second 3-phase half-bridge
19	VFW2_SENSE	Forward voltage of second 3-phase MOSFET half-bridge
20	VDCL2_SENSE	DC-link voltage of second 3-phase MOSFET half-bridge
21	IU2_P	Phase D current (+) positive
22	IU2_N	Phase D current (-) negative
23	IV2_P	Phase E current (+) positive
24	IV2_N	Phase E current (-) negative
25	IW2_P	Phase F current (+) positive
26	IW2_N	Phase F current (-) negative
27	GNDA	Analog ground
28	GNDA	Analog ground
29	GND	Digital ground
30	GND	Digital ground
31	VoBU	Buck converter output voltage
32	Vo	Output voltage of Buck or Flyback converter
33	VoBU	Buck converter output voltage
34	Vo	Output voltage of Buck or Flyback converter

2.2 Adapter board PCB description

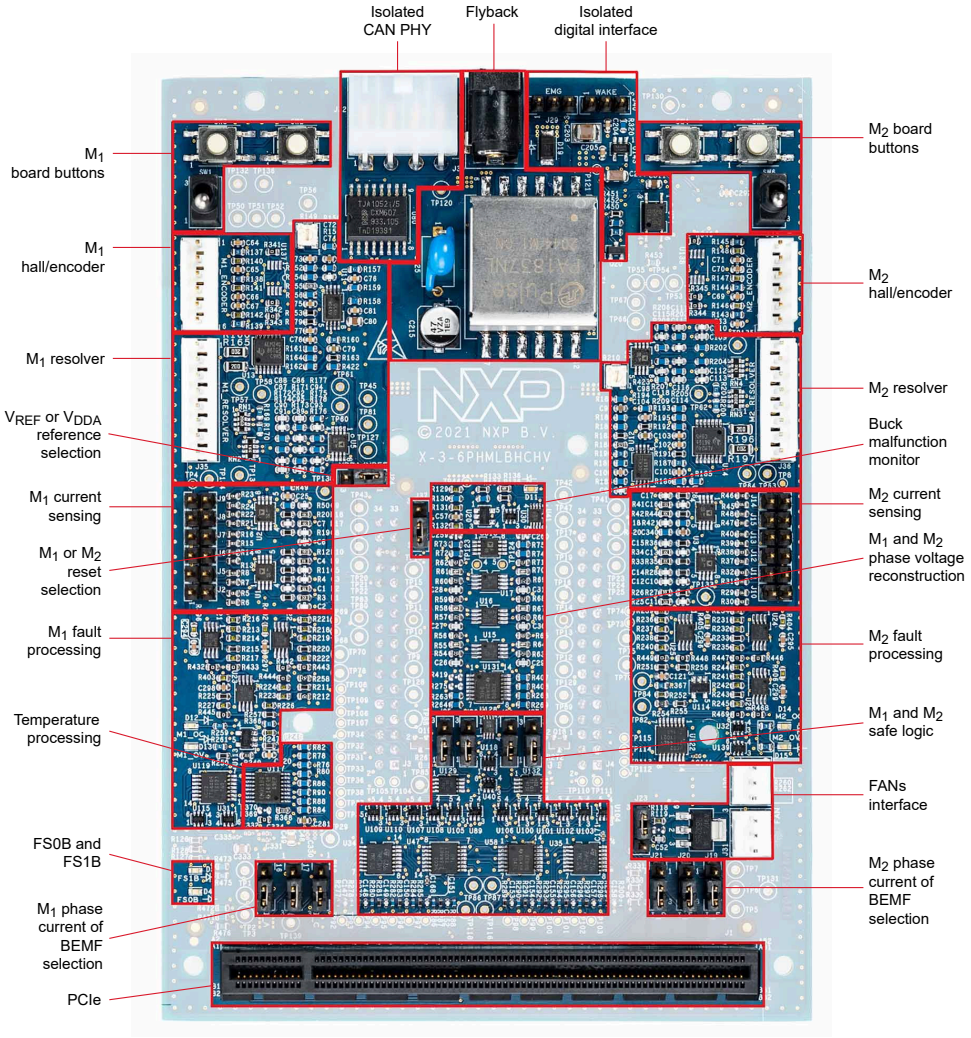


Figure 13. Adapter board: block locations on top side of PCB

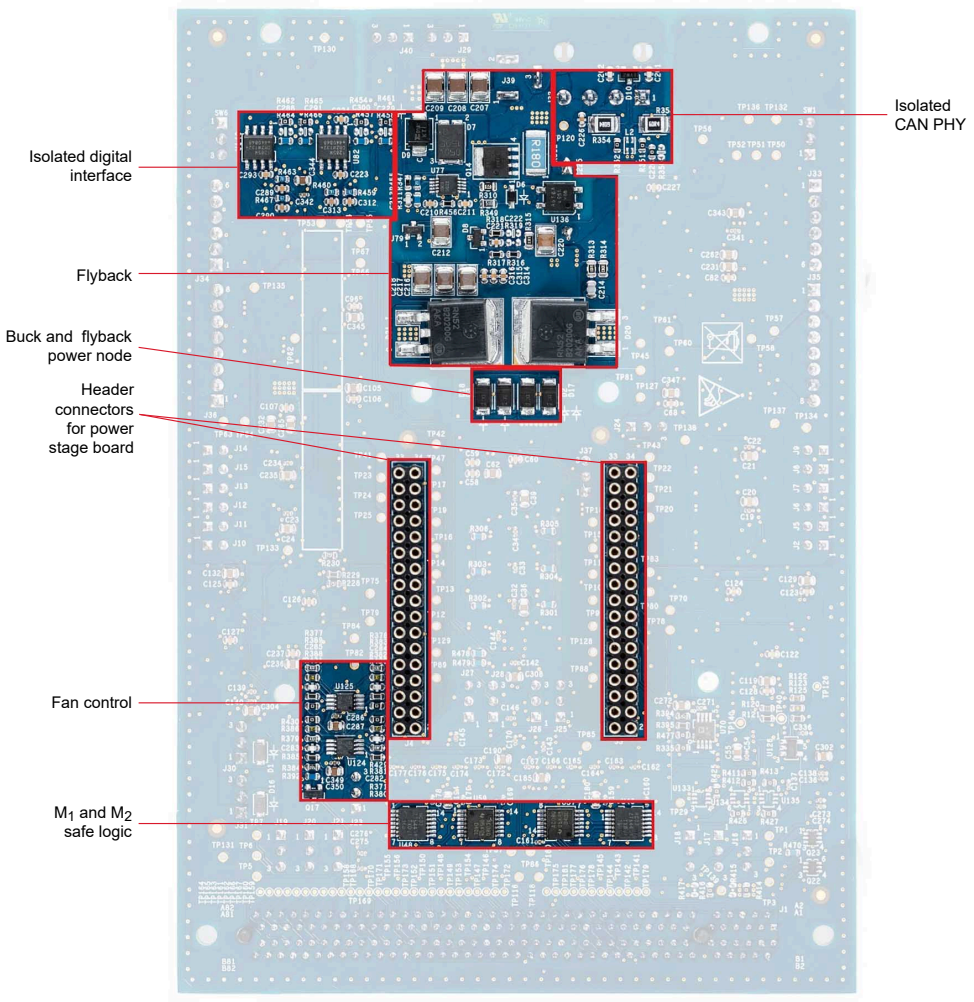


Figure 14. Adapter board: block locations on bottom side of PCB

2.2.1 Default jumper configuration

The Adapter board contains several jumpers and allows to change configuration of several circuits based on user requirements. Description and particular configuration of Adapter board jumpers are summarized in the following table.

Table 5. Adapter board jumper configuration

Jumper	Function	Setting	Description
J16, J17, J18	Phase current or BEMF voltage signals for first 3-phase MOSFET half-bridge	1-2	BEMF voltage measurement (Block commutation technique)
		2-3	**Phase current measurement (FOC technique) (default)**
J19, J20, J21	Phase current or BEMF voltage signals for second 3-phase MOSFET half-bridge	1-2	BEMF voltage measurement (Block commutation technique)
		2-3	**Phase current measurement (FOC technique) (default)**

Table 5. Adapter board jumper configuration*...continued*

J2, J5, J6, J7, J8, J9	Current measurement gain configuration of first 3-phase MOSFET half-bridge	**Open**	**Operational amplifiers gain is set to 50 (default)**
		Close	Operational amplifiers gain is set to 25
J10, J11, J12, J13, J14, J15	Current measurement gain configuration of second 3-phase MOSFET half-bridge	**Open**	**Operational amplifiers gain is set to 50 (default)**
		Close	Operational amplifiers gain is set to 25
J23	Fan control	1-2	Autonomous mode of fan control
		2-3	**Microcontroller mode of fan control (default)**
J37	Selection Reset 1 or Reset 2 for power supply fault monitor	1-2	Reset M1 resets latched fault of Buck monitor
		2-3	**Reset M2 resets latched fault of Buck monitor(default)**
J24	Fault logic reference voltage	**1-2**	**VREF is selected as reference voltage for fault logic (default)**
		2-3	VDDA is selected as reference voltage for fault logic
J25	First 3-phase half-bridge safe state activation (by fault logic)	**1-2**	**Safe open activated by operational faults (default)**
		2-3	Safe short activated by operational faults
J26	First 3-phase half-bridge safe state activation (by superior system)	1-2	Safe short activated by superior system
		2-3	**Safe open activated by superior system (default)**
J27	Second 3-phase half-bridge safe state activation (by fault logic)	**1-2**	**Safe open activated by operational faults (default)**
		2-3	Safe short activated by operational faults
J28	Second 3-phase half-bridge safe state activation (by superior system)	1-2	Safe short activated by superior system
		2-3	**Safe open activated by superior system (default)**

2.2.2 Socket connector

The Adapter board is populated by two socket connectors in order to transfer signals of both 3-phase MOSFET half-bridges separately. Signals are transferred in between Power Stage board and Adapter board. The connector pinout description is summarized in the following table.

Figure 15. Socket connector for first and second 3-phase MOSFET half-bridge

Matting connector: Fischer Electronic SL16 SMD 247 Samtec part no. SSW-117-01-S-D

Table 6. Pinout description of socket connector J3 for first 3-phase MOSFET half-bridge

Terminals	Signal name	Description
1	D_PWM1	Safe PWM signal phase A top
2	D_PWM2	Safe PWM signal phase A bottom
3	D_PWM3	Safe PWM signal phase B top
4	D_PWM4	Safe PWM signal phase B bottom
5	D_PWM5	Safe PWM signal phase C top
6	D_PWM6	Safe PWM signal phase C bottom
7	OC_DCL_M1	Desaturation fault of pre-charge MOSFETs for first DC-link
8	/STO_0	Shutdown for first 3-phase MOSFET half-bridge
9	MCU_VDD	Digital power supply
10	S_ON_M1	Enable of pre-charge for first 3-phase MOSFET half-bridge
11	U1_SENSE	BEMF_A
12	U1_NTC	Temperature of Phase A
13	V1_SENSE	BEMF_B
14	V1_NTC	Temperature of Phase B
15	W1_SENSE	BEMF_C
16	W1_NTC	Temperature of Phase C
17	VBAT_SENSE	Battery voltage
18	PRECHARGE_M1_NTC	Temperature of pre-charge MOSFETs for first 3-phase MOSFET half-bridge
19	VFW_M1_SENSE	Forward voltage of first 3-phase MOSFET half-bridge
20	VDCL_M1_SENSE	DC-link voltage of first 3-phase MOSFET half-bridge
21	IU1_P	Phase A current (+) positive
22	IU1_N	Phase A current (-) negative
23	IV1_P	Phase B current (+) positive
24	IV1_N	Phase B current (-) negative
25	IW1_P	Phase C current (+) positive
26	IW1_N	Phase C current (-) negative
27	GNDA	Analog ground
28	GNDA	Analog ground
29	GND	Digital ground
30	GND	Digital ground
31	VoBU	Buck converter output voltage
32	Vo	Output voltage of Buck or Flyback converter
33	VoBU	Buck converter output voltage
34	Vo	Output voltage of Buck or Flyback converter

Table 7. Pinout description of socket J4 for second 3-phase MOSFET half-bridge

Terminals	Signal name	Description
1	D_PWM6	Safe PWM signal phase D top
2	D_PWM7	Safe PWM signal phase D bottom
3	D_PWM8	Safe PWM signal phase E top
4	D_PWM9	Safe PWM signal phase E bottom
5	D_PWM10	Safe PWM signal phase F top
6	D_PWM11	Safe PWM signal phase F bottom
7	OC_DCL_M2	Desaturation fault of pre-charge MOSFETs for second DC-link
8	/STO_1	Shutdown for second 3-phase MOSFET half-bridge
9	MCU_VDD	Digital power supply
10	S_ON_M2	Enable of pre-charge for second 3-phase MOSFET half-bridge
11	U2_SENSE	BEMF_D
12	U2_NTC	Temperature of Phase D
13	V2_SENSE	BEMF_E
14	V2_NTC	Temperature of Phase E
15	W2_SENSE	BEMF_F
16	W2_NTC	Temperature of Phase F
17	VBAT_SENSE	Battery voltage
18	PRECHARGE_M2_NTC	Temperature of pre-charge MOSFETs for second 3-phase half-bridge
19	VFW_M2_SENSE	Forward voltage of second 3-phase MOSFET half-bridge
20	VDCL_M2_SENSE	DC-link voltage of second 3-phase MOSFET half-bridge
21	IU2_P	Phase D current (+) positive
22	IU2_N	Phase D current (-) negative
23	IV2_P	Phase E current (+) positive
24	IV2_N	Phase E current (-) negative
25	IW2_P	Phase F current (+) positive
26	IW2_N	Phase F current (-) negative
27	GNDA	Analog ground
28	GNDA	Analog ground
29	GND	Digital ground
30	GND	Digital ground
31	VoBU	Buck converter output voltage
32	Vo	Output voltage of Buck or Flyback converter
33	VoBU	Buck converter output voltage
34	Vo	Output voltage of Buck or Flyback converter

2.2.3 PCIe connector – socket

The purpose of this connector is to connect Adapter board and Controller board to each other and ensure sufficient mechanical robustness. High number of ports allows to transfer numerous analogs, digital or power supply signals. The pinout description of this connector is compressed and summarized in the following table.

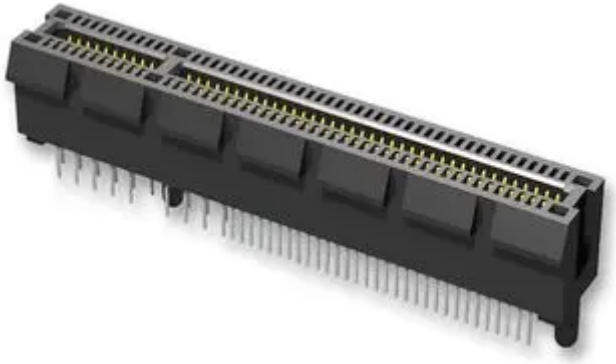


Figure 16. PCIe female connector

Amphenol ICC part no. 10082378-11113TLF

Table 8. Pinout description of PCIe J1 female connector

Terminals	Signal name	Description
B1	VREF	Reference voltage
B2, B11, B82, A2, A11, A82	GNDA	Analog ground
B3, B74, B81, A6, A7, A10, A77-79	Analog input	Spare analog inputs
B4	V_DCL_M1	DC-link voltage of first 3-phase MOSFET half-bridge
B5	V_FW_M1	Forward voltage of first 3-phase MOSFET half-bridge
B6	V_BAT	Battery voltage
B7-9	BEMF_U1/V1/W1	BEMF voltages of first motor
B10	TEMP	Temperature of power stage
B12	MCU_SUP	Voltage for specific MCU ports
B13, B32, B51, A13, A51	GND	Digital ground
B14-16	HALL_A1/B1/C1 – PH_A1, PH_B2, INDEX1	Hall/Encoder signals of first motor
B17-18, B34, B38-39, B41, B45, B50, B55, B64-69, B72-73	Not connected	N/A
B19, A8, A9	EXC_M1, SIN_M1, COS_M1	Resolver excitation and sin/cos signals for first motor configuration
B20, A31, A32	SW_RUN/UP/DOWN_M1	Application control signals for first motor configuration
B21-24	MISO/MOSI/SCK/SS	SPI signals (not applicated in 48V platform)

Table 8. Pinout description of PCIe J1 female connector*...continued*

Terminals	Signal name	Description
B25, A69	SBC_FS0B/FS1B	Fault safe signals of SBC
B26-27	SCI_TX/SCI_RX	Serial communication (not applicated in 48V platform)
B28	SW_ON_M1	Enable of DC-link pre-charge for first 3-phase MOSFET half-bridge
B29	DRV_ON_M1	Enable of gate-drivers for first 3-phase MOSFET half-bridge
B30, A29	BUCK_FAULT_L, BUCK_FAULT	Fault of Buck converter: latched and non-latched
B31	Vo	Output voltage of Buck or Flyback converter
B33, A33	CAN_RX, CAN_TX	CAN receive and transmit signals for isolated CAN PHY
B35-37	HALL_A2/B2/C2 – PH_A1 PH_B2, INDEX2	Hall/Encoder signals of second motor
B40, A80, A81	EXC_M2, SIN_M2, COS_M2	Resolver excitation and sin/cos signals for second motor
B42-44	A1-3	Temperature multiplexor control signals
B46	MCU_RUN	Control of fan by microcontroller
B47-49	SW_RUN/UP/DOWN_M2	Application control signals for second motor configuration
B52	M2_RESET	Reset of latched faults for second motor configuration
B53	DRV_ON_M2	Enable of gate-drivers for second 3-phase MOSFET half-bridge
B54	SW_ON_M2	Enable of DC-link pre-charge for second 3-phase MOSFET half-bridge
B56-58, A59-61	TRG4/5/6/3/2/1	MCU trigger signals (not used in 48V system)
B59-61	SBC_WAKE1, SBC_IO2/3	SBC input ports (IO3 – not used in 48V system)
B62-63, B70-71	I/O_28/29, GPIO2/4	Input/Output ports (not used in 48V system)
B75	V_DCL_M2	DC-link voltage of second 3-phase MOSFET half-bridge
B76	V_FW_M2	Forward voltage of second 3-phase MOSFET half-bridge
B78-80	BEMF_U2/V2/W2	BEMF voltages for second motor
A1	VDDA	Supply voltage for analog circuitry
A3-5	I_PHA/B/C – BEMF_U1/V1/W1	Phase currents or BEMF voltages of first motor configuration
A12	VDD	Supply voltage for digital circuitry
A14-A21	PWM1-6, PWM13-14	PWM signals for first 3-phase MOSFET half-bridge
A22-24	PHA, PHB, PHC	Phase voltage digital signals of first motor
A26-28	OC/OV/OC_DCL_M1	Latched faults of first motor configuration
A30	M1_RESET	Reset of latched faults for first motor configuration
A35-42	PWM7-12, PWM18-19	PWM signals for second 3-phase MOSFET half-bridge
A43-45	PHD, PHE, PHF	Phase voltage digital signals of second motor
A47-49	OC/OV/OC_DCL_M2	Latched faults for second motor configuration
A50	OT	Over-temperature fault

Table 8. Pinout description of PCIe J1 female connector...*continued*

Terminals	Signal name	Description
A52-57	TM13-18	Spare timer inputs (not used in 48V system)
A68	KL15	Ignition switch
A70	FAN_CTRL	Monitoring of autonomous control of fan
A71-73	APP_LED2/3/1	Application LED signals (not used in 48V system)
A74-76	I_PHD/E/F – BEMF_U2/V2/W2	Phase currents or BEMF voltages of second motor configuration

2.2.4 Fan connector

Adapter board has an interface, which is intended to power two external fans. External fans actively support cooling of Power Stage board. There are two connectors for two external fans, which are connected to the same signals. The pinout description is summarized in the following table.

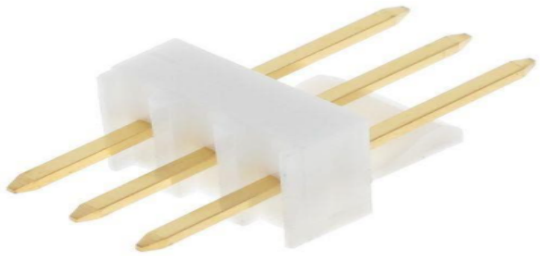


Figure 17. Header connector for external Fan

Mating connector: part No. MX-22-01-3037 Molex part no. 22-23-2031

Table 9. Pinout description of fan connectors J30 and J31

Terminals	Signal name	Description
1	Positive (+)	Positive pole
2	Negative (-)	Negative pole
3	NC	N/A

2.2.5 Rotor position sensors interface

There are two types of interfaces for rotor position sensors. Hall/Encoder rotor position interface utilizes connector with 6 pins, which pinout description is summarized in Table 10. Resolver position interface utilizes connector with 8 pins, which pinout description is summarized in Table 11. The Adapter board contains two sets of resolver and Hall/Encoder rotor position sensor interfaces to support dual motor control operation.

Figure 18. Hall/Encoder sensor connector

Mating connector: part No.22-01-2061 Molex part no. 22-27-2061

Table 10. Pinout description of Hall/Encoder connectors

Terminals	Signal name	Description
J33 connector		
1	VDD	Positive (+) pin
2	GND	Negative (-) pin
3	HALL_A/PH_A	Input signal Hall A/Encoder Channel A
4	HALL_B/PH_B	Input signal Hall B/ Encoder Channel B
5	HALL_C/INDEX1	Input signal Hall C/ Encoder Index 1
6	Not connected	N/A
J34 connector		
Terminals	**Signal name**	**Description**
1	VDD	Positive (+) pin
2	GND	Negative (-) pin
3	HALL_D/PH_D	Input signal Hall D/Encoder Channel D
4	HALL_E/PH_E	Input signal Hall E/ Encoder Channel E
5	HALL_F/INDEX2	Input signal Hall F/ Encoder Index 2
6	Not connected	N/A

Figure 19. Resolver sensor connector

Mating connector: part No.22-01-2087 Molex part no. 22-23-2031

Table 11. Pinout description of Resolver connectors

Terminals	Signal name	Description
J35 connector		
1	RES_GENP_M1	Square signal, 10kHz output for first motor configuration
2	RES_GENM_M1	
3	RES_SIN_M1	Resolver sine signal input for first motor
4	RES_SIN_REF_M1	
5	RES_COS_M1	Resolver cosine signal input for first motor
6	RES_COS_REF_M1	
7	GND	Ground
8	VDDA	Analog power supply
J36 connector		
1	RES_GENP_M2	Square signal 10kHz output for second motor configuration
2	RES_GENM_M2	
3	RES_SIN_M2	Resolver sine signal input for second motor
4	RES_SIN_REF_M2	
5	RES_COS_M2	Resolver cosine signal input for second motor
6	RES_COS_REF_M2	
7	GND	Ground
8	VDDA	Analog power supply

2.2.6 Isolated layer interface

Adapter board isolated layer contains flyback converter as a redundant power supply source. This converter is supplied from external 12 V voltage source by Center Positive Barrel type connector with outer diameter 5.5mm, inner diameter 2.1mm. Supervisor system is connected to system by means of two 3-pin header connectors (Figure 21), which allow to transfer control and wake-up signals. CAN communication interface uses Molex type of connector (Figure 22). The pinout descriptions of all mentioned connectors are summarized in tables below:

Figure 20. Power supply barrel connector for flyback converter

Mating connector: KLDX-PA-0202-A-LT Wurth Electronic part no. 694106301002

Table 12. Pinout description of power supply jack J39 for flyback converter

Terminals	Signal name	Description
1	T30	Positive input pin
2	GND	Digital isolated ground
3	GND	Digital isolated ground

Figure 21. Header connector for external digital signals and Ignition signal

Samtec part no. TSW-103-14-G-S

Table 13. Pinout description of header connectors for external control signals

Terminals	Signal name	Description
J29 connector		
1	EMG_M1_EXT	Energency signal for first motor configuration
2	EMG_M2_EXT	Energency signal for second motor configuration
3	KL15_EXT	Ignition signal
J40 connector		
Terminals	**Signal name**	**Description**
1	GND	Digital isolated ground
2	WAKE1	First wake up signal
3	WAKE2	Second wake up signal

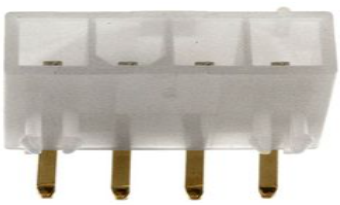


Figure 22. CAN connector of isolated CAN communication interface

Mating connector: part No. 39-01-4040 Molex part no. 39-30-3047

Table 14. Pinout description of CAN connector J32

Terminals	Signal name	Description
1	CAN_H	CAN_HI signal
2	CAN_L	CAN_LI signal
3	GND	Isolated digital ground
4	Not connected	N/A

2.2.7 Test points of Adapter board

The below summarizes test points of Adapter board.

Table 15. Adapter board test points

Test point	Signal name	Description
TP1, TP2, TP3	I_PHA, I_PHB, I_PHC	Phase currents for first motor configuration
TP4, TP8	VA_REF_M1, VA_REF_M2	Reference for bidirectional current measurement for first and second motor configuration
TP5, TP6, TP7	I_PHD, I_PHE, I_PHF	Phase currents for second motor configuration
TP9, TP10, TP11	U1_SENSE, V1_ SENSE, W1_SENSE	BEMF voltages of first motor
TP12, TP13, TP14	U2_SENSE, V2_ SENSE, W2_SENSE	BEMF voltages of second motor
TP18	VDCL_M1_SENSE	DC-link voltage of first 3-phase MOSFET half-bridge
TP19	VDCL_M2_SENSE	DC-link voltage of second 3-phase MOSFET half-bridge
TP20, TP21, TP22	PH_V_A, PH_V_B, PH_V_C	Phase voltage digital signals of first motor
TP23, TP24, TP25	PH_V_D, PH_V_E, PH_V_F	Phase voltage digital signals of second motor
TP123, TP124	V_REF_M1, V_REF_M2	Voltage references for phase voltage reconstruction of first and second motor
TP29	TEMP_OUT	Temperature of power stage
TP31, TP32, TP33	U1_TEMP, V1_TEMP, W1_TEMP	Temperature of first 3-phase MOSFET half-bridge
TP34	PCH1_TEMP	Temperature of DC-link pre-charge MOSFETs for first 3-phase MOSFET half-bridge
TP35, TP36, TP37	U2_TEMP, V2_TEMP, W2_TEMP	Temperature of second 3-phase MOSFET half-bridge
TP38	PCH2_TEMP	Temperature of DC-link pre-charge MOSFETs for second 3-phase MOSFET half-bridge
TP140	VDD_AUX_REF	Voltage reference for temperature measurement
TP40	V_TH_REF_OT	Voltage reference for over-temperature monitoring
TP126	OT	Over-temperature fault

Table 15. Adapter board test points*...continued*

Test point	Signal name	Description
TP41	V_Buck	Buck output voltage
TP42	V_Flyback	Flyback output voltage
TP43	Vo	Output voltage of Buck or Flyback converter
TP44	V_Buck Scaled	Scaled voltage of Buck converter
TP45	BUCK_FAULT	Fault of Buck converter: non-latched
TP47	BUCK_FAULT_L	Fault of Buck converter: latched
TP130-132	GND	Digital ground
TP133-135	GNDA	Analog ground
TP136	VDD	Supply voltage for digital circuitry
TP137	VDDA	Supply voltage for analog circuitry
TP138	VREF	Reference voltage
TP139	MCU_SUP	Voltage for specific MCU ports
TP50, TP51, TP52	HALL_A1, HALL_B1, HALL_C1	Hall/Encoder signals of first motor
TP53, TP54, TP55	HALL_A2, HALL_B2, HALL_C2	Hall/Encoder signals of second motor
TP56	RES_GEN_M1 Scaled	Scaled resolver excitation signal generated by microcontroller for first motor configuration
TP57, TP58	RES_GENP_M1, RES_GENM_M1	Resolver excitation signals for first motor configuration
TP60, TP61	M1_SIN, M1_COS	Resolver sin/cos signals for first motor configuration
TP62	RES_GEN_M2 Scaled	Scaled resolver excitation signal generated by microcontroller for second motor configuration
TP63, TP64	RES_GENP_M2, RES_GENM_M2	Resolver excitation signals for second motor configuration
TP66, TP67	M2_SIN, M2_COS	Resolver sin/cos signals for second motor configuration
TP68, TP69	V_TH_M1, V_TL_M1	Upper and lower threshold of phase over-current detection of first motor configuration
TP70	OC_M1	Over-current fault of first motor configuration: non-latched
TP73, TP74	V_TH_M2, V_TL_M2	Upper and lower threshold of phase over-current detection of second motor configuration
TP75	OC_M2	Over-current fault of second motor configuration: non-latched
TP78	OV_M1	Over-voltage fault of first motor configuration: non-latched
TP79	OV_M2	Over-voltage fault of second motor configuration: non-latched
TP80, TP83	OC_M1_L, OV_M1_L	Over-current and Over-voltage faults of first motor configuration: latched
TP82, TP84	OC_M2_L, OV_M2_L	Over-current and Over-voltage faults of second motor configuration: latched
TP81, TP127	M1_RESET, M2_RESET	Reset signals for first and second motor configuration
TP85	FS0B or FS1B	Fault safe signals of SBC

Table 15. Adapter board test points*...continued*

Test point	Signal name	Description
TP86, TP87	SAFE_SHORT_M1, SAFE_SHORT_M2	Safe short signals for first and second motor configuration
TP88, TP89	/STO_0, /STO_1	Shutdown signals for first and second motor configuration
TP128, TP129	S_SW_ON_M1, S_SW_ON_M2	Enable of DC-link pre-charge MOSFETs for first and second 3-phase MOSFET half-bridge
TP92-97	PWM1-6	PWM signals for first 3-phase MOSFET half-bridge
TP98-103	PWM7-12	PWM signals for second 3-phase MOSFET half-bridge
TP104-109	S_PWM1-6	Safe PWM signals for first 3-phase MOSFET half-bridge
TP110-115	S_PWM7-12	Safe PWM signals for second 3-phase MOSFET half-bridge
TP116, TP117	SAFE_OPEN_M2, SAFE_OPEN_M1	Safe open signals for second and first motor configuration
TP120	T30	12V battery input voltage
TP121	5V_ISO	5V output voltage for digital circuits of isolated layer
TP141-143, TP161-163, TP179, TP164, TP165, TP166	AN7, AN9, AN15, AN22, AN24, AN26, ADC0_ P1, AN31, AN23, AN17	Spare analog inputs
TP15	V_FW_M1	Forward voltage of first 3-phase MOSFET half-bridge
TP16	V_FW_M2	Forward voltage of second 3-phase MOSFET half-bridge
TP17	V_BAT	Battery voltage
TP144-147	PWM13, PWM14, PWM18, PWM19	Spare PWM signals
TP148-153	TM13-18	Spare timer signals
TP154-156, TP172-TP174	TRG3-1, TRG6-4	MCU trigger signals
TP158-160	APP_LED2, APP_ LED3, APP_LED1	Application LED signals
TP175-TP178	SS, SCK, MOSI, MISO	SPI signals
TP180-181	SCI_TX, SCI_RX	Serial communication
TP169-170	I/O_29, I/O_28	Input/Output ports
TP171	SBC_IO3	SBC input ports
TP167-168	GPIO4, GPIO2	Input/Output ports

2.3 Controller board PCB description

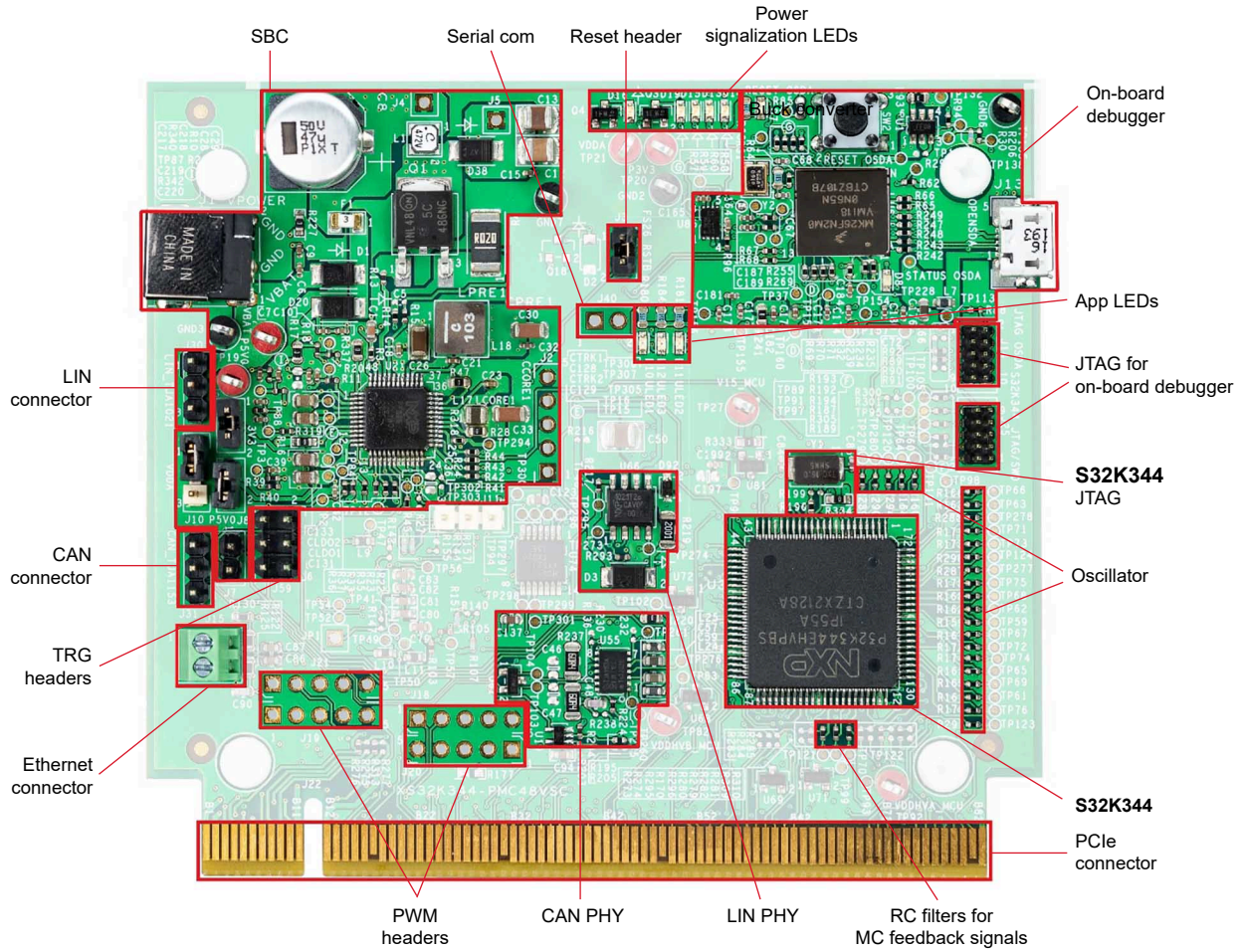


Figure 23. Controller board: block locations on top side of PCB

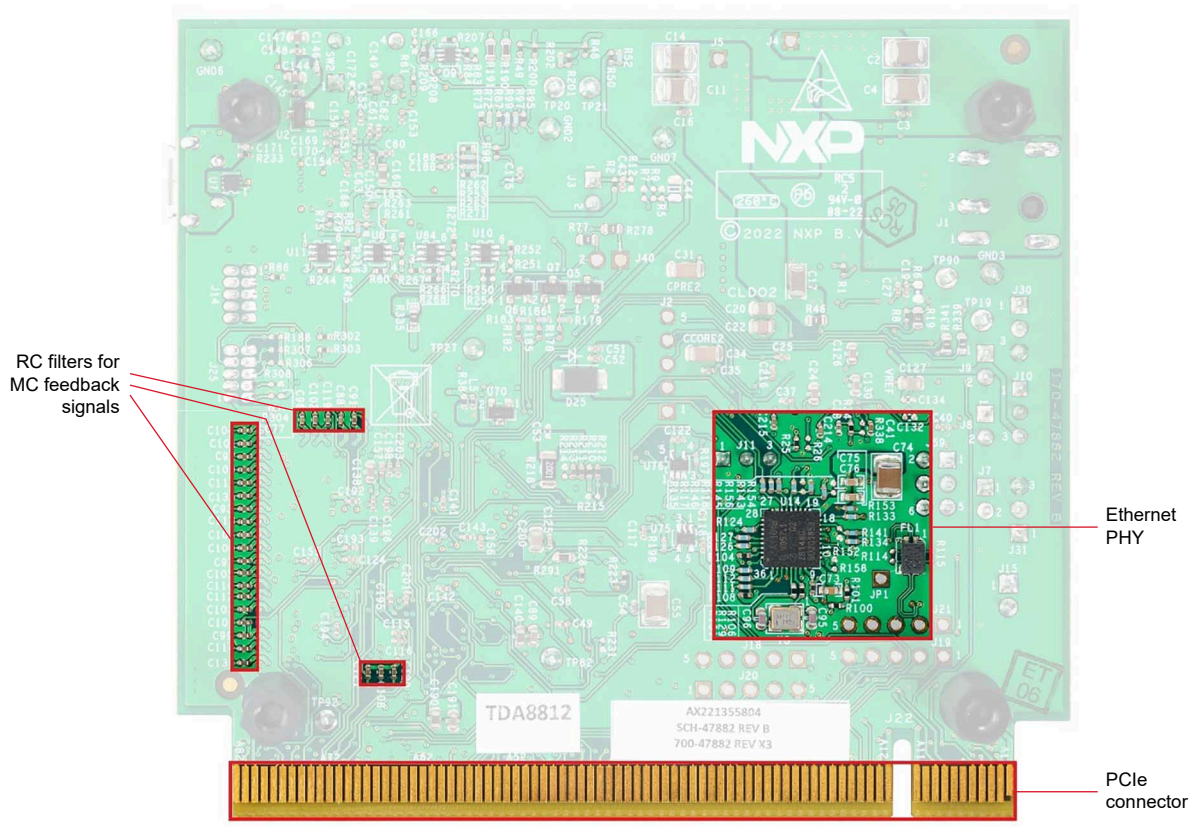


Figure 24. Controller board: block locations on bottom side of PCB

2.3.1 Default jumper configuration

The Controller board contains several jumpers and allows to change configuration based on user requirements. Description and particular configuration of Controller board jumpers are summarized in the following table.

Table 16. Controller board jumper configuration

Jumper	Function	Setting	Description
J7	Connection/disconnection of reset signal in between MCU and SBC	**Open**	**Reset signal isn't connecting microcontroller and SBC chip (default)**
		Close	Reset signal is connecting microcontroller and SBC chip.
J8	LDO1 regulator connection	Open	LDO1 regulator is not connected to the VDD rail
		Close	**LDO1 regulator is connected to the VDD rail (default)**
J9	LDO2 regulator connection	Open	LDO2 regulator is not connected to the P3V3 rail
		Close	**LDO2 regulator is connected to the P3V3 rail (default)**
J10	TRK1 or TRK2 voltage source connection	**1-2**	**TRK1 voltage source is connected to the VDDA voltage rail (default)**
		2-3	TRK2 voltage source is connected to the VDDA voltage rail

Table 16. Controller board jumper configuration*...continued*

J3	SBC debug signal connection	Open	Debug pin of SBC is not powered
		Close	**Debug pin of SBC is powered (default)**
J11	Ethernet physical layer configuration	1-2	Master operation of ethernet physical layer
		2-3	**Slave operation of ethernet physical layer (default)**

2.3.2 PCIe connector – card

This card connector enables connection to PCIe connector at Adapter board. High number of connector pins is needed for transferring numerous analogs, digital and power supply signals. The pinout description of this connector is summarized in the following table.

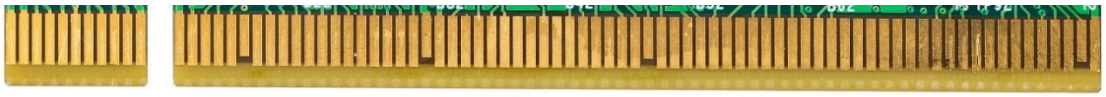


Figure 25. PCIe x16 card (male) connector

Table 17. Pinout description of PCIe male connector J22

Terminals	Signal name	Description
B1	VREF	Reference voltage
B2, B11, B82, A2, A11, A82	GNDA	Analog ground
B3, B77, B81, A77-78	Analog input	Spare analog inputs
B4	M1_DCBV	DC-link voltage of first 3-phase MOSFET half-bridge
B5	M1_VFW	Forward voltage of first 3-phase MOSFET half-bridge
B6	VBAT_48V	Battery voltage
B7-9	BEMF_A/B/C	BEMF voltages for first motor
B10	V_TEMP	Temperature of power stage
B12	P3V3	3.3V power supply
B13, B51, A13, A51	GND	Digital ground
B32	GNDP	Digital ground - power
B14-16	HALL_A/B/C – ENC_A/B, ENC_INDEX1	Hall/Encoder signals of first motor
B17-18, B34, B38-39, B41, B45, B50, B55, B63-69, B73-74, A6-7, A10, A25, A34, A46, A58, A62-67, A79	Not connected	N/A
B19, A8, A9	M1_RES_EXC, M1_ RES_SIN, M1_RES_COS	Resolver excitation and sin/cos signals for first motor
B20, A31, A32	M1_SW_RUN/UP/DOWN	Application control signals for first motor configuration
B21-24	GD3000/3100_SOUT/SIN/SCK/PCS	SPI signals (not applicated in 48V platform)
B25, A69	SBC_FS0B/FS1B	Fault safe signals of SBC
B26-27	LP_UART_RX/TX	Serial communication (not applicated in 48V platform)

Table 17. Pinout description of PCIe male connector J22 *...continued*

Terminals	Signal name	Description
B28	M1_SW_ON	Enable of DC-link pre-charge MOSFETs for first motor configuration
B29	M1_DRV_EN	Enable of gate-drivers for first 3-phase MOSFET half-bridge
B30, A29	BUCK_FAULT_L, BUCK_FAULT	Fault of Buck converter: latched and non-latched
B31	Vo_PCIe	Output voltage of Buck or Flyback converter
B33, A33	ISO_CAN_RX, ISO_CAN_TX	CAN receive and transmit signals for isolated CAN PHY
B35-37	HALL_D/E/F – ENC_D/E/INDEX2	Hall/Encoder signals of second motor
B40, A80, A81	M2_RES_EXC, M2_ RES_SIN, M2_RES_COS	Resolver excitation and sin/ cos signals for second motor
B42-44	A1-3	Temperature multiplexor control signals
B46	MCU_RUN	Fan control by microcontroller
B47-49	M2_SW_RUN/UP/DOWN	Application control signals for second motor configuration
B52	M2_RESET	Reset of latched faults for second motor configuration
B53	M2_DRV_EN	Enable of gate-drivers for second 3-phase MOSFET half-bridge
B54	M2_SW_ON	Enable of DC-link pre-charge MOSFETs for second motor configuration
B56-58	TRG4/5/6	MCU trigger signals
A59-61	TRG3/2/1	MCU trigger signals
B59-61	SBC_WAKE1, SBC_GPIO1/2	SBC input/output ports
B62, B70-72	I/O_28/29, GPIO2/4	Input/Output ports (not used in 48V system)
B75	M2_DCBV	DC-link voltage of second 3-phase MOSFET half-bridge
B76	M2_VFW	Forward voltage of second 3-phase MOSFET half-bridge
B78-80	BEMF_D/E/F	BEMF voltages for second motor
A1	VDDA	Supply voltage for analog circuitry
A3-5	BEMF_A/B/C_PHA/B/C_I	Phase currents or BEMF voltages of first motor configuration
A12	VDD	Supply voltage for digital circuitry
A14-A19	PWMA/B/C_HS/LS	PWM signals for first 3-phase MOSFET half-bridge
A20-21	LCU1_OUT0/1	Additional PWM signals
A22-24	PH_A/B/C_REC	Phase voltage digital signal of first motor
A26-28	M1_OC/OV/OC_DCL_FAULT	Latched faults of first motor configuration
A30	M1_RESET	Reset of latched faults for first motor configuration
A35-40	PWMD/E/F_HS/LS	PWM signals for second 3-phase MOSFET half-bridge
A41-42	LCU1_OUT2/3	Additional PWM signals

Table 17. Pinout description of PCIe male connector J22 *...continued*

Terminals	Signal name	Description
A43-45	PH_D/E/F_REC	Phase voltage digital signal of second motor
A47-49	M2_OC/OV/OC_DCL_FAULT	Latched faults of second motor configuration
A50	OT_FAULT	Over-temperature fault
A52-57, A62-63	eMIOS_0_CH [4/5/7/6/1/3]_G eMIOS_1_CH [7/8]_H/X	Spare timer outputs (not used in 48V system)
A68	SBC_KL15	Ignition switch
A70	FAN_CTRL	Monitoring autonomous fan control
A71-73	MCU_LED2/3/1 – APP_LED2/3/1	APP LEDs signals (not used in 48V system)
A74-76	BEMF_D/E/F_PHD/E/F_I	Phase currents or BEMF voltages of second motor configuration

2.3.3 Communication Interfaces

Controller board is equipped with several communication interfaces like CAN, LIN, Ethernet or Serial communication interface (SCI). The following subsection will describe all these interfaces.

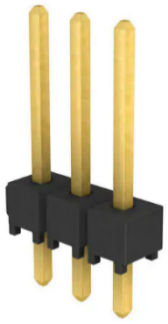


Figure 26. CAN connector of non-isolated CAN communication interface

Würth Elektronik part no. 61300311121

Table 18. Pinout description of CAN connector J31

Terminals	Signal name	Description
1	CAN_H	CAN_Hi signal
2	CAN_L	CAN_Li signal
3	GND	Ground

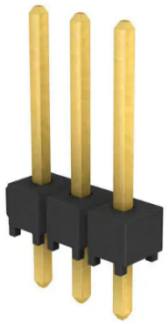


Figure 27. Header connector for LIN communication interface

Würth Elektronik part no. 61300311121

Table 19. Pinout description of header connector J30 for LIN communication interface

Terminals	Signal name	Description
1	VBAT	12V Battery voltage
2	LIN1_OUT	LIN data signal
3	GND	Ground

Figure 28. Terminal block connector for Ethernet communication interface

On Shore Technology Inc. part no. OSTVN02A150

Table 20. Pinout description of Ethernet connector J15

Terminals	Signal name	Description
1	TRX_N_CONN	- terminal for transmit/receive signal
2	TRX_P_CONN	+ terminal for transmit/receive signal

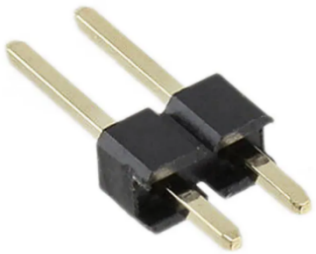


Figure 29. Header connector for SCI communication interface

Würth Elektronik part no. 61300211121

Table 21. Pinout description of header connector J40 for SCI communication interface

Terminals	Signal name	Description
1	OPEN_SDA_RX	Receive signal of SCI
2	OPEN_SDA_TX	Transmit signal of SCI

2.3.4 Debug Interfaces

Figure 30. Header connector for S32K344 JTAG debug interface

Samtec Inc. part no. FTS-105-01-F-D

Table 22. Pinout description of header connector J25 for S32K344 JTAG debug interface

Terminals	Signal name	Description
1	VCC	Power supply
2	JTAG_TMS/SWD_DIO	Test Mode select signal/ Bidirectional data signal
3	GND	Ground
4	JTAG_TCLK/SWD_CLK	Test Clock signal/ Clock signal
5	GND	Ground
6	JTAG_TDO	Test Data Out signal
7	KEY	Selectable voltage level
8	JTAG_TDI	Test Data In signal

Table 22. Pinout description of header connector J25 for S32K344 JTAG debug interface *...continued*

Terminals	Signal name	Description
9	GND	Ground
10	RESET_MCU	MCU Reset signal

Figure 31. Header connector of JTAG interface for on-board debugger

Samtec Inc. part no. FTS-105-01-F-D

Table 23. Pinout description of header connector J14 of JTAG interface for on-board debugger

Terminals	Signal name	Description
1	P3V3_SDA	Power supply
2	SDA_JTAG_TMS	Test Mode select signal
3	GND	Ground
4	SDA_JTAG_TCLK	Test Clock signal/ Clock signal
5	GND	Ground
6	SDA_JTAG_TDO	Test Data Out signal
7	Not connected	Selectable voltage level
8	SDA_JTAG_TDI	Test Data In signal
9	Not connected	Ground
10	SDA_RST_B	MCU Reset signal

Figure 32. USB connector for on-board debug interfacePower Bolt

Molex part no. 47589-0001

Table 24. Pinout description of USB connector J13 for on-board debug interface

Terminals	Signal name	Description
1	P5V0_OSDA	Power supply
2	OSDA_USB_DN	USB data +
3	OSDA_USB_DP	USB data -
4	OSDA_USB_ID	Determines default host (grounded)
5	GND	Ground

Figure 33. Header connector for PWM signals

Samtec part no. TSW-105-07-F-S

Table 25. Pinout description of header connectors J18-J21 for PWM signals

	Terminals	Signal name	Description
J18	1	LCU1_OUT0	Additional PWM signal
	2	LCU1_OUT1	Additional PWM signal
	3	LCU1_OUT2	Additional PWM signal
	4	LCU1_OUT3	Additional PWM signal
	5	GND	Ground
J19	1	PWMC_HS	PWM signal for phase C HS MOSFET
	2	PWMC_LS	PWM signal for phase C LS MOSFET
	3	PWMD_HS	PWM signal for phase D HS MOSFET
	4	PWMD_LS	PWM signal for phase C LS MOSFET
	5	GND	Ground
J20	1	PWMF_HS	PWM signal for phase F HS MOSFET
	2	PWMF_LS	PWM signal for phase F LS MOSFET
	3	PWME_HS	PWM signal for phase E HS MOSFET
	4	PWME_LS	PWM signal for phase E HS MOSFET
	5	GND	Ground

Table 25. Pinout description of header connectors J18-J21 for PWM signals *...continued*

	Terminals	Signal name	Description
J21	1	PWMA_HS	PWM signal for phase A HS MOSFET
	2	PWMA_LS	PWM signal for phase A LS MOSFET
	3	PWMB_HS	PWM signal for phase B HS MOSFET
	4	PWMB_LS	PWM signal for phase B HS MOSFET
	5	GND	Ground

Figure 34. Header connector for trigger signals

Samtec part no. TSW-103-07-F-D

Table 26. Pinout description of header connector J59 for trigger signals

Terminals	Signal name	Description
1	TRG1	TRG1 signal
2	TRG2	TRG2 signal
3	TRG3	TRG3 signal
4	TRG4	TRG4 signal
5	TRG5	TRG5 signal
6	TRG6	TRG6 signal

2.3.5 Power supply connector

Figure 35. Power supply barrel connector

CUI Devices part no. PJ-051A

Table 27. Pinout description of power supply jack connector J1

Terminals	Signal name	Description
1	VBAT	12V VBAT input power supply signal
2	GND	Ground
3	GND	Ground

2.3.6 Test points of Controller board

The below table summarizes test points of Controller board.

Table 28. Controller board test points

Test point	Signal name	Description
J4	VBATP	Input voltage of SBC
J5	VSUP	Boost output voltage
JP1	ENET_INH	Ethernet inhibit signal
TP2, TP3	SBC_FS0B, SBC_FS1B	Fault safe signals of SBC
TP4, TP6	SBC_KL15, SBC_WAKE1	Input wake-up signals of SBC: Ignition switch and wake1
TP12	FS26_VCORE	SBC output voltage: MCU supply voltage
TP15	FS26_VLDO1	SBC output voltage: LDO1
TP16	FS26_VLDO2	SBC output voltage: LDO2
TP19	VDD	Supply voltage for digital circuits
TP20	P3V3	Supply voltage for specific microcontroller ports
TP21	VDDA	Supply voltage for analog circuits
TP84	FS26_VMONEXT_1V	SBC monitor input signal
TP87, TP88	FS26_GPIO2, FS26_GPIO1	GPIO ports of SBC
TP294	AMUX	Multiplexed analog output signal of SBC
TP302, TP303	SBC_FCCU2, SBC_FCCU1	Fault Control Collection Unit signals 1 and 2
TP305	FS26_VPRE	Pre-regulator output voltage of SBC

Table 28. Controller board test points*...continued*

Test point	Signal name	Description
TP306	FS26_VTRK1	SBC output voltage: tracker 1
TP307	FS26_VTRK2	SBC output voltage: tracker 2
TP83	VDD_HV_B_MCU	Supply voltage of B voltage domain of S32K344 microcontroller
TP93	VDD_HV_A_MCU	Supply voltage of A voltage domain of S32K344 microcontroller
TP96	V25_MCU	Supply voltage of S32K344 microcontroller
TP99	V15_MCU	Supply voltage of S32K344 microcontroller
TP102	V11_MCU	Supply voltage of S32K344 microcontroller
GND2, GND3, GND6, GND7	GND	Digital ground
TP71, TP73, TP74	PTE0_BEMF_A, PTE1_ BEMF_B, PTE2_BEMF_C	Filtered BEMF voltages of first motor
TP67, TP59, TP75	PTE21_BEMF_D, PTE22_ BEMF_E, PTE25_BEMF_F	Filtered BEMF voltages of second motor
TP61	PTD30_V_TEMP	Filtered signal of power stage temperature
TP64	PTD1_M1_DCBV	Filtered signal of DC-link voltage of first 3-phase MOSFET half-bridge
TP69	PTD31_M1_V_FW	Filtered signal of forward voltage of first 3-phase MOSFET half-bridge
TP72	PTA14_M2_DCBV	Filtered signal of DC-link voltage of second 3-phase MOSFET half-bridge
TP70	PTD21_M2_V_FW	Filtered signal of forward voltage of second 3-phase MOSFET half-bridge
TP76	PTD29_V_BAT	Filtered signal of battery voltage
TP277, TP279	PTA12_M1_RES_COS, PTE10_M1_RES_SIN	Filtered resolver sin/cos signals for first motor configuration
TP278, TP280	PTE26_M2_RES_COS, PTE11_M2_RES_SIN	Filtered resolver sin/cos signals for second motor configuration
TP62, TP63, TP60	PTA13_BEMF_A/ PHA_I, PTA8_BEMF_B/PHB_I, PTA18_BEMF_C/PHC_I	Filtered phase currents or BEMF voltages of first motor
TP65, TP66, TP68	PTE6_BEMF_D/ PHD_I, PTA9_BEMF_ E/ PHE_I, PTE23_BEMF_F/ PHF_I	Filtered phase currents or BEMF voltages of second motor
TP120-124	PTD0_ADC0_P, PTD20_ADC0_ S22/PTD20_GPIO, PTD22_ ADC2_S18, PTD28_ADC1_ S22/KL15, PTA11_ADC1_S10	Spare analog input signals
TP89, TP91, TP95, TP97, TP98, TP100, TP101, TP105	JTAG_TDI, JTAG_TDO, (KEY), JTAG_TCLK, VDD_HV_A_MCU, GND, JTAG_TMS, JTAG_RST	S32K344 JTAG debug signals
TP295, TP296	M1_OC_FAULT, M1_OV_FAULT	Over-current and Over-voltage faults of first motor configuration: latched

Table 28. Controller board test points*...continued*

Test point	Signal name	Description
TP298, TP299	M2_OC_FAULT, M2_OV_FAULT	Over-current and Over-voltage faults of second motor configuration: latched
TP94	M1_OCDCL_FAULT	Desaturation fault of pre-charge MOSFETs for first motor configuration
TP297	BUCK_FAULT_L	Fault of Buck converter: latched
TP300	PTD5_M1_FAULT	Merged latched fault signal for first motor configuration
TP301	PTE3_M2_FAULT	Merged latched fault signal for second motor configuration
TP37	P3V3_SDA	Supply voltage of on-board debugger
TP38, TP113	P5V0_OSDA	USB supply voltage
TP44	SDA_RST_B	Reset signal of on-board debugger microcontroller
TP132	P5V0_OSDA_OUT	Supply voltage for power switch of on-board debugger
TP135, TP136	POWER_EN_R	Power enable signal of on-board debugger
TP137	P3V3_SDA	Reference voltage of on-board debugger microcontroller
TP138	VTRG_FAULT_B	Fault signal indication for on-board debugger
TP141	SDA_LVLRST_EN	Enable of reset for S32K344 microcontroller
TP142	SDA_RST_TGTMCU	Reset signal for S32K344 microcontroller
TP146	SDA_RST_TGTMCU	Control of manual reset of S32K344 microcontroller
TP150	VREF_OUT	Reference voltage of on-board debugger microcontroller
TP151	VDDIO_SDA	Supply voltage for voltage translator of on-board debugger
TP153-157, TP160	SDA_SWD_SCK, SDA_SWD_EN, SDA_SWD_DOUT, SDA_SWD_OE, SDA_SWD_DIN, SDA_SWD_SWO	Digital signal for on-board debugger
TP158, TP159	SDA_ADC0_CH0	Measured analog input signal of A voltage domain of S32K344 microcontroller
TP161, TP162	SDA_ADC1_CH0	Measured analog input signal of B voltage domain of S32K344 microcontroller
TP228	SDA_USB_P5V_SENSE	Measured analog input signal of USB voltage
TP41	ENET_WAKE_LED_TJA1101	Wake in out signal for ethernet physical layer
TP47	VDDIO_ENET	Supply voltage for Ethernet physical layer
TP49	VBAT_TJA1101	Supply voltage for Ethernet physical layer
TP50	VDDD_3V3_ENET	Supply voltage for Ethernet physical layer
TP52, TP54	TRX_P_CONN, TRX_N_CONN	+- terminals for transmit/receive signals
TP56	CLK_IN_OUT	Clock signal of ethernet layer
TP57	ENET_RESET_TJA1101	Reset input signal to ethernet physical layer
TP273, TP274	TJA1021_LIN_RX, TJA1021_LIN_TX	Receive and transmit signals of LIN
TP48	LIN1_INH	LIN inhibit signal
TP275, TP276	TJA1153_CAN_TX, TJA1153_CAN_RX	CAN receive and transmit signals generated by MCU
TP103, TP104	CANH, CANL	CAN_HI signal, CAN_LI signal

Table 28. Controller board test points*...continued*

Test point	Signal name	Description
TP260	VDD	Supply voltage for digital circuitry
TP261	VDD_HV_B_MCU	Supply voltage for B voltage domain of MCU

3 Application Consideration

This chapter provides additional information about the functional blocks of the NXP 48 V MC development platform.

3.1 The S32K3x MCU family

The S32K3x MCU family is an automotive powerful 32-bit microcontroller with Arm Cortex-M7 based core in single, dual or lockstep configuration. It offers broad range of memory, real time control peripheral set, effective security modules and various performance options. In addition, this MCU family is suitable for ASIL B/D functional safety applications due to development according ISO26262 standard. For more information about S32K3x MCU family, please refer to the S32K3xx MCU Family - Reference Manual and datasheet.

NXP 48V MC development platform is equipped with S32K344 microcontroller situated on Controller board. This microcontroller offers following features:

- 32-bit Arm Cortex-M7 lock-step core with 160 MHz core frequency and floating-point unit enables to efficiently execute various and complex motor control algorithms
- Flash memory up to 4 MB and up to 512 KB SRAM (including 192 KB TCM)
- 32 DMA channels and three ADC instances with great number of channels supporting full 3-phase current measurement
- Powerful timers supporting motor control and non-motor control applications:
  - 3 instances of eMIOS and PIT timers
  - 2 instances of STM and SWT
- Real time control peripherals:
  - 2 LCU instances, BCTU and Trigger-mux unit
- Broad range of Serial communication interfaces:
  - 16 instances of LPUART, 6 instances of LPSPI and 2 instances of LPI2C
  - 6 instances of FlexCAN with ISOCAN-FD support, Ethernet and QuadSPI
- EVITA full and light functionality compliant HSE_B
- Power supply 3.0 – 5.5 V
- Functional safety supporting features:
  - Lockstep core
  - Multiple internal watchdogs
  - Voltage monitors
  - Clock monitors
  - Memory protection
  - Data transport checks
  - ECC on memories
  - Cyclic redundancy checking
- Ambient operation temperature range: –40°C to 125°C
- Junction temperature range: –40°C to 150°C

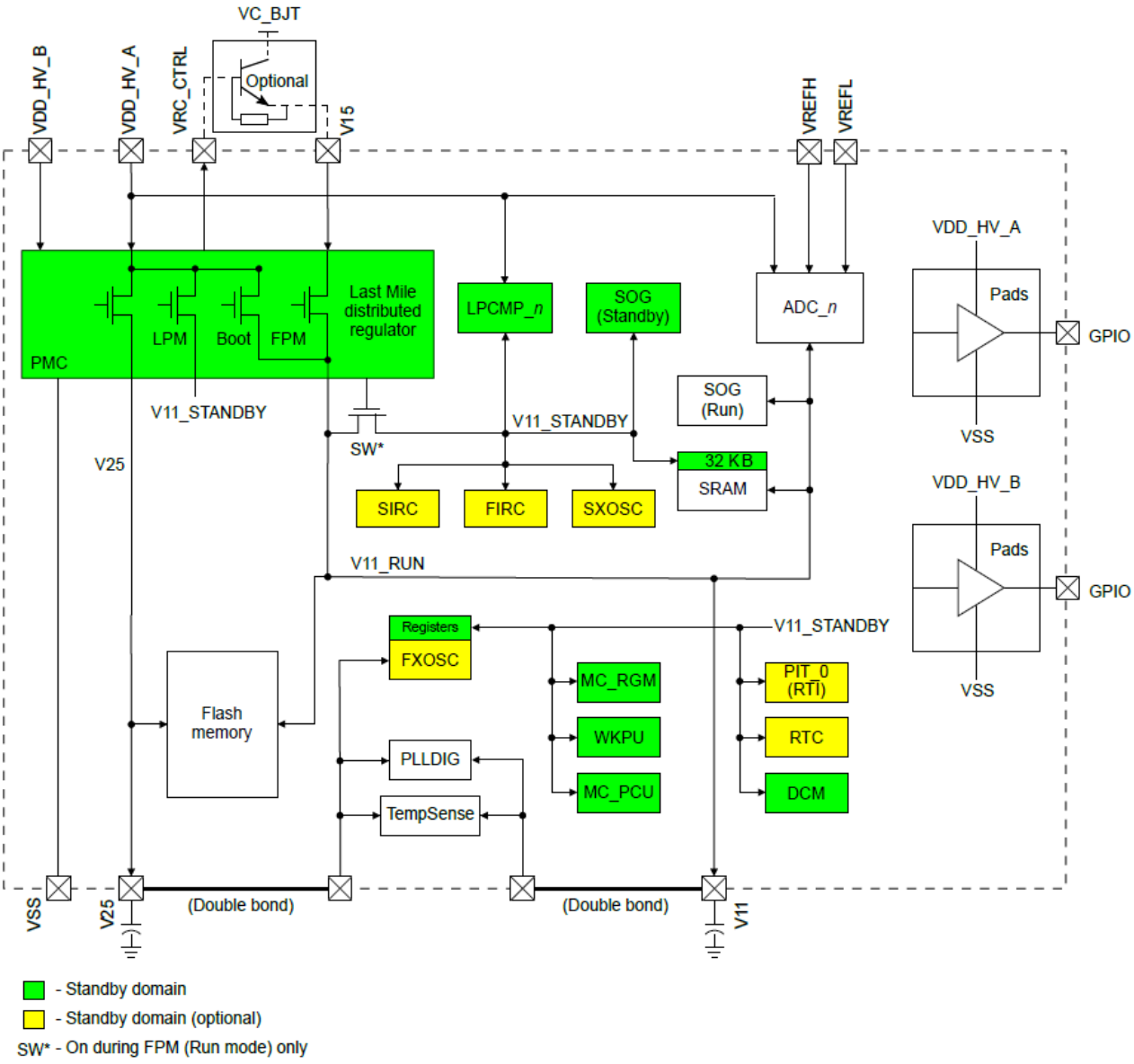


Figure 36. Power management system inside of S32K344

Microcontroller S32K344 is powered by several voltage sources. The above figure shows block diagram of power management of S32K344 microcontroller. There are two separate voltage domains, and each of them supplies different set of peripherals. In case of NXP 48V MC development platform, the voltage domain A of S32K344 microcontroller is powered by 5V whereas voltage domain B of S32K344 microcontroller is powered by 3.3 V. The core logic of S32K344 microcontroller is powered from separate voltage source, which provides high output current capability and 1.5 V voltage level. The VCORE voltage output of system basis chip is connected to V15 pin of S32K344 microcontroller, where internal regulator adjusts this voltage level on 1.1 V. All analog input pins together with some peripherals like ADC peripheral are powered from voltage domain A. Reference voltage for ADC peripheral is used from separate precise and stable voltage source VREF of SBC. High speed communication interfaces like Ethernet or QSPI are powered from voltage domain B of S32K344 microcontroller with 3.3 V voltage level.

For more details about power management of S32K344, please refer to S32K3xx MCU Family - Reference Manual and datasheet.

3.2 The FS26x system basis chip

The FS26x integrated circuit is an automotive Safety System Basis Chip with multiple power supplies designed to support S32K3x family. This SBC is targeting automotive electrification applications such as powertrain, chassis, safety, and low-end gateway applications.

The FS26x SBC family is comprised of several and configurable versions, which are pin to pin and software compatible. It offers a great number of output rails, output voltage settings, operating frequency, power up sequencing and integrated system level features to address multiple functional safety automotive applications with ASIL B or D level.

The power supply possibilities of FS26x SBC are summarized in following points:

- VPRE: synchronous buck converter with integrated FETs. The output voltage is configured at 6 V and switching frequency is set at 2.25 MHz. The output DC current capability is 1.5 A and PFM mode for Low Power Standby mode operation.
- VCORE: synchronous buck converter with integrated FETs. VCORE is dedicated for microcontroller core logic supply. The output voltage can be configured from 0.8 V to 3.3 V and delivered output DC current can be up to 0.8 A or 1.5 A.
- VBST: asynchronous boost controller with external low side switch, diode, and current sense resistor. VBST is configured as front-end supply to withstand low voltage cranking profiles.
- LDO1: internal linear regulator for microcontroller input/output support with selectable output voltage between 3.3 V and 5.0 V. It can provide DC output current up to 400 mA.
- LDO2: internal linear regulator for microcontroller input/output support with selectable output voltage between 3.3 V and 5.0 V. It can provide DC output current up to 400 mA.
- VREF: high precision reference voltage with 1% accuracy for external ADC reference and internal tracking reference.
- TRK1: Voltage tracking regulator 1 is linear voltage regulator, which can follow source VREF, LDO2 or Internal LDO reference. This TRK1 is intended to supply analog peripheral ICs with the current capability up to 150 mA.
- TRK2: Voltage tracking regulator 2 is linear voltage regulator, which can follow source VREF, LDO2 or Internal LDO reference. This TRK2 is intended to supply analog peripheral ICs with the current capability up to 150 mA.

The FS26x device is developed according to ISO26262 standard likewise S32K3x microcontrollers and includes enhanced safety features with multiple fail-safe outputs which are utilized for safe control of specific subsystems. Several safety features are summarized in following points:

- Independent Monitoring Circuitry
- Dedicated interface for microcontroller monitoring
- Simple and challenger watchdog
- Analog Built-In Self-Test (ABIST) and Logical Built-In Self-Test (LBIST) at start up
- Analog Built-In Self-Test (ABIST) on demand
- Safety Outputs with latent fault detection mechanism (RSTB, FS0B, FS1B)

System supporting functions of FS26x SBC are summarized in following points:

- Two Wake-up inputs with high voltage support for system robustness
- Two programable GPIOs with Wake-up capability or HS/LS driver
- Programable Long Duration Timer (LDT) for system Shutdown and Wake-up control
- System Voltages monitoring (Including Battery voltage monitoring) through the Analog Multiplexer
- Selectable Wake-up sources from: WAKE/GPIO pins, LDT or SPI activity
- Device control via 32 bits SPI interface with CRC

For more information about FS26x System Basis Chip, please refer to the FS26x System Basis Chip - Datasheet.

The FS2613D version of System Basis Chip is used in NXP 48V MC development platform. More details about configuration of this SBC are mentioned in System Basis Chip FS2613D.

3.3 Input/Output power connection, DC-link pre-charging

Figure 37 shows input terminals of 48 V system and pre-charge MOSFETs circuitry. The input terminals J1 and J2 are used for connection of appropriate 48 V power supply source. The DC energy from power supply source is transferred through the fuse, which is connected on terminals J5 and J6. The fuse protects 48 V system against short in power circuit or against fatal damage of system in case of reverse connection of input terminals. Subsequently, the flow of input DC current is divided in power node and start to feed two separate DC-link circuits with their individual pre-charging circuits and choke coils. The first motor configuration contains pre-charging MOSFETs Q1 and Q2 with choke L1, while second motor configuration contains pre-charging MOSFETs Q3 and Q4 with choke L2. The DC-link circuit of one motor configuration consist of four 990 µF bulk capacitors and several 0.1 µF decoupling capacitors.

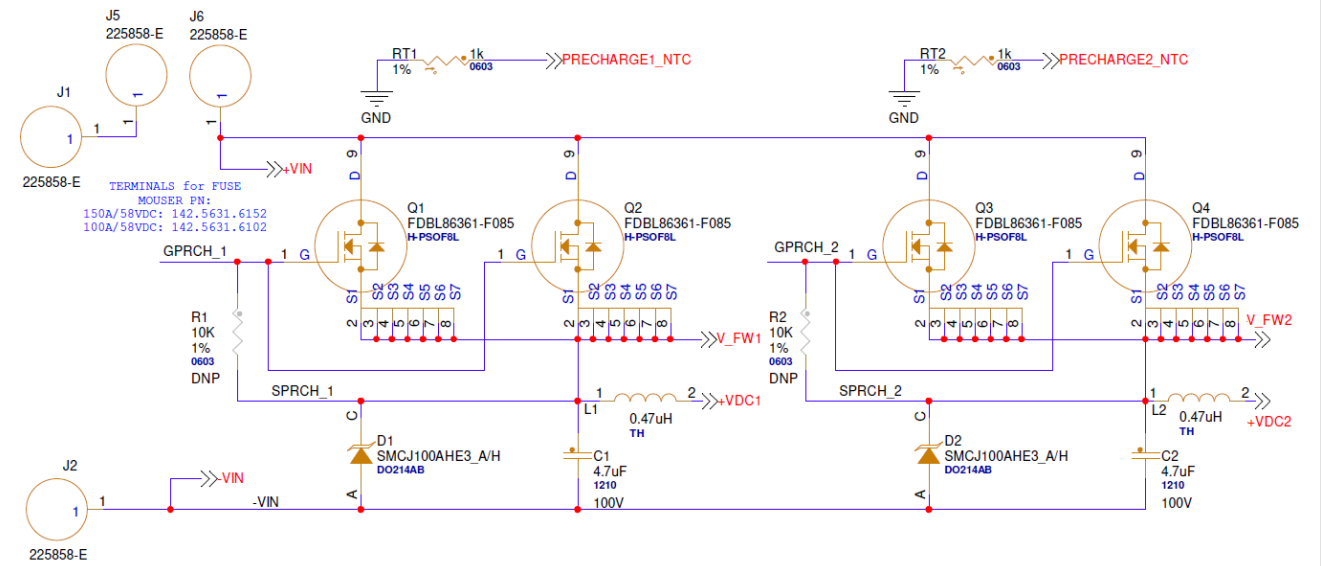


Figure 37. Input terminals of 48V system and pre-charge MOSFETs for both motor configurations

The pre-charging MOSFETs require high side excitation pre-driving circuitry. This circuit is shown in Figure 38. Pre-charging of DC-link capacitors of NXP 48 V MC development platform is working in two operational intervals. First interval starts when the system is powered by appropriate 48 V power supply source connected on input terminals J1 and J2. The pre-charging MOSFETs Q1 and Q2 for first 3-phase MOSFET half-bridge arrangement and Q3 and Q4 for second 3-phase MOSFET half-bridge arrangement are turned off and DC-link circuits are approximately pre-charged on 15 V by Buck converter. This first level of pre-charging is managed by diode D33 and resistor R138 for first 3-phase MOSFET half-bridge arrangement and by diode D34 and resistor R139 for second 3-phase MOSFET half-bridge arrangement.

Once the DC-link capacitors are approximately pre-charged on 15 V, system can be charged to 48 V by control signal ON_1 for first 3-phase MOSFET half-bridge arrangement and by control signal ON_2 for second 3-phase MOSFET half-bridge arrangement. Deactivation of pre-charging MOSFETs can be achieved by toggling ON_1 signal to log. 0 for first 3-phase MOSFET half-bridge arrangement and toggling ON_2 signal to log. 0 for second 3-phase MOSFET half-bridge arrangement.

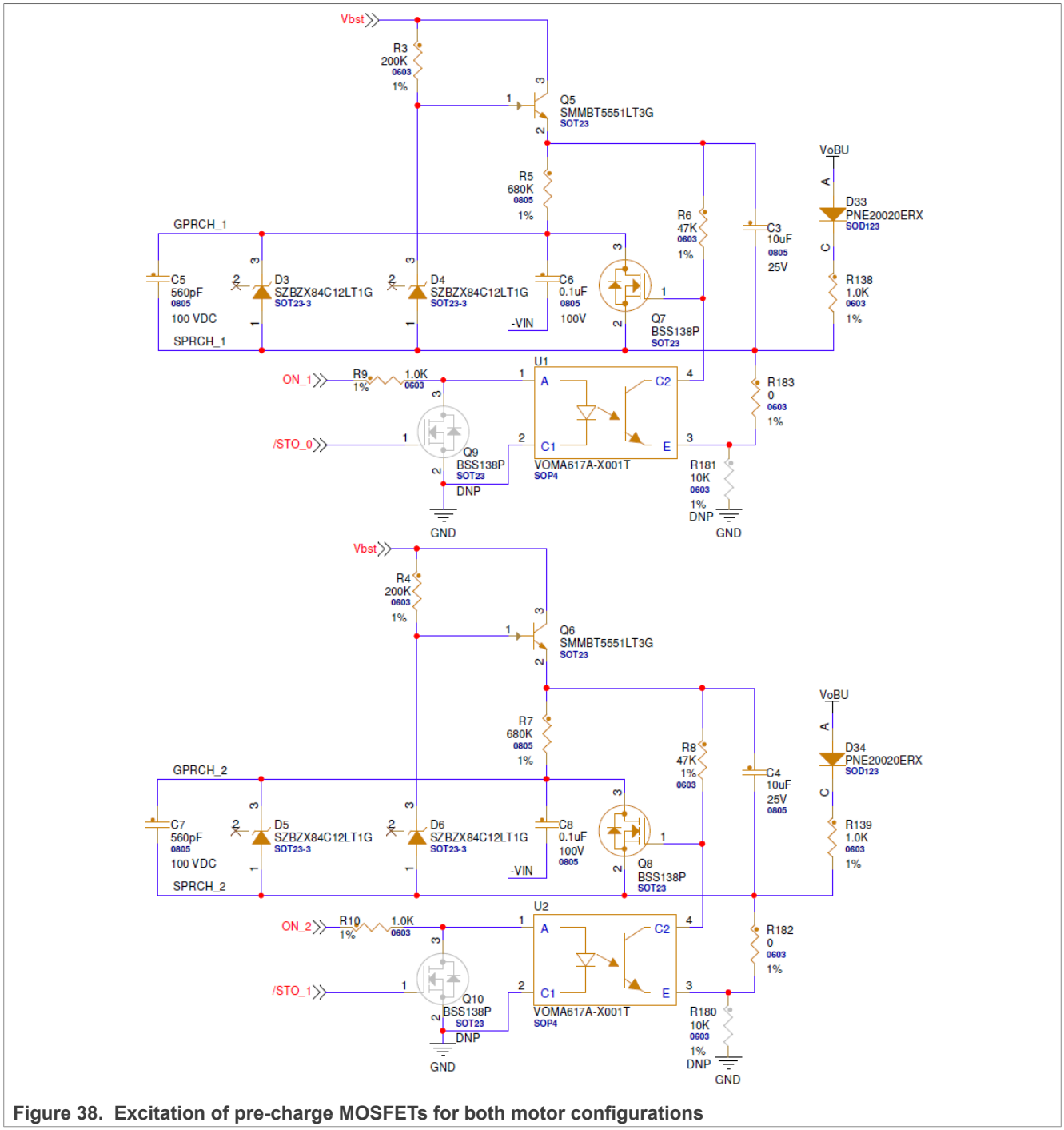


Figure 38. Excitation of pre-charge MOSFETs for both motor configurations

Voltage drop over drain and source MOSFET terminals is monitored by comparator and external ballast due to undesired short in power circuit. This circuit is shown in Figure 39. The short circuit fault is transferred over the OVCI_1 signal for first 3-phase MOSFET half-bridge arrangement and OVCI_2 for second 3-phase MOSFET half-bridge arrangement. Those faults are detected by log. 0 and processed by microcontroller.

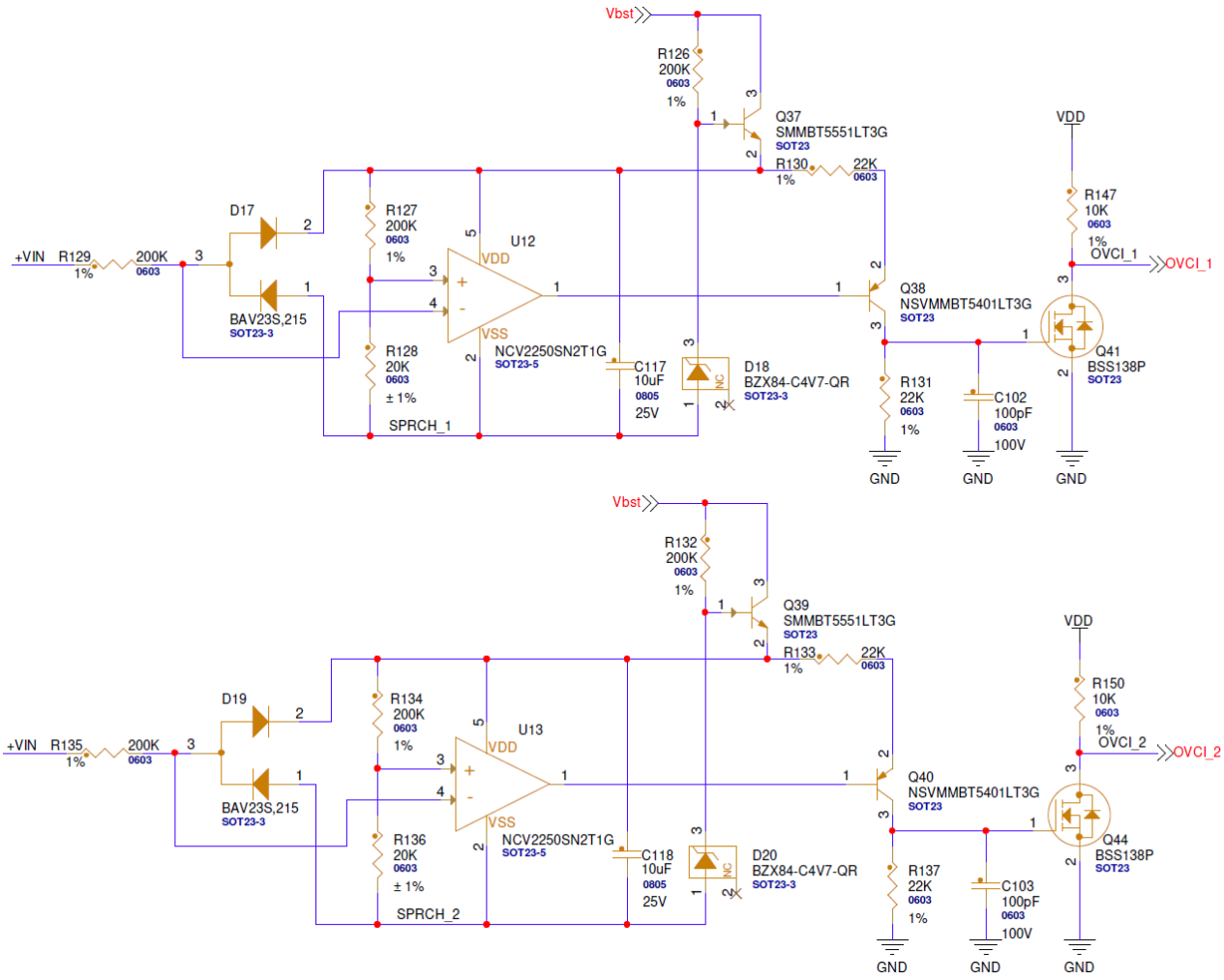


Figure 39. Desaturation detection of pre-charge MOSFETs for both motor configurations

Pre-charge MOSFETs temperature is monitored by external NTC sensors RT1 for first motor configuration and RT2 for second motor configuration. Analog signals of temperatures are transmitted to the Adapter board for additional processing. Description of temperature processing is discussed in Temperature sensing.

Power output terminals are mechanically and electrically identical with power input terminals. The motor phases can be connected by wiring ring-eye terminals with metric M3 screw to the power stage similarly as input power supply source.

3.4 3-phase MOSFET half-bridge

The NXP 48 V MC development platform contains two identical 3-phase MOSFET half-bridges, which are capable of controlling two 3-phase PMSMs independently or one 6-phase PMSM up to 80 A(rms).

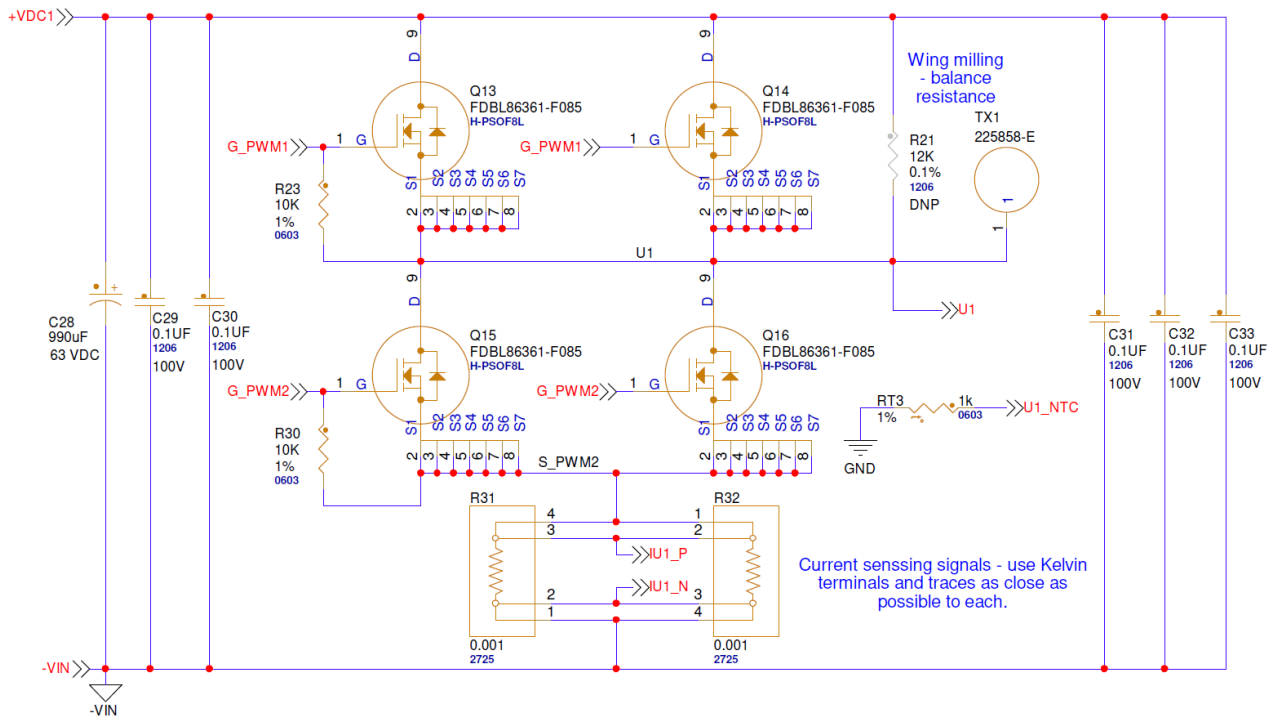


Figure 40. One leg of 3-phase MOSFET half-bridge

Figure 40 shows one leg of MOSFET half-bridge. Entire 3-phase MOSFET half-bridge consists of three complementary MOSFETs legs with shunt resistors and BEMF voltage dividers. The complementary MOSFETs in each leg are doubled in order to achieve demanded power rating of system. Figure 41 shows model of power MOSFET, which is used in NXP 48 V MC development platform for half-bridge and pre-charge. The parameters of the MOSFET are summarized in Table 29 . The shunt resistors in each leg of 3-phase MOSFET half-bridge are doubled as well due to same reason. The temperature of power MOSFETs is sensed by NTC sensor close to each leg of inverter and signals are processed on Adapter board. The design of both 3-phase MOSFET half-bridges support wind milling motor control technique. Balance resistor R21 for one leg of first 3-phase MOSFET half-bridge is connected parallelly to high side MOSFETs and can be used for balancing BEMF voltage. Each phase of 3-phase MOSFET half-bridge contains such balancing resistor. Resistors are not populated by default but can be assembled in case of need.

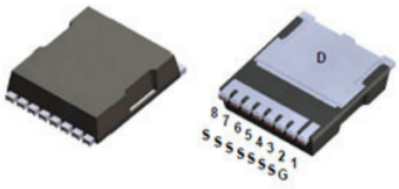


Figure 41. MOSFET FDBL86361-F085

Table 29. MOSFET parameters

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{DS}	Drain to source voltage	25°C≤T_j≤175°C	-	-	80	V
I_D	Drain current	V_{GS}=10V; T_{amb}=25°C	-	-	300	A
P_{TOT}	Total power dissipation	T_{amb}=25°C	-	-	429	W

Table 29. MOSFET parameters *...continued*

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
$R_{DS(ON)}$	Drain to source resistance	V_{GS}=10V; I_D=80A; T_j=25°C	-	1.1	-	mΩ
$Q_{G(TOT)}$	Total gate charge	I_D=80 A; V_{GS}=10 V	-	172	188	nC

Each leg of 3-phase MOSFET half-bridge is excited by a simple gate driver in a half-bridge configuration. Figure 42 shows gate driver circuit for one leg of 3-phase MOSFET half-bridge. All gate drivers are activated by default. Deactivation of gate drivers can be carried out over shutdown signals /STO_0 for first 3-phase MOSFET half-bridge arrangement and /STO_1 for second 3-phase MOSFET half-bridge arrangement.

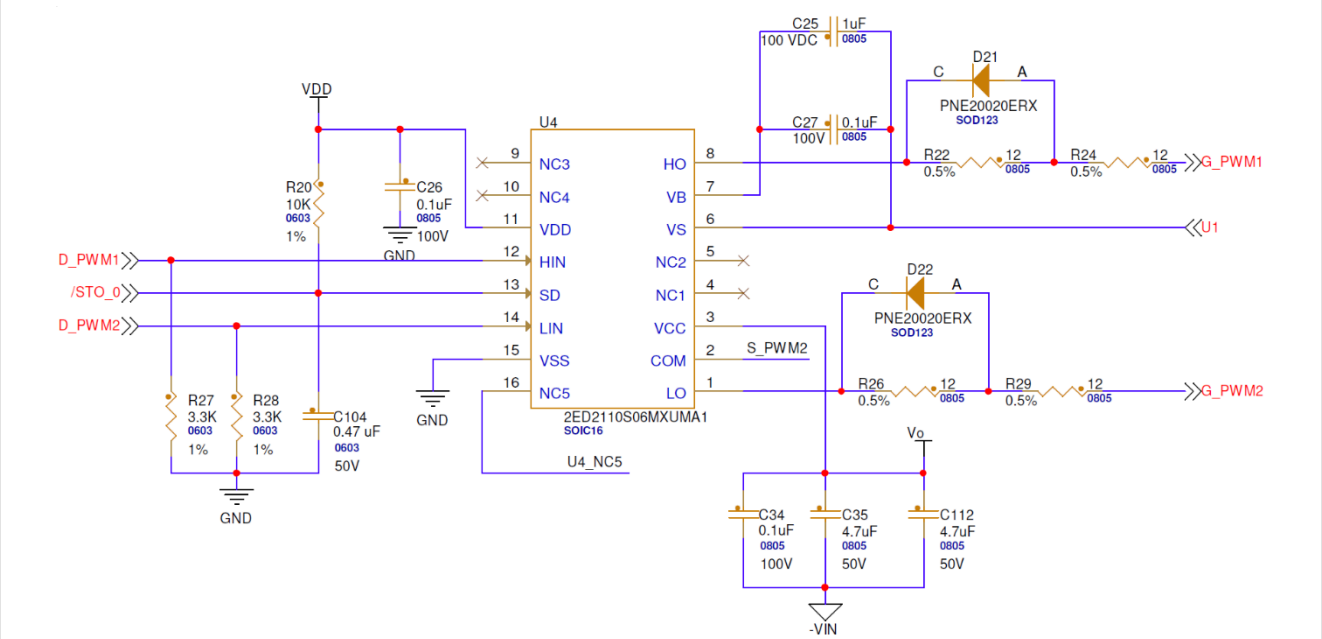


Figure 42. Half-bridge configuration of gate driver circuit

The high side MOSFETs are switched on by means of bootstrap capacitor C25. Each leg of inverter contains such bootstrap capacitor. This approach of high side MOSFET switching allows to optimize switching performance based on designer needs but, it limits utilization of duty cycle.

The MOSFET excitation currents are limited by two serial gate resistors R22 and R24 for high side MOSFETs and R26 and R29 for low side MOSFETs during turn-on time. During the turn-off time, the MOSFET excitation currents are limited only by resistor R24 for high side MOSFETs and R29 for low side MOSFETs. The resistors R22 and R26 are bypassed with Schottky diode in opposite direction. This configuration helps to improve system switching performance during turn-off process. All gate drivers are supplied by VDD supply voltage from SBC, and Vo supply voltage.

3.5 Measurement of analog quantities

3.5.1 Voltage sensing

All analog voltage signals are measured at multiple circuits of 48 V system. Galvanic isolation of analog signals measurement is not used in NXP 48 V system. The voltage level adjustment is managed by voltage dividers, which are set to meet the range of AD converter of microcontroller. The scale of all voltage dividers intended for system voltage measurement is set on 1:12. This scale refers to maximum operation voltage of system, which is 60 V for 5 V range of ADC converter.

There is a summary of voltage signals, which are measured in system:

- DC-link voltage of first 3-phase MOSFET half-bridge
- DC-link voltage of second 3-phase MOSFET half-bridge
- Forward voltage of first 3-phase MOSFET half-bridge
- Forward voltage of second 3-phase MOSFET half-bridge
- Battery voltage of system
- 3-phase back-EMF voltages for first motor configuration
- 3-phase back-EMF voltages for second motor configuration

The analog signals of back-EMF voltages are adjusted by voltage dividers and transferred from Power Stage board through Adapter board to the Controller board in order to be processed by ADC modules. These signals are primarily utilized for block commutation algorithms and wind milling algorithm. For more information about block commutation algorithms, please refer to the AN12435: 3-Phase Sensorless BLDC Motor Control Kit with S32K144.

The analog signals of Back-EMF voltages are also utilized for real 3-phase voltage reconstruction and measurement. The 3-phase inverter's output voltages are scaled by back-EMF voltage dividers to meet the range of AD converter. Three comparators, populated on the Adapter board, compare 3-phase inverter's output voltages with scaled DC-link voltage and provide three digital square-wave signals on the outputs. The real 3-phase voltages can be reconstructed from measured duty cycles of the square wave signals and actual DC-link voltage.

The below figure shows the comparator circuit for phase voltage reconstruction of one motor phase. Square wave signal of phase voltage is filtered by low pass filter R54 and C26 and applied to non-inverting input of comparator U15A. A small hysteresis is used in order to achieve stable operation of comparator. The reference voltage is provided by follower U18A from DC-link voltage. This comparator is designed in open collector configuration. The level of comparator output signal is adjusted according to level of MCU_VCC voltage, which is 3.3 V for Controller board with S32K344 microcontroller.

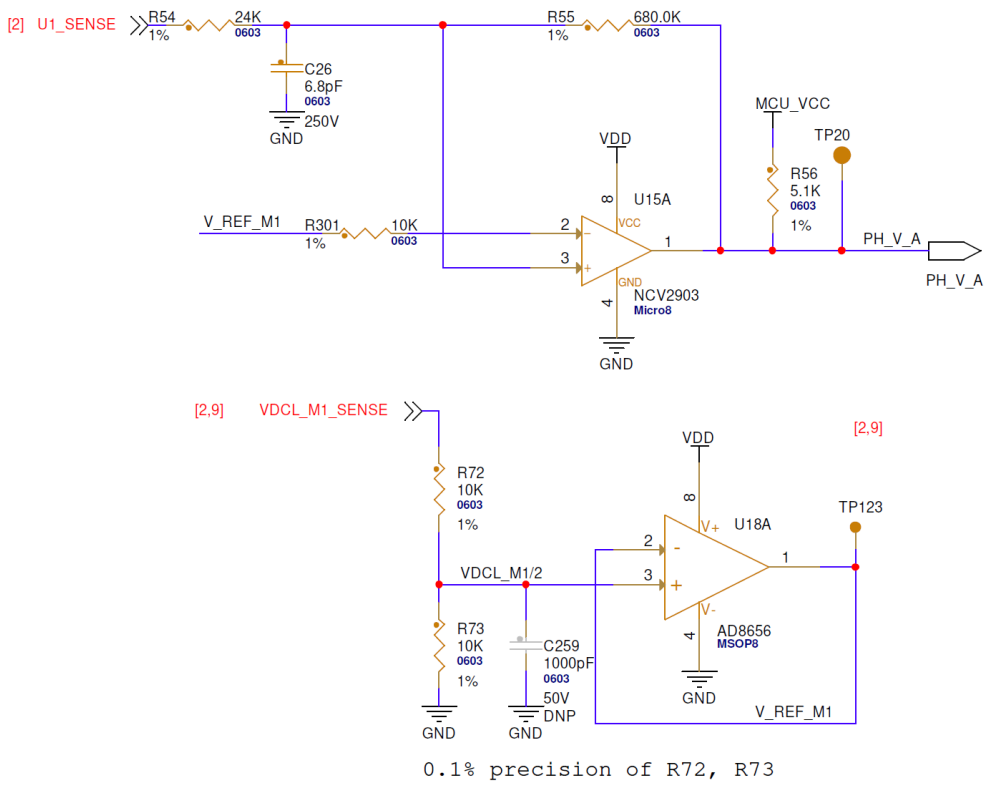


Figure 43. Phase voltage reconstruction circuit of one phase

3.5.2 Current sensing

The signal processing of motor phase currents measurement is managed by operational amplifier circuits. The phase current is sensed by two shunt resistors in parallel connection which are placed in each leg of inverter below the low side MOSFETs. The current measurement technique where each leg of voltage inverter contains shunt resistor is called triple shunt current sensing. This technique brings benefits of 100% duty-cycle utilization and accomplishment of functional safety requirements. On the other hand, additional resistance in power paths decreases efficiency and increases the cost of the system. This subchapter describes triple shunt current sensing technique and signal processing of current measurement in NXP 48 V MC development platform.

Triple shunt current sensing technique allows to measure 3-phase currents directly without additional software calculation. The shunt resistors are placed below the low side MOSFETs, so current can be measured when corresponding low side MOSFET is turned on. Figure 44 shows waveforms of PWM signals for all MOSFETs in 3-phase voltage inverter, motor phase currents and currents flowing through shunt resistors. The current flow generates voltage drop over the shunt resistor in range of millivolts. This voltage drop is amplified by operational amplifier with static offset and amplified value of voltage drop is processed by ADC module. Figure 44 also illustrates beginning of conversion by red dash line in the middle of PWM pulse. The 3-phase current measurement technique requires parallel conversion of all three signal, which require to use three ADC modules with synchronized trigger source.

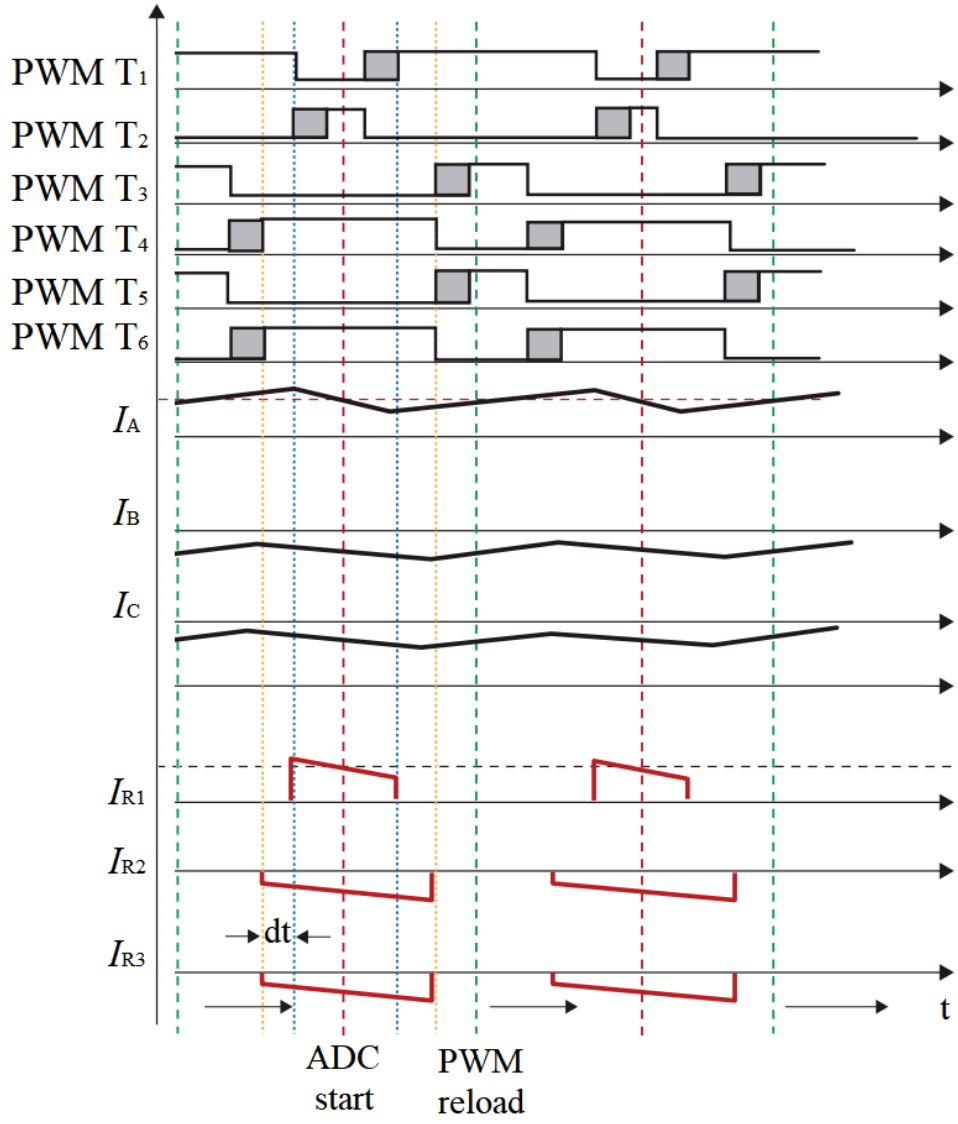


Figure 44. Waveforms of PWM signals, phase currents and shunt resistor currents

Figure 45 shows operational amplifier circuit for signal processing of motor phase current measurement. The voltage drop differential signals are transferred from Power Stage board through header connector to the Adapter board. The rail-to-rail operational amplifier is powered by VDDA voltage source. The 48 V MC development platform allows to change current measurement range by shunt resistors change or by change of operational amplifier gain. The resistors R1-R8 set the gain of operational amplifier while jumper J2 and J5 allows to change the gain value. Change of current measurement range can be carried out only during power off state of the system. The capacitors C1-C3 are responsible for noise mitigation. Developer can increase the capacitance if filtration is not good enough. However, modification of this capacity influences bandwidth of current measurement circuit. Bidirectional current measurement is ensured by stable and precise voltage reference VA_REF_M1, which is applied to the non-inverting port of operational amplifier through R7, R8 resistors and jumper J5. Level of voltage reference is set in the middle AD converter voltage range. The below table shows configuration of range for phase current measurement.

Table 30. Configuration of current measurement range

ADC voltage range	5 V

Table 30. Configuration of current measurement range*...continued*

Gain	50		25	
Jumpers J2 and J5	Open		Close	
Shunt resistor value	1 mΩ	0.5 mΩ	1 mΩ	0.5 mΩ
Range of current measurement	<-50…50> [A]	<-100…100> [A]	<-100…100> [A]	<-200…200> [A]
ADC voltage range	**3.3 V**			
Gain	50		25	
Jumpers J2 and J5	Open		Close	
Shunt resistor value	1 mΩ	0.5 mΩ	1 mΩ	0.5 mΩ
Range of current measurement	<-33…33> [A]	<-66…66> [A]	<-66…66> [A]	<-132…132> [A]

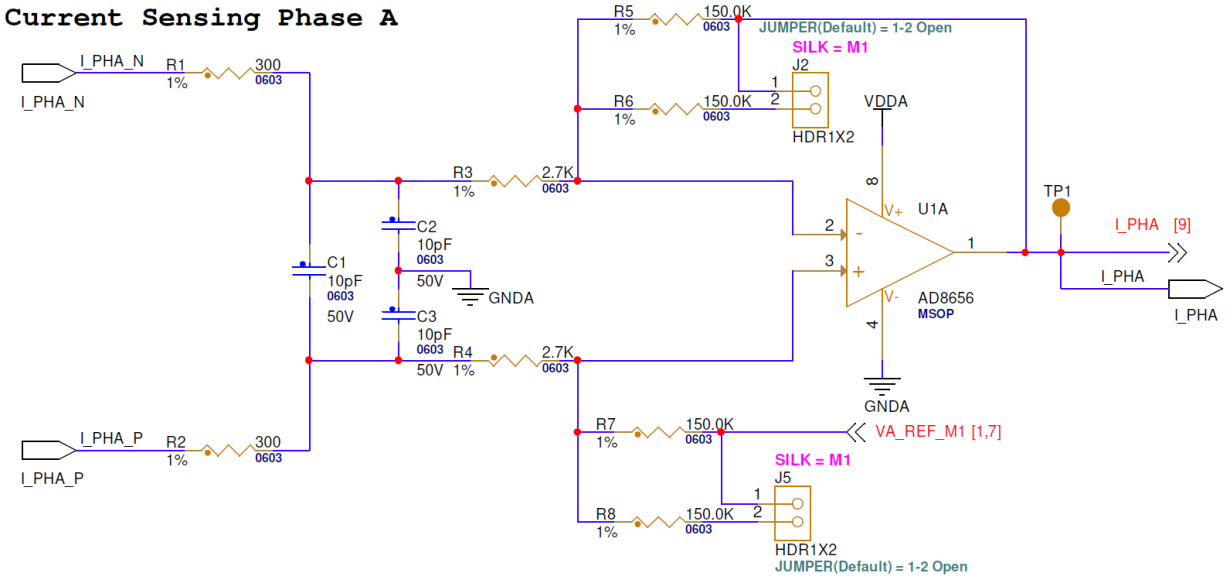


Figure 45. Phase current measurement circuit based on operational amplifier

The Adapter board current sensing processing circuit contains also jumper selection between phase current or back-EMF voltage measurement. Figure 46 shows jumpers J16, J17 and J18 for first motor configuration and J19, J20, J21 for second motor configuration. Position 1-2 of those jumpers allows to route phase current signals to the PCIe connector while position 2-3 allows to route back-EMF voltages.

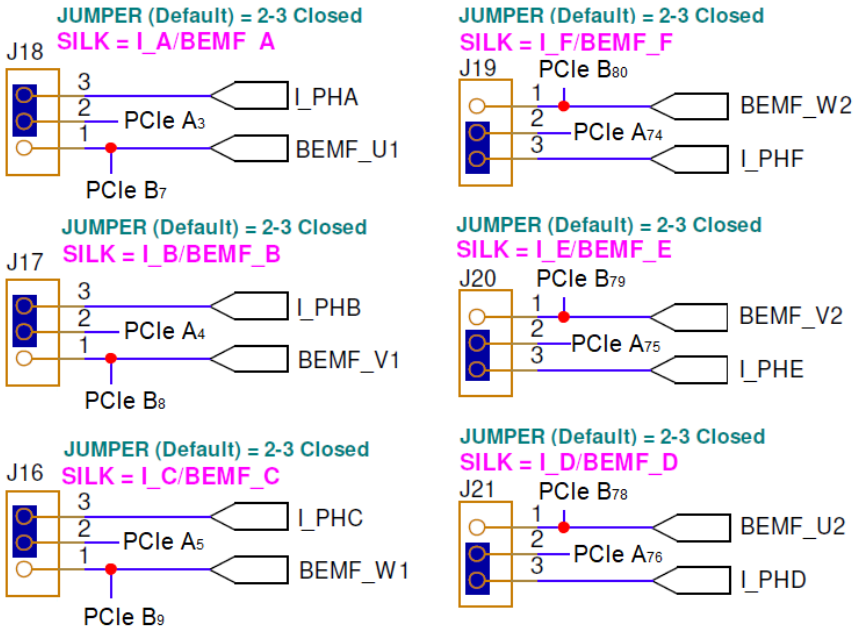


Figure 46. Jumpers for phase currents measurement or Back-EMF voltages measurement

3.5.3 Temperature sensing

The measurement of temperature is essential for higher system reliability. The temperature is measured by Negative Temperature Coefficient (NTC) thermistor, which is populated close to each leg of inverter and close to pre-charging MOSFETs. The thermistor output is transferred through header connector of Power Stage board to the Adapter board and connected to the simple resistor. Those two components create a voltage divider, which is connected to the input of multiplexor. Figure 47 shows circuit of temperature signal processing based on 8-channel multiplexor. This circuit arrangement of temperature signal processing is populated on Adapter board and contains low pass filter R368 and C281 at the output of multiplexor and level translators U133, U134 and U135 at the inputs of control signals. The multiplexor output depends on combination of voltage level of 3 GPIO pins A1, A2 and A3. Those control signals are set by microcontroller and routed through PCIe connector. The level shifters are by default bypassed by resistors R411, R412 and R413 however, can be populated in in case of need.

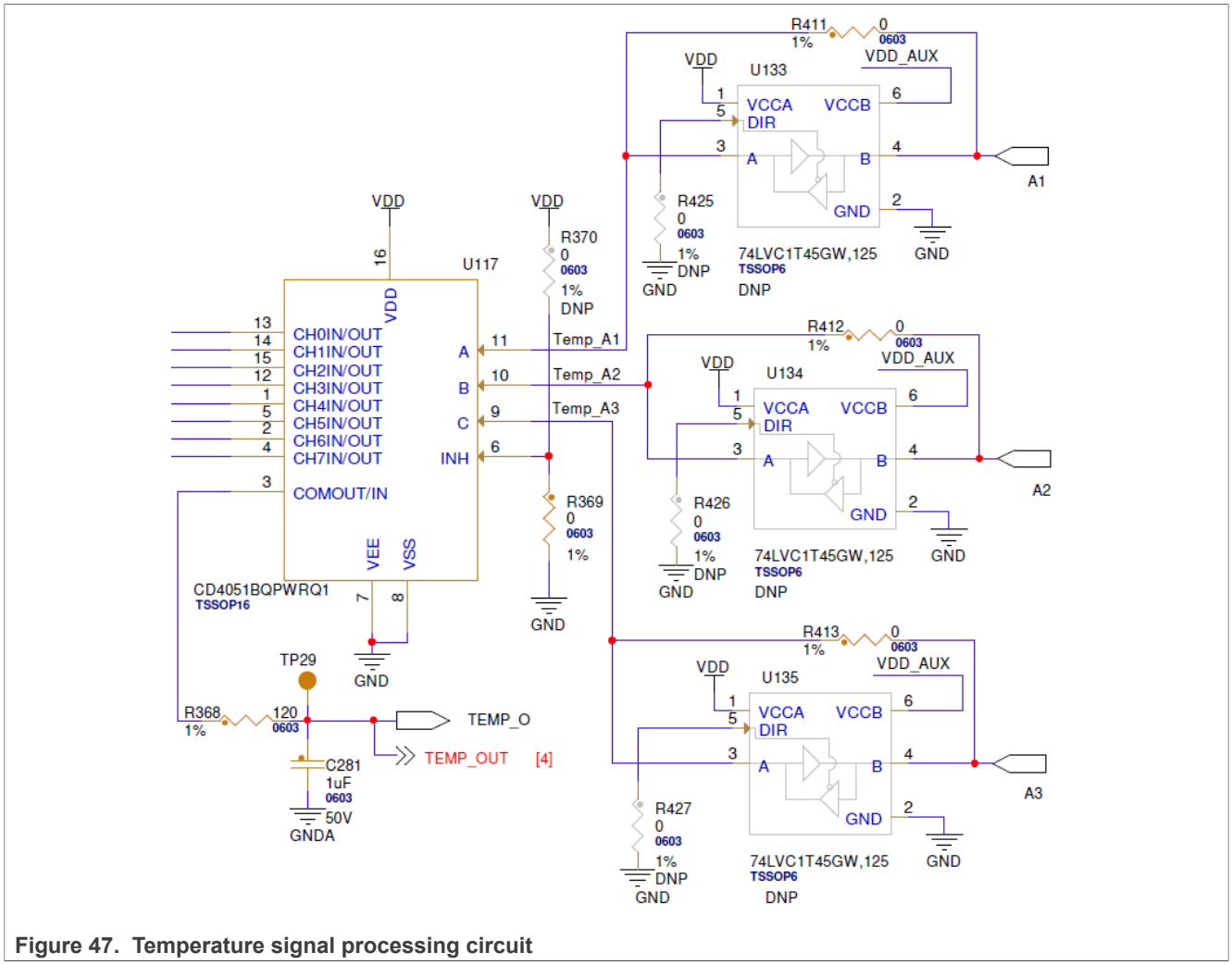


Figure 47. Temperature signal processing circuit

The temperature signal processing circuit includes control of active cooling fans. Signals of temperature in the middle of both 3-phase MOSFET half-bridges and pre-charging MOSFETs are processed by comparator logic. Figure 48 shows this comparator circuit where all comparator outputs are connected to the common pull-up resistor R384 and inverted by Q17 transistor. Input signals of temperature are routed to the non-inverting inputs of comparators though low pass filters R371 and C282, R379 and C283, R378 and C284, R377 and C285. The reference signal is created by follower U70B and routed to the inverting inputs of comparator. Output signal “FAN_CTRL” controls the power MOSFET and activates two cooling fans.

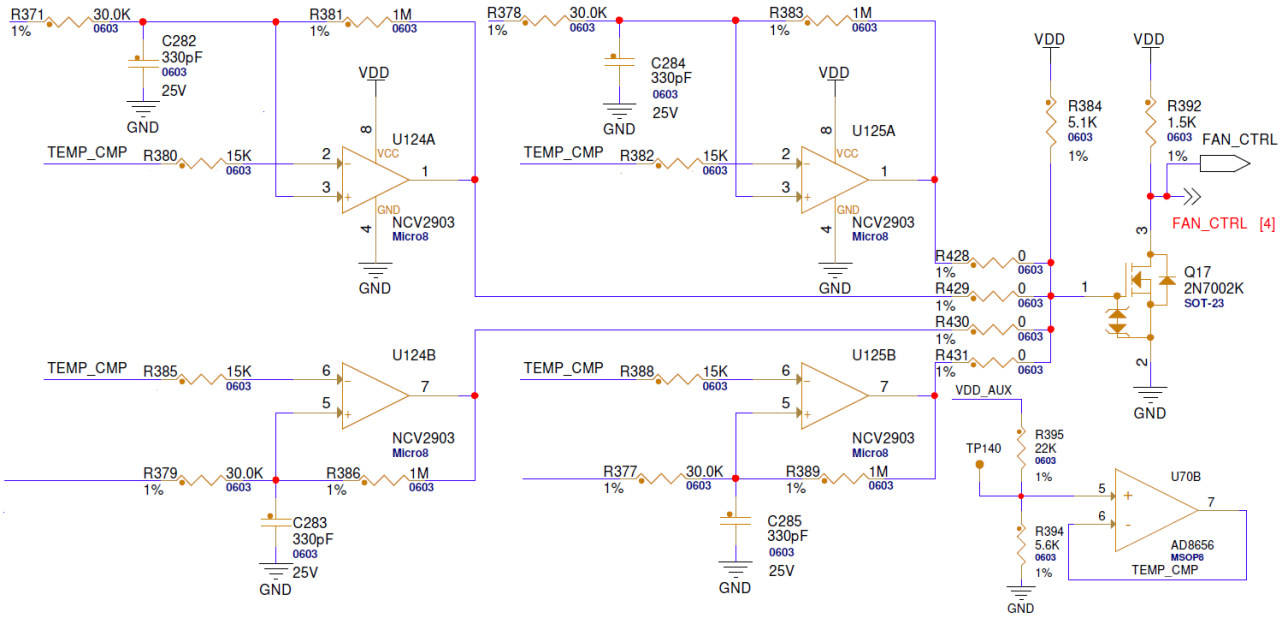


Figure 48. Comparator logic for active cooling system

Figure 49 shows power circuit of active cooling. This circuit allows autonomous control of active cooling, however the cooling fans may be driven directly by microcontroller. Two cooling fans are connected to the connectors J30 and J31. Header J23 in Figure 49 allows to select control signal to the MOSFET Q9. Position 1-2 allows to drive MOSFET Q9 directly by MCU and position 2-3 allows autonomous operation of cooling fans. In addition, the “FAN_CTRL” signal is routed directly to the microcontroller through PCIe connector and enable to monitor of autonomous active cooling operation.

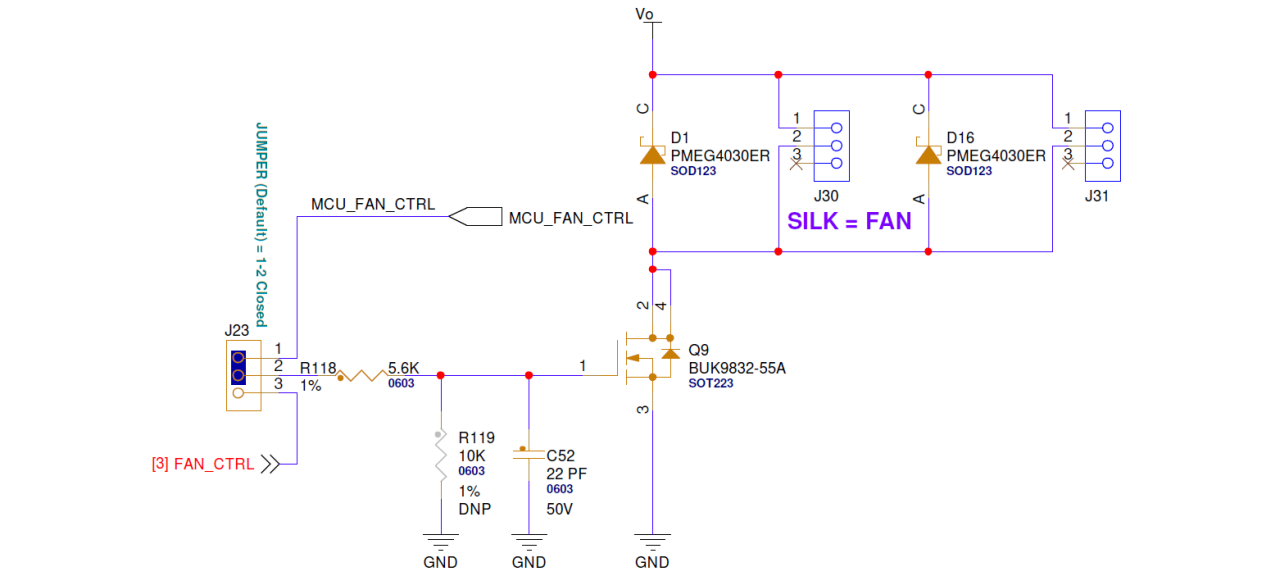


Figure 49. Power circuit of active cooling system

3.6 Power supply management

The NXP 48 V MC development platform is built on complex power supply strategy including redundancy. This redundancy improves system reliability and allows to supply circuits and microcontroller in case of malfunction

of main power supply source. The below figure shows block diagram of power supply chain. The main supply chain is built on step-down buck converter. The back-up source is flyback converter. The outputs of both converters are connected to the common node through diodes in common cathode connection. Output of this node is voltage V_o and is routed to the system basis chip though PCIe connector. The system basis chip creates several voltage outputs for analog and digital circuits, microcontroller and for external sensors. Next subchapters describe individual parts of power supply chain.

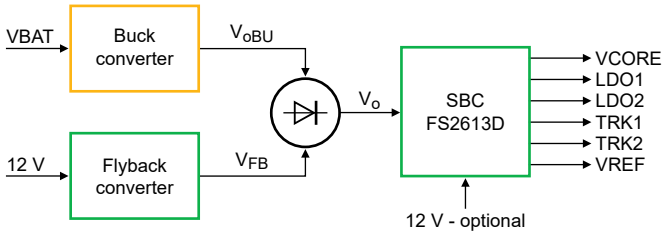


Figure 50. Power supply chain

3.6.1 Step-down Buck converter

Figure 51 shows schematic of step-down Buck converter located on Power Stage board. It is powered directly from main 48 V voltage source. This input voltage is converted to 15 V and routed to the Adapter board through header connector. This converter topology doesn't provide galvanic isolation of input and output but it converts energy effectively and provide sufficient current capability on the output. The step-down Buck converter utilizes LM5118 automotive qualified driver. Threshold of minimal input operation voltage is set by voltage divider R11 and R15 to 17 V. The switching frequency is set by resistor R16 to approximately 250 kHz. The output voltage is filtered by Π filter C114, C17 and L4 in order to mitigate noise generated by synchronous operation. The circuit of Buck converter is extended by simple charge pump circuit, composed by diode D7, capacitors C13 and C9. The output of charge pump circuit is connected to the pre-charge excitation circuit and desaturation detection circuit in order to turn-on high side pre-charging MOSFETs and monitor pre-charging MOSFETs respectively.

The output voltage V_{oBU} of Buck converter is routed to header connector and is connected to common node through diodes connected in common cathode configuration.

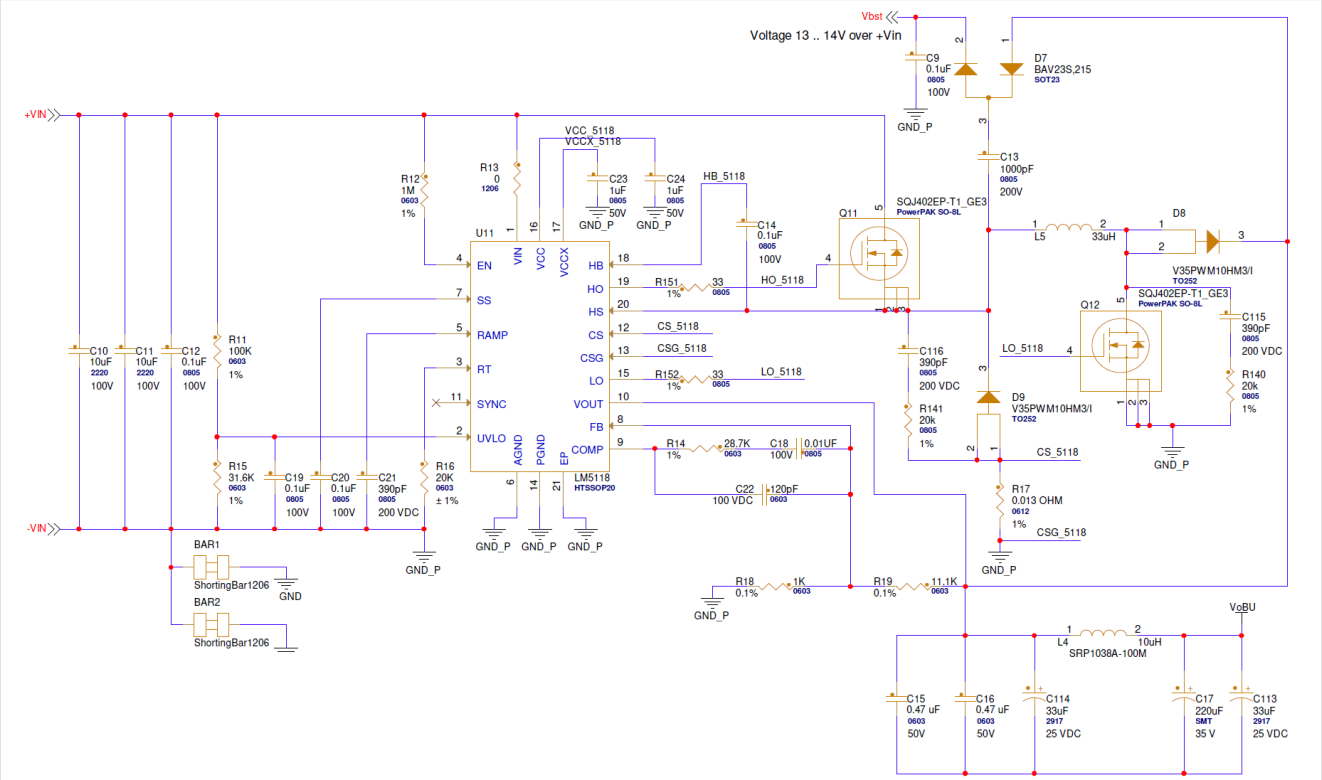


Figure 51. Step-down Buck converter

3.6.2 Flyback converter

Figure 52 shows schematic of Flyback converter. The Flyback converter represents back-up voltage source to Buck converter. It overtakes the role of main voltage source if Buck converter fails. It is located on Adapter board and powered by external 12 V voltage source through barrel connector J39. Step-up/down operation of converter is not needed during development in laboratory environment with stable power supply source and 12 V on the input of Flyback, however, the input voltage might vary from 8 V to 16 V in real application. This variation of input voltage is acceptable for this design of Flyback converter.

The design of Flyback converter utilizes LM5022 controller. The switching frequency is set by resistor R456 to 160 kHz, and threshold of input operating voltage is set by voltage divider R347 and R455 to approximately 7.1 V. The Flyback operates in discontinuous conduction mode (DCM) with isolated feedback loop in order to keep constant output voltage. The output voltage V_{oFB} of Flyback converter is connected to common node through diodes connected in common cathode configuration.

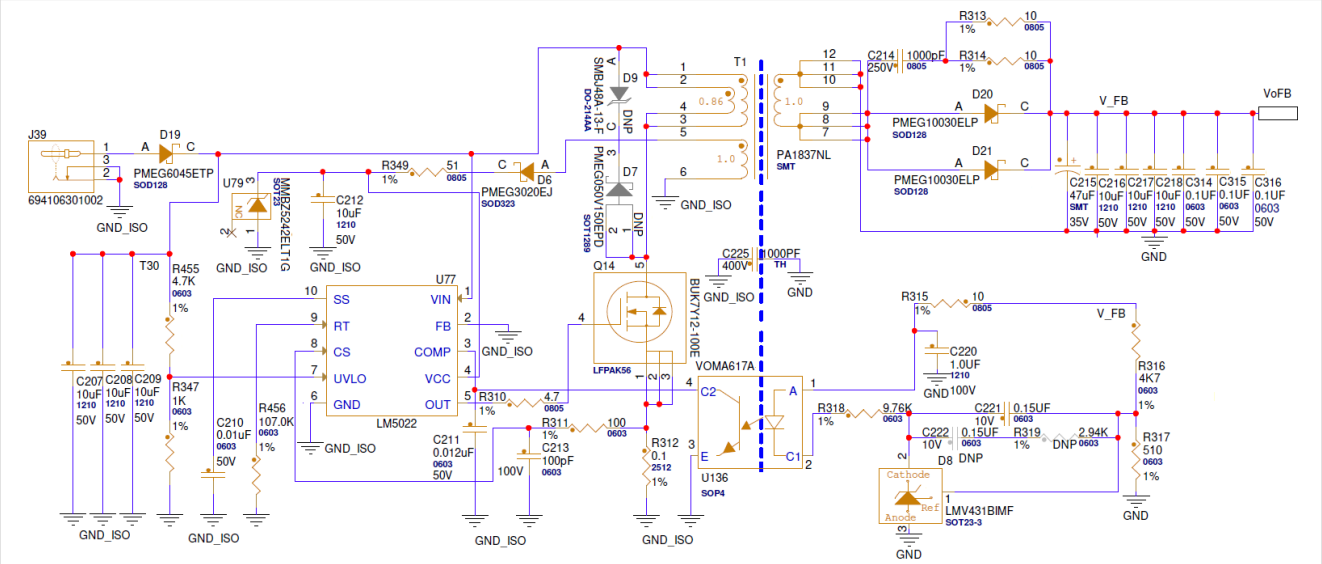


Figure 52. Flyback converter

3.6.3 System Basis Chip FS2613D

General description of the system basis chip was already noted in The FS26x system basis chip. This section describes circuit implementation of SBC FS2613D in NXP 48 V MC development platform and its role in power supply chain. The SBC device is placed on the Controller board, and it is powered by step-down Buck converter or Flyback converter. Besides of power supply role of the device, the SBC device is capable to communicate with microcontroller through SPI interface, processes external signals or generate fail-safe signals. There are two modes of SBC operation, front-end or back-end mode. The configuration of SBC in NXP 48 V MC development platform supports front-end mode of operation. It is the most typical use-case for many automotive applications because enable an operation of SBC in low voltage.

Figure 53 shows schematic of System Basis chip FS2613D. Assembled barrel connector J1 allows to power the SBC and complete Controller board in the case of standalone operation. The Controller board mustn't be connected in NXP 48V MC development platform. If the Controller board is connected to PCIe connector of NXP 48V MC development platform, the SBC and complete Controller board is powered by Buck or Flyback converter. This configuration of SBC allows to withstand low voltage cranking profiles. If the input supply voltage of SBC device is from 4.3 V to 7 V, the boost converter is activated. The output signal of boost converter is labeled as "VSUP", and it is connected to internal high voltage Buck converter, so-called VPRE regulator. The output of this regulator, so-called "FS26_VPRE" signal, is used for supplying internal LDO regulators, tracker sources and voltage reference. In addition, VPRE regulator's output voltage is used also for low voltage Buck regulator, which provides power supply output signal, so-called VCORE.

The SBC output power supply sources are summarized in Table 31. The first output voltage source is VCORE, which provides 1.5 V and up to 800 mA at the output. It is used for supplying microcontroller core logic.

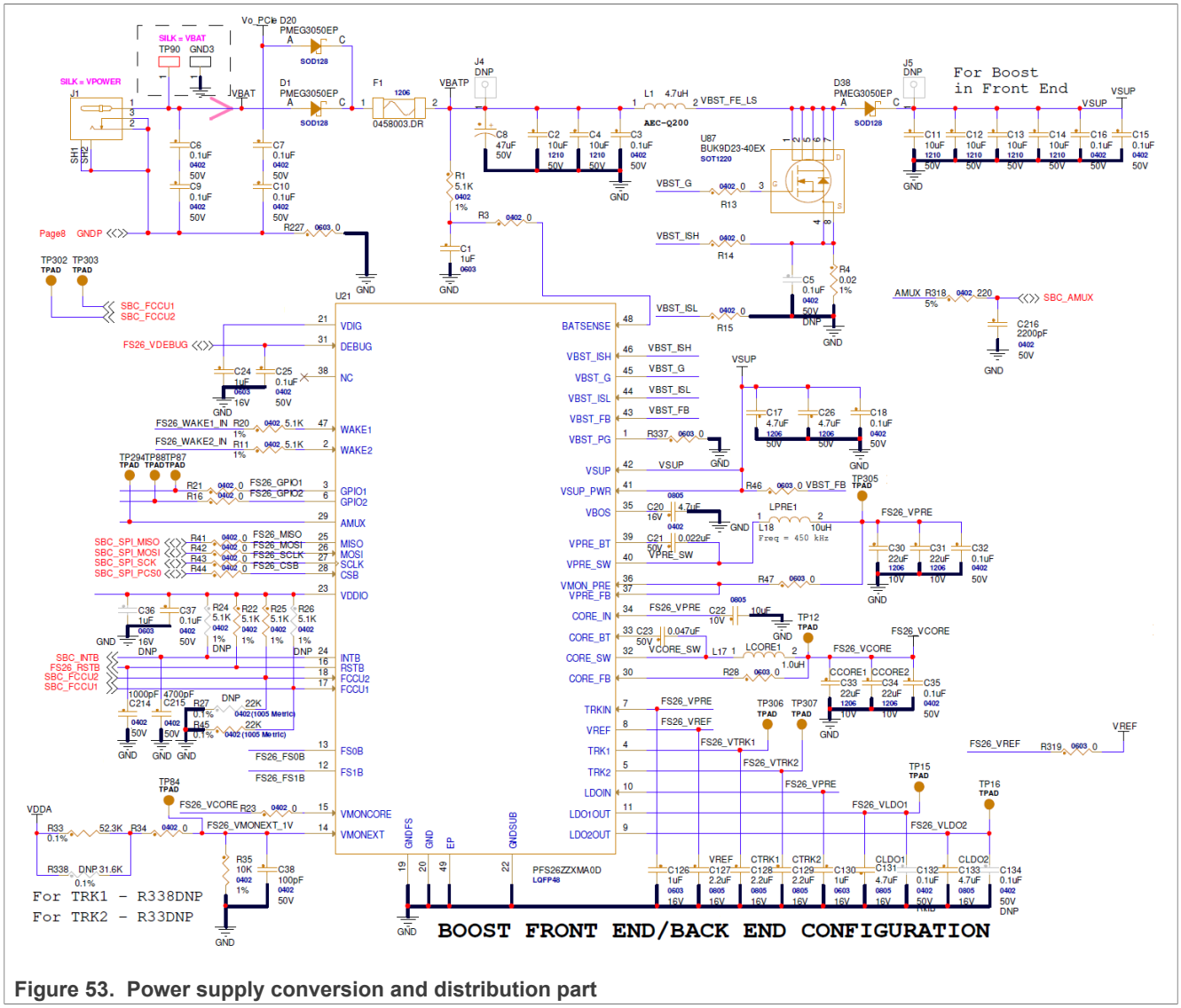


Figure 53. Power supply conversion and distribution part

Second and third output voltage source are created by internal regulators LDO1 and LDO2. The LDO1 generates 5 V and up to 400 mA at the output and LDO2 generates 3.3 V and up to 400 mA at the output. The signals of those voltage outputs are labeled as “FS26_VLDO1” and “FS26_VLDO2” in the schematic. The LDO1 and LDO2 voltage outputs supply both microcontroller voltage domains and digital circuits. Fourth and fifth output voltage sources are voltage tracking regulators TRK1 and TRK2. The TRK1 voltage tracking regulator generates 5 V and up to 150 mA, while TRK2 generates 3.3 V and up to 150 mA. Voltage tracking regulator TRK1 follows LDO1 voltage source, while voltage tracking regulator TRK2 follows LDO2 voltage source. These voltage sources supply analog circuits and signals are labeled as “FS26_VTRK1” and “FS26_VTRK1” in the schematic. The last output voltage source is voltage reference which provides 5 V and up to 30 mA at the output. This voltage reference provides precise and stable output voltage for AD converter, analog measurement circuits, fault logic and resolver signal processing circuit. Figure 54 shows power-up sequence for all power supply sources of SBC FS2613D but also behavior of GPIO pins during start-up.

Table 31. SBC power supply possibilities

	Output Voltage	Maximum Output Current	Precision of output voltage	Purpose
VCORE	1.5 V	800 mA	±2%	MCU core and flash memory

Table 31. SBC power supply possibilities*...continued*

	Output Voltage	Maximum Output Current	Precision of output voltage	Purpose
LDO1	5 V	400 mA	±2%	MCU HV_A domain, digital circuits
LDO2	3.3 V	400 mA	±2%	MCU HV_B domain, digital circuits
TRK1	5 V	150 mA	±2%	Analog circuits
TRK2	3.3 V	150 mA	±2%	Analog circuits (optional)
VREF	5 V	30 mA	±0.75%	ADC reference, measurement circuits

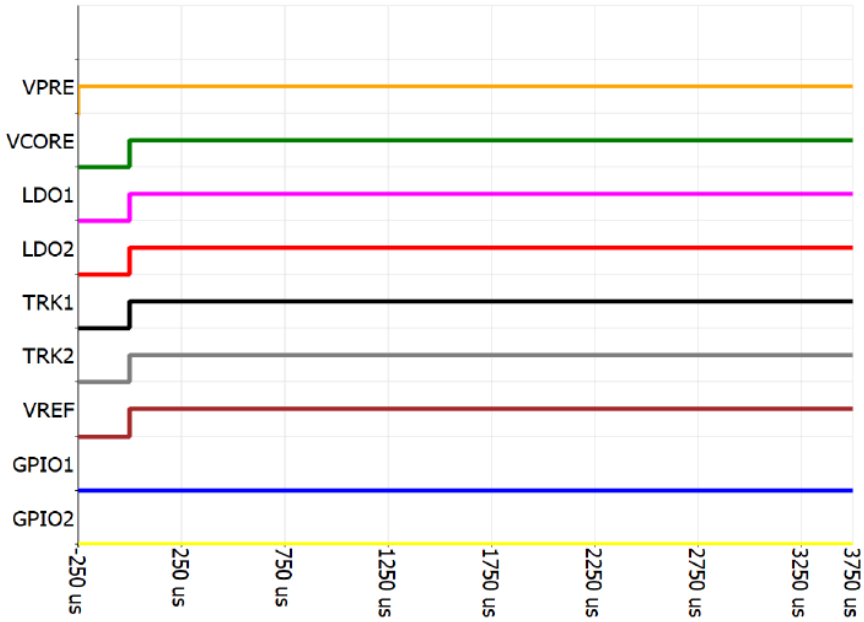


Figure 54. Power-up sequence of FS2613D

Figure 55 shows circuit of signal processing of wake-up, GPIO pins and fault safe outputs of SBC. Beside the power management role, the SBC 2613D can processes four digital signals. They are routed from PCIe connector to the SBC through simple RC adjustment circuits. These signals are primarily used for wake up the system. The “SBC_FS0B” and “SBC_FS1B” signals are used for safe logic located on Adapted board. The role of those signal is to achieve safe state of the system via SBC while any system fault is occurred.

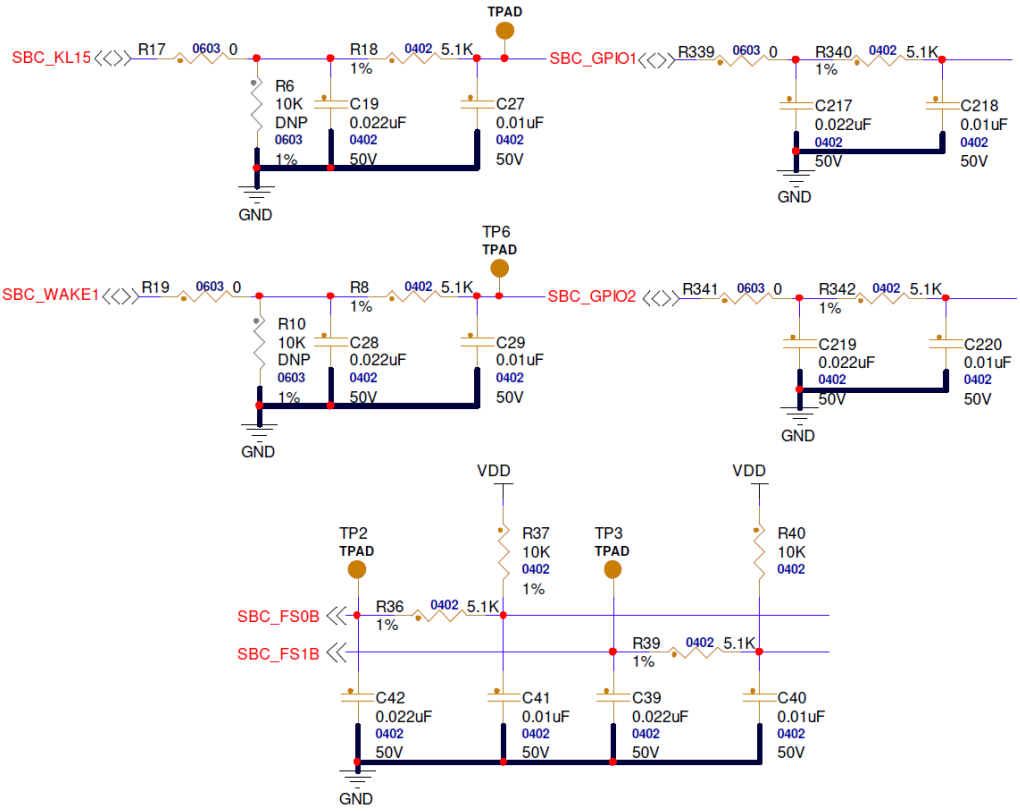


Figure 55. SBC: Input/Output signal processing circuit

Figure 56 shows debug control circuit and power LEDs indicators. The power LEDs indicators signalize function of all power supply outputs of SBC. The debug control circuit ensures debug mode of SBC operation. This mode is intended for first MCU software development, so the watchdog window is infinitely opened, reset (RSTB) counter is disabled and fault safe output “FS0B” is maintained low and cannot be released.

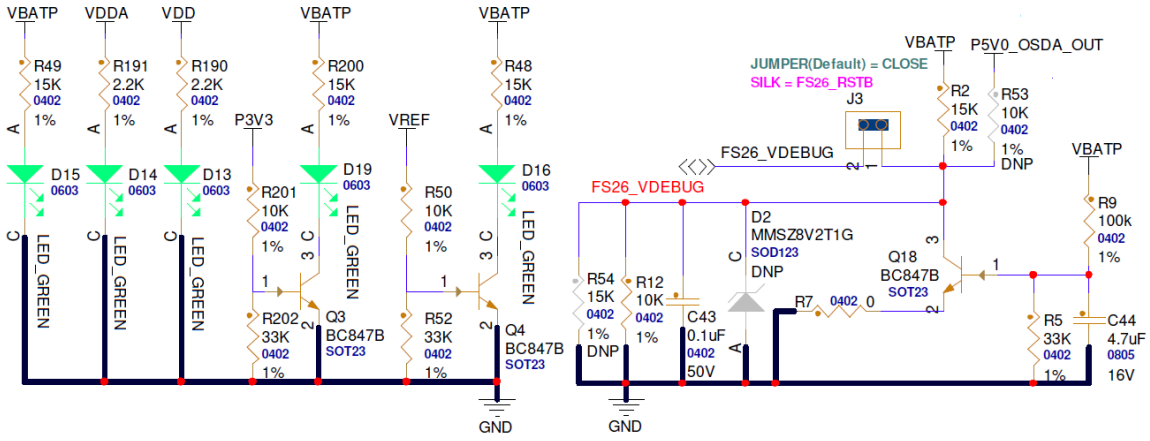


Figure 56. SBC: Debug control circuit and power LEDs indicators

3.6.4 Power supply management

Figure 57 shows power supply outputs distribution situated on Adapter board. The low voltage power supply outputs “VDD”, “VDDA” and “VREF” are directly distributed to the Adapter board communication and

signal processing circuits. The “MCU_SUP” power supply output is distributed among the “MCU_VDD” and “MCU_VCC” signals. The “VDD”, “VDDA”, “VREF” and “MCU_SUP” power supply signals are generated by SBC and transferred through PCIe connector. The “VDD” signal is used for supplying digital and communication circuits, while “VDDA” is used for supplying analog signal processing circuits. The “VREF” provides precise and stable voltage reference signal for analog signal processing circuits and fault logic. The “MCU_SUP” signal is linked with outputs of digital circuits and allows to adjust their voltage level.

The “MCU_VDD” and “MCU_VCC” signals are solely distributed in Adapter board circuits. They are linked with outputs of digital circuits with open collector or open drain configuration and support adjustment of voltage level for microcontroller GPIO pins. The “MCU_VDD” provides 5 V of voltage level adjustment while the “MCU_VCC” provides 3.3 V of voltage level adjustment. Distribution of appropriate voltage level to the “MCU_VDD” and “MCU_VCC” signals is carried out over the 0 Ω resistors R414, R415, R416 and R417. The configuration of those resistors for NXP 48 V MC development platform with S32K344 MCU is depicted in Figure 57.

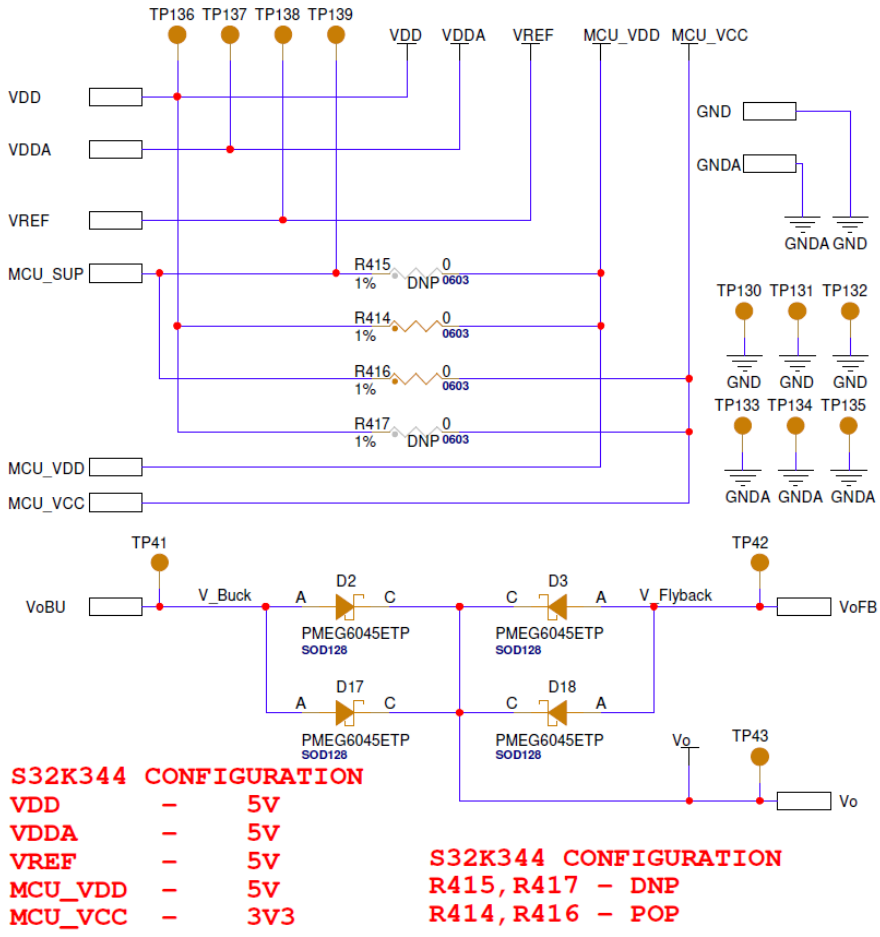


Figure 57. Power supply management

The outputs of Buck converter and Flyback converter are connected to the common node through the diodes D2, D3, D17 and D18 in order to achieve power supply redundancy. Those diodes are connected in common cathode configuration, where the cathode node provides voltage V_o. The output voltage of Buck converter is around 15 V and output voltage of Flyback converter is around 12 V, which is lower than Buck output voltage. Different of output voltage levels of converters enables it to prioritize main power supply source, redundant and provide smooth transition if main power supply source fails. If the Buck converter operates reliably, the V_o voltage represents Buck output voltage V_{oBU} and the current path is created by diodes D2 and D17. In case of

Buck converter malfunction, the V_o voltage represents Flyback output voltage V_{oFB} the current path is created by diodes D3 and D18.

3.7 Resolver signal processing

Resolver sensor can be viewed as two inductive position sensors, which, upon a supplied by sinusoidal shaped signal on the input, generate two sinusoidal signals on the output. The output signals' amplitudes depend on the position of the shaft. The amplitude of first signal is proportional to the sine of rotor position. The amplitude of the second signal is proportional to the cosine of the shaft angle position.

The input (excitation) signal to a resolver, called a resolver reference voltage, and the output signals behave according to following equations:

$$U_{ref} = U_{amp} sin(\omega t) \tag{1}$$

$$U_{sin} = K.U_{ref} sin(\theta) \tag{2}$$

$$U_{cos} = K.U_{ref} cos(\theta) \tag{3}$$

Rotor position can be determined as the inverse tangent function to the amplitudes of the resolver output voltages. The calculation needs to take into account the signs of the measured amplitudes in order to place the computed angle position correctly within a single 360-degree rotation:

$$\theta = atan\left(\frac{U_{sin}}{U_{cos}}\right) \tag{4}$$

The second method (algorithm), widely used for estimation of the rotor angle and speed, is known as an Angle Tracking Observer, for more information refer to AN1942 - 56F80x Resolver Driver and Hardware Interface.

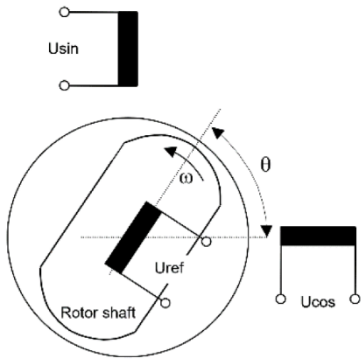


Figure 58. Resolver Principal Schematic

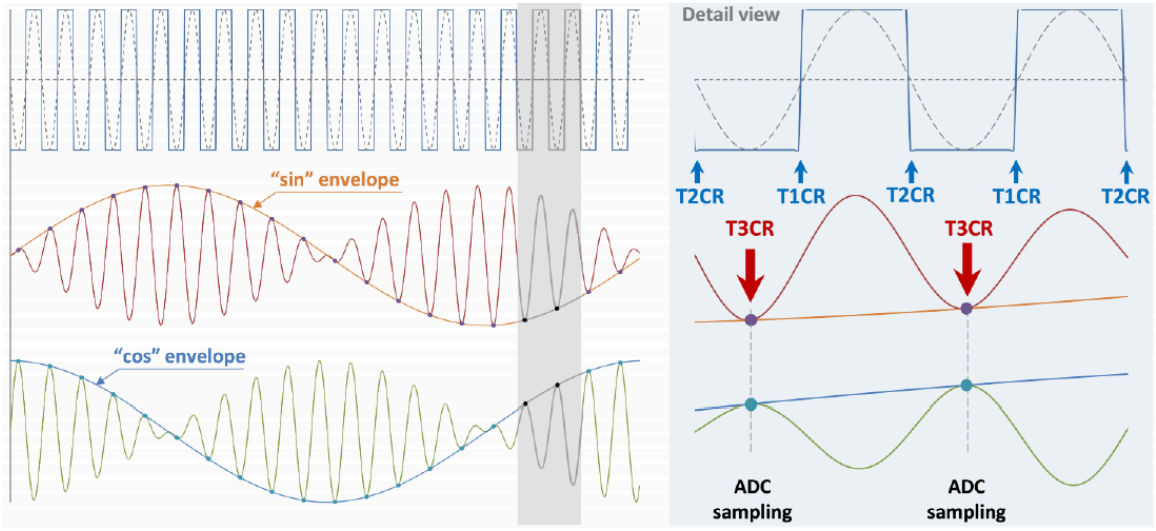


Figure 59. Operation principle of resolver

Figure 58 shows resolver principal schematic and Figure 59 shows resolver operation principle in details. Position carrying sine and cosine signals contain the 10 kHz carrier (excitation) frequency, which can be easily removed when the sampling is synchronized with the excitation signal generator. Further information on application software design can be found in AN1942: 56F80x Resolver Driver and Hardware Interface.

The NXP 48 V MC development platform contains two independent resolver signal processing circuits in order to achieve individual control of two 3-phase PMSM motors.

3.7.1 Hardware interface of resolver circuit

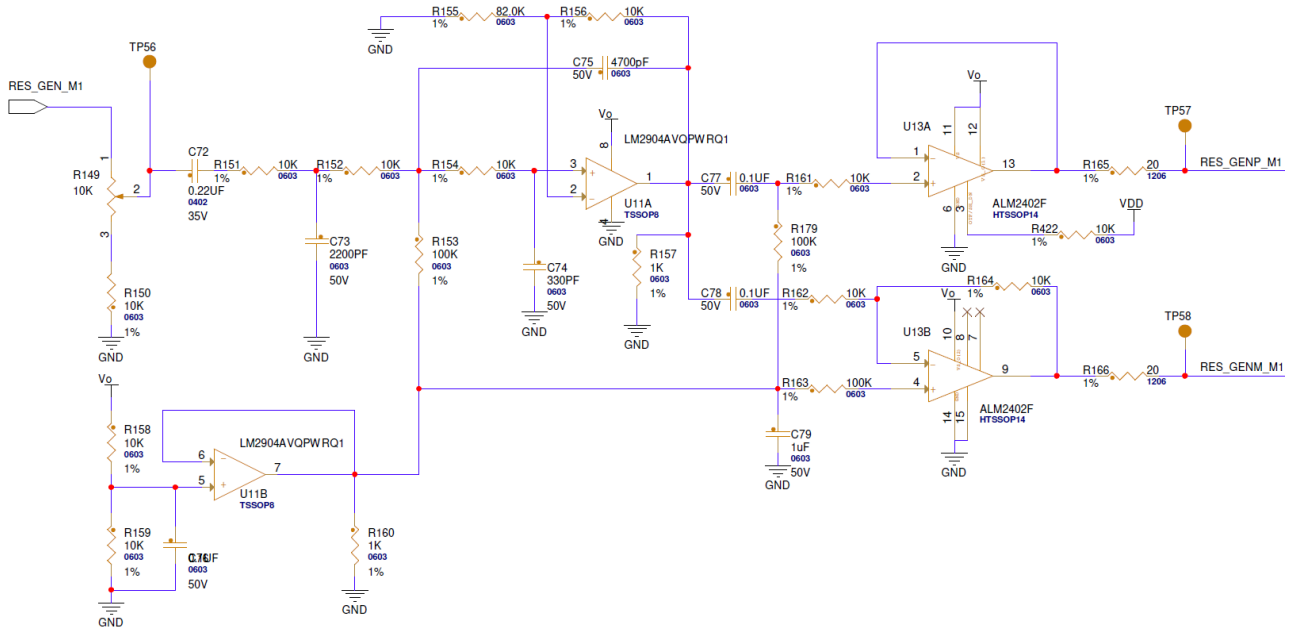


Figure 60. Resolver excitation circuit

Resolver interface circuit consists of hardware part, which processes excitation square wave signal for the resolver reference winding and hardware part, which processes sine/cosine resolver output signal for ADC

module. Processing of square-wave excitation signal is depicted in Figure 60, while processing of sine/cosine signals is depicted in Figure 61.

The resolver driving circuitry shapes a rectangular reference signal from the microcontroller timer output to a sinusoidal waveform. The U11A operational amplifier is a 3rd order Sallen-Key Low-pass filter which transforms the rectangular signal into a sinusoidal wave with DC offset. The U11B operational amplifier generates a virtual ground as a reference for the input signal to achieve symmetrical voltage supply for operational amplifiers. The U13A stage is a voltage-follower, i.e., buffer, to increase the output current for the resolver reference winding. The U13B stage is a differential amplifier for removal of a direct current voltage component in sinusoidal reference signal. The resolver reference winding is connected between output U13A and U13B. The resistors R155 and R156 control the Q factor of filter. The cut-off frequency for filter is set by R151, R152, R154, C73, C74 and C75 components. Stages U11A, U11B, U13A, U13B are powered by voltage from common cathode node of Buck or Flyback converters, which can float from 12 V up to 15 V.

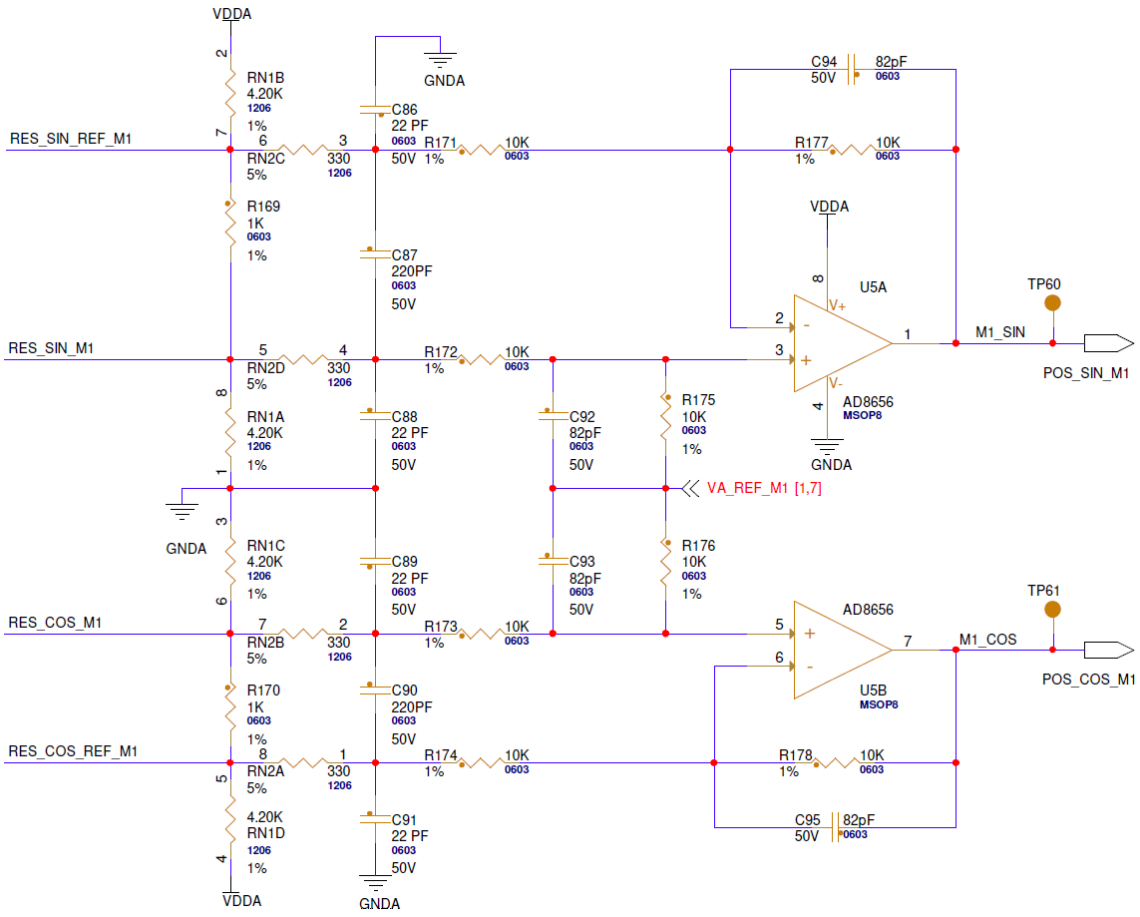


Figure 61. Resolver processing circuit

The resolver sine/cosine signals conditioning circuitry adjusts voltage levels from resolver sin/cos signals to the range acceptable by ADC module. It also carries out level shifting, which places a zero level of the signals to the middle of the ADC range. U5A, U5B amplifiers act as differential unity amplifiers with output level referenced to virtual ground (middle of the VREF). U5A, B amplifiers are rail-to-rail (AD8656) or similar ones capable of 5 V single supply operation. The capacitors C92, C94 and C95, C93 add low pass filtering to suppress unwanted high frequency noise, which is often present in systems with power electronics. The ADC0 (AN0_P5) and ADC1 (AN1_P1) channels are used for measurement of sin/cos signals of first motor configuration and ADC0 (AN0_6) and ADC2(AN2_P6) channels are used for measurement of sin/cos signal of second motor configuration.

The cut-off frequency of the U5A and U5B amplifiers is set according to the resolver reference frequency and should be well above to not affect resolver signals. U5A, B amplifiers should be placed as close as possible to the ADC inputs to avoid noise crosstalk from other components.

All values of the schematic's component given in Figure 60 and Figure 61 are designed for 10 kHz resolver reference frequency for resolver ration 2:1, which is in accordance of motor control sampling frequency. This interface might be adjusted in cases when reference signal frequency or the resolver transformation ratio is different. The gain of the resolver signal conditioning circuitry is unity and therefore the levels on the sin/cos signal inputs must have peak-to-peak amplitude up to the ADC reference voltage (with small headroom to avoid limiting).

Driving circuitry introduces a phase shift between timer output signal and resulting resolver reference waveform. This phase shift together with resolver phase shift and signal conditioning circuitry phase shift are corrected in trigger unit relative to the ADC sampling point, which is in most motor control applications synchronized to PWM. In this way, the sampling at peaks of the sin/cos signals is ensured, resulting in better achieved resolution.

3.8 Hall/Encoder signal processing

Encoder sensor or Hall sensors are used to obtain speed and position of the PMSM or BLDC motors.

3.8.1 Hardware interface

Hall or Encoder sensor signal processing uses passive low pass filters to remove alternating components of the signals. RC filter composed of R140, C65, R141, C66 and R142, C67. The "VDD" power supply signal is used for Hall sensors or Encoder sensor power supply purpose. In addition, this circuit contains U137 triple buffer stage in order meet voltage level of Encoder and particular microcontroller. Encoder and Hall sensor signal processing circuit is doubled in Adapter board for dual motor control.

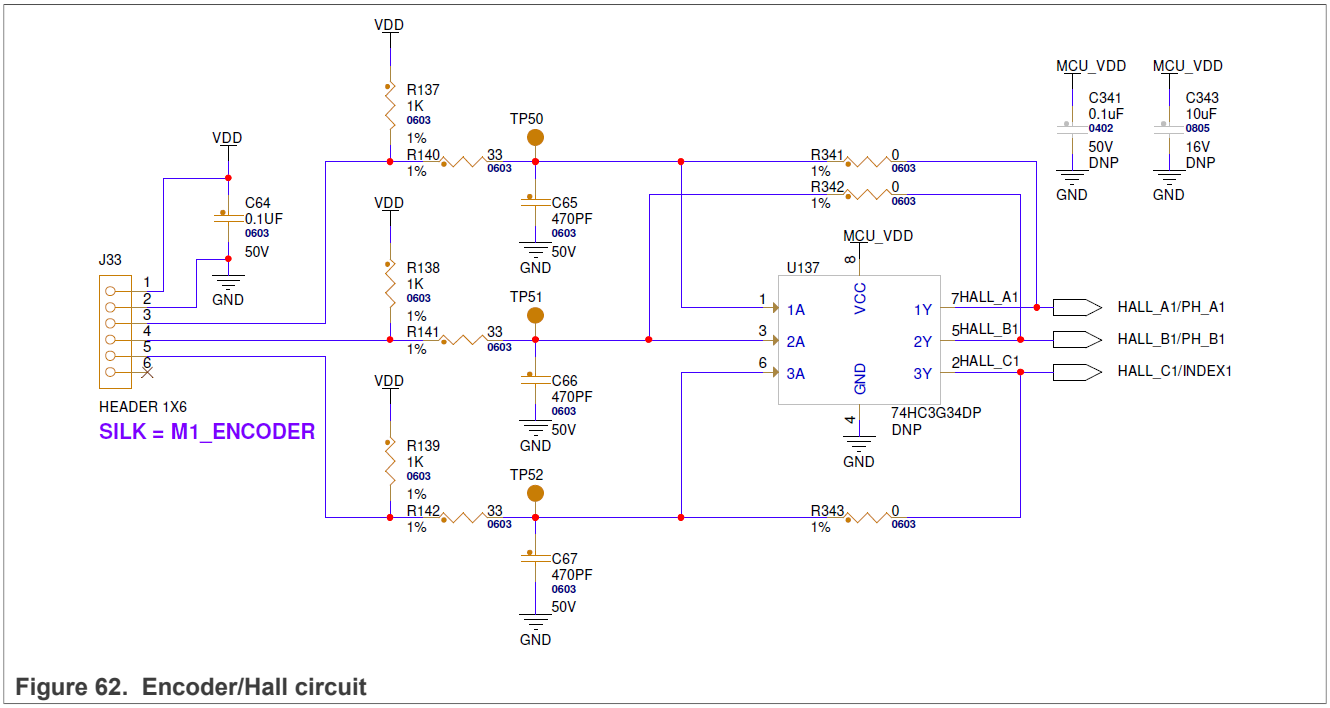


Figure 62. Encoder/Hall circuit

3.9 Fault logic

Fault logic forms an essential part of safe and reliable motor control. Mostly, design of safe logic is realized in embedded software. This approach is less complex, cost optimized and flexible, but also less agile in case of high dynamic systems and depends on reliable software execution. Hardware design of safe logic brings complexity higher cost and lower flexibility, on the other hand it is fully independent from control process and acts immediately. Such approach of fault logic is highly demanded in many safety applications and represents important feature in NXP 48 V MC development platform.

Figure 63 shows overcurrent fault logic circuit based on window comparator scheme with open drain configuration of output for one phase. This arrangement monitors both polarities of sine wave of phase current. Stages U21A and U21B monitor phase current signal, which is filtered at first by low pass RC filter. This filter is composed by R396 and C294 parts. Monitored phase current signal is pulled out from current sensing circuitry, so it is already amplified by operational amplifier. Lower and upper thresholds of current are configurable by resistors R258, R211 and R212, which determine the overcurrent fault at 82% of I_{max}. Maximum range of current sensing is depicted in Table 31. The outputs of overcurrent window comparators for all phases of first 3-phase MOSFET half-bridge are connected to the common node and form single overcurrent state.

The fault state is indicated by logic 0 at output of comparator and is evaluated in measured range of sensing circuit. Jumper J24 allows to select appropriate voltage source used for thresholds setting. By default, it is selected VREF voltage source, because reflects measured range of sensing circuits.

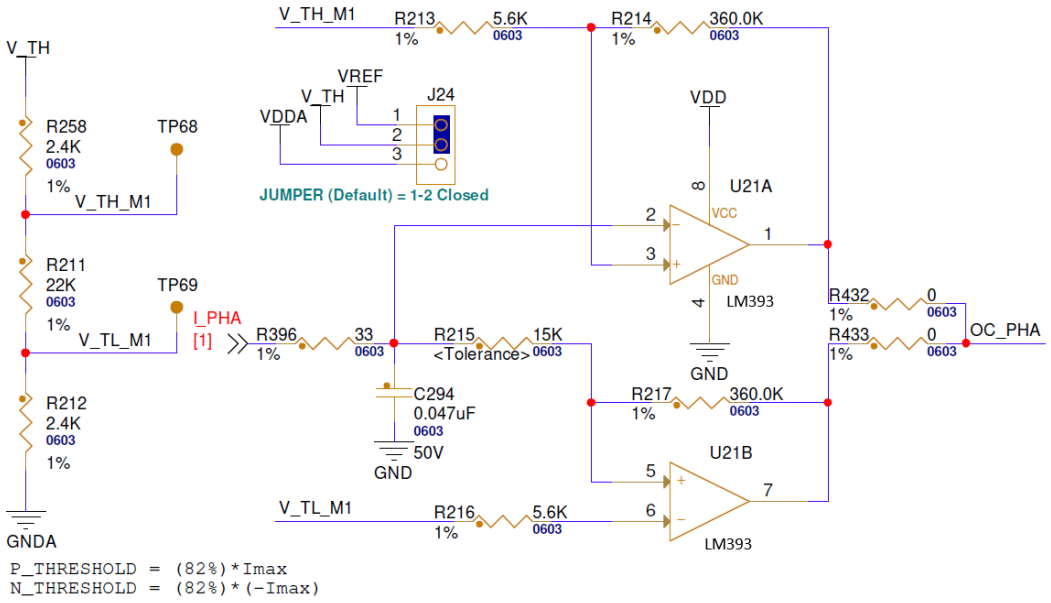


Figure 63. Overcurrent fault logic based on window comparator scheme

Figure 64 shows overvoltage fault logic circuit based on single comparator in open drain configuration and static threshold. Input signal of DC-link voltage is filtered by low pass RC filter. This filter is composed by resistor R246 and capacitor C120. The overvoltage threshold is configured by resistors R366 and R247 and fault state, indicated by logic 0 at output of comparator, is invoked when DC-link voltage exceeds 54 V.

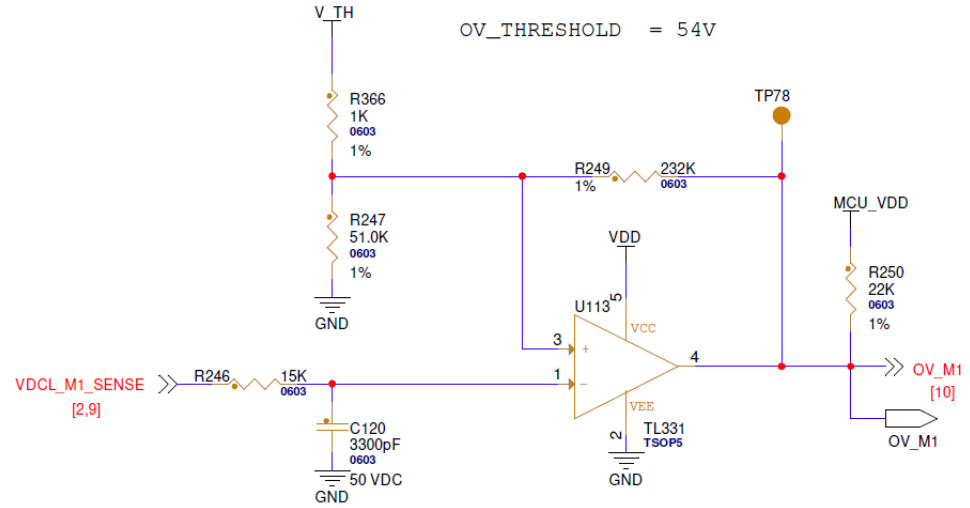


Figure 64. Overvoltage fault logic based on single comparator

Figure 65 shows Buck converter malfunction monitor formed by single comparator with open drain configuration and static threshold. Output voltage of Buck converter is scaled by voltage divider R129 and R130 and filtered by low pass RC filter R131 and C57. The undervoltage threshold is configured by voltage divider R133 and R134. Stage U20 processes both inputs and generate log. 0 at the output in case of low voltage on the output of Buck converter. The output of stage U20 is processed by latch circuit, which holds the fault state. Release of latched fault is carried out by “M1_RESET” or “M2_RESET” signals, which can be selected by jumper J37. In addition, fault of Buck converter is signalized by red LED D11. The voltage level of output of all comparators of fault logic is determined by “MCU_VDD”.

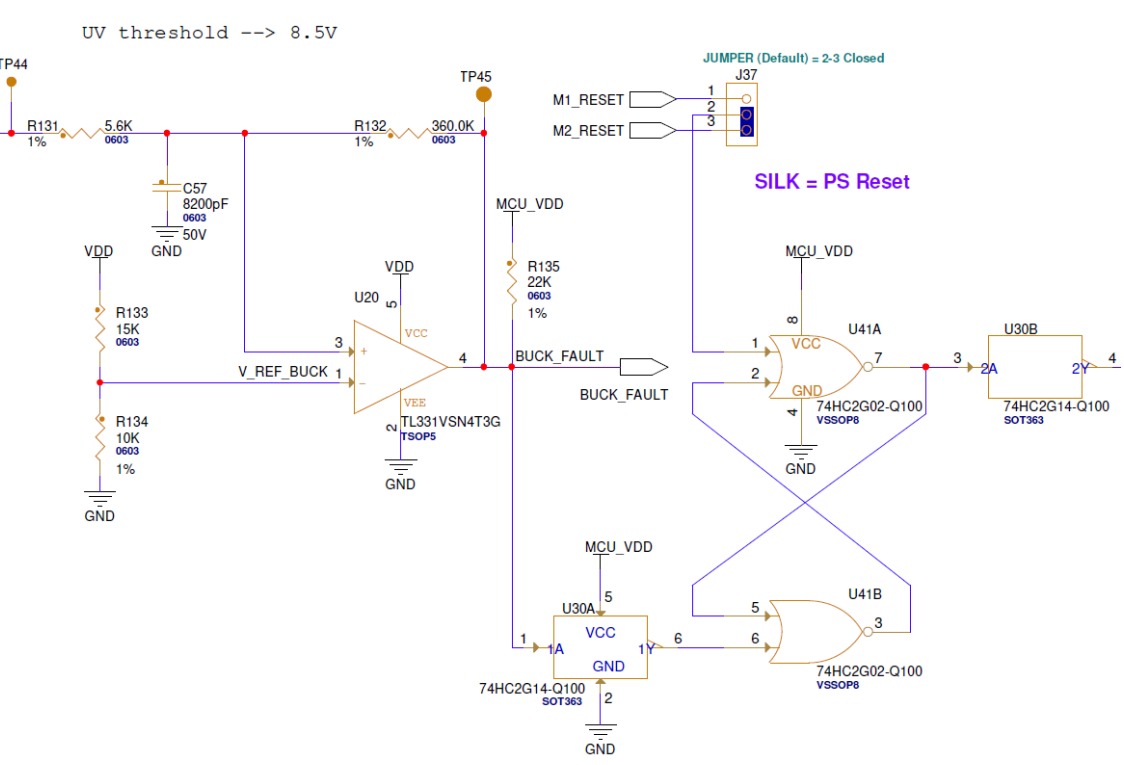


Figure 65. Buck converter malfunction monitor

3.10 Safe logic

Safe logic circuit is in charge of processing fault, control and actuate signals generated by MCU, superior system and fault logic. The safe logic is divided in levels from execution point of view.

First level of safe logic keeps system blocked up by default until it is not enabled by superior system. This execution level ensures deactivation of operation if internal monitoring and fault mechanisms fail.

Second level of safe logic keeps system operation blocked up if any fault state is detected by system internal monitoring and fault mechanisms i.e., over-current, overvoltage faults or SBC fault states, etc.

Third level of safe logic keeps propagation of PWM signals blocked up if they are not generated complementary.

The PWM signals are propagated through the array of logic gates and outputs are behaving according to operation of system. Either there is normal operation and PWM signals are propagated from input of safe logic to the output with slight delay, or there is fault state or situation when 48V system is not responding to the supervisor system and PWM signals are not propagated. Such situation establishes system into safe state. There is an option to select between those safe states:

- Safe open state
- Safe short state

The safe state can be triggered by monitoring mechanisms of system like fault logic or SBC, however it can be triggered by superior system as well. The external trigger from superior system has higher priority than trigger from monitoring mechanisms of system. If execution of control process is stuck and, or doesn’t response to the superior system, operation must be interrupted, and safe state must be formed. In case of any inner system malfunction detection, operation is interrupted by internal mechanisms and safe state is formed too. Both trigger sources can invoke safe open or safe short state. Selection of safe state is determined by user and depends on type of application.

In following lines, hardware design of all levels of safe logic is introduced.

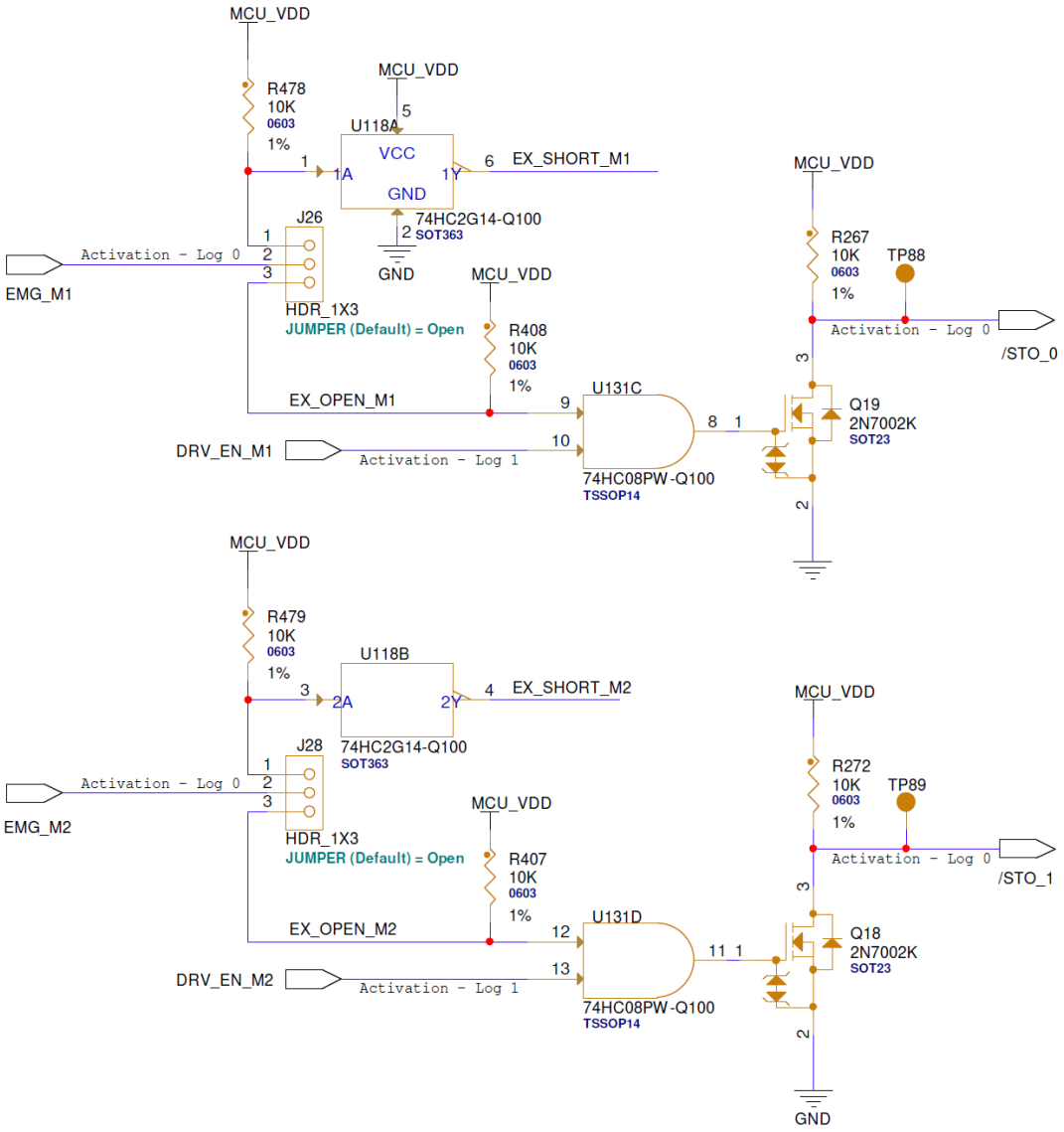


Figure 66. First level of safe logic

Figure 66 shows schematic of first level of safe logic for both 3-phase MOSFET half-bridge configurations. Those circuits consist of signal MOSFETs Q19 and Q18, logic gates U131C, U118A and U131D, U118B, and jumpers J26 and J28. The purpose of these circuits is to process control signals generated by MCU, “DRV_EN_M1” and “DRV_EN_M2”, and external control signals generated by supervisor system, “EMG_M1” and “EMG_M2”. The external control signals are galvanically isolated from 48V system.

The output control signals, “/STO_0” and “/STO_1” of this logic disable the MOSFET gate drivers and interrupt pre-charging of DC-link circuits by logic 1, which is achieved with this circuit topology. Gate drivers are enabled if Q19 and Q18 MOSFETs are turned off. There are two options how those MOSFETs can be turned off.

First option, the Q19 and Q18 MOSFETs are only driven by “DRV_EN_M1” and “DRV_EN_M2” signals respectively. The jumpers J26 and J28 are configured in 1-2 position and additional pull-up resistors R408 and R407 enables to achieve logic 1 on the output of stages U131C and U131D. This option invokes safe short state when system is not responding to the superior system.

Second option, the Q19 and Q18 MOSFETs are driven by two signals, “DRV_EN_M1” and “DRV_EN_M2”, and “EMG_M1” and “EMG_M2” respectively. The jumpers J26 and J28 are configured in 2-3 position and pull-up

resistors R478 and R479 ensure idleness of safe short activation by superior system. This option invokes safe open state only when system is not responding to the superior system.

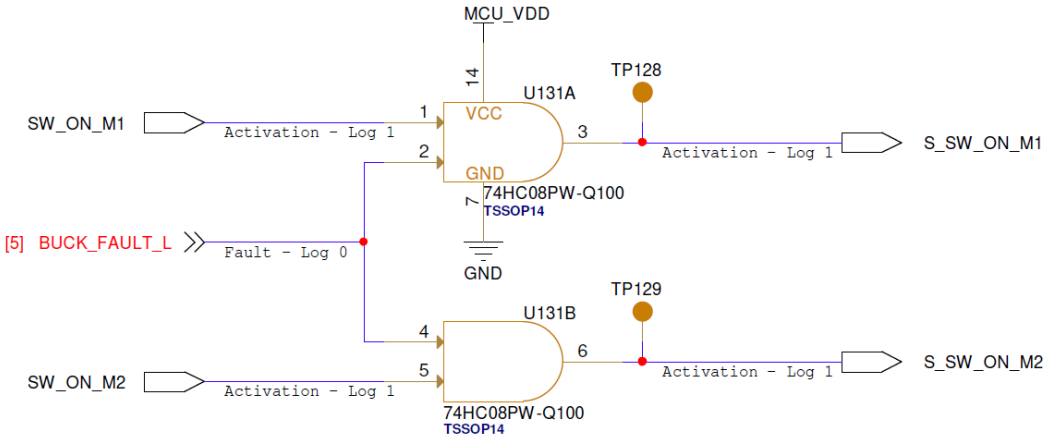


Figure 67. Safe control of DC-link pre-charge

Figure 67 shows circuit of safe control of DC-link pre-charging. It is formed by AND gates U131A and U131B. First input of AND gate represents control signal of microcontroller responsible for enable of DC-link pre-charging. Second input represents latched fault signal of Buck converter malfunction. The purpose of this circuit is to prevent DC-link pre-charging in the situation when Buck converter is faulty and represent second level of safe logic.

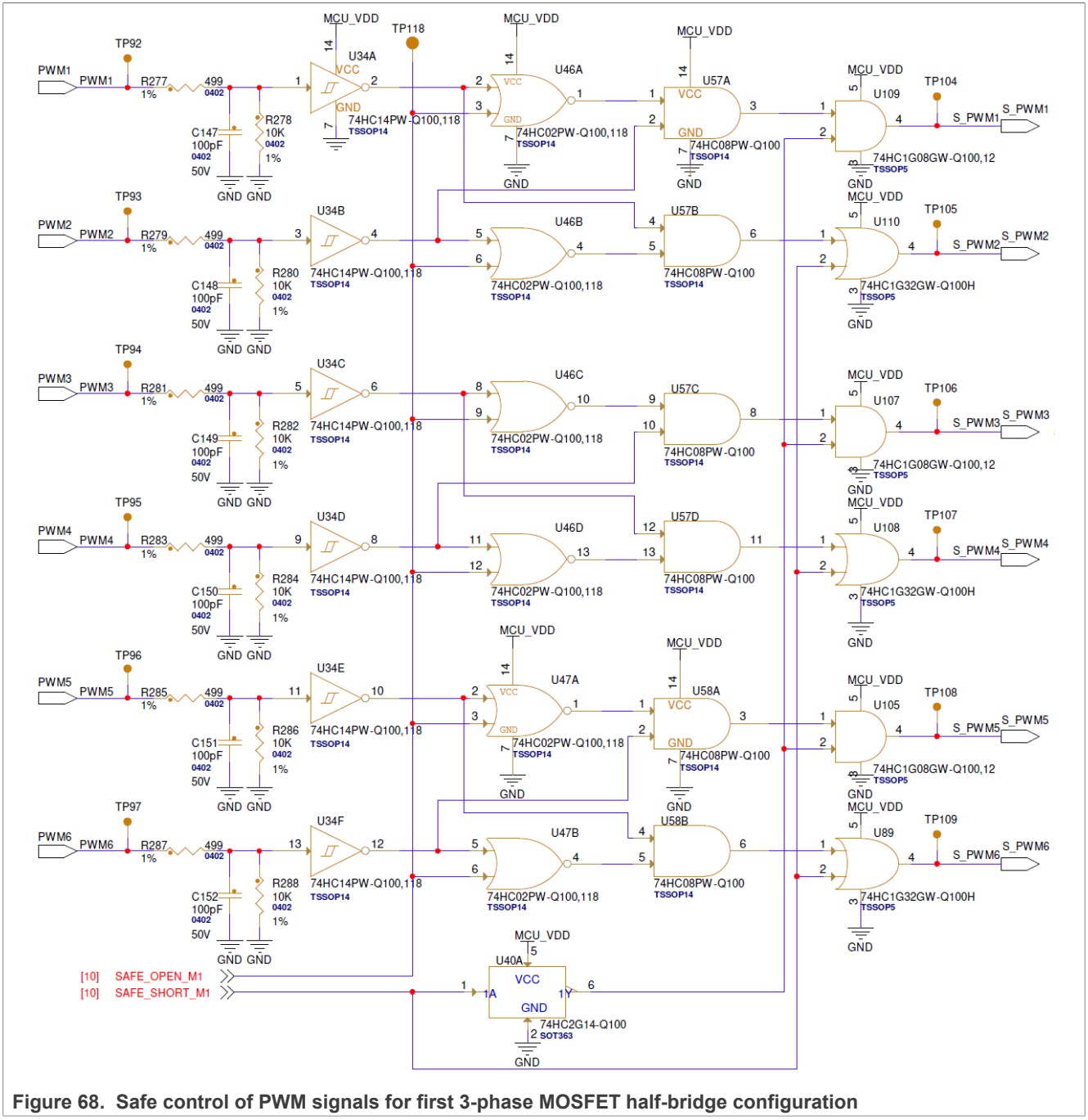


Figure 68. Safe control of PWM signals for first 3-phase MOSFET half-bridge configuration

Figure 68 shows scheme of safe control of PWM signals for first 3-phase MOSFET half-bridge configuration. The safe control of PWM signals for second 3-phase MOSFET half-bridge configuration is identical. This circuit arrangement combines function of second and third level of safe logic. The third level of safe logic is realized by design of logic gates. Input PWM signals are propagated on the output only if they are complementary to each other.

The second level of safe logic is formed of combination of this circuit and by design of circuit depicted in Figure 69.

The purpose circuit depicted in Figure 68 is to process input PWM signals at the output according operation state of system. If system is operating normally and safe state is not invoked, input PWM signals are transferred

trough array of logic gates directly on the output. If system is not operating normally and safe states is invoked, input PWM signals are not transferred trough array of logic gates on the output. The outputs are changed to pre-defined safe state in that case.

If any system fault is detected i.e., over-current, over-voltage or SBC faults, input signal “SAFE_OPEN_M1” changes from logic. 0 to logic 1 and all PWM output signals of logic gates array immediately change the states to logic 0.

If any system fault is detected or supervisor system invoke safe state through “EMG_M1” and header J26 in position 1-2, input signal “SAFE_SHORT_M1” changes from logic. 0 to logic 1. All odd PWM signals immediately change the state to logic 0 and all even PWM signals change the state to logic 1. This safe state forces all low side MOSFETs to be turned-on and forces all high side MOSFETs to be turned-off.

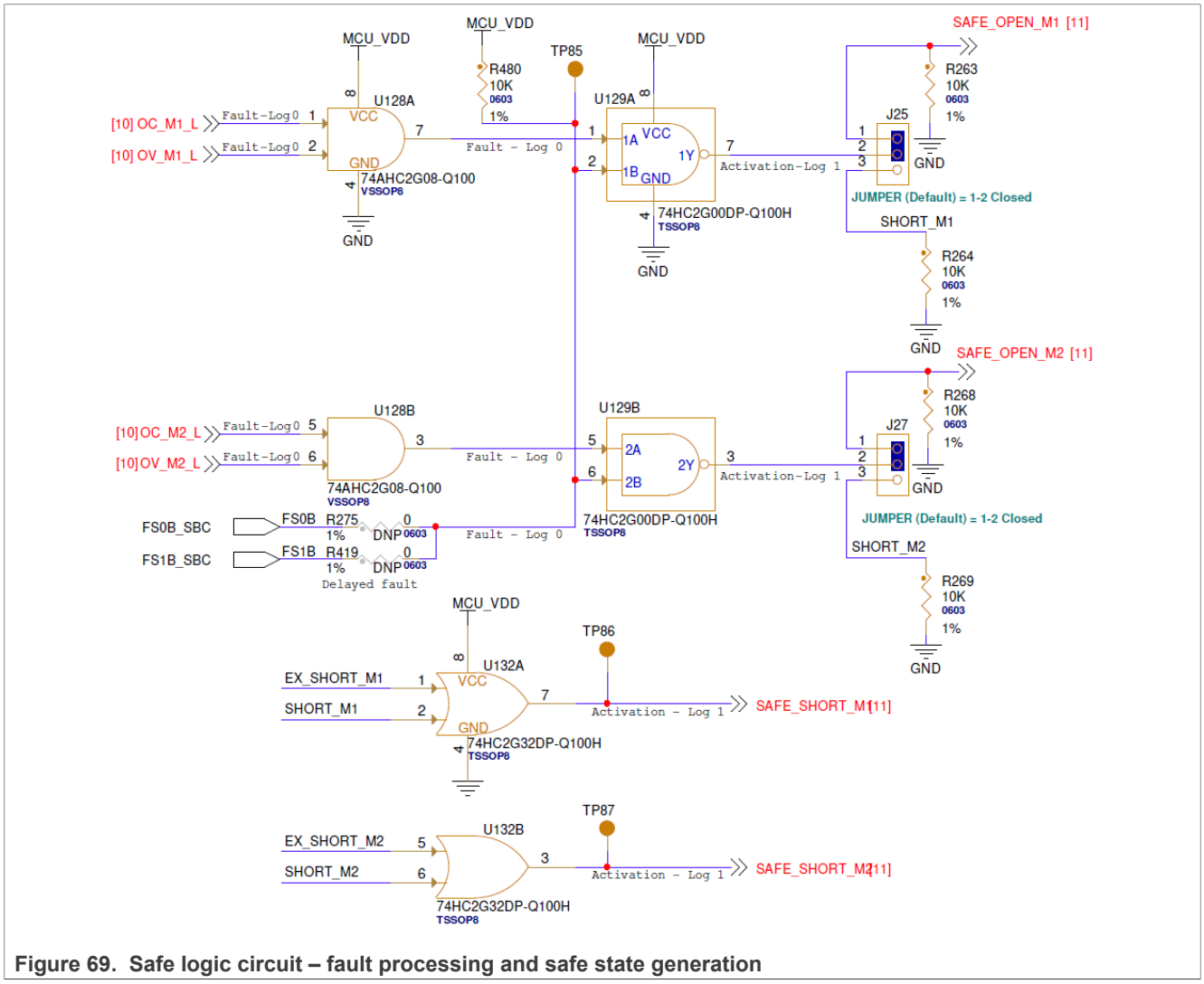


Figure 69. Safe logic circuit – fault processing and safe state generation

Figure 69 shows safe logic circuit which processes system faults and generate safe states. The AND gates U128A and U128B follow latched fault signals of over-currents and over-voltages. The output of AND gate U128A is changed to logic 0, which represent fault detection event, if either over-current or over-voltage fault is detected in the system. There is identical situation of processing fault signals of second 3-phase MOSFET half-bridge configuration by AND gate U128B. The fail-safe signals of SBC “FS0B” or “FS1B” are included to the signal processing of this logic by means of additional NAND gates U129A for first 3-phase MOSFET half-bridge configuration and U129B for second 3-phase MOSFET half-bridge configuration. Additional pull-up resistor

R480 enables to achieve logic 1 on the input of stages U129A and U129B if fail-safe signals of SBC “FS0B” or “FS1B” are not included. The outputs of NAND gates U129A and U129B provide safe state signals for array of logic gates depicted in Figure 68. These safe state signals have an opposite logic level than fault signals. They are connected to the jumpers J25 and J27, which enable to select safe short or safe open state.

If the jumper J25 for first 3-phase MOSFET half-bridge configuration, and the jumper J27 for second 3-phase MOSFET half-bridge configuration are configured in position 1-2, system fault occurrence invokes safe open state.

If the jumper J25 for first 3-phase MOSFET half-bridge configuration and the jumper J27 for second 3-phase MOSFET half-bridge configuration are configured in position 2-3, system fault occurrence invokes safe short state. This safe short state, generated by system monitoring and fault detection logic is merged with safe short state, generated by superior system by means of OR gates U132A for first 3-phase MOSFET half-bridge configuration and OR gate U132B for second 3-phase MOSFET half-bridge configuration.

Activation of safe open state on behalf of supervisor system is managed by circuit depicted in Figure 66. If the jumper J26 for first 3-phase MOSFET half-bridge configuration, and the jumper J28 for second 3-phase MOSFET half-bridge configuration is set in position 2-3, superior system can invoke safe open state by means of “EMG_M1” and “EMG_M2” signals.

If the jumper J26 for first 3-phase MOSFET half-bridge configuration and the jumper J28 for second 3-phase MOSFET half-bridge configuration is set in position 1-2, superior system can invoke safe short state by means of “EMG_M1” and “EMG_M2” signals.

The “EMG_M1” and “EMG_M2” trigger signals of superior system can invoke safe open or safe short state by change of logic 1 to logic 0. In case of signal interruption, normal operation of system is automatically interrupted, and particular safe state is activated.

Table 32 shows safe states configuration, which is carried out by particular jumpers. The safe states generated by system fault mechanisms have lower priority than safe states generated by superior system.

Table 32. Configuration of safe states

Source of safe state activation	**System faults – lower priority**				**Superior system – higher priority**			
Safe state	Safe open		Safe short		Safe open		Safe short	
Jumper	J25	J27	J26	J28	J25	J27	J26	J28
Jumper position	1-2	1-2	2-3	2-3	2-3	2-3	1-2	1-2

3.11 Automotive communication interfaces

The NXP 48 V MC development platform introduces several automotive edge-node communication interfaces like LIN, CAN, or Ethernet. The subsections describe all the communication layers.

3.11.1 LIN communication interface

LIN (Local Interconnect Network) provides simple, single wire serial communication interface compliant with LIN Physical Layer 2.2 specification and with the SAE J2602-2 LIN standard. The LIN communication interface is realized by TJA1021T physical layer. Figure 70 shows schematic of LIN communication interface, which is located on Controller board. This communication layer is not isolated from 48 V MC system and utilizes second “B” voltage domain with 3.3 V voltage level. This LIN transceiver is configured in Commander mode by default. Responder mode configuration would require removing D3 diode.

For more information, please refer to datasheet of TJA1021.

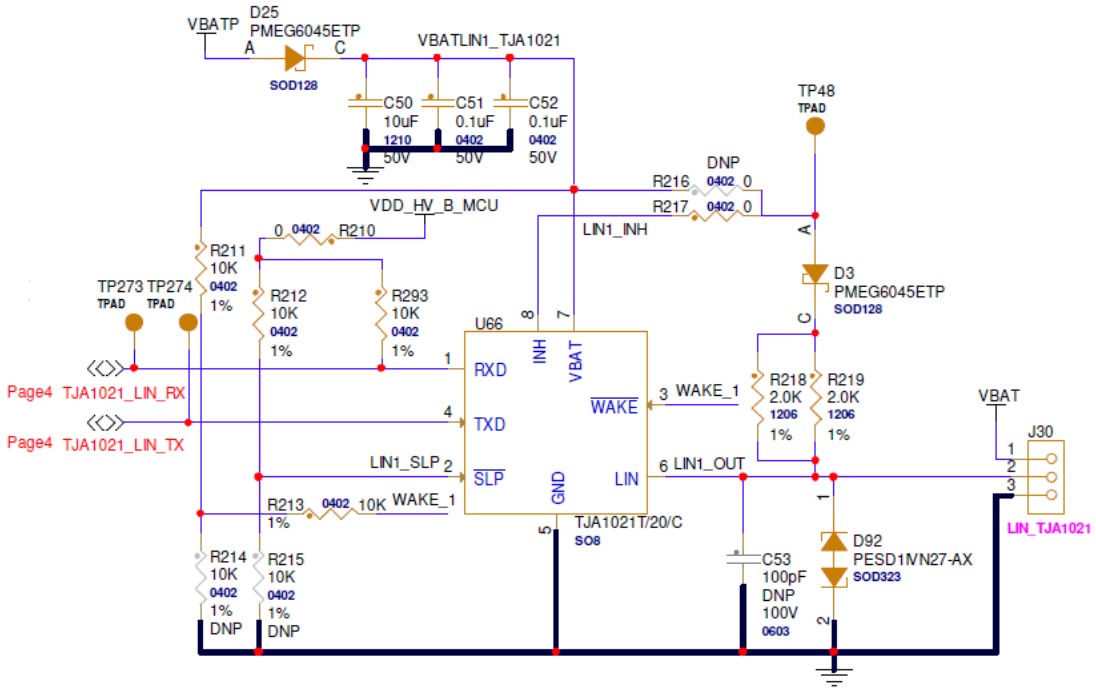


Figure 70. LIN Physical interface schematic

3.11.2 CAN communication interface

The CAN (Controller Area Network) communication interface extends the functionality of the system and provides two-wire CAN-bus connectivity for the standard automotive hi-speed data transfer applications up to 5 Mbit/s. The NXP 48 V MC development platform provides two separate CAN physical layers, which first one provides galvanic isolation and second one provides high speed secure communication. Both transceivers are fully compliant with ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 standards.

Figure 71 shows schematic of CAN communication interface with galvanically isolated transceiver TJA1052i. This communication transceiver is placed on the Adapter board together with other galvanic isolated circuitry, which represents isolated communication and control interface for supervisor systems.

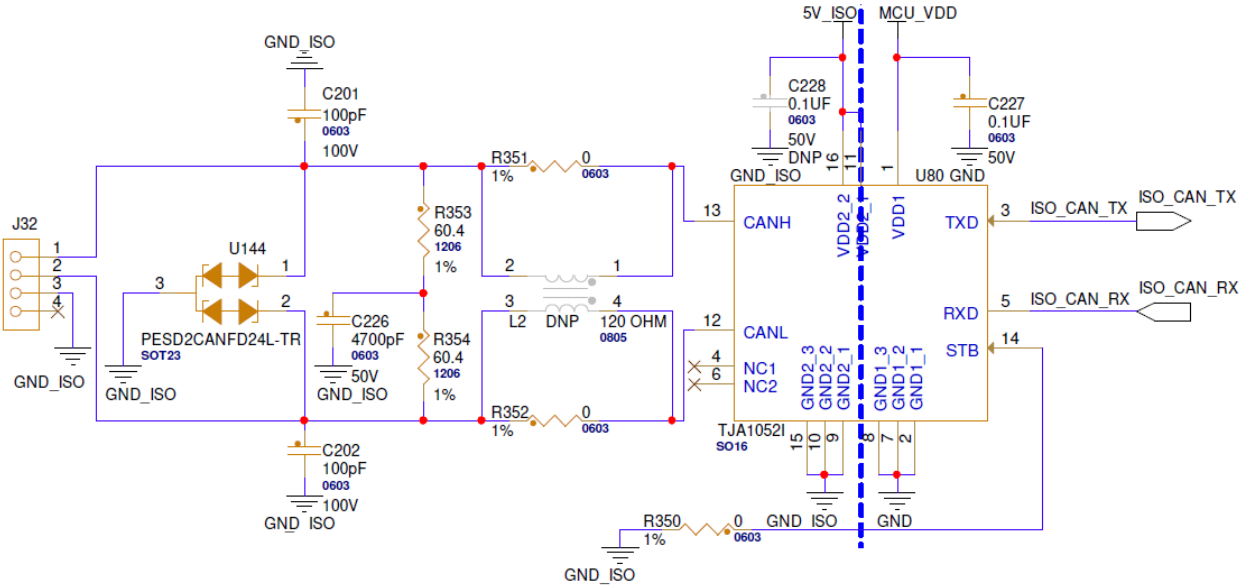


Figure 71. Isolated CAN Physical interface schematic

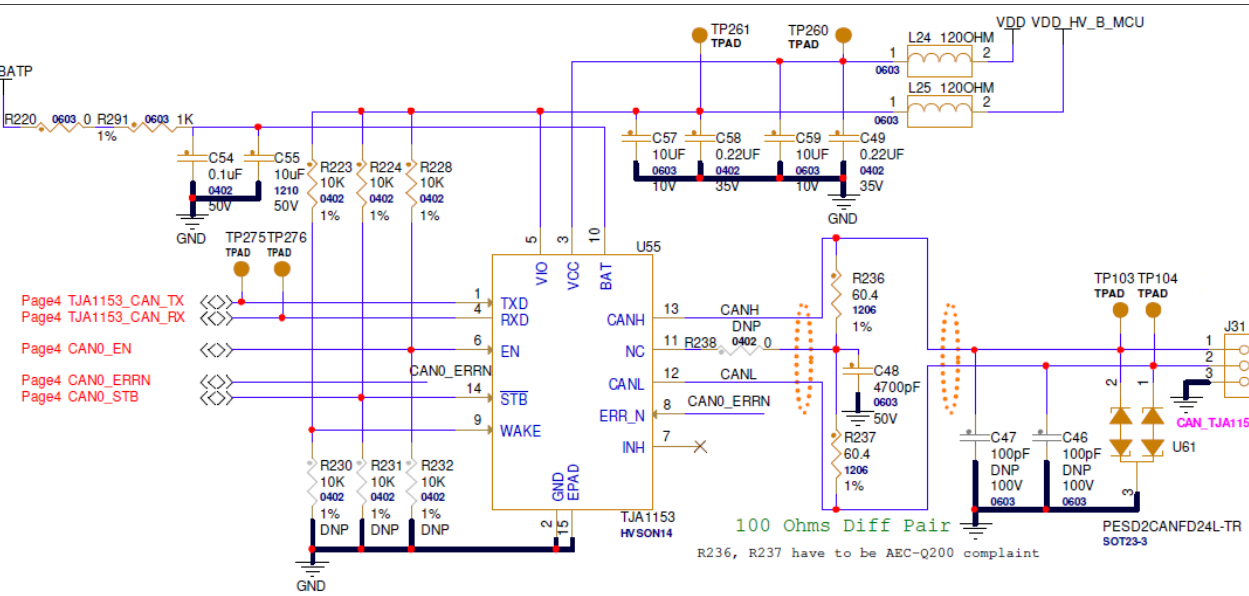


Figure 72. CAN Physical interface schematic

Figure 72 shows schematic of secure CAN communication transceiver, based on TJA1153. This CAN physical layer provides following security functions:

- Spoofing protection:
- Flooding protection
- Tamper protection

For more information, please refer to datasheet of TJA1153.

This CAN transceiver is placed on the Controller board together with S32K344 microcontroller and utilizes voltage domain B with 3.3 V voltage level similarly with LIN transceiver. This communication interface allows to communicate with environment, which does not require galvanic isolation of 48 V level. However, initialization

of the transceiver is required before start-up. For more information about the initialization, please refer to datasheet of TJA1153.

3.11.3 Ethernet communication interface

The TJA1101B is a 100BASE-T1-compliant Ethernet PHY optimized for automotive application use cases such as gateways, IP camera links, radar modules, driver assistance systems and back-bone networks. This physical layer provides 100 Mbit/s transmit and receive capability over a single unshielded twisted-pair cable, supporting a cable length of up to 15 m. The TJA1101B has been designed for automotive robustness and ISO 26262, ASIL-A compliance.

For more details about TJA1101B ethernet communication layer, please refer to datasheet.

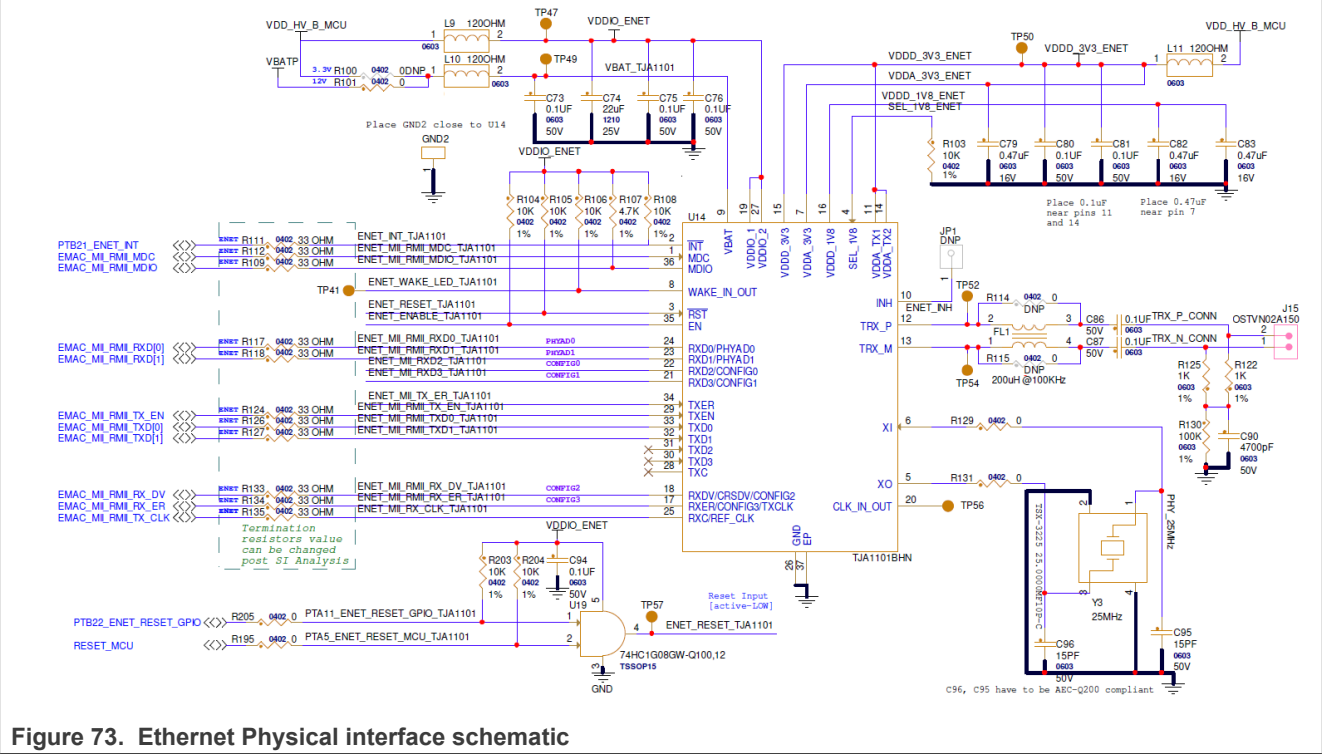
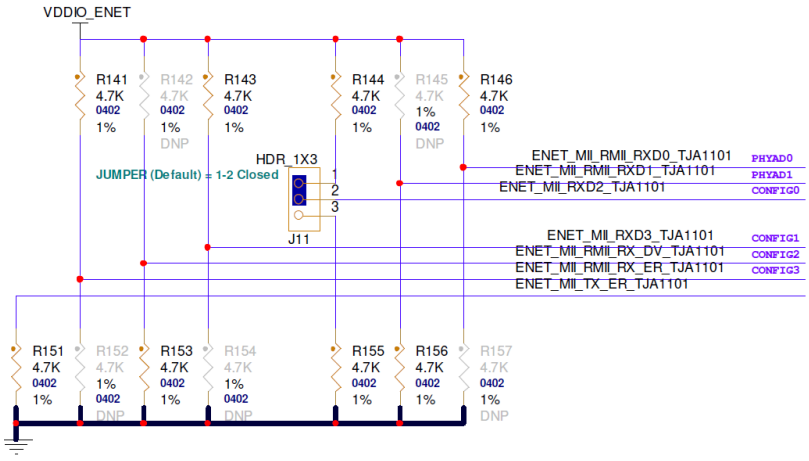


Figure 73. Ethernet Physical interface schematic

Figure 73 shows schematic of Ethernet communication, which is placed on the Controller board and provides non-isolated communication. Ethernet transceiver is linked with microcontroller over pins operated at 3.3 V voltage level. This voltage level is required for most of Ethernet communication interfaces. The clock source is provided by external 25 MHz crystal. The microcontroller reset signal is merged with GPIO port over AND gate, which allows manual reset the Ethernet transceiver over software routine. Output communication signals are connected to simple socket J15. Internal configuration of physical layer is managed by hardware strapping, which is shown in Figure 74. The header J11 is configured in position 1-2 by default.



Hardware Strapping Options

Pin Name	Config	Selected Mode
CONFIG0	LOW	PHY configured as Slave
CONFIG0	HIGH	PHY configured as Master
CONFIG1	HIGH	Autonomous operation
CONFIG2	LOW	RMII mode (25 MHz crystal)
CONFIG3	HIGH	
PHYAD0	HIGH	PHY address bits 0 & 1
PHYAD1	LOW	

Figure 74. Ethernet hardware strapping option

3.12 Board interfaces

The NXP 48 V MC development platform offers several communication interfaces, debug interfaces and control interfaces. Besides of common control and communication interfaces, galvanically isolated interface is used for processing of control signals transferred from superior system. Debugging of motor control algorithm is carried out over on-board debug interface or JTAG interface. The on-board debug interface also offers virtual serial port for FreeMASTER communication.

3.12.1 Galvanically isolated interfaces

The 48V vehicle domain is always separated from 12 V or 24 V voltage domain. Communication of 48V system with 12 V systems in car is usually realized over galvanically isolated interface due to safety reasons. The NXP 48V MC development platform provides galvanically isolated CAN communication interface, which was already introduced in CAN communication interface. However, there is used galvanically isolated control interface for processing of control and wake-up signals.

This subchapter introduces galvanically isolated control interface created by two dual channel digital isolators ADUM1285. Schematic of control interface with two isolators is shown in Figure 75. Control signals are connected to the system through connectors J29 and J40. Two pins of connector J29 are utilized for “EMG_M1_EXT” and “EMG_M2_EXT” trigger signals and one port is used for “KL15” signal. The “KL15” represents ignition signal and it is processed by SBC. Schematic of galvanically isolated “KL15” signal transfer interface is shown in Figure 76. Wake up signals processing is done similarly to the trigger signals “EMG_M1_EXT” and “EMG_M2_EXT”.

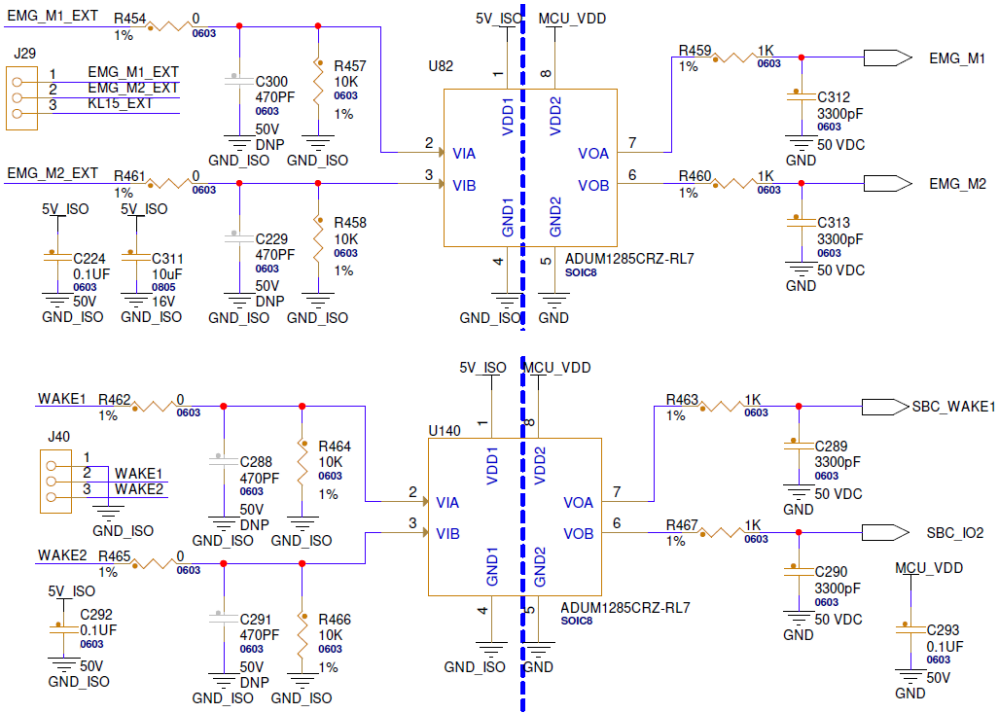


Figure 75. Galvanically isolated control interface for wake-up signals

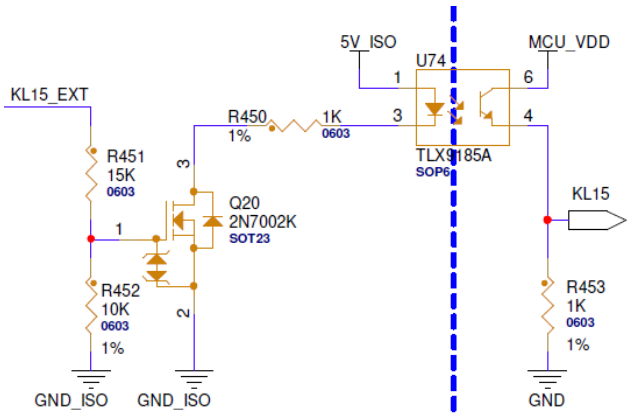


Figure 76. Galvanically isolated control interface for ignition KL15 signal

3.12.2 On-board debug interface

Built-in debug interface is provided to support debugging or flashing the software and to implement the USB-to-Serial communication interface using single USB cable. The microcontroller of on-board debugger (U6, MK26FN2M0VMI18) is preloaded with the necessary software. In case of damage and replacement of the microcontroller, the software must be flashed using connector J14 and external debugger first (e.g., P&E MICRO Cyclone). The software package of on-board debugger is available at https://www.pemicro.com/opensda/.

If the software is outdated, the P&E driver will be automatically downloaded and updated during debug process.

When the system is connected to the computer, USB device installs virtual serial communication port as well. If not recognized by your system, please download the latest drivers for your system at https://www.pemicro.com/opensda/.

4 Application Support

4.1 Toolset

NXP Semiconductors provides a set of documentation and software tools to speed up your development. More documents and software can be found at S32K3 web page.

Table 33. Recommended documentation and software tools

Tools	Description
S32K3 web page	S32K3 MCU family web page
S32K3xx RM	S32K3 MCU Reference manual
S32K3xx DS	S32K3 MCU Datasheet
https://www.nxp.com/s32-design-studio	S32 Design Studio for S32 Platform – Development Environment for ARM S32 MCUs
https://www.nxp.com/ammclib	Automotive Math and Motor Control Library Set web page
https://www.nxp.com/FREEMASTER	FreeMASTER Run-time debug tool
https://www.nxp.com/MCAT	MCAT: Motor Control Application Tuning tool
https://www.nxp.com/RTD	Combines SDK and MCAL environments in one software product
https://www.nxp.com/MBDT	Model based design toolbox
https://www.nxp.com/automcdevkits	Automotive Development Kits web page
AN13414	Migration Guide for S32K Devices: S32K1 to S32K3 Migration Guidelines
AN13767	3-phase Sensorless PMSM Motor Control Kit with S32K344 using RTD Low Level API
AN4912	Tuning 3-Phase PMSM Sensorless control application using MCAT Tool
AN13435	SDK/MCAL to Real Time Drivers: Migration Guide

4.2 Step-by-step instructions

1. Make sure that all three boards of NXP 48 V MC development platform are connected together (see Figure 9).
2. Check the jumper settings of Adapter board and Controller board (see Table 5 and Table 16).
3. Connect the power supply:
   a. Use 12 V power supply source with stabilized output and power range at least 2A. Connect this power supply source to terminal J39 on Adapter board.
   b. Use 48 V power supply with stabilized output and appropriate power range. Please note that charging the DC-bus capacitors may induce high current peak. Laboratory DC power supply of 48 V / 100 A covers most of application use-cases for this type of hardware.
   c. Use M5 ring-eye connectors and proper wiring. Use shielded cables or other methods to prevent emission if needed.
4. Check following Controller board LEDs:
   a. LED D15 (green) indicates proper operation of Buck converter supply voltage (48 V input).
   b. LED D14 (green) indicates the supply voltage of VDDA.

c. LED D13 (green) indicates the supply voltage of VDD.
d. LED D19 (green) indicates the supply voltage of 3V3.
e. LED D16 (green) indicates the supply voltage of VREF.

5. Connect the Controller board to the PC using the USB cable. Allow the PC to automatically configure the USB drivers if needed. In case drivers are not found, please visit https://www.pemicro.com/opensda/ and follow the instructions to install PEDrivers. Please try to avoid USB hubs and use direct connection with PC. The LED D8 (orange) signalizes on-board debugger proper connection with the PC.
6. Re-program the MCU using S32 Design studio for S32 platform v3.5.
   a. In case of error, try to reconnect the USB cable or check the P&E Micro drivers are installed properly. If the MCU is not responding, check the LED indicators and voltages using a multimeter or an oscilloscope.
7. Switch off the power supply.
8. Connect motor speed/position sensors:
   a. Connector J33 for Hall/Encoder of first 3-phase PMSM motor or 6-phase PMSM motor.
   b. Connector J34 for Hall/Encoder of second 3-phase PMSM motor.
   c. Connector J35 for resolver of first 3-phase PMSM motor or 6-phase PMSM motor.
   d. Connector J36 for resolver of second 3-phase PMSM motor.
9. Connect one or two motors. Use M5 ring-eye connectors and proper wiring. Use shielded cables or other methods to prevent emission if needed. Please note that the order of phases impacts the direction of rotation:
   a. First 3-phase PMSM motor is connected to the PHASE_U1, PHASE_V1, PHASE_W1 terminals.
   b. Second 3-phase PMSM motor is connected to the PHASE_U2, PHASE_V2, PHASE_W2 terminals.
   c. The 6-phase PMSM motor is connected to the PHASE_U1, PHASE_V1, PHASE_W1, PHASE_U2, PHASE_V2, PHASE_W2 terminals.
10. Switch on the power supply and reconnect the USB connection.
11. Start the FreeMASTER application for control and tune the motor control application.

5 Revision history

Table 34. Revision history

Document ID	Release date	Description
UG10246 v.2.0	10 November 2025	• Updated Table 1
UG10246 v.1.0	13 June 2025	• Initial release

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