UG10111

MCX Nx4x TSI User Guide

Rev. 1 — 7 May 2024 User guide

Document information

Information	Content
Keywords	MCX, MCX Nx4x, TSI, touch.
Abstract	The Touch Sensing Interface (TSI) of the MCX Nx4x series is the upgraded IP with new features to implement the baseline/threshold autotuning.

1 Introduction

The MCX N series of the Industrial and IoT (IIoT) MCU feature dual Arm Cortex-M33 cores operates up to 150 MHz. The MCX N series are high-performance, low-power microcontrollers with intelligent peripherals and accelerators providing multitasking capabilities and performance efficiency. The Touch Sensing Interface (TSI) of the MCX Nx4x series is the upgraded IP with new features to implement the baseline/threshold autotuning.

2 MCX Nx4x TSI overview

TSI provides touch-sensing detection on capacitive touch sensors. The external capacitive touch sensor is typically formed on PCB and the sensor electrodes are connected to the TSI input channels through the I/O pins in the device.

2.1 MCX Nx4x TSI block diagram

MCX Nx4x has one TSI module and supports 2 kinds of touch sensing methods, the self-capacitance (also called self-cap) mode and the mutual-capacitance (also called mutual-cap) mode.

The block diagram of MCX Nx4x TSI I shown in Figure 1:

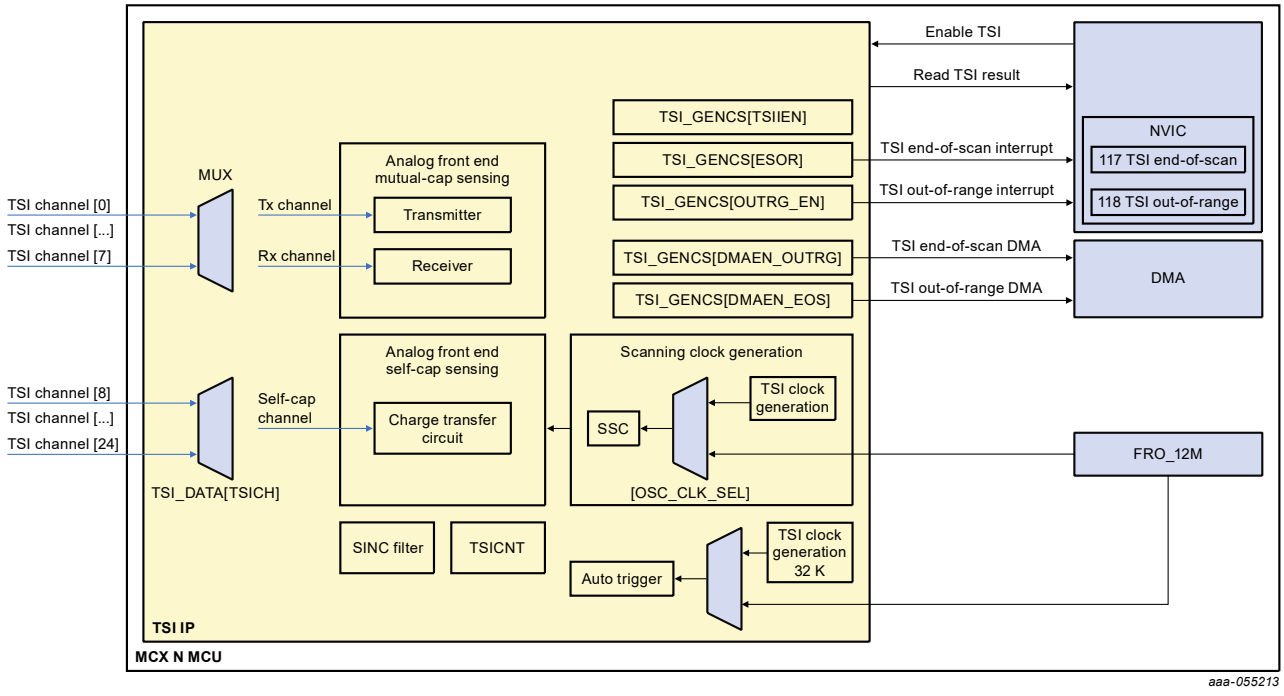

Figure 1. MCX Nx4x TSI block diagram

The TSI module of MCX Nx4x has 25 touch channels. 4 of these channels can be used as shield channels to enhance the drive strength of touch channels.

The 4 shield channels are used to enhance the liquid tolerance and improve the driving ability. The enhanced driving ability also enables users to design a larger touchpad on the hardware board.

The TSI module of MCX Nx4x has up to 25 touch channels for self-cap mode and up to 8 x 17 touch channels for mutual-cap mode. Both mentioned methods can be combined on a single PCB, but the TSI channel is more flexible for Mutual-cap mode. The TSI[0:7] are TSI Tx pins and TSI[8:25] are TSI Rx pins in Mutual-cap mode.

In self-capacitive mode, developers can use 25 self-cap channels to design 25 touch electrodes.

In mutual-capacitive mode, design options expand to up to 136 (8 x 17) touch electrodes.

Several use cases such as a multiburner induction cooker with touch controls, touch keyboards, touchscreen, require a lot of touch key design. The MCX Nx4x TSI can support up to 136 touch electrodes when mutual-cap channels are used.

The MCX Nx4x TSI can expand more touch electrodes to meet the requirements of multiple touch electrodes. Some new features have been added to make the IP easier to be used in low-power mode. TSI has advanced EMC robustness, which makes it suitable for use in industrial, home appliance, and consumer electronics applications.

2.2 MCX Nx4x parts supported TSI

Table 1 shows the number of TSI channels corresponding to different parts of the MCX Nx4x series. All these parts support one TSI module that has 25 channels.

Table 1. MCX Nx4x parts supporting TSI module

Parts	Frequency [Max] (MHz)	Flash (MB)	SRAM (kB)	TSI [Number, channels]	GPIOs	Package type
MCXN546VDFT	150	1	352	1 x 25	124	VFBGA184
MCXN546VNLT	150	1	352	1 x 25	74	HLQFP100
MCXN547VDFT	150	2	512	1 x 25	124	VFBGA184
MCXN547VNLT	150	2	512	1 x 25	74	HLQFP100
MCXN946VDFT	150	1	352	1 x 25	124	VFBGA184
MCXN946VNLT	150	1	352	1 x 25	78	HLQFP100
MCXN947VDFT	150	2	512	1 x 25	124	VFBGA184
MCXN947VNLT	150	2	512	1 x 25	78	HLQFP100

2.3 MCX Nx4x TSI channel assignment on different packages

Table 2. TSI channel assignment for MCX Nx4x VFBGA and LQFP packages

184BGA ALL	184BGA ALL pin name	100HLQFP N94X	100HLQFP N94X pin name	100HLQFP N54X	100HLQFP N54X pin name	TSI channel
A1	P1_8	1	P1_8	1	P1_8	TSI0_CH17/ADC1_A8
B1	P1_9	2	P1_9	2	P1_9	TSI0_CH18/ADC1_A9
C3	P1_10	3	P1_10	3	P1_10	TSI0_CH19/ADC1_A10
D3	P1_11	4	P1_11	4	P1_11	TSI0_CH20/ADC1_A11
D2	P1_12	5	P1_12	5	P1_12	TSI0_CH21/ADC1_A12
D1	P1_13	6	P1_13	6	P1_13	TSI0_CH22/ADC1_A13
D4	P1_14	7	P1_14	7	P1_14	TSI0_CH23/ADC1_A14
E4	P1_15	8	P1_15	8	P1_15	TSI0_CH24/ADC1_A15
B14	P0_4	80	P0_4	80	P0_4	TSI0_CH8
A14	P0_5	81	P0_5	81	P0_5	TSI0_CH9
C14	P0_6	82	P0_6	82	P0_6	TSI0_CH10
B10	P0_16	84	P0_16	84	P0_16	TSI0_CH11/ADC0_A8

Table 2. TSI channel assignment for MCX Nx4x VFBGA and LQFP packages*...continued*

184BGA ALL	184BGA ALL pin name	100HLQFP N94X	100HLQFP N94X pin name	100HLQFP N54X	100HLQFP N54X pin name	TSI channel
A10	P0_17	85	P0_17	85	P0_17	TSI0_CH12/ADC0_A9
C10	P0_18	86	P0_18	86	P0_18	TSI0_CH13/ADC0_A10
C9	P0_19	87	P0_19	87	P0_19	TSI0_CH14/ADC0_A11
C8	P0_20	88	P0_20	88	P0_20	TSI0_CH15/ADC0_A12
A8	P0_21	89	P0_21	89	P0_21	TSI0_CH16/ADC0_A13
C6	P1_0	92	P1_0	92	P1_0	TSI0_CH0/ADC0_A16/CMP0_IN0
C5	P1_1	93	P1_1	93	P1_1	TSI0_CH1/ADC0_A17/CMP1_IN0
C4	P1_2	94	P1_2	94	P1_2	TSI0_CH2/ADC0_A18/CMP2_IN0
B4	P1_3	95	P1_3	95	P1_3	TSI0_CH3/ADC0_A19/CMP0_IN1
A4	P1_4	97	P1_4	97	P1_4	TSI0_CH4/ADC0_A20/CMP0_IN2
B3	P1_5	98	P1_5	98	P1_5	TSI0_CH5/ADC0_A21/CMP0_IN3
B2	P1_6	99	P1_6	99	P1_6	TSI0_CH6/ADC0_A22
A2	P1_7	100	P1_7	100	P1_7	TSI0_CH7/ADC0_A23

Figure 2 and Figure 3 show the assignment of dual TSI channels on the two packages of MCX Nx4x. In the two packages, the pins marked in green are the location of the TSI channel distribution. To make reasonable pin assignment for hardware touch board design, refer to pin location.

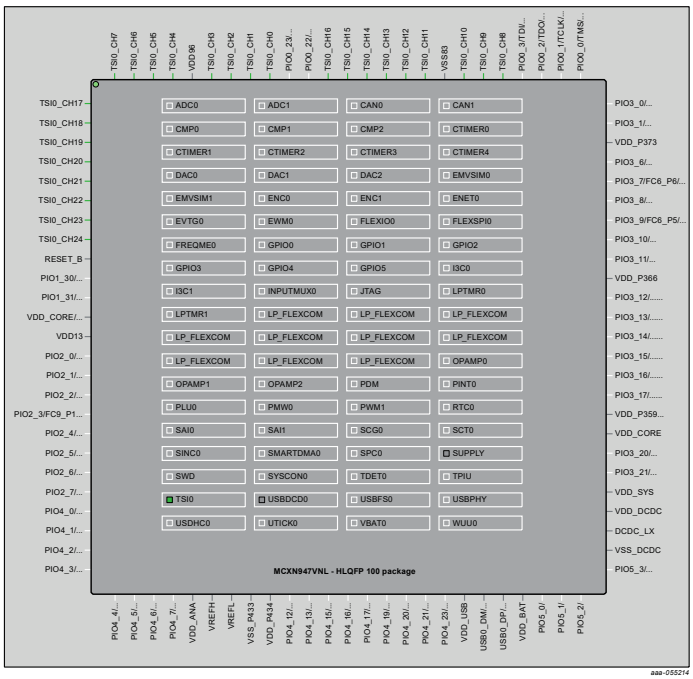

Figure 2. TSI channel assignment of MCX Nx4x 100LQFP and 164VFBGA

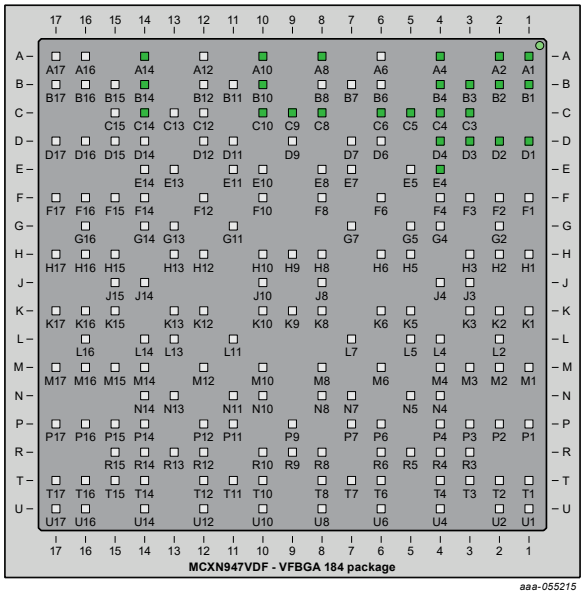

Figure 3. TSI channel assignment of MCX Nx4x 100LQFP and 164VFBGA

3 MCX Nx4x TSI features

This section gives the detals of MCX Nx4x TSI features.

3.1 TSI comparison between MCX Nx4x TSI and Kinetis TSI

MCX Nx4x of TSI and TSI on the NXP Kinetis E series TSI are designed on different technology platforms. Therefore, from the basic features of TSI to the registers of TSI, there are differences between MCX Nx4x TSI and TSI of the Kinetis E series. Only the differences are listed in this document. To check the TSI registers, use the reference manual.

This chapter describes the features of MCX Nx4x TSI by comparing it to the TSI of the Kinetis E series.

As shown in Table 3, MCX Nx4x TSI is not affected by the VDD noise. It has more function clock choices. If the function clock is configured from the chip system clock, the TSI power consumption can be decreased. Even though the MCX Nx4x TSI has only one TSI module, it supports designing more hardware touch keys on a hardware board when using mutual-cap mode.

Table 3. The difference between MCX Nx4x TSI and Kinetis E TSI (KE17Z256)

	MCX Nx4x series	Kinetis E series
Operating voltage	1.71 V – 3.6 V	2.7 V – 5.5 V
VDD noise impact	No	Yes
Function clock source	• TSI IP internal generated • Chip system clock	TSI IP internal generated
Function clock range	30 KHz - 10 MHz	37 KHz - 10 MHz
TSI channels	Up to 25 channels (TSI0)	Up to 50 channels (TSI0, TSI1)
Shield channels	4 shield channels: CH0, CH6, CH12, CH18	3 shield channels for each TSI: CH4, CH12, CH21
Touch mode	Self-cap mode: TSI[0:24]	Self-cap mode: TSI[0:24]

Table 3. The difference between MCX Nx4x TSI and Kinetis E TSI (KE17Z256)*...continued*

	MCX Nx4x series	Kinetis E series
	Mutual-cap mode: Tx[0:7], Rx[8:24]	Mutual-cap mode: Tx[0:5], Rx[6:12]
Touch electrodes	self-cap electrodes: up to 25 mutual-cap electrodes: up to 136 (8x17)	self-cap electrodes: up to 50 (25+25) mutual-cap electrodes: up to 72 (6x6 +6x6)
Products	MCX N9x and MCX N5x	KE17Z256

The features supported both by MCX Nx4x TSI and Kinetis TSI are shown in Table 4.

Table 4. The features supported both by MCX Nx4x TSI and Kinetis TSI

	MCX Nx4x series	Kinetis E series
Two kinds of Sensing mode	Self-cap mode: Basic self-cap mode Sensitivity boost mode Noise cancellation mode Mutual-cap mode: Basic mutual-cap mode Sensitivity boost enable	
Interrupt support	End of scan interrupt Out of range interrupt	
Trigger source support	1. Software trigger by writing the `GENCS[SWTS]` bit 2. Hardware trigger through `INPUTMUX` 3. Automatic trigger by `AUTO_TRIG[TRIG_EN]`	1. Software trigger by writing the `GENCS[SWTS]` bit 2. Hardware trigger through `INPUTMUX`
Low-power support	Deep Sleep: fully function when `GENCS[STPE]` is set to 1 Power Down: If the WAKE domain is active, TSI can operate as in "Deep Sleep" mode. Deep Power Down, VBAT: not available	STOP mode, VLPS mode: fully functioning when `GENCS[STPE]` is set to 1.
Low-power wake-up	Each TSI channel can wake up the MCU from low-power mode.	
DMA support	The out of range event or end of scan event can trigger the DMA transfer.	
Hardware noise filter	SSC reduces the frequency noise and promotes the signal-to-noise ratio (PRBS mode, up-down counter mode).	

3.2 MCX Nx4x TSI new features

Some new features are added to MCX Nx4x TSI. The most significant are listed in the table below. MCX Nx4x TSI provides a richer range of features for users. Like the functions of Baseline auto trace, Threshold auto trace, Debounce, these features can realize some hardware calculations. It saves software development resources.

Table 5. MCX Nx4x TSI new features

	MCX Nx4x series
1	Proximity channels merge function
2	Baseline auto trace function
3	Threshold auto trace function

Table 5. MCX Nx4x TSI new features*...continued*

4	Debounce function
5	Automatic trigger function
6	Clock from chip system clock
7	Test finger function

3.3 MCX Nx4x TSI function description

Here is the description of these newly added features:

1. The proximity channels merge function
   The proximity function is used to merge multiple TSI channels for scanning. Configure `TSI0_GENCS[S_PROX_EN]` to 1 to enable the proximity mode, the value in `TSI0_CONFIG[TSICH]` is invalid, it is not used to select channel in proximity mode. The 25-bit register `TSI0_CHMERGE[CHANNEL_ENABLE]` is configured to select multiple channels, the 25-bit controls the selection of 25 TSI channels. It can select up to 25 channels, by configuring the 25 bits to 1 (1_1111_1111_1111_1111_1111_1111b). When a trigger occurs, the multiple channels selected by `TSI0_CHMERGE[CHANNEL_ENABLE]` are scanned together, and generate one set of the TSI scan value. The scan value can be read from register `TSI0_DATA[TSICNT]`. The proximity merge function theoretically integrates the capacitance of the multiple channels and then starts scanning, which is only valid in self-cap mode. The more touch channels merged can get a shorter scanning time, the smaller is the scanning value, and the poorer is the sensitivity. Therefore, when touch detect, more touch capacitance is needed to get the higher sensitivity. This function is suitable for the large area touch detect and large area proximity detect.
2. Baseline auto trace function
   The TSI of MCX Nx4x provides the register to set the baseline of TSI and the baseline trace function. After the TSI channel software calibration is complete, fill an initialize baseline value in the `TSI0_BASELINE[BASELINE]` register. The initial baseline of the touch channel in the `TSI0_BASELINE[BASELINE]` register is written in the software by the user. The setting of the baseline is valid only for one channel. The baseline trace function can adjust the baseline in the `TSI0_BASELINE[BASELINE]` register to make it close to the TSI current sample value. The baseline trace enable function is enabled by the `TSI0_BASELINE[BASE_TRACE_EN]` bit, and the autotrace ratio is set in the register `TSI0_BASELINE[BASE_TRACE_DEBOUNCE]`. The baseline value is increased or decreased automatically, the change value for each increase/decrease is `BASELINE * BASE_TRACE_DEBOUNCE`. The baseline trace function is only enabled in low-power mode and the setting is valid only for one channel. When the touch channel is changed, the baseline-related registers must be reconfigured.
3. Threshold auto trace function
   The threshold can be calculated by the IP internal hardware if the threshold trace is enabled by configuring the `TSI0_BASELINE[THRESHOLD_TRACE_EN]` bit to 1. The calculated threshold value is loaded to threshold register `TSI0_TSHD`. To get the desired threshold value, select the threshold ratio in `TSI0_BASELINE[THRESHOLD_RATIO]`. The threshold of the touch channel is calculated according to the below formula in the IP internal.
   Threshold_H: `TSI0_TSHD[THRESH] = [BASELINE + BASELINE >>(THRESHOLD_RATIO+1)]`
   Threshold_L: `TSI0_TSHD[THRESL] = [BASELINE - BASELINE >>(THRESHOLD_RATIO+1)]`
   BASELINE is the value in `TSI0_BASELINE[BASELINE]`.
4. Debounce function
   MCX Nx4x TSI provides the hardware debounce function, the `TSI_GENCS[DEBOUNCE]` can be used to configure the number of out-of-range events that can generate an interrupt. Only the out-of-range interrupt event mode supports the debounce function and the end-of-scan interrupt event does not support it.

5. Automatic trigger function. There are three trigger sources of TSI, including the software trigger by writing the TSI0_GENCS[SWTS] bit, the hardware trigger through INPUTMUX, and the automatic trigger by TSI0_AUTO_TRIG[TRIG_EN]. Figure 4 shows the automatically trigger-generated progress.

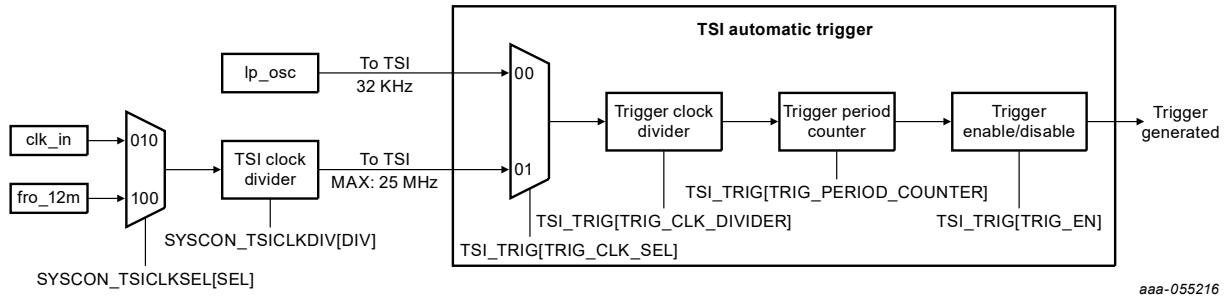

Figure 4. TSI automatic trigger generation block diagram

The automatic trigger function is a new feature in MCX Nx4x TSI. This feature is enabled by setting TSI0_AUTO_TRIG[TRIG_EN] to 1. Once the automatic trigger is enabled, the software trigger and hardware trigger configuration in TSI0_GENCS[SWTS] is invalid. The time period between each trigger can be calculated by the below formula:

Timer period between each trigger = trigger clock / trigger clock divider * trigger clock counter.

Trigger clock: configure TSI0_AUTO_TRIG[TRIG_CLK_SEL] to select the automatic trigger clock source.

Trigger clock divider: configure TSI0_AUTO_TRIG[TRIG_CLK_DIVIDER] to select the trigger clock divider.

Trigger clock counter: configure TSI0_AUTO_TRIG[TRIG_PERIOD_COUNTER] to configure the trigger clock counter value.

For the clock of the automatic trigger clock source, one is the lp_osc 32k clock, another is the FRO_12Mhz clock or the clk_in clock can be selected by TSICLKSEL[SEL], and divided by TSICLKDIV[DIV].

6. Clock from chip system clock

Usually, Kinetis E series TSI provides an internal reference clock to generate the TSI functional clock. For the TSI of MCX Nx4x, the operating clock cannot only be from the IP internal, but it can be from the chip system clock. MCX Nx4x TSI has two function clock source choices (by configuring TSICLKSEL[SEL]). As shown in Figure 5, one from the chip system clock can decrease the TSI operate power consumption, another is generated from the TSI internal oscillator. It can decrease the jitter of the TSI operate clock.

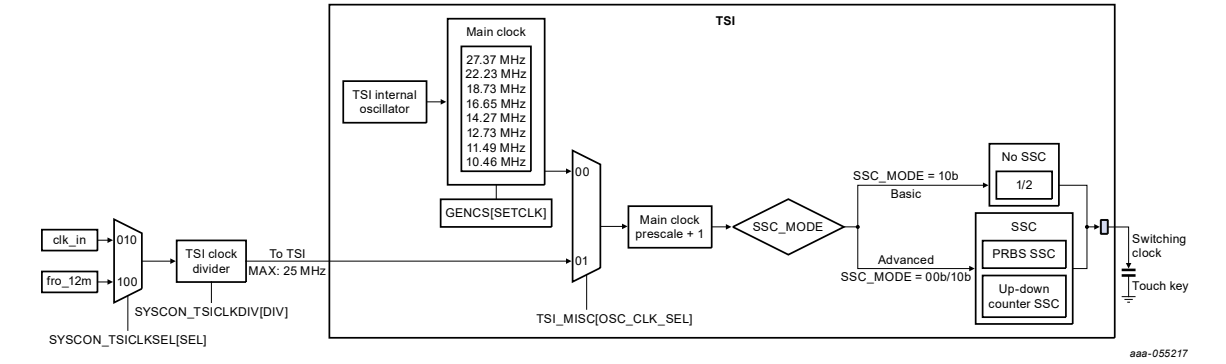

Figure 5. Clock generation block diagram

FRO_12 MHz clock or the clk_in clock is the TSI function clock source, it can be selected by TSICLKSEL[SEL] and divided by TSICLKDIV[DIV].

7. Test finger function

MCX Nx4x TSI provides the test finger function that can simulate a finger touch without a real finger touch on the hardware board by configuring the related register. This function is useful during the code debug and hardware board test.

The strength of the TSI test finger can be configured by `TSI0_MISC[TEST_FINGER]`, the user can change the touch strength through it. There are 8 options for the finger capacitance: 148pF, 296pF, 444pF, 592pF, 740pF, 888pF, 1036pF, 1184pF. The test finger function is enabled by configuring `TSI0_MISC[TEST_FINGER_EN]` to 1.
The user can use this function to calculate the hardware touchpad capacitance, the TSI parameter debug and do the software safety /failure tests (FMEA). In the software code, configure the finger capacitance first and then enable the test finger function.

3.4 Example use case of MCX Nx4x TSI new function

MCX Nx4x TSI has a feature for the low-power use case:

- Use the chip system clock to save the IP power consumption.
- Use automatic trigger function, proximity channels merge function, baseline auto trace function, threshold auto trace function, debounce function to do an easy low-power wake-up use case.

4 MCX Nx4x TSI hardware and software support

NXP has four kinds of hardware boards to support the MCX Nx4x TSI evaluation. The X-MCX-N9XX-TSI board is the internal evaluation board, contract FAE/Marketing to request it. The other three boards are NXP official release boards and can be found on in the NXP web where the user can download the official supported software SDK and touch library.

4.1 MCX Nx4x series TSI evaluation board

NXP provides evaluation boards to help users to evaluate the TSI function. The following is the detailed board information.

4.1.1 X-MCX-N9XX-TSI board

The X-MCX-N9XX-TSI board is a touch sensing reference design including multiple touch patterns based on the NXP high-performance MCX Nx4x MCU that has one TSI module and supports up to 25 touch channels demonstrated on the board. The board can be used to evaluate the TSI function for the MCX N9x and N5x series MCU. This product has passed the IEC61000-4-6 3V certification.

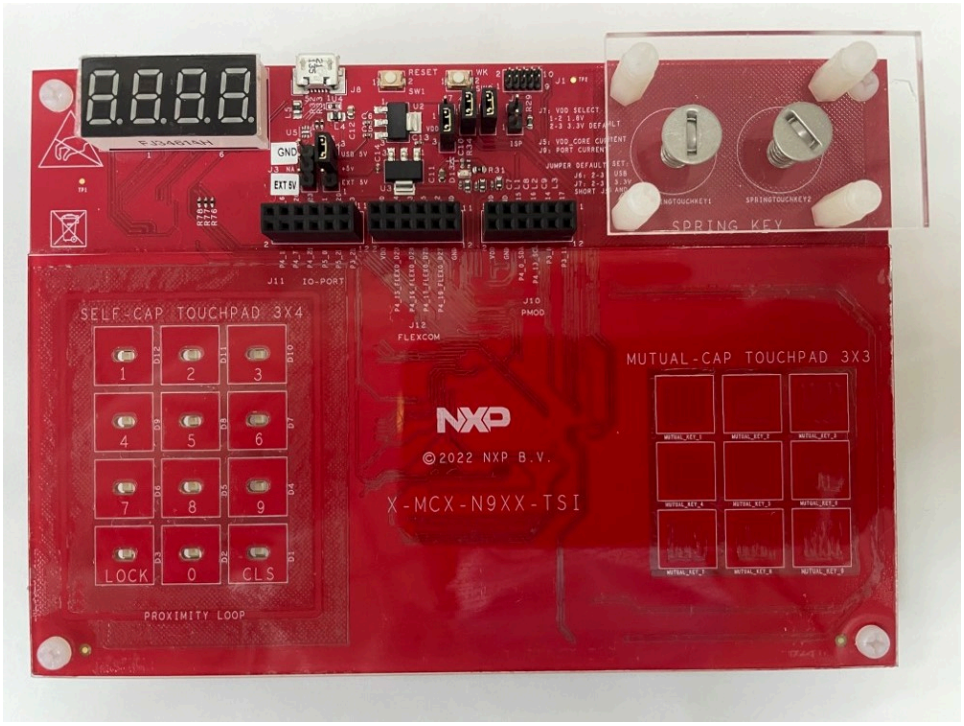

Figure 6. X-MCX-N9XX-TSI, MCX N5/N9 dedicated TSI evaluation board

4.1.2 MCX-N5XX-EVK

MCX-N5XX-EVK provides the touch slider on the board, and it is compatible with the FRDM-TOUCH board. NXP provides a touch library to realize the functions of keys, slider, and rotary touches.

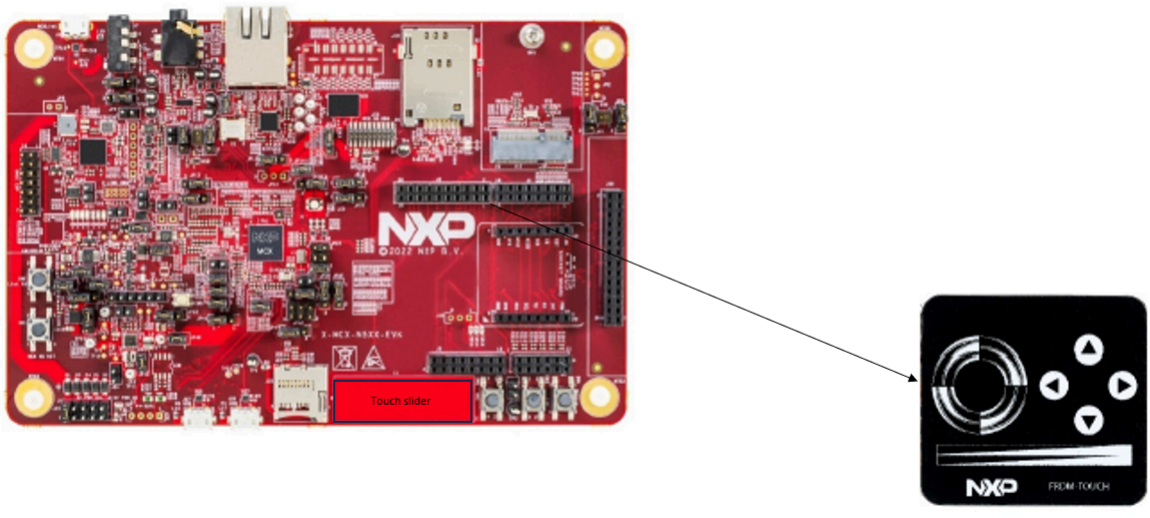

Figure 7. MCX-N5XX-EVK with touch

4.1.3 MCX-N9XX-EVK

MCX-N9XX-EVK provides the touch slider on the board, and it is compatible with the FRDM-TOUCH board. NXP provides a touch library to realize the functions of keys, slider, and rotary touches.

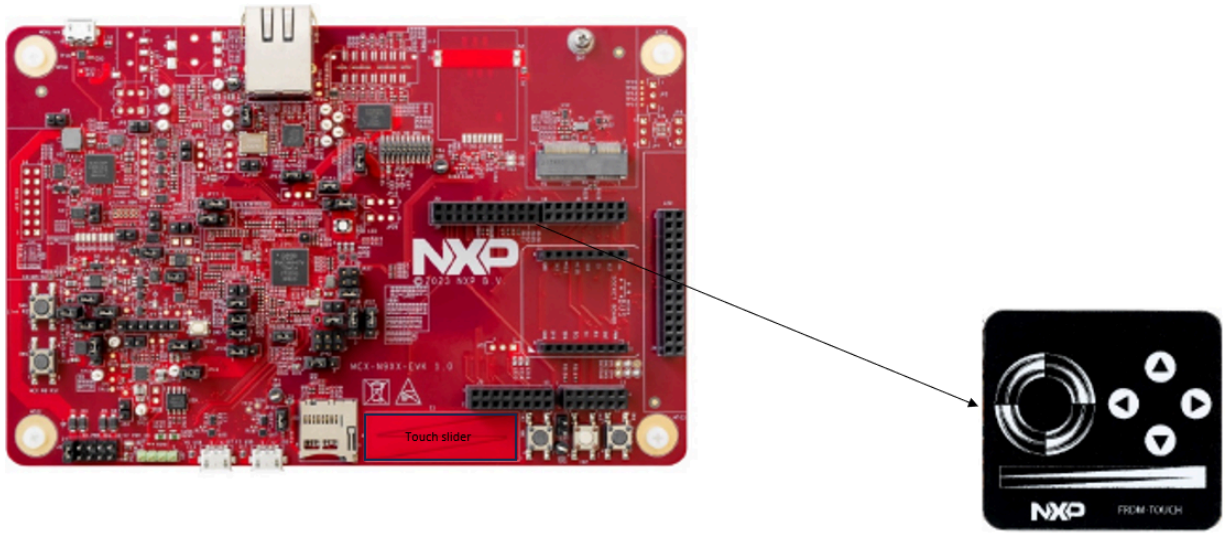

Figure 8. MCX-N9XX-EVK with touch

4.1.4 FRDM-MCXN947

FRDM-MCXN947 provides a one-touch key on the board and it is compatible with the FRDM-TOUCH board. NXP provides a touch library to realize the functions of keys, slider, and rotary touches.

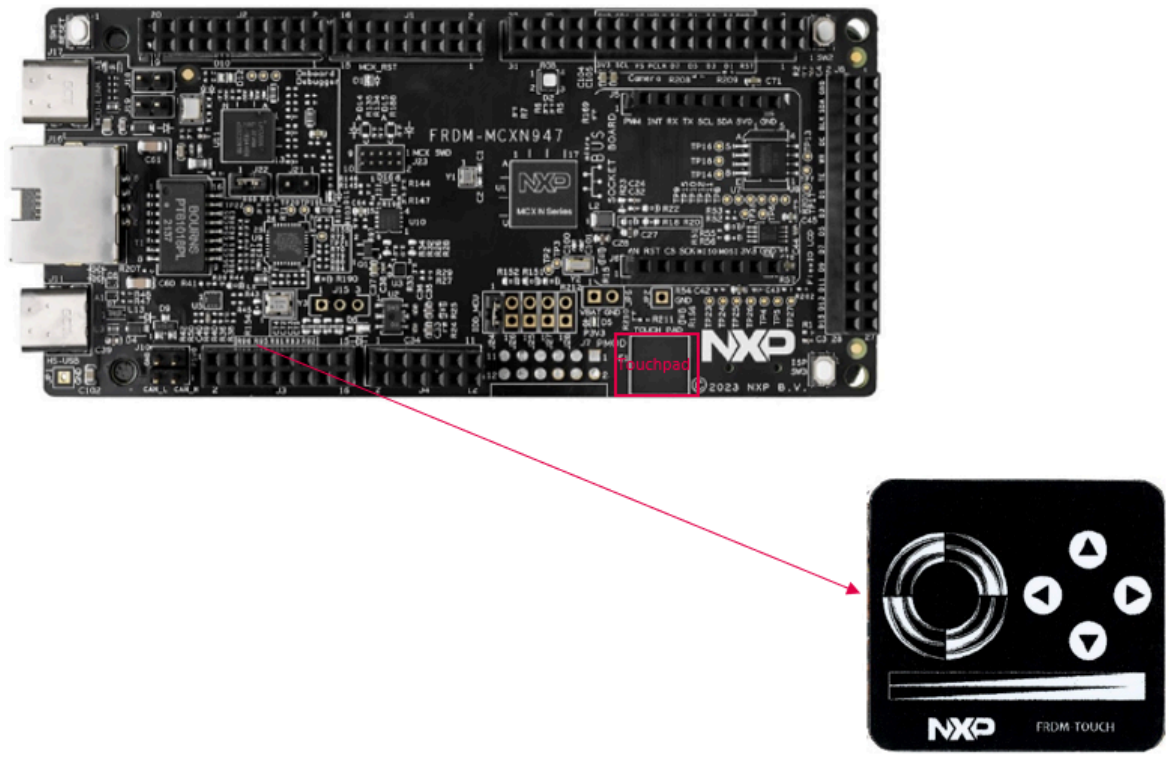

Figure 9. FRDM-MCXN947 with touch

4.2 NXP touch library support for MCX Nx4x TSI

NXP offers a touch software library free of charge. It provides all the software required to detect touches and to implement more advanced controllers like sliders or keypads. TSI background algorithms are available for touch keypad and analog decoders, sensitivity auto calibration, low-power, proximity, water tolerance. The SW is distributed in source code form in “object C language code structure”. And a touch tuner tool based on FreeMASTER is provided for TSI configuration and tune.

4.2.1 SDK build and touch library download

The user can build SDK of MCX hardware boards from https://mcuxpresso.nxp.com/en/welcome, add the touch library to the SDK and download the package. The process is shown on Figure 10, Figure 11, and Figure 12.

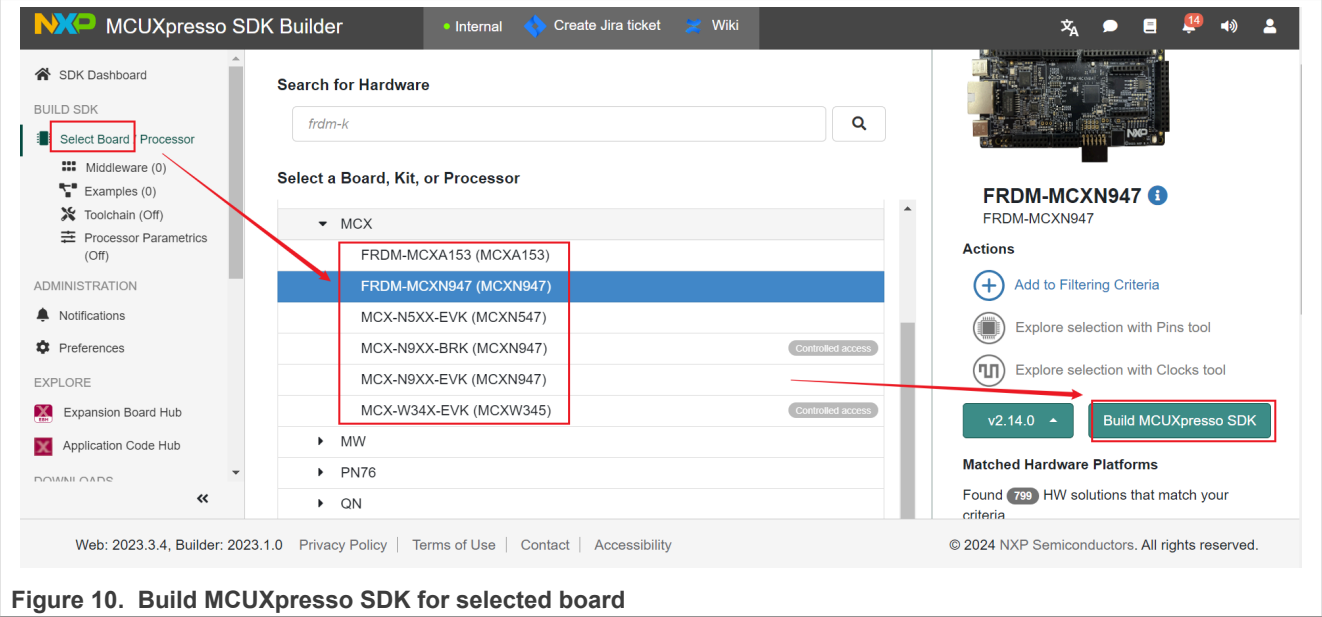

Figure 10. Build MCUXpresso SDK for selected board

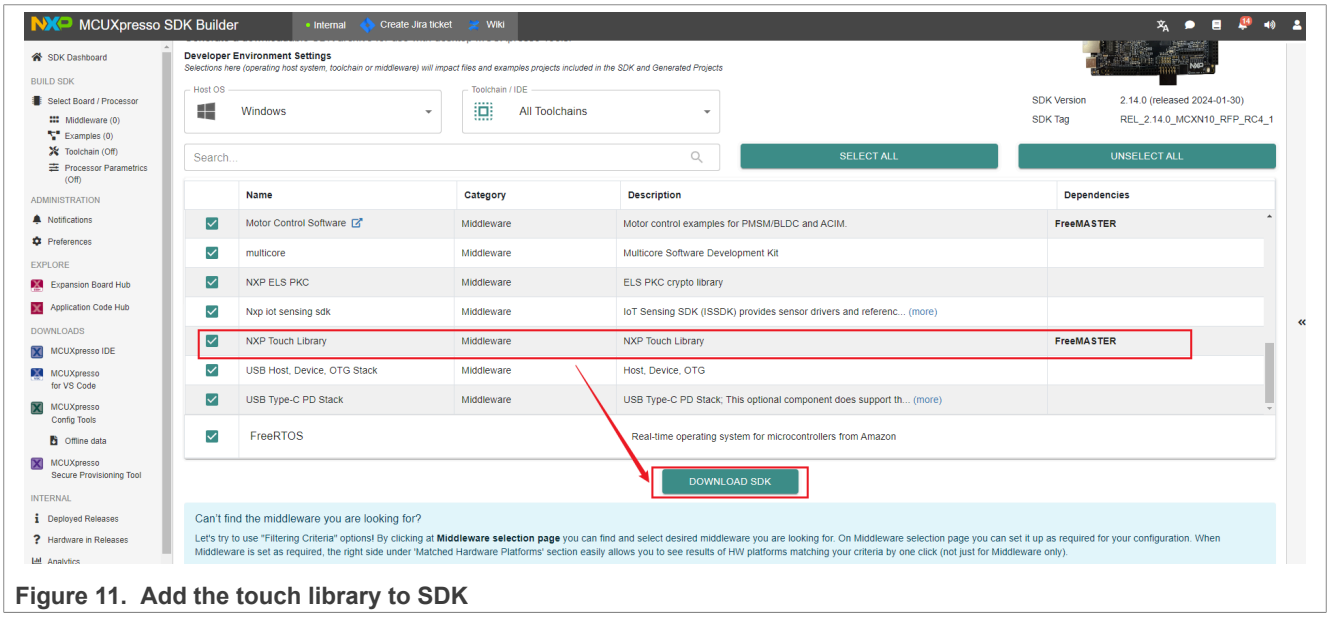

Figure 11. Add the touch library to SDK

Figure 12. Download SDK

4.2.2 NXP touch library

The touch sensing code in the downloaded SDK folder …`\boards\frdmmcxn947\demo_apps\touch_sensing` is developed using the NXP touch library.

The NXP Touch Library Reference Manual can be found in the folder …`/middleware/touch/freemaster/html/index.html`, it describes the NXP Touch software library for implementing touch-sensing applications on NXP MCU platforms. The NXP Touch software library provides touch-sensing algorithms to detect finger touch, movement, or gestures.

The FreeMASTER tool for TSI configure and tune is included into the NXP touch library. For more information, see the *NXP Touch Library Reference Manual* (document NT20RM) or *NXP Touch Development Guide* (document AN12709) .

The basic building blocks of the NXP Touch library are shown in Figure 13:

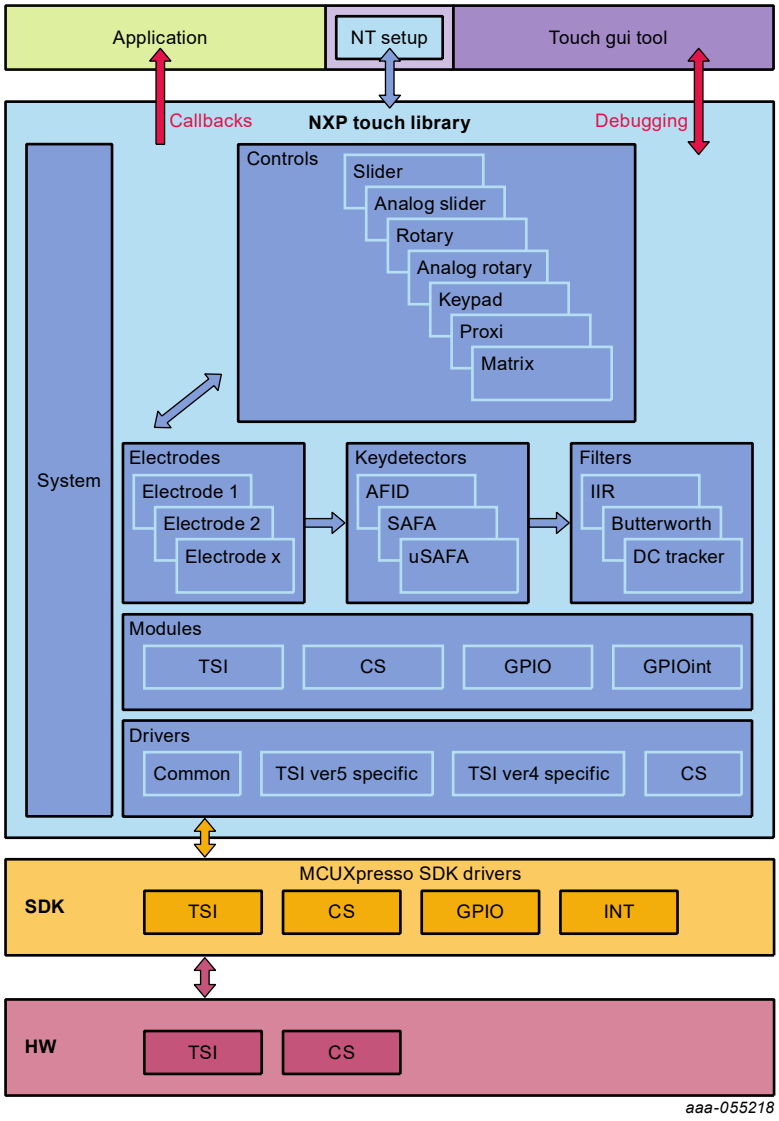

Figure 13. The basic building blocks of the NXP Touch library

5 MCX Nx4x TSI performance

For MCX Nx4x TSI, the following parameters have been tested on the X-MCX-N9XX-TSI board. Here is the performance summary.

Table 6. Performance summary

	MCX Nx4x series	
1	SNR	Up to 200:1 for self-cap mode and mutual-cap mode
2	Overlay thickness	Up to 20 mm
3	Shield drive strength	Up to 600pF at 1MHz, Up to 200pF at 2MHz
4	Sensor capacitance range	5pF – 200pF

1. SNR test
   The SNR is calculated according to the raw data of the TSI counter value. In the case when no algorithm is used to process the sampled values, SNR values of 200:1 can be achieved in self-cap mode and mutual-cap mode.
   As shown in Figure 14, the SNR test has been performed on the TSI board on EVB.

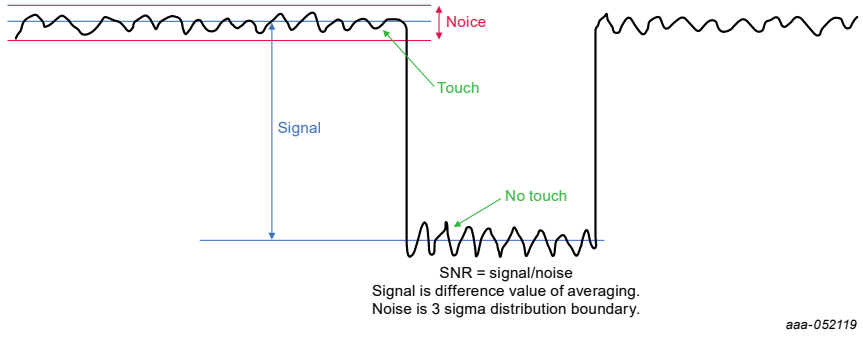

Figure 14. SNR tested on board

2. Shield drive strength test
   The strong shield strength of TSI can improve the waterproof performance of the touchpad and can support a larger touchpad design on hardware board. When the 4 TSI shield channels are all enabled, the maximum driver capability of the shield channels is tested at 1 MHz and 2 MHz TSI working clocks in self-cap mode. The higher the TSI operating clock, the lower the drive strength of the shielded channel. If the TSI operating clock is lower than 1MHz, the maximum drive strength of the TSI is larger than 600 pF.
   To do the hardware design, refer to the test results shown in Table 7.

Table 7. Shield driver strength test result

Shield channel on	Clock	Max shield drive strength
CH0, CH6, CH12, CH18	1 MHz	600 pF
	2 MHz	200 pF

3. Overlay thickness test
   To protect the touch electrode from the interference of the external environment, the overlay material must be closely attached to the surface of the touch electrode. There should be no air gap between the touch electrode and the overlay. An overlay with a high dielectric constant or an overlay with a small thickness improves the sensitivity of the touch electrode.
   The maximum overlay thickness of the acrylic overlay material was tested on the X-MCX-N9XX-TSI board as shown in Figure 15 and Figure 16. The touch action can be detected on the 20 mm acrylic overlay. Here are the conditions to be fulfilled:
   - SNR>5:1
   - Self-cap mode
   - 4 shield channels on
   - The sensitivity boost

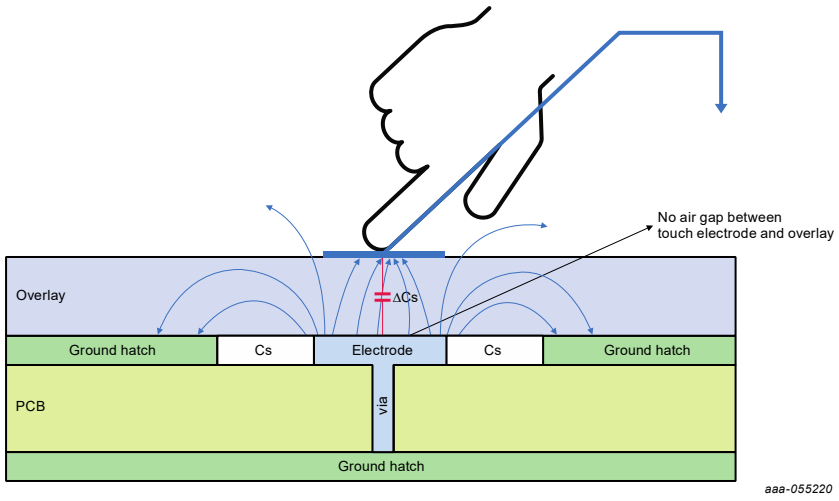

Figure 15. Overlay thickness test base on the acrylic

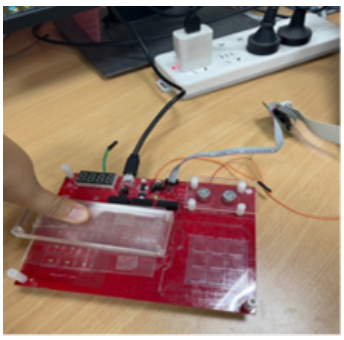

Figure 16. Overlay thickness test base on the acrylic

4. Sensor capacitance range test
   The recommended intrinsic capacitance of a touch sensor on a hardware board is in the range of 5 pF to 50 pF. The area of the touch sensor, the material of the PCB, and the routing trace on the board affect the size of the intrinsic capacitance. These must be considered during the hardware design of the board.
   After testing on the X-MCX-N9XX-TSI board, MCX Nx4x TSI can detect a touch action when the intrinsic capacitance is as high as 200 pF, the SNR is larger than 5:1. Therefore, the requirements for touch board design are more flexible.

6 Conclusion

This document introduces the basic functions of TSI on MCX Nx4x chips. For details on the MCX Nx4x TSI principle, refer to the TSI chapter of the *MCX Nx4x Reference Manual* (document MCXNx4xRM). For suggestions of the hardware board design and touchpad design, refer to the *KE17Z Dual TSI User Guide* (document KE17ZDTSIUG).

7 References

The following references are available on NXP website:

1. *MCX Nx4x Reference Manual* (document MCXNx4xRM)

2. *KE17Z Dual TSI User Guide* (document KE17ZDTSIUG)

3. *NXP Touch development guide* (document AN12709)

4. *NXP Touch Library Reference Manual* (document NT20RM)

8 Revision history

Table 8. Revision history

Document ID	Release date	Description
UG10111 v.1	7 May 2024	Initial version

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