P1024RDB-PA Quick Start Guide

1.1 Introduction

This quick start guide applies to boards with assembly rev "700-26815 Rev A". Please check the top side of the board to see the revision number.

1.2 P1024RDB-PA Board Details

Figure 1 shows the P1024RDB-PA board details.

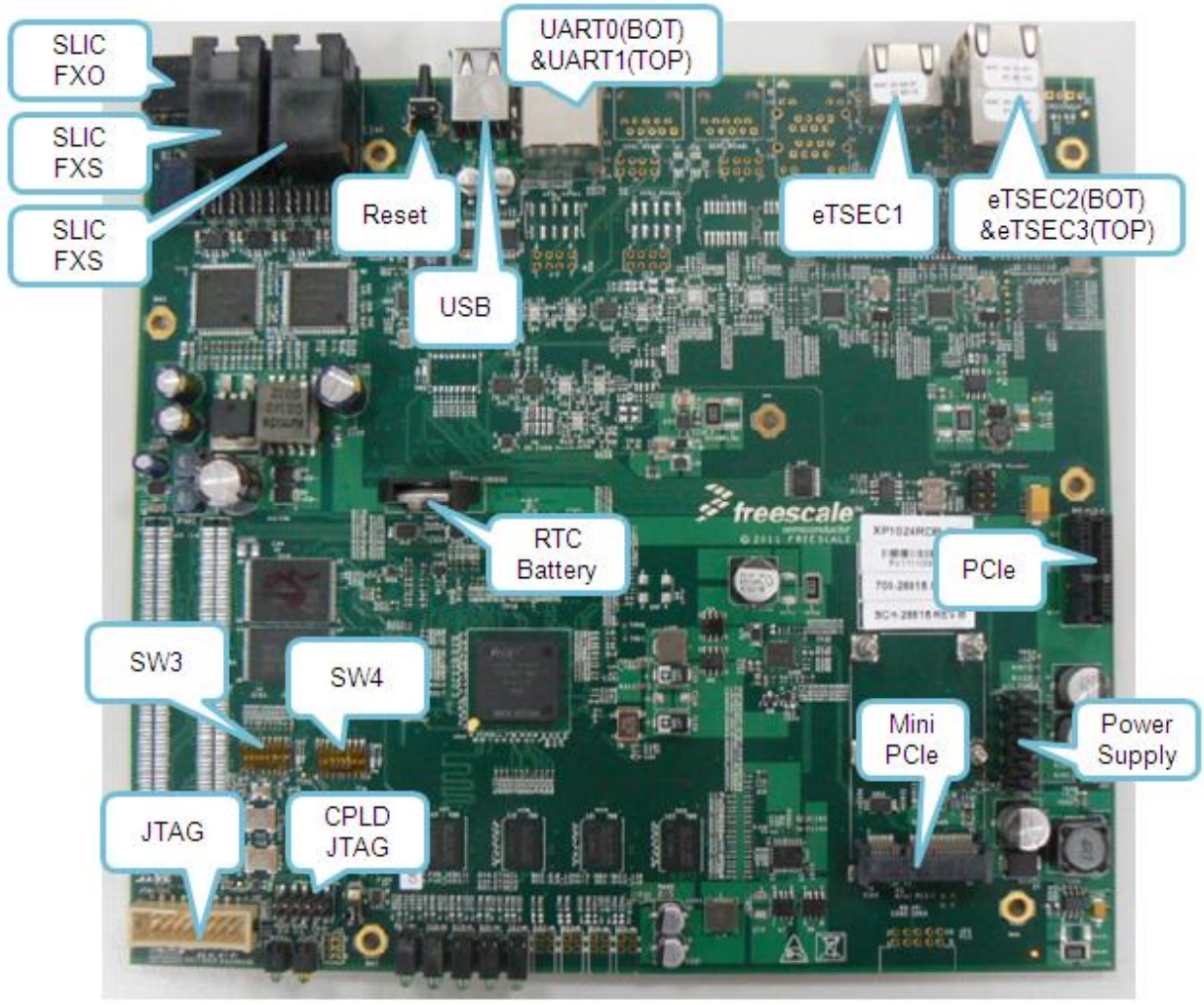

Figure 1: P1024RDB-PA Board Details

Figure 2 shows the high level block diagram of P1024RDB-PA.

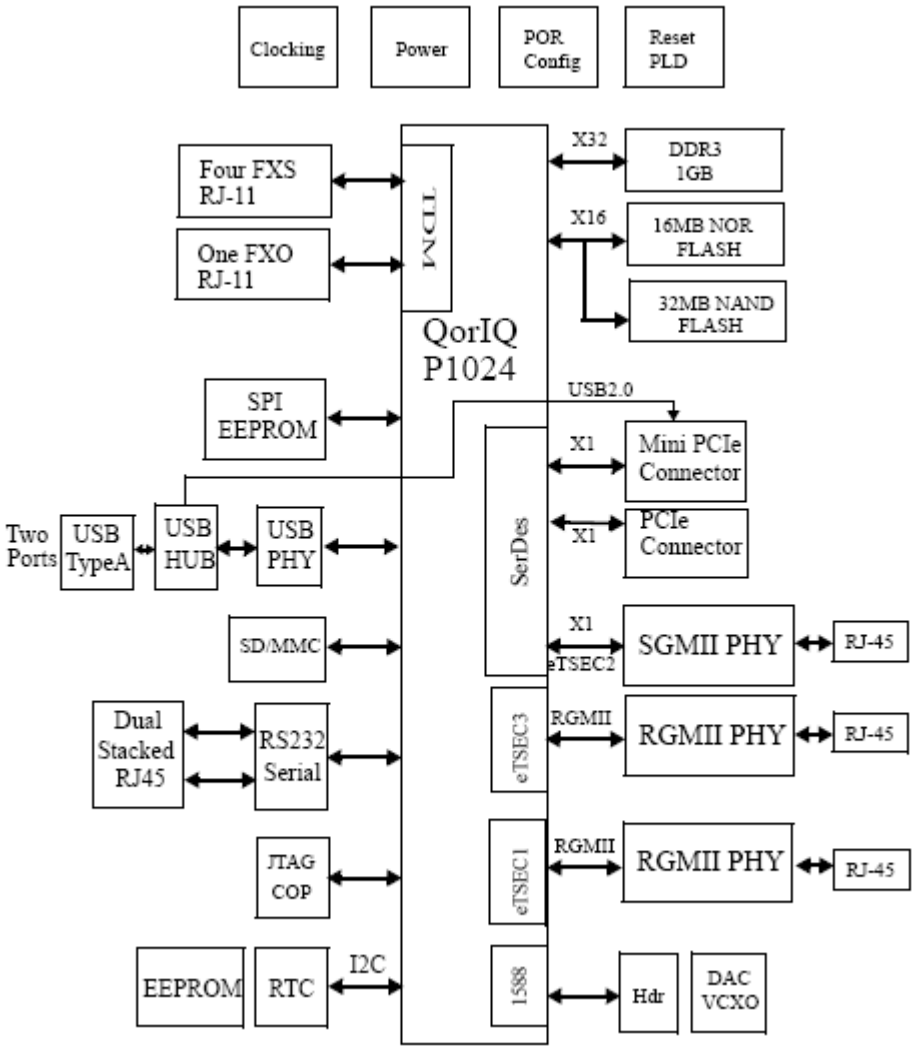

Figure 2: High Level Block Diagram

1.2.1 Key Features of the P1024RDB-PA

- Freescale QorIQ architecture CPU
  - QorIQ P1024E, 533 MHz
- Memory Sub-system
  - SDRAM
    - The 1Gbyte (8bit x 4 chip) DDR3 SDRAM

- NOR Flash
  - 16MB 16bit NOR Flash
- NAND Flash:
  - 32MB SLC NAND Flash
- 256 Kbit M24256 I2C EEPROM
- 128 Mbit SPI flash
- I2C Board 128x8 bit memory
- SD/MMC connector to interface with the SD memory card

- PCI-E
  - PCI-E lane 0: mini-PCI-E X1 connector with USB 2.0 signal
  - PCI-E lane 1: One PCI-E X1 connector
- USB 2.0
  - Dual Type A USB slot, connected to USB via USB HUB
- Ethernet
  - eTSEC1: Connected to RGMII PHY –AR8021
  - eTSEC2: Connected to SGMII PHY -VSC8221
  - eTSEC3: Connected to RGMII PHY –AR8021
- UART
  - DUART interface: Supports two UARTs up to 115200 bps for console display; Dual RJ45 slots are used for these 2 UART ports
- TDM
  - 4 FXS ports connected via two on-board SLICs to the TDM interface. The SLIC is controlled via P1024 SPI
  - 1 FXO port connected via a relay to FXS for switchover to POTS
- MISC
  - LED
    - Power LED (Green)
    - Link LED (Green) on each RJ45 ethernet connector
    - Activities LED (Yellow) on each RJ45 ethernet connector
  - JTAG/COP for debugging
  - Reset: Manual Reset and software reset function will be used on the design
  - I2C
    - Serial eeprom – board identification (Defined in Memory Subsystem already)
    - Real-time clock
- POR (Power On Reset Configurations)
  - Support critical POR setting changed via SW on board

- PCB
  - Power/reset button are located at the rear of the casing
  - Power LED and Ethnet LED are located at the front of the casing
- Power
  - External power adapter, which converts 220V AC to 12V DC is available
- Schematics – OrCad; PCB - Allegro

1.3 Default Booting Method

By default, the boot loader executes from NOR flash.

1.4 Switch Settings

Table 1 displays the default switch settings

Table 1: Board Default Switch Settings

Reference	P1024RDB-PA Switch Setting for NOR flash boot
SW3.1~SW3.8	OFF,ON,OFF,ON,ON,ON,ON,ON
SW4.1~SW4.8	ON,ON,OFF,OFF,OFF,OFF,ON,ON

Figure 3 shows the SW3 and SW4 default setting on the board.

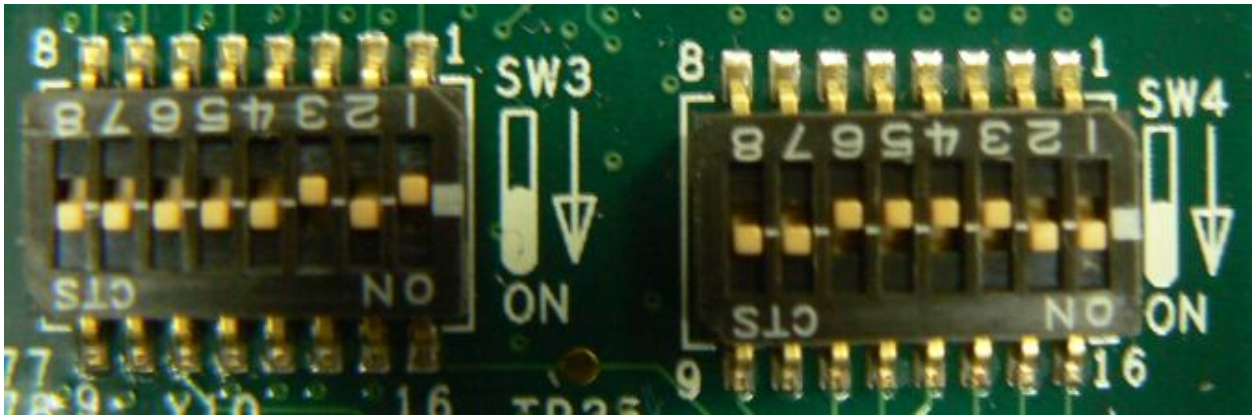

Figure 3: Switch Setting

Table 2 displays the other setting for the different frequency and boot location.

Table 2: Switch setting for different Frequency and boot location

Switch Settings SW4[1:6]	Core1 Freq(MHz)	Core2 Freq(MHz)	Platform (MHz)	DDR Freq(MHz)	Boot Location	Boot Hold-off
110000	533	533	267	667	NOR	Core0 boot; Core1 hold-off
110001	533	533	267	667	SD/MMC	Core0 boot; Core1 hold-off
110010	533	533	267	667	SPI	Core0 boot; Core1 hold-off
110011	533	533	267	667	NAND	Core0 boot; Core1 hold-off
110100	400	400	267	667	NOR	Core0 boot; Core1 hold-off
110101	400	400	267	667	SD/MMC	Core0 boot; Core1 hold-off
110110	400	400	267	667	SPI	Core0 boot; Core1 hold-off
110111	400	400	267	667	NAND	Core0 boot; Core1 hold-off

Table 3 lists the other configuration options that are available on the board.

Table 3: Other Configuration Options

Switch	Signal name	Signal Meaning	Setting
SW4[7]	LGPL5 (cfg_boot_seq[1])	Selects whether the boot sequencer is enabled during boot-up	OFF: boot sequencer enabled and configuration information loaded from I2C ROM. A valid ROM must be present. If not the card will hang. ON: boot sequencer disabled

SW4[8]	FBANK_SELECT	Selects which NOR flash bank is selected	OFF: upper 4 sectors used for booting ON: middle 4 sectors used for booting
SW3[1]	CFG_SDWIDTH	Configs the width of the SD/MMC bus, 4-bit or 8-bit	OFF: then width = 4bits, SPI interface active ON: then width = 8bits Software can read the status of this bit by reading the I2C 8-bit register.
SW3[2]	TEST_SEL	Personality Selection	OFF: Single e500 Core Device (P1015) ON: Dual e500 Core Device (P1024)
SW3[3]	DMA1_DACK_N	Freescale use only	Must be set to OFF for P1024E
SW3[4]	LA19 (cfg_host_agt[2])	Controls the setting of the cfg_host_agt[2] pin	ON: cfg_host_agt[2] = 1 OFF: cfg_host_agt[2] = 0
SW3[5]	USB1_STP	Freescale use only	Must be set to ON for P1024E
SW3[6]	SWITCH7	Reserved	Default ON
SW3[7]	LA18(cfg_host_agt[1])	Controls the setting of the cfg_host_agt[1] pin	ON: cfg_host_agt[0] = 1 OFF: cfg_host_agt[0] = 0
SW3[8]	LWE1_N (cfg_host_agt[0])	Controls the setting of the cfg_host_agt[0] pin	ON: cfg_host_agt[0] = 1 OFF: cfg_host_agt[0] = 0

Table 4 lists the default jumper setting on the board.

Table 4: Jumper Default Setting

J20											
2-3											

1.5 Ethernet Port Settings

Figure 4 shows the Ethernet ports on P1024RDB-PA.

Figure 4: Ethernet Ports on P1024RDB-PA

Table 5 lists Ethernet ports on P1024RDB-PA.

Table 5: Ethernet ports on P1024RDB-PA

Marking on board	P1024 Interface	In uboot	In Linux	Mode of operation
eTSEC1	eTSEC1	eTSEC1	eth0	RGMII
eTSEC2	eTSEC2	eTSEC2	eth1	SGMII
eTSEC3	eTSEC3	eTSEC3	eth2	RGMII

1.6 USB Ports on P1024RDB-PA

Figure 5 shows the two USB ports on P1024RDB-PA.

Figure 5: Dual USB Ports on P1024RDB-PA

Table 6 lists USB ports on P1024RDB-PA.

Table 6: USB Ports on P1024RDB-PA

Marking on board	P1024 Interface	In uboot	In Linux	Mode of operation
USB	external PHY(ULPI)+HUB	USB1	USB1	ULPI(external PHY)

1.7 UART Ports on P1024RDB-PA

P1024RDB-PA has two UART connectors marked as UART0 and UART1 on the back side of the board as shown in Figure 6. Default UART port is UART0.

Figure 6: UART Ports on P1024RDB-PA

Table 7 lists UART Ports on P1024RDB-PA.

Table 7: UART Ports on P1024RDB-PA

Marking on board	P1024 Interface	In uboot	In Linux	Mode of operation
TOP UART1	UART1	eserial1/ttyS1	ttyS1	
BOT UART0	UART0	eserial0/ttyS0	ttyS0	Default control display port

1.8 TDM Ports on P1024RDB-PA

P1024RDB-PA has Four FXS and one FXO ports as shown in Figure 7.

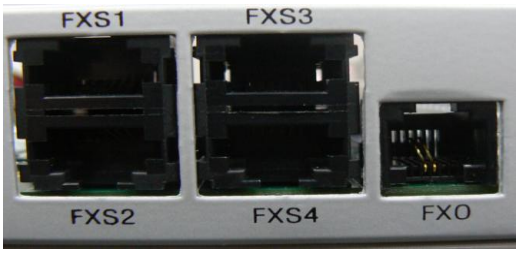

Figure 7: TDM ports

Table 8 lists TDM ports on P1024RDB-PA.

Table 8: TDM ports on P1024RDB-PA

Marking on board	On SLIC Le88266DLC	On P1024
FXS1	SLIC Channel1	SPI CS1
FXS2	SLIC Channel2	SPI CS1
FXS3	SLIC Channel1	SPI CS2
FXS4	SLIC Channel2	SPI CS2
FXO	SLIC Channel2	SPI CS2

1.9 Preparing the Board

1. Ensure that board is not connected to the power.
2. Ensure that the power switch is OFF.
   Note: It is recommended to wear the wrist strap before preparing the P1024RDB-PA board to get protection from electrical charges.
3. Set switches and jumper header settings, as mentioned in the *Switch Settings* section.

4. Ensure power cable is plugged into the chassis.
5. Attach a RS-232 cable between the P1024RDB-PA (UART0) and a host PC.
6. Any serial console emulator, like TeraTerm, HyperTerminal can be used for communicating with P1024-RDB.
7. Configure the host PC's serial port with the following settings:

   - Data rate: 115200 bps
   - Number of data bits: 8
   - Parity: None
   - Number of Stop bits: 1
   - Flow Control: Hardware/None

8. Push the Power button on the front of the unit. Board should boot and show the U-boot console messages. Example u-boot log is given in *Example U-boot log* section.

1.9.1 Example U-boot log

```
U-Boot 2010.12-00063-g8669298-dirty (Jul 09 2011 - 14:33:07)

CPU0:  P1024E, Version: 1.1, (0x80ec0211)
Core:  E500, Version: 5.1, (0x80212051)
Clock Configuration:
      CPU0:533.333 MHz, CPU1:533.333 MHz,
      CCB:266.667 MHz,
      DDR:333.333 MHz (666.667 MT/s data rate) (Asynchronous), LBC:16.667 MHz
L1:    D-cache 32 kB enabled
      I-cache 32 kB enabled
Board: P1024RDB CPLD: V2.2 PCBA: V2.0
rom_loc: nor lower bank
SD/MMC : 4-bit Mode
eSPI : Enabled
I2C:   ready
SPI:   ready
DRAM:  Detected UDIMM(s)
WARNING: Calling __hwconfig without a buffer and before environment is ready
WARNING: Calling __hwconfig without a buffer and before environment is ready
DDR: 1 GiB (DDR3, 32-bit, CL=5, ECC off)
FLASH: 16 MiB
L2:    256 KB enabled
NAND:  32 MiB
MMC:  FSL_ESDHC: 0
PCIe1: Root Complex of mini PCIe SLOT, no link, regs @ 0xffe0a000
PCIe1: Bus 00 - 00
```

```
PCIe2: Root Complex of PCIe SLOT, no link, regs @ 0xffe09000
PCIe2: Bus 01 - 01
Video: No radeon video card found!
In:    serial
Out:   serial
Err:   serial
Net:   eTSEC2 is in sgmii mode.
eTSEC1, eTSEC2, eTSEC3
Hit any key to stop autoboot:  0
```

NOTE: Linux login: **root**, Password: **root**

1.10 Caution

1. **Aviod touching any area of open frame power circuitry inside the chassis. High Voltage in the power circuitry can prove fatal and hazardous.**
2. **Avoid touching areas of integrated circuitry and connectors; static discharge can damage circuits.**

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