PowerPC™

Errata to
MPC801 PowerQUICC™ User's Manual

This errata describes corrections to the *MPC801 PowerQUICC User's Manual* (MPC801UMAD/AD).

freescale™ semiconductor

Section/Page	Changes
9.4.7, 9-10	Table 9-1, IC_ADR Bits Functionality for the Cache Read Command: Correct the table to show bits ‘20–21’ as reserved and bits ‘22-27’ as the set select field. All other fields are correct.
10..3.3.3, 10-6	Table 10-1, DC_ADR Bits Functionality for Reading the Cache: Correct the table to show bits ‘20–22’ as reserved and bits ‘22-27’ as the set number field. All other fields are correct..
16.3.3.4.6, 16-33	I^2C Receive Data Hold Register: Correct the I2CRD figure and text to show the Valid bit in bit position 0. Bits 1–5 are still reserved.
22.3, 22-3	PBGA package bottom view: Correct the pin labels by exchanging ‘A’ and ‘1’, ‘B’ and ‘2’, etc.