

7.2.4.3 Last Cell Processing Time

This read-only register contains the cell time. This value may be used to find the most recent cell that is updated in a cyclical fashion.

31	30	29	28	27	26	25	24
							LC
15	14	13	12	11	10	9	8
							LC

Figure 7-6. Last Cell Processing Time

7.2.4.4 ATMC CFB Revision Register

This read-only register contains the ATMC CFB revision number.

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	AMRV			

Figure 7-7. ATMC CFB Revision Register

- **ATMC CFB Major Revision (AMRV)** Revision Number.
- **ATMC CFB Sub-Revision (ASRV)** Revision Number.

The following values of AMRV and ASRV are shown.

Table 7-2. Values of AMRV and ASRV

AMRV	ASRV
000000	000000
000001	000000
000001	000001

Addendum

MC92501 ATM Cell Processing

This technical update provides additional changes to the MC92501GCA, Revision A) and clarifies some previous pages that are attached to this addendum (pages 4-29) and replacement pages that may be removed and placed in the new version.

- Page 4-29, Figure 4-29: The \overline{MSEL} signal has been added to indicate a one-wait state access, and a note has been added indicating the wait state requirement.
- Page 7-11, Table 7-2: Revision A was added.
- Page 9-12, Table 9-4: The following changes were made:
 - I_{IN} Input leakage values:
 - with pullup resistor—minimum change
 - with pulldown resistor—maximum change
 - I_{OH}/I_{OL} minimum values for \overline{EACEN} , \overline{EMBSLx} were changed from 24 mA to 20 mA
 - Input Capacitance was changed from 8 pF to 10 pF
- Page G-1: Old reference 15 was deleted.

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Figure 4-42 shows a maintenance read/clear. Memory extends for three MCLK phases (three MCLK cycles, which is the minimum length for the clear signal to the **MEMEN** Interface). Thus, the clear does not extend

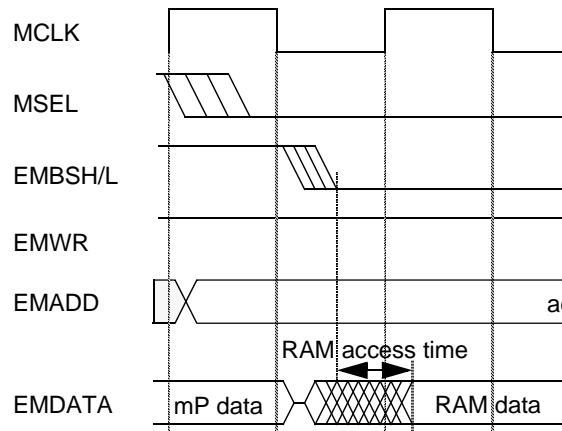


Figure 4-42. External Memo

NOTE: When performing a read/command, one wait state is required for the duration of an MCLK phase.

4.4.4 External Address Com

Normal (non-maintenance) accesses to the EAC Device must have the same timing as normal External Memory accesses. When asserted instead of the EM bank select signal, the address signal with all 1s when accessing the EAC Device. When asserted with all 1s when accessing the EAC Device, the address signal have the same timing as External Memory accesses. When the address signal is asserted instead of the EM bank select signal, the address signal driven on EMADD, so 24 bits (16 MB) of External Memory address space are available to the microprocessor. The EAC circuitry of the MC92C62 is a read-only register. Note that the MC92C62 is a read-only register. The microprocessor is free to control and/or program the address control signal.

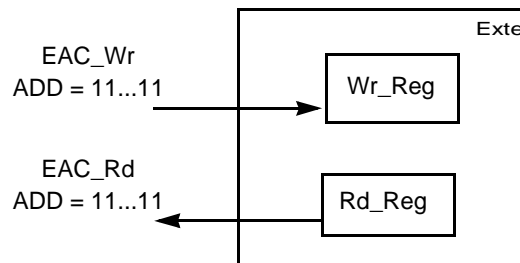


Figure 4-43. Example Implementation

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MC9250

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Go to: www.freescale.com**

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2. ITU-T Recommendation I.610, "B-ISDN Basic Reference Model", November, 1995
3. ATM Forum, "ATM User-Network Interface", September, 1994
4. ATM Forum, "BISDN Inter Carrier Interconnection", September, 1994
5. ATM Forum, "BISDN Inter Carrier Interconnection Letter Ballot", November, 1995
6. ATM Forum, "Traffic Management", September, 1994
7. ANSI T1S1.5/93-004R2, "Broadband ISDN Principles and Functions", January, 1994
8. Bellcore TA-NWT-01110, "Broadband ISDN Requirements", Issue 1, August, 1993
9. Bellcore GR-1113-CORE, "Asynchronous Transfer Mode Adaptation Layer (AAL) Protocol", Issue 1, August, 1994
10. Bellcore GR-1248-CORE, "Generic Functional Elements", Issue 1, August, 1994
11. Motorola, "MC68360 Quad Integrator User's Manual", 1993
12. "UTOPIA, An ATM-PHY Interface", Issue 1, August, 1994
13. "UTOPIA Level 2 Specification, Version 1.0", Issue 1, August, 1994
14. Bellcore TA-TSV-001408, "Generic Functional Elements", Issue 1, August, 1993
15. P. Bardell, W. McAnney, and J. Savolainen, *ATM Techniques*, John Wiley & Sons, 1994

9.3.3 DC Electrical Characteristics

Table 9-4. DC Electrical Characteristics

Symbol	Parameter	Test Conditions
V_{IH}	TTL Inputs (5V Tolerant)	
V_{IL}	TTL Inputs (5V Tolerant)	
I_{IN}	Input Leakage Current, No Pull Resistor	$V_{IN} = V_{DD}$
	With Pullup Resistor *	
	With Pulldown Resistor *	
I_{OH}	Output High Current, LVTTL Output Type Outputs: \overline{EACEN} , \overline{EMWR} , \overline{EMADDx} , \overline{EMBSHx} , \overline{EMBSLx}	$V_{OH} = V_{DD} - 0.4V$
	Output High Current, LVTTL Output Type Outputs: All other outputs	
I_{OL}	Output Low Current, LVTTL Output Type Outputs: \overline{EACEN} , \overline{EMWR} , \overline{EMADDx} , \overline{EMBSHx} , \overline{EMBSLx}	$V_{OL} = 0.4V$
	Output Low Current, LVTTL Output Type Outputs: All other outputs	
I_{OZ}	Output Leakage Current, Tri-State Output	Output High or Low $V_{OH} = V_{DD} - 0.4V$ $V_{OL} = 0.4V$
I_{DDQ}	Max Quiescent Supply Current	$V_{IN} = V_{DD}$
I_{DD}	Max Dynamic Supply Current	Normal Operation Clock = 25 Mhz ACLK/MCLK
C_I	Input Capacitance (TTL)	

- Notes:**
1. Under Typical Load, 25 Mhz ACLK/MCLK
 2. $T_A = -40^\circ\text{C}$ to 85°C , $V_{DD} = 3.3V \pm 0.3V$ Guaranteed
 3. Inputs may be modified to include pullup resistor
 4. See Section 9.2 Signal Description for pin input/output