M52259EVBUM
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M52259 Evaluation Board

For MCF52259 Evaluation/Validation

by: Microcontroller Division

1 Introduction

The M52259 Evaluation Board (EVB) is based on Freescale ColdeFire V2 family microprocessor MCF52259. This board is shipped with the MCF52259 soldered down to allow for the evaluation of all of the functionality of this part.

This board was designed as a validation and evaluation platform for MCF52259 silicon. It also implemented a CPLD on board to show some extension features.

2 Applicable Documents

- MCF52259 Reference Manual
- Universal Serial Bus Specification, Revision 2.0

Contents

3 Evaluation Board Overview

3.1 Features

The following is a list of evaluation board features.

M52259 External Interfaces:

- Fast Ethernet Controller connected to external PHY
- USB Support
  - MCF52259 on-chip OTG transceiver with device, host, and OTG support (Mini-AB receptacle)
- Crystal/Clock
- BDM/JTAG
- Three UARTs
- Fast ADC
- FlexBus
- Timers
- External Interrupts
- CAN Support
  - External CAN transceiver (DB9 connector)
- University Breakout Connector for serial interfaces (I2C, QSPI, GPIO, etc.)

Memory Subsystems:

- On-chip 64K SRAM
- On-chip 512K Flash
- On board 512KB MRAM

Power:

- Inputs:
  - 5 V Input to the voltage regulator circuitry
- Regulated On-board voltages:
  - 3.3 V - I/O Voltage
  - 1.8 V - CPLD Core Voltage

3.2 Board Diagram

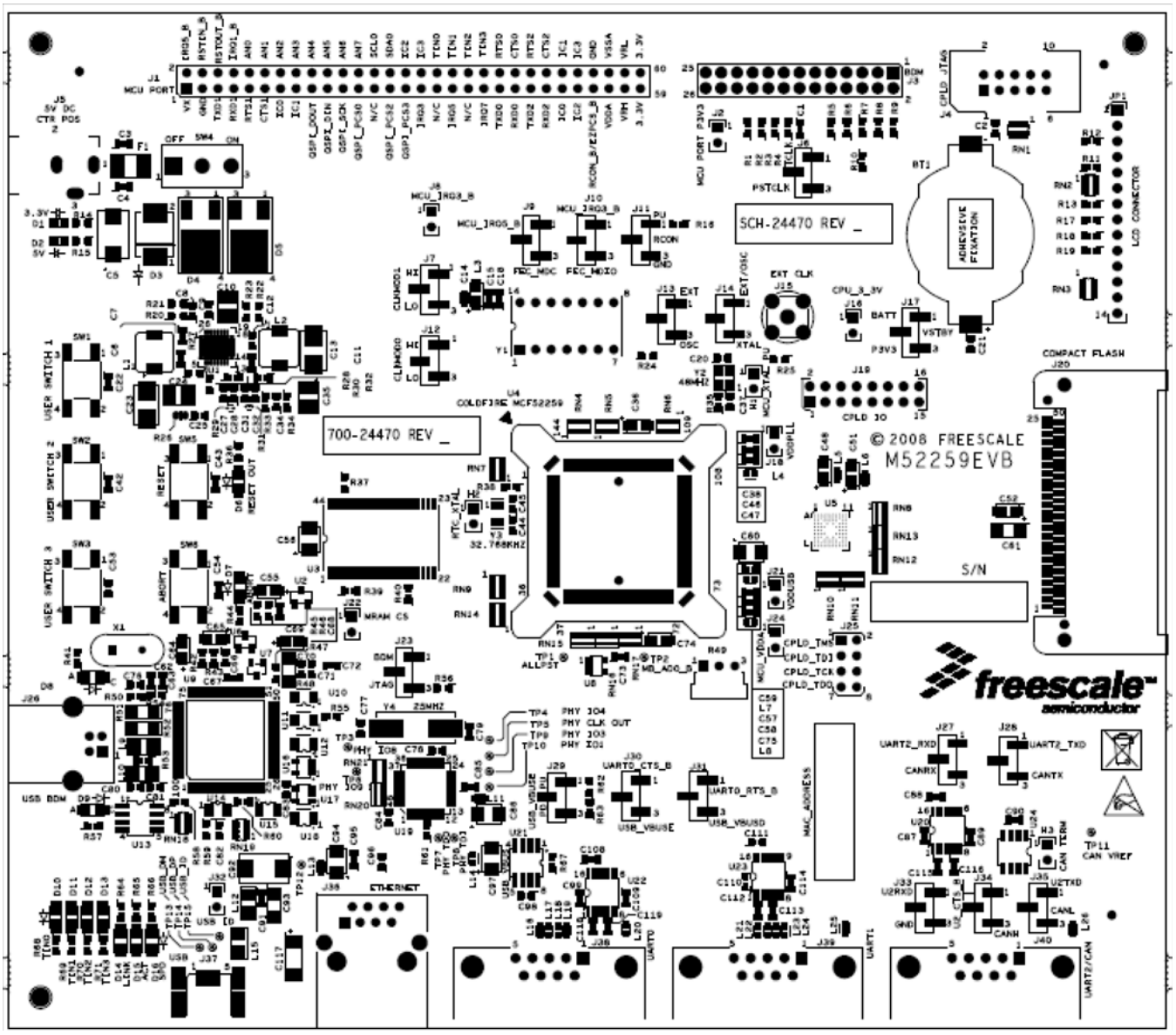

Figure 1. Board Diagram

4 Memory Map

The MCF52259 integrates 512KB internal flash and 64KB internal SRAM. Additionally the M52259EVB implements a 512K MRAM on FlexBus.

Table 1. Memory Map

Component	Start Address	End Address	Size
Internal Flash Memory			
Internal	0x0000_0000	0x0007_FFFF	512KB
Internal SRAM			
Internal	0x2000_0000	0x2000_FFFF	64 KB
Registers			
Internal	0x4000_0000		
MRAM			
Freescale MR2A16ACYS35	0x8000_0000	0x8007_FFFF	512KB
CPLD			
Altera EPM240ZM	0x8008_0000		2GB

5 Hardware Submodules

This section describes the major sections of the M52259EVB.

5.1 Processor

The MCF52259 processor is the fundamental control chip on the M52259EVB. This is a Version 2 ColdFire processor running at a maximum core speed of 80MHz, offering high performance and low power consumption. The M52259EVB allows you to fully evaluate the feature set of the MCF52259 silicon. Refer to section 3.1 to review the list of board features.

5.2 Reset

Reset can be asserted through a push button switch, SW5. The push button switch is connected to the reset line on the chip directly. Reset of the chip can also be caused by the on-board BDM circuit, or the University Breakout Connector. MCF52259 silicon also provides a Reset Out signal for peripherals, there is an on board LED D6 as indicator.

5.3 System Clocks

There are two on board clock sources on the M52259EVB -- a 48MHz crystal, and a full size oscillator socket. Alternatively, an input clock signal can be provided via an SMA connector for test purposes. The different clock signals and configurations are described below. Please refer to the MCF52259 Reference Manual for further information on the clocking requirements for the MCF52259.

Table 2. M52259EVB Clock Definitions

Clock	Description	Frequency
Socketed Oscillator Input	Jumpers J13 and J14 are used to select between clock options. Setting J13 to 2-3 and J14 to 1-2 selects the Oscillator option.	Variable
48MHz Input Crystal	Setting J14 to 2-3 selects the 48MHz Crystal option (In this mode, the setting of J13 is a don't care).	48MHz
External Clock Input	Setting J13 to1-2 and J14 to 1-2 selects the External Clock Input option. The external clock can be input on the SMA connector J15.	Variable

5.4 MRAM Interface

The M52259EVB provides 512 Kbytes of on-board MRAM (16bit x 256K Freescale MRAM). The MCF52259 is connected to the MRAM via the Mini-FlexBus 8-bit non-multiplexed mode. The AD0 signal (as well as $\overline{\text{AD0}}$) is used to select upper byte or lower byte in a 16-bit word of the 16-bit MRAM.

5.5 BDM and JTAG Interfaces — Processor

The M52259EVB provides a BDM (Background Debug Mode) header, J3, to give the end-user the ability to utilize the BDM/JTAG features of the MCF52259 processor. In addition, the M52259EVB provides an on board USB to BDM interface, J26.

5.6 FEC

The integrated Fast Ethernet Controller interfaces with an external PHY on board. The PHY also supports IEEE 1588 capability. There are 3 LEDs near RJ45 connector J36 to indicate speed, link and activity.

5.7 USB 2.0 Host and Device

The MCF52259 Processor contains a USB OTG module. This module is USB 2.0 compliant. It supports host and device modes, and provides an on-chip full-speed/low-speed transceiver. One mini-AB receptacle (USB 2.0 OTG) is provided on the M52259EVB.

5.8 Interrupts

There are four external interrupt pins provided on the MCF52259. IRQ7_B is connected to push button switch SW6 to provide a user driven ABORT signal. This signal is also connected to the LED D7 to denote when this signal is asserted.

IRQ1_B, IRQ3_B and IRQ5_B are available on the University Breakout Connector, J1. IRQ3_B is also used as the GPIO input/output for the Ethernet PHY.

5.9 Timers

The MCF52259 provides four 32-bit timers with DMA support. DT0 - DT3 are connected to LEDs D10 - D13.

5.10 QSPI

The QSPI interface is available on University Breakout Connector for user's external use.

5.11 RS232

The MCF52259 includes 3 UART modules. The M52259EVB provides three RS232 transceivers necessary to interface with RS232 connectors J38 to J40. J40 is also used as CAN connector, to enable UART function on J40, please set J33-J35 to 1-2.

5.12 CAN

MCF52259 integrates a FlexCAN module. The M52259EVB implements a CAN transceiver and connector J40 on board. J40 is multiplex with UART2, to enable CAN on J40, please set J34-J35 to 2-3.

5.13 ADC

The M52259EVB provides 8-channel 12-bit fast analog to digital converters. AN0 is connected to a variable resistor input, AN1-AN7 are available on University Breakout Connector.

5.14 Power Regulation

The M52259EVB provides one Freescale MC34717 dual switch-mode power regulator. This power regulator provide 3.3V and 1.8V to devices on the board. The regulator generates these voltages from a 5V external supply. The 5V supply is provided through a barrel jack connector. A power switch is provided to turn power to the board off.

Jumpers are provided that allow for the 3.3V supplies to be separated from the MCF52259. The intention of these jumpers is to connect a current meter to measure the power consumed by the MCF52259 processor.

5.15 Clocking Mode

The M52259EVB provides four clocking mode options as below,

- PLL disabled, clock driven by on-chip oscillator
- PLL disabled, clock driven by external crystal
- PLL in normal mode, clock driven by on-chip oscillator
- PLL in normal mode, clock driven by external crystal

The clocking mode is determined by the CLKMOD[1:0] and XTAL inputs into the MCF52259. The Jumpers J7, J12 and H1 control the CLKMOD[1:0] and XTAL inputs to the MCF52259.

5.16 Jumpers, Headers, and Switches

There are several jumpers on the M52259EVB that allow for user control of the hardware configuration. The following table provides descriptions for all the jumper settings.

Table 3. Jumper Settings

Reference Designator	Setting[1,2]	Function
H1	ON	Pull up XTAL
	OFF	External crystal input
H2	**ON**	Connects RTC_XTAL
	OFF	Leaves RTX_XTAL disconnected
H3	ON	Connects terminator to CAN bus
	OFF	No terminator on CAN bus
J2	**ON**	Connects 3.3V to University Breakout Connector
	OFF	No power to University Breakout Connector
J6	1-2	Connects TCLK to BDM
	2-3	Connects PSTCLK to BDM
J7	**1-2**	Pull up CLKMOD1
	2-3	Pull down CLKMOD1
J8	ON	Connects IRQ3 to Ethernet PHY GPIO
	OFF	Disconnects IRQ3 to Ethernet PHY GPIO
J9	**1-2**	Multiplex pin, select IRQ5
	2-3	Multiplex pin, select FEC_MDC
J10	**1-2**	Multiplex pin, select IRQ3
	2-3	Multiplex pin, select FEC_MDIO
J11	**1-2**	Single chip mode
	2-3	SFP mode
J12	**1-2**	Pull up CLKMOD0
	2-3	Pull down CLKMOD0
J13	1-2	Select external clock input from SMA connector
	2-3	Select external clock input from socketed oscillator
J14	1-2	Select external clock input from J13
	2-3	Select on board crystal input
J16	**ON**	CPU VDD is powered
	OFF	No power to CPU VDD
J17	1-2	Connects battery to VSTBY
	2-3	Connects 3.3V to VSTBY

Table 3. Jumper Settings (continued)

Reference Designator	Setting[1,2]	Function
J18	**ON**	CPU VDDPLL is powered
	OFF	No power to CPU VDDPLL
J21	**ON**	CPU VDDUSB is powered
	OFF	No power to CPU VDDUSB
J22	**ON**	Connects CS0 to MRAM
	OFF	Disconnects CS0 to MRAM
J23	**1-2**	Enable BDM mode
	2-3	Enable JTAG mode
J24	**ON**	CPU VDDA is powered
	OFF	No power to CPU VDDA
J27	1-2	Multiplex pin, select UART2_RXD
	2-3	Multiplex pin, select CANRX
J28	1-2	Multiplex pin, select UART2_TXD
	2-3	Multiplex pin, select CANTX
J29	1-2	Disable USB power
	2-3	Enable USB power
J30	1-2	Multiplex pin, select UART0_CTS
	2-3	Multiplex pin, select USB_VBUSE
J31	1-2	Multiplex pin, select UART0_RTS
	2-3	Multiplex pin, select USB_VBUSD
J32	ON	Connects USB_ID
	OFF	Disconnects USB_ID
J33	1-2	Connects UART2_RXD to J40 pin3
	2-3	Connects GND to J40 pin3
J34	1-2	Connects UART2_CTS to J40 pin7
	2-3	Connects CANH to J40 pin7
J35	1-2	Connects UART2_TXD to J40 pin2
	2-3	Connects CANL to J40 pin2

1 Bold indicates the default setting

2 ON indicates that a shunt should be fitted on the jumper; OFF indicates that no shunt should be applied.

The following table provides a description for the interface connectors.

Table 4. Interface Connectors

Reference Designator	Function
J1	University Breakout Connector
J3	BDM Header
J4	CPLD JTAG Header
J5	5V power connector
J15	SMA connector
J19	CPLD IO header
J20	Compact Flash connector
J26	USB B Connector - Used for on board BDM_USB module
J36	RJ45 connector
J37	Mini USB connector
J38	DB9 Socket used for UART0
J39	DB9 Socket used for UART1
J40	DB9 Socket used for UART2/CAN

The following table provides a description of the various switches on the board.

Table 5. Switches

Reference Designator	Function
SW1	User switch 1
SW2	User switch 2
SW3	User switch 3
SW4	Power switch
SW5	Reset switch
SW6	Abort switch

The following table provides a description of the various test points on the board.

Table 6. Test Points

Reference Designator	Signal
TP1	ALLPST
TP2	AD0_B
TP3	Ethernet PHY GPIO8
TP4	Ethernet PHY GPIO4
TP5	Ethernet PHY CLKOUT
TP6	Ethernet PHY GPIO9
TP7	Ethernet PHY TDO
TP8	Ethernet PHY TDI
TP9	Ethernet PHY GPIO3
TP10	Ethernet PHY GPIO1
TP11	CAN VREF
TP12	USB VBUS
TP13	USB_DM
TP14	USB_DP
TP15	USB_ID