IMX8ULPHDG

i.MX 8ULP Hardware Developer’s Guide

Rev. 1 — 10 August 2023 User guide

Document information

Information	Content
Keywords	i.MX 8ULP
Abstract	This document helps hardware engineers design and test the i.MX 8ULP series processors. It provides examples of board layout and design checklists to ensure first-pass success and solutions to avoid board bring-up problems.

1 Overview

This document helps hardware engineers design and test the i.MX 8ULP series processors. It provides examples of board layout and design checklists to ensure first-pass success and solutions to avoid board bring-up problems.

The reader should understand board layouts and the board-hardware terminology.

This guide is released together with relevant device-specific hardware documentation, such as datasheets, reference manuals, and application notes. All these documents are available on www.nxp.com/imx8ulpevk.

1.1 Device supported

This document supports the i.MX 8ULP device (15 x 15 mm package).

1.2 Essential references

This guide supplements the i.MX 8ULP series chip reference manuals and data sheets. For reflow profile and thermal limits during soldering, see the *General Soldering Temperature Process Guidelines* (document AN3300). These documents are available on www.nxp.com/imx8ulp.

1.3 Supplementary references

1.3.1 General information

The following resources introduce the Arm processor architecture and computer architecture:

- For information about the Arm Cortex-A35 processor, see www.arm.com/products/processors/cortex-a/cortex-a35-processor.php.
- For information about the Arm Cortex-M33 processor, see www.arm.com/products/processors/cortex-m/cortex-m33-processor.php.
- *Computer Architecture: A Quantitative Approach (Fourth Edition) - by John L. Hennessy and David A. Patterson*
- *Computer Organization and Design: The Hardware/Software Interface (Second Edition), by David A. Patterson and John L. Hennessy*

The following resources introduce the high-speed board design:

- *Right the First Time - A Practical Handbook on High-Speed PCB and System Design - Volumes I and II - Lee W. Ritchey (Speeding Edge) - ISBN 0-9741936- 0-72*
- *Signal and Power Integrity Simplified (2nd Edition) - Eric Bogatin (Prentice Hall)- ISBN 0-13-703502-0*
- *High-Speed Digital Design- A Handbook of Black Magic - Howard W. Johnson and Martin Graham (Prentice Hall) - ISBN 0-13-395724-1*
- *High-Speed Signal Propagation- Advanced Black Magic - Howard W. Johnson and Martin Graham - (Prentice Hall) - ISBN 0-13-084408-X*
- *High-Speed Digital System Design- A handbook of Interconnect Theory and Practice - Hall, Hall and McCall (Wiley Interscience 2000) - ISBN 0-36090-2*
- *Signal Integrity Issues and Printed Circuit Design - Doug Brooks (Prentice Hall) ISBN 0-13-141884-X*
- *PCB Design for Real-World EMI Control - Bruce R. Archambeault (Kluwer Academic Publishers Group) - ISBN 1-4020-7130-2*
- *Digital Design for Interference Specifications - A Practical Handbook for EMI Suppression -David L. Terrell and R. Kenneth Keenan (Newnes Publishing) - ISBN 0-7506-7282-X*

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

- *Electromagnetic Compatibility Engineering - Henry Ott (1st Edition - John Wiley and Sons) - ISBN 0-471-85068-3*
- *Introduction to Electromagnetic Compatibility - Clayton R. Paul (John Wiley and Sons) - ISBN 978-0-470-18930-6*
- *Grounding and Shielding Techniques - Ralph Morrison (5th Edition - John Wiley and Sons) - ISBN 0-471-24518-6*
- *EMC for Product Engineers - Tim Williams (Newnes Publishing) - ISBN 0-7506- 2466-3*

1.4 Related documentation

Additional literature will be published when new NXP products become available.

For the list of current documents, see www.nxp.com/imx8ulp.

1.5 Conventions

Table 1 lists the notational conventions used in this document.

Table 1. Conventions used in the document

Conventions	Description
`Courier`	Used to indicate commands, command parameters, code examples, and file and directory names.
Italics	Used to indicate command or function parameters.
Bold	Function names are written in bold.
cleared/set	When a bit takes the value of zero, it means to be cleared. When it takes a value of one, it means to be set.
mnemonics	Instruction mnemonics are shown in lowercase bold. Book titles in text are set in italics.
sig_name	Internal signals are written in all lowercase.
nnnn nnnnh	Denotes a hexadecimal number.
0b	Denotes a binary number.
rA, **r**B	Instruction syntax used to identify a source GPR.
rD	Instruction syntax used to identify a destination GPR.
REG[FIELD]	Abbreviations for registers are shown in uppercase. Specific bits, fields, or ranges appear in brackets. For example, MSR[LE] refers to the little-endian mode enable bit in the machine state register.
x	An italicized *x* indicates an alphanumeric variable.
n, m	An italicized *n* indicates a numeric variable.

In this guide, the notation for all logical, bit-wise, arithmetic, comparison, and assignment operations follow the C language conventions.

1.6 Acronyms and abbreviations

Table 2 defines the acronyms and abbreviations used in this document.

Table 2. Definitions and acronyms

Acronym	Definition
ARM	Advanced RISC Machines processor architecture

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Table 2. Definitions and acronyms*...continued*

Acronym	Definition
BGA	Ball Grid Array package
BOM	Bill Of Materials
BSDL	Boundary Scan Description Language
CAN	Flexible Controller Area Network peripheral
CGC	Clock Generation and Control
CSI	MIPI Camera Serial Interface
DDR	Dual Data Rate DRAM
DFP	Downstream Facing Port (USB Type-C)
DRP	Dual Role Port (USB Type-C)
DSI	MIPI Display Serial Interface
ENET	10/100 Mbit/s Ethernet MAC peripheral
ESR	Equivalent Series Resistance
GND	Ground
GPIO	General-Purpose Input/Output
GPR	General-Purpose Register
I^2C	Inter-Integrated Circuit interface
I^3C	Improved Inter-Integrated Circuit interface
IBIS	Input output Buffer Information Specification
IOMUX	i.MX 8ULP chip-level I/O Multiplexing
JTAG	Joint Test Action Group
LDO	Low Drop-Out regulator
LPDDR3	Low-Power DDR3 DRAM
LPDDR4	Low-Power DDR4 DRAM
LPDDR4x	Low-Power DDR4 DRAM
MII	Media Independent Interface (Ethernet)
MIPI	Mobile Industry Processor Interface
ODT	On-Die Termination
OTP	One-Time Programmable
PCB	Printed-Circuit Board
PDN	Power Distribution Network
PMIC	Power Management Integrated Circuit
POR	Power-On Reset
PTH	Plated Through Hole PCB (no microvias)
RMII	Reduced Media Independent Interface (Ethernet)
ROM	Read-Only Memory
UFP	Upstream Facing Port

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Table 2. Definitions and acronyms*...continued*

Acronym	Definition
USB	Universal Serial Bus
uSDHC	Ultra-Secured Digital Host Controller

2 i.MX 8ULP design checklist

This document provides a design checklist for the i.MX 8ULP (15 x 15 mm package) processor. The design checklist tables recommend optimal design and provide explanations to help users to understand it better. All supplemental tables referenced by the checklist appear in sections following the design checklist tables.

2.1 Design checklist table

Table 3. LPDDR4/ LPDDR4x recommendations (i.MX 8ULP)

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Connect the DDR_ZQ ball on the processor to a 240-Ω, 1-% resistor to GND.	This is a reference used during DRAM output buffer driver calibration.
	2. The ZQ0 and ZQ1 ball(s) on the LPDDR4 device should be connected through 240-Ω, 1-% resistors to the LPDDR4/ LPDDR4x VDDQ rail.	—
	3. Place a 10-kΩ pull-down resistor on DDR_RESET and this 10-kΩ resistor can be DNP. The 8ULP DDR PHY will always drive the DDR_RESET pin, even with the PHY during reset.	This ensures adherence to the JEDEC specification until the control is configured and starts driving the DDR.
	4. The ODT_CA balls on the LPDDR4/ LPDDR4x device should be connected directly to the LPDDR4/ LPDDR4x VDD2 rail.	The LPDDR4/4x ODT on the i.MX 8ULP is command-based, making the processor ODT_CA output balls unnecessary.
	5. The architecture for each chip inside the DRAM package must be x 16.	The processor does not support the byte mode specified in JESD209-4B.
	6. The processor balls DDR_DTO0/1 and DDR_PLL_TEST_P/ DDR_PLL_TEST_N should be left unconnected.	These are observability ports for manufacturing and they are not used otherwise.
	7. For a single-rank LPDDR4/LPDDR4x, both CKE0_A and CKE0_B must be connected to the DDR_CKE0 pin on the processor and DDR_CKE1 can be left unconnected. For dual-rank LPDDR4/LPDDR4x, both CKE0_A and CKE0_B should be connected to the DDR_CKE0 pin on the processor and both CKE1_A and CKE1_B should be connected to the DDR_CKE1 pin on the processor.	—
	8. If a 16-bit LPDDR4/LPDDR4x memory device is used, the signals should only be connected to channel A of the i.MX 8ULP DDR controller.	—
	9. The maximum density of an LPDDR4/LPDDR4x device that the SoC supports is 2 GB (16 Gbit).	—
	10. VDDQ_DDR is the DDR I/O supply input and VDDQX_DDR is the DDR pre-driver supply input. VDDQX_AO_DDR is the I/O supply for the CKE and	—

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Table 3. LPDDR4/ LPDDR4x recommendations (i.MX 8ULP)*...continued*

Check box	Recommendations	Explanation/Supplemental recommendations
	RESET_N pads. VDDQX_AO_DDR and VDD_DIG2 must be kept ON during the DRAM retention.	

Table 4. LPDDR3 recommendations (i.MX 8ULP)

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Connect the DDR_ZQ ball on the processor to a 240-Ω, 1-% resistor to GND.	This is a reference used during the DRAM output buffer driver calibration.
	2. The ZQ0 and ZQ1 ball(s) on the LPDDR3 device should be connected through a 240-Ω, 1-% resistors to GND.	—
	3. Place a 10-kΩ pull-down resistor on DDR_RESET and this 10-kΩ resistor can be DNP. The 8ULP DDR PHY will always drive the DDR_RESET pin, even with the PHY during reset.	This ensures the adherence to the JEDEC specification until the control is configured and starts driving the DDR.
	4. For a single-rank LPDDR3, CKE0 must be connected to the DDR_CKE0 pin on the processor. DDR_CKE1 can be left unconnected. For a dual-rank LPDDR3, CKE0 should be connected to the DDR_CKE0 pin on the processor and CKE1 should be connected to the DDR_CKE1 pin on the processor.	—
	5. The maximum density of an LPDDR3 device that the SoC supports is 2 GB (16 Gbit).	—
	6. Connect the VREFCA on the LPDDR3 device to a source that is 50 % of the voltage value of the VDDCA.	JEDEC requirements
	7. Connect the VREFDQ on the LPDDR3 device to a source that is 50 % of the voltage value of the VDDDQ when the ODT is disabled.	JEDEC requirements
	8. Connect the VREFDQ on the LPDDR3 device to a source that is 50 % of the VODTR when the ODT is enabled.	JEDEC requirements
	9. VDDQ_DDR is the DDR I/O supply input, and VDDQX_DDR is the DDR pre-driver supply input. VDDQX_AO_DDR is the I/O supply for the CKE and RESET_N pads. VDDQX_AO_DDR and VDD_DIG2 must be kept ON during the DRAM retention.	—

Table 5. I^2C/I3C recommendations

Check box	Recommendations	Explanation/supplemental recommendations
	1. Verify the target I^2C interface clock rates.	The I^2C bus can only operate as fast as the slowest peripheral on the bus. If faster operation is required, move the slow devices to another I^2C port.
	2. Verify that there are no I^2C address conflicts on any of the I^2C buses used.	There are multiple I^2C ports available on the chip. If a conflict occurs, move one of the conflicting devices to a different I^2C bus. If it is

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Table 5. I²C/I3C recommendations...*continued*

Check box	Recommendations	Explanation/supplemental recommendations
		not possible, use an I²C bus switch (NXP part number PCA9646).
	3. Do not place more than one set of pull-up resistors on the I²C lines.	This may result in excessive loading and potential incorrect operation. Choose the pull-up value to commensurate with the bus speed being used.
	4. Ensure that the VCC rail powering the i.MX 8ULP I²C interface balls matches the supply voltage used for the pull-up resistors and the slave I²C devices.	Prevent device damage or incorrect operation due to a voltage mismatch.
	5. A 1-kΩ resistor is required between I3C_PUR and I3C_SDA.	The I3C masters control an active pull-up resistance on the SDA, which they can enable and disable.

Table 6. JTAG recommendations

Check box	Recommendations	Explanation/supplemental recommendations
	1. Ensure that the on-chip pull-up/pull-down configuration is followed when external resistors are used with the JTAG signals. For example, do not use an external pull-down resistor on an input that has an on-chip pull-up resistor.	—

Table 7. Reset and ON/OFF recommendations

Check box	Recommendations	Explanation/supplemental recommendations
	1. RESET0_b must be asserted immediately at power-up and remain asserted until the real-time domain power supplies are powered and stable.	—
	2. For portable applications, the ONOFF pin may be connected to an ON/OFF SPST pushbutton switch to ground. An external pull-up resistor is required on this pin.	A brief connection to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to GND generates an interrupt (intended to initiate a software-controllable power-down). The connection to GND for approximate 5 seconds or more causes a forced OFF.
	3. RESET0_b and RESET1_b must not be tied together at the board level.	RESET0_b is the power-on reset signal for the M33 domain (real-time domain). When the M33 core is in reset, RESET0_b is driven low as an open-drain output by default. When the M33 core is not in reset, RESET0_b is an input with an on-chip pull-up resistor by default. At the system level, the system must reset the i.MX 8ULP (POR) by pulling RESET0_b low. RESET1_b is the reset indication associated with the A35 core. When the A35 core is in reset, RESET1_b is driven low as an open-drain output in default. When the A35 core is not in

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Table 7. Reset and ON/OFF recommendations*...continued*

Check box	Recommendations	Explanation/supplemental recommendations
		reset, RESET1_b is an input with an on-chip pull-up resistor by default.
	4. S/W is not able to get the status of the ON/OFF pin. In a case that requires to get the status of the ON/OFF pin, use a GPIO to sense the ON/OFF pin. It is recommended to add an N-MOS between the ON/OFF pin and the GPIO pin to prevent the potential current leakage from ON/OFF to the GPIO pin in the VBAT mode.	—

Table 8. Boot mode input recommendations

Check box	Recommendations	Explanation/supplemental recommendations
	1. For BOOT_MODE1 and BOOT_MODE0, use one of the following options to achieve logic 0: • Tie to GND through an external resistor of any size. • Tie directly to GND. • Leave unconnected. • Use one of the following options to achieve logic 1: – Tie directly to VDD_PTA. – Tie to VDD_PTA through an external 10-kΩ resistor. A value of 4.7 kΩ is preferred in high-noise environments. If switch control is desired, no external pull-down resistors are necessary. Simply connect the SPST switches directly to the VDD_PTA rail. If desired, a 4.7-kΩ to 10-kΩ series resistor can be used when the current drain is critical.	Boot inputs BOOT_MODE1 and BOOT_MODE0 each have on-chip pull-down devices. Be aware that when these are logic-high, current is drawn from the VDD_PTA supply. In production, when the on-chip fuses determine the boot configuration, both boot mode inputs can remain unconnected.
	2. Make sure that BOOT_MODE1 and BOOT_MODE0 are driven when either RESET1_b or RESET0_b is LOW.	The type of boot is controlled by BOOT_MODE1 and BOOT_MODE0, sampled at the return from reset and stored in the Boot Mode Register.

Table 9. Reset and ON/OFF recommendations

Check box	Recommendations	Explanation/supplemental recommendations
	1. The BT0_CFGn and BT1_CFGn signals are required for a proper functionality and operation and must not remain unconnected when the chip boot configuration is not determined by the fuses (during development).	See the “System Boot” chapter in the chip reference manual for the correct boot configuration. Note that an incorrect setting may result from an improper booting sequence. In production, when the on-chip fuses determine the boot configuration, both boot mode inputs can remain unconnected.
	2. Make sure that BT0_CFGn is driven before the VDD_DIG0 ramp up in the M33 LDO bypass mode or no later than when the VDD_PMC18_DIG0 is in the M33 LDO enable mode.	BT0_CFGn are sampled after the VDD_DIG0 is ON.

All information provided in this document is subject to legal disclaimers.
© 2023 NXP B.V. All rights reserved.

Table 9. Reset and ON/OFF recommendations*...continued*

Check box	Recommendations	Explanation/supplemental recommendations
	3. Make sure that BT1_CFGn is driven before the RESET0_b is de-asserted.	BT1_CFGn are sampled between RESET0_b is de-asserted and RESET1_b is is de-asserted.
	4. In the serial download mode, make sure that BT0_CFG0 (LP BOOT) has been pulled down if the [BT_FUSE_SEL] fuse is not blown. The A35 will be reset if the BT0_CFG0 (LP BOOT) has been pulled up while the [BT_FUSE_SEL] fuse is not blown, causing the serial download not to work.	—

Table 10. USB recommendations

Check box	Recommendations	Explanation/supplemental recommendations
	1. Route all USB differential signals with a 90-Ω differential impedance.	—
	2. Implement ESD protection at the connector pins. Choose a low-capacitance device recommended for high-speed interfaces.	This prevents potential damage to the board components from ESD.

Table 11. Power/decoupling recommendations

Check box	Recommendations	Explanation/supplemental recommendations
	1. Comply with the power-up sequence guidelines, as described in the data sheet to guarantee reliable operation of the device.	Any deviation from these sequences may result in the following situations: • Excessive current during power-up phase • Prevention of the device from booting • Irreversible damage to the processor (worst case)
	2. Maximum ripple voltage requirements	A common requirement for the ripple noise peak-to-peak value should be less than 5 % of the supply voltage nominal value.
	3. When using the M33 LDO bypass mode, connect a pull-down resistor to LDO_EN or tie LDO_EN to GND. A 10-kΩ pull-down resistor should be connected to VDD_PMC18_DIG0. A 10-kΩ pull-down resistor should be connected to VDD_PMC11_DIG0_CAP. VDD_DIG0 should be driven by PMIC.	—
	4. VDD_DIG1 and VDD_DIG2 must derive from the same source as a part of PMIC with no more than 50-mV (TBD) difference.	—
	5. VDD_ANA33 and VDD_PTA must be powered from the same source.	A 120-Ω ferrite bead is recommended to provide AC isolation between the digital supply (VDD_PTA) and the analog supply (VDD_ANA33).
	6. AC isolation must be provided between VDD_ANA18 and the digital 1.8-V supply it is connected to.	A 120-Ω ferrite bead is recommended to provide AC isolation between the analog supply (VDD_ANA18) and the digital 1.8-V supply.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Table 11. Power/decoupling recommendations...*continued*

Check box	Recommendations	Explanation/supplemental recommendations
	7. For PTA, PTB, PTE, and PTF, when the I/O(s) is(are) strongly driven to a high level by the peripheral device, do not turn OFF the corresponding I/O supply.	It may cause high current leakage from the I/O(s) to the corresponding I/O power supply.

Table 12. Oscillator and clock recommendations

Check box	Recommendations	Explanation/supplemental recommendations
	1.Precision 32.768-kHz oscillator: • Connect a crystal between EXTAL32 and XTAL32. • Choose a crystal with a maximum ESR of 70 kΩ and a drive level of at least 0.5 μW. • Follow the manufacturer's recommendation for loading capacitance. • Do not use an external biasing resistor because the bias circuit is on the chip.	The integrated oscillation amplifier has an on-chip self-biasing scheme, but it is high-impedance (relatively weak) to minimize power consumption. Limit the parasitic leakage from EXTAL32 and XTAL32 to either the power or the ground (> 100 MΩ) because this negatively affects the amplifier bias and causes a reduction of the startup margin. Use short traces between the crystal and the processor with a ground plane under the crystal, load capacitors, and associated traces.
	2. External kHz source: • If feeding an external clock into the device, EXTAL32 can be driven DC-coupled with the XTAL32 left unconnected or driven with a complimentary signal.	The voltage level of this driving clock must not exceed the voltage of VDD_VBAT18_CAP and the frequency must be <100 kHz under typical conditions. Do not exceed VDD_VBAT18_CAP or damage/malfunction may occur. The EXTAL32 signal must not be driven if the VDD_VBAT18_CAP supply is off. This can lead to damage or malfunction. Note that if this external clock is stopped, the internal ring oscillator starts automatically.
	3. Precision 24-MHz oscillator: • Connect a fundamental-mode crystal between EXTAL0 and XTAL0. • Choose a crystal with a maximum ESR of 100 Ω and a drive level of at least 150 μW. • Do not use an external biasing resistor because the bias circuit is on the chip.	The NXP BSP software requires 24 MHz on this clock. This clock is used as a reference for the USB, so there are strict frequency-tolerance and jitter requirements. See Table 14 for guidelines.
	4. Use an external MHz source if feeding an external clock into the device. EXTAL0 can be driven DC-coupled with the XTAL0 floating.	The NXP BSP software requires 24 MHz on this clock. This clock is used as a reference for the USB, so there are strict frequency-tolerance and jitter requirements.

Table 13. Decoupling capacitors recommendations (i.MX 8ULP)

Check box	Supply	0.22 µF	1 µF	2.2 µF	4.7 µF	10 µF	22 µF	Notes
	VDD_VBAT42	1	—	—	1	—	—	—
	VDD_FUSE18	1	—	—	—	—	—	—
	VDDQ_DDR	2	3	2	—	2	—	—
	VDDQX_DDR	2	2	—	—	—	—	—

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Table 13. Decoupling capacitors recommendations (i.MX 8ULP)*...continued*

Check box	Supply	0.22 µF	1 µF	2.2 µF	4.7 µF	10 µF	22 µF	Notes
	VDDQX_AO_DDR	—	1	—	—	—	—	—
	VDD_DIG0	1	—	1	—	1	—	—
	VDD_DIG1, VDD_DIG2, VDD_DDR_PLL, VDD_DSI11, VDD_CSI11	6	5	—	1	—	1	They are tied together on MCIMX8ULP-EVK.
	VDD_PMC18_DIG0	—	—	—	1	—	—	—
	VDD_PLL18	1	1	—	—	—	—	—
	VDD_PMC18	1	1	—	—	—	—	—
	VDD_ANA18, VREFH_ANA18	2	1	—	—	—	—	—
	VDD_VBAT18_CAP	1	—	1	—	—	—	—
	VDD_PTA, VDD_USB0_33, VDD_USB1_33	2	1	—	—	—	—	They are tied together on MCIMX8ULP-EVK.
	VDD_PTB	1	1	—	—	—	—	—
	VDD_PTC	1	1	—	—	—	—	—
	VDD_PTD	2	1	—	—	—	—	—
	VDD_PTE, VDD_PTF	4	2	—	—	—	—	They are tied together on MCIMX8ULP-EVK.
	VDD18_IOREF_1, VDD18_IOREF_2	1	—	—	—	—	—	—
	VDD_DSI18, VDD_CSI18	2	—	—	—	—	—	—
	VDD_PMC11_ DIG0_CAP	1	—	1	—	—	—	—
	VDD_USB0_18, VDD_USB1_18	2	—	—	—	—	—	—
	VDD_ANA33	1	—	—	—	—	—	—
	The capacitor part numbers used on MCIMX8ULP-EVK are as follows: • 0.22 µF --- JMK063BJ224MP-F • 1 µF --- 02016D105MAT2A • 2.2 µF --- GRM033R61A225ME47D • 4.7 µF --- C1005X5R0J475M • 10 µF --- GRM155C80J106ME11D • 22 µF --- CL10A226MQ8NRNE							

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Table 14. PCB design recommendations

Check box	Recommendations	Explanation/supplemental recommendations
	1. High-speed signal traces have the reference plane in an adjacent layer and they are impedance-controlled.	Controlled impedance is the key factor to have good signal integrity. Note that the reference plane can only be GND or the signal's own I/O power. Do not use other nets as reference.
	2. High-speed signal traces never cross gap or slot in a reference plane.	A crossing gap in a reference plane causes reflection and increases crosstalk.
	3. Place at least one GND stitching via within 50 mils of a signal via when switching reference planes.	The GND stitching via helps to keep impedance continuous and reduces the via crosstalk.
	4. Appropriate delay matching is done for the parallel bus.	Signals within a bus should have the delay time matched to maintain the timing margin.
	5. The true and complementary signal of a differential pair must have the delay matched to within 1 ps.	The true and complementary signal within a differential pair should have the delay time tightly matched.
	6. The DDR interface passed the SI simulation. Alternatively, copy the EVK DDR layout design directly.	Generally, the SI simulation should be performed for the DDR interface to ensure a stable performance. If this is not feasible, just copy the EVK DDR layout design as well as the board stack-up.
	7. Place the test point on key signals to simplify debugging. When placing the test point on high-speed signal traces, make sure that its diameter is not larger than 20 mils and the test point can be placed directly on the trace with no stub.	Test points can bring excessive capacitance and they should be handled carefully on high-speed signal traces.
	8. Decoupling capacitors are placed as close to the IC power pins as possible.	This reduces the inductance from the decoupling capacitor to the IC power pin to improve decoupling effectiveness.

Table 15. Miscellaneous recommendations

Check box	Recommendations	Explanation/supplemental recommendations
	1. For the termination of unused analog interfaces, see the data sheet for this part.	—
	2. When using PCA9460 as the PMIC, ensure that the PCB layout follows the PCA9460 data sheet. Especially for the GND vias, ensure that there are several GND vias on the PGND shapes of each BUCK.	A poor PCB layout may make the system unstable.
	3. For the boot device connection, it must be aligned with the IOMUX settings description in the system boot flow chapter.	The boot device connection must follow the ROM requirements.
	4. RMII/MII PHY must provide the reference clock to the MAC (if used).	—
	5. The 8ULP has three domains: RTD, APD, and LPAV. For details, see the architecture diagram in the reference manual and avoid using the IPs/Pins across domains. Using the IP/Pin across domains will cause extra software work, which may not be supported by the SDK.	—

All information provided in this document is subject to legal disclaimers.
© 2023 NXP B.V. All rights reserved.

2.2 JTAG signal termination

Table 16 is a JTAG termination chart showing what terminations to place on PCB designs.

Table 16. Recommended JTAG board terminations

JTAG signal	I/O type	External termination	Comments
JTAG_TCK	Input	None	Internal weak pulled down to GND
JTAG_TMS	Input	None	Internal pulled up to VDD_PTA
JTAG_TDI	Input	None	Internal pulled up to VDD_PTA
JTAG_TDO	output	100-kΩ pull-up resistor is recommended	—
JTAG_TRST_b	Input	None	Internal pulled up to VDD_PTA

2.3 Unused analog interfaces

For recommendations for unused interfaces, see the "Requirements for unused interfaces" section in the i.MX 8ULP data sheet.

3 i.MX 8ULP layout/routing recommendations

3.1 Introduction

This chapter helps design engineers with the layout of an i.MX 8ULP-based system.

3.2 Basic design recommendations

When using the Allegro design tool, the schematic symbol and the PCB footprint created by NXP is recommended. When not using the Allegro tool, use the Allegro footprint export feature (supported by many tools). If the export is not possible, create the footprint per the package dimensions outlined in the product data sheet.

The native Allegro layout and the Gerber files are available on www.nxp.com/imx8ulpevk.

3.2.1 Placing decoupling capacitors

Place small decoupling and larger bulk capacitors on the bottom side of the PCB.

The 0201 or 0402 decoupling and 0603 or larger bulk capacitors should be mounted as close to the power vias as possible. The distance should be less than 50 mils. Additional bulk capacitors can be placed near the edge of the BGA via array. Placing the decoupling capacitors close to the power balls is critical to minimize inductance and ensure high-speed transient current required by the processor. See the MCIMX8ULP-EVK layouts for examples of the desired decoupling capacitor placement.

The following list describes how to choose a correct decoupling scheme:

- Place the largest capacitance in the smallest package that the budget and manufacturing can support.
- For high-speed bypassing, select the required capacitance with the smallest package (for example, 0.1 µF, 0.22 µF, 1.0 µF, or even 2.2 µF in a 0201 package size).
- Minimize the trace length (inductance) to small caps.
- Series inductance cancels out capacitance.
- Tie capacitors to the GND plane directly with a via.
- Place capacitors close to the power ball of the associated package from the schematic.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

- A preferred BGA power decoupling design is available on the EVK board design available on www.nxp.com/imx8ulpevk. Customers should use the NXP design strategy for power and decoupling.

3.3 Stack-up and manufacturing recommendations

3.3.1 Stack-up recommendation (i.MX 8ULP)

Due to the number of balls on the i.MX 8ULP processor in the 15 mm x 15 mm package, at least a 6-layer PCB stack-up is recommended. For the 6 layers on the PCB, a sufficient number of layers must be dedicated to the power-on routing to meet the IR drop target of 2 % for the i.MX 8ULP CPU power rails.

The constraints for the trace width depend on such factors as the board stack-up and the associated dielectric and copper thickness, the required impedance, and the required current (for power traces). The stack-up also determines the constraints for routing and spacing. Consider the following requirements when designing the stack-up and selecting board material:

- The board stack-up is critical for high-speed signal quality.
- The preplanning impedance of critical traces is required.
- The high-speed signals must have the reference planes on adjacent layers to minimize crosstalk.
- The PCB material used on the MCIMX8ULP-EVK is TU768.

3.3.2 Manufacturing recommendation (i.MX 8ULP)

Because the i.MX 8ULP 15 x 15 processor uses a 0.5-mm-pitch BGA package, the PCB technology must meet the following requirements to fully fan out all the signals of the processor using PTHs (Plated Through Holes):

- The minimum trace width is 2.75 mil.
- The minimum trace to trace/pad spacing is 3.2 mil.
- The minimum via size is an 8-mil-diameter hole and a 16-mil-diameter pad.
- The minimum via-pad-to-pad spacing is 4 mil.

Figure 1 shows the reference routing of the i.MX 8ULP. The PTH is good for the fanout and the HDI is not needed.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

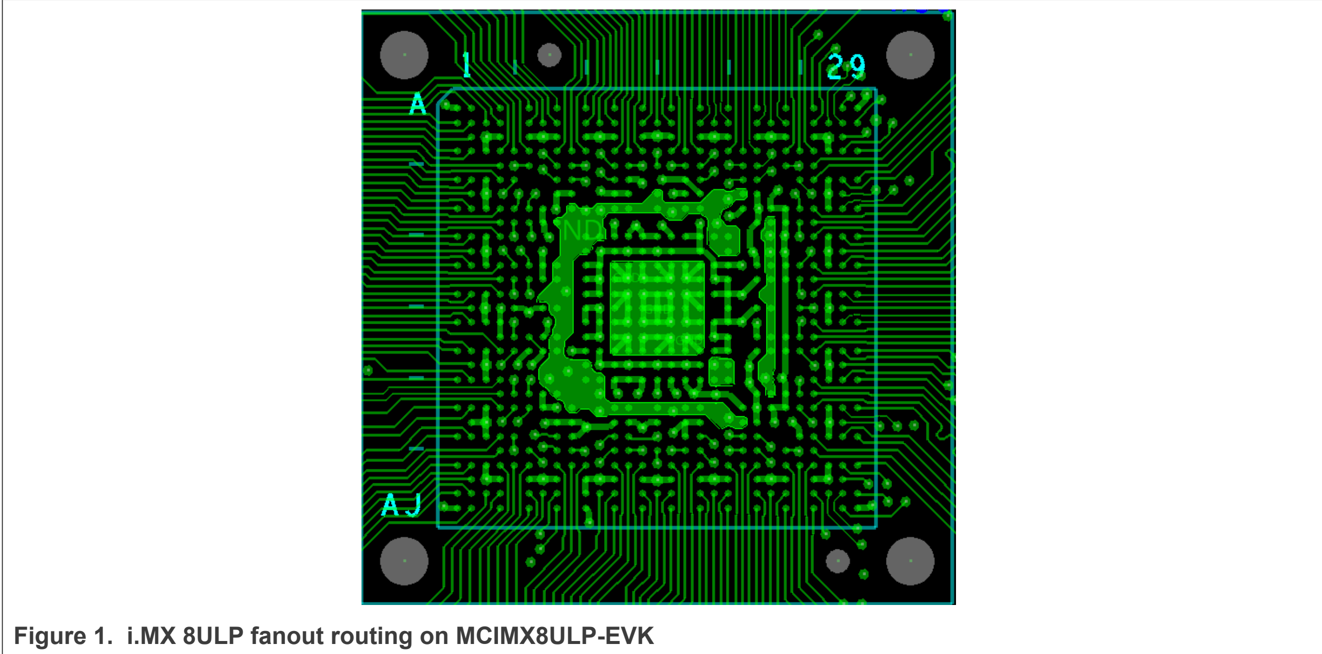

Figure 1. i.MX 8ULP fanout routing on MCIMX8ULP-EVK

3.3.3 EVK PCB stack-up (i.MX 8ULP)

Table 17 shows the stack-up of the MCIMX8ULP-EVK SOM board.

Table 17. MCIMX8ULP-SOM board stack-up information

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
1	Signal	0.33 + plating			1.15 mil
	Dielectric		106 RC77%	3.90	2.16 mil
2	GND	0.33 + plating			
	Dielectric		1080 RC69%	4.10	2.74 mil
3	Signal	1			
	Dielectric		7628 RC50% 1506 RC45% 1506 RC45% 7628 RC50%	4.70 4.80 4.80 4.70	27.56 mil
4	Power	1			
	Dielectric		1080 RC69%	4.10	3.12 mil
5	GND	0.33 + plating			
	Dielectric		106 RC77%	3.90	2.1 mil
6	Signal	0.33 + plating			1.15 mil
Finished:	47.24 (+/- 4.72) mil			1.2 (+/- 0.12) MM	
Material:	FR4				

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

3.4 DDR design recommendations

3.4.1 DDR connection information

The i.MX 8ULP processor can be used with the LPDDR4, LPDDR4x, or LPDDR3 memory. Because these memory types have different I/O signals, there are 12 generically named functional balls, depending on the type of memory used. See Table 18 for the connectivity of these generic balls for the LPDDR4, LPDDR4x, and LPDDR3 memory.

Table 18. LPDDR4/LPDDR4x/LPDDR3 connectivity

Ball name	LPDDR4 function	LPDDR4x function	LPDDR3 function
DDR_A0	CA0_A	CA0_A	CA0
DDR _A1	CA1_A	CA1_A	CA1
DDR _A2	CA2_A	CA2_A	CA2
DDR _A3	CA3_A	CA3_A	CA3
DDR _A4	CA4_A	CA4_A	CA4
DDR _A5	CA5_A	CA5_A	CA5
DDR _A6	CA0_B	CA0_B	CA6
DDR _A7	CA1_B	CA1_B	CA7
DDR _A8	CA2_B	CA2_B	CA8
DDR _A9	CA3_B	CA3_B	CA9
DDR _A10	CA4_B	CA4_B	-
DDR _A11	CA5_B	CA5_B	-

3.4.2 LPDDR4/LPDDR4x/LPDDR3 design recommendations

The following list provides some generic guidelines to adhere to when implementing an i.MX 8ULP design using LPDDR4/LPDDR4x/LPDDR3 memory.

1. Refer to the solid GND plane only for all the high-speed signal traces.
2. Keep the edge-to-edge spacing of high-speed signal traces no less than 2 times the trace width to minimize trace crosstalk.
3. The CLK and DQS signals can be routed on a different layer with the DQ/CA signals to ease routing. When doing this, keep no less than 5 times the trace width spacing from other signals.
4. Use the time delay instead of the length when performing the delay matching. The delay matching includes the PCB trace delay and the IC package delay. Incorporate the package pin delay into the CAD tool's constraint manager.
5. Include the delay of vias when performing delay matching. This can be realized in the Allegro tool by enabling the **Z-Axis Delay** in "Setup -> Constraints -> Modes".
6. For the LPDDR4/LPDDR4x memory, the byte swapping within each 16-bit channel is good. The bit swapping within each slice/byte lane is good.
7. For LPDDR3, the byte swapping within the 32-bit channel is good. The bit swapping within each slice/byte lane is good.
8. The bit swapping of the Command/Address (CA[5:0] for LPDDR4/ LPDDR4x and CA[9:0] for LPDDR3) signals is **NOT** recommended.
9. For the LPDDR4 and LPDDR4x memory, i.MX 8ULP does not drive the DDR_ODT0 and DDR_ODT1 signals. The ODT_CA balls on the LPDDR4 and LPDDR4x devices should be connected directly to the VDD2 supply.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

10. Enable the DBI (Data Bus Inversion) feature. It reduces both power consumption and power noise.

3.4.2.1 i.MX 8ULP LPDDR4/LPDDR4x routing recommendations

Table 19. LPDDR4/LPDDR4x routing recommendations

	LPDDR4/4x-1066				
	LPDDR4/4x signal	Group	PCB + package prop delay		Considerations
			Min	Max	
Ch A	CK_t_A/CK_c_A	Clock	Short as possible	300 ps	Match the true/ complement signals within 2ps.
	CAx_A/CSx_A/ CKEx_A	Address/ Command/ Control	CK_t_A - 75 ps	CK_t_A + 75 ps	
	DQS0_t_A/DQS0_ c_A	Byte 0 - DQS	CK_t_A - 75 ps	CK_t_A + 75 ps	Match the true/ complement signals of DQS within 2ps.
	DQ[7:0]_A/DMI0_A	Byte 0 - Data	DQS0_t_A	DQS0_t_A +50 ps	
	DQS1_t/DQS1_c	Byte 1 - DQS	CK_t_A - 75 ps	CK_t_A + 75 ps	
	DQ[15:8]/DMI1_A	Byte 1 - Data	DQS1_t_A	DQS1_t_A +50 ps	
Ch B	CK_t_B/CK_c_B	Clock	Short as possible	300 ps	Match the true/ complement signals within 2ps.
	CAx_B/CSx_B/ CKEx_B	Address/ Command/ Control	CK_t_B - 75 ps	CK_t_B + 75 ps	
	DQS0_t_B/DQS0_ c_B	Byte 0 - DQS	CK_t_B - 75 ps	CK_t_B + 75 ps	Match the true/ complement signals of DQS within 2ps.
	DQ[7:0]_B/DMI0_B	Byte 0 - Data	DQS0_t_B	DQS0_t_B +50 ps	
	DQS1_t_B/DQS1_ c_B	Byte 1 - DQS	CK_t_B - 75 ps	CK_t_B + 75 ps	
	DQ[15:8]_B/DMI1_ B	Byte 1 - Data	DQS1_t_B	DQS1_t_B +50 ps	

The delay of the via transitions must be included in the overall calculation. This can be realized in the Allegro tool by enabling the **Z-Axis Delay** in “Setup - Constraints - Modes”.

NXP recommends to simulate your LPDDR4/LPDDR4x implementation before fabricating PCBs.

3.4.2.2 LPDDR4/LPDDR4x routing example (i.MX 8ULP)

Figure 2 to Figure 4 show the placement and routing of the LPDDR4/LPDDR4x signals on the MCIMX8ULP-EVK. The CLK and DQS signals are routed on the bottom layer to save routing space on the top layer and layer 3. The channel A data byte lane 1 and channel B data byte lane 1 signals are routed on the top layer. The channel A data byte lane 0, channel B data byte lane 0, and CA/CTL signals are routed on layer 3. This makes the signal travel on the via as short as possible to minimize the via crosstalk.

 All information provided in this document is subject to legal disclaimers. © 2023 NXP B.V. All rights reserved.

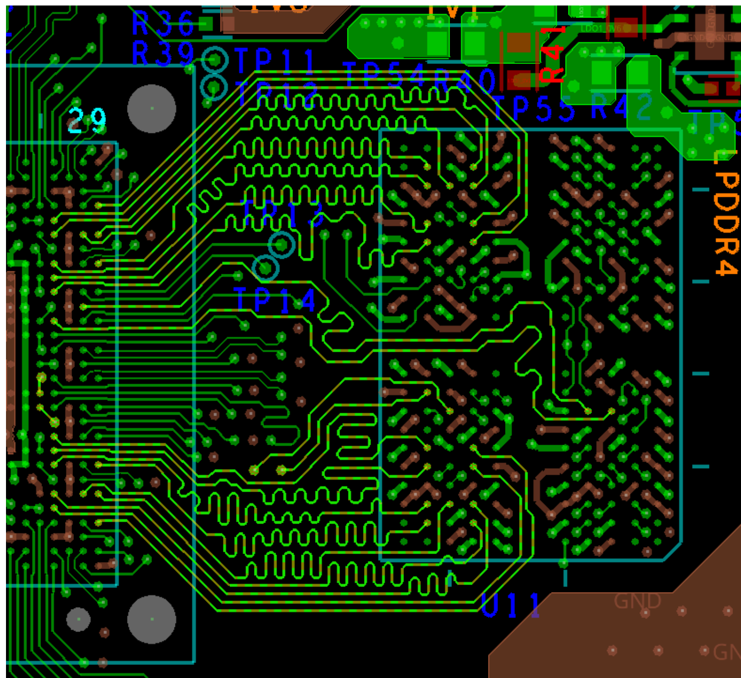

Figure 2. MCIMX8ULP-EVK LPDDR4/LPDDR4x routing (top layer)

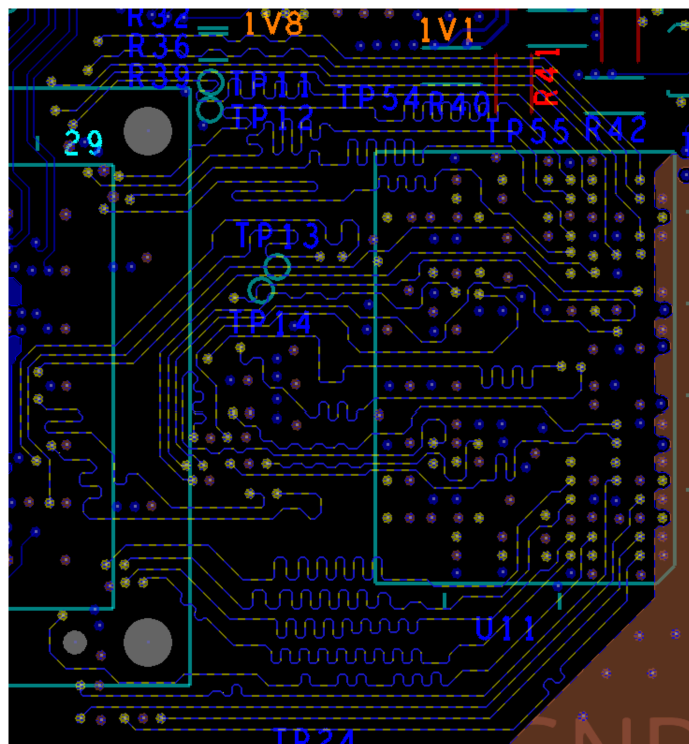

Figure 3. MCIMX8ULP-EVK LPDDR4/LPDDR4x routing (layer 3)

© 2023 NXP B.V. All rights reserved.

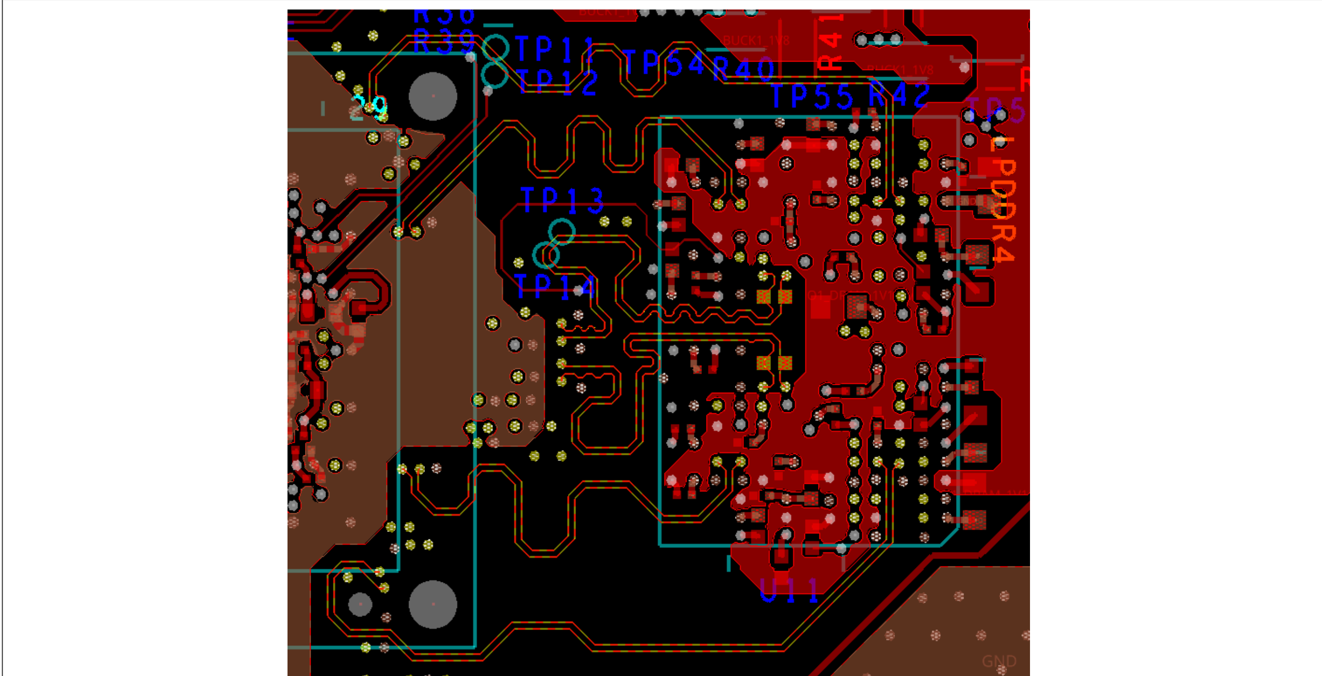

Figure 4. MCIMX8ULP-EVK LPDDR4/LPDDR4x routing (bottom layer)

3.4.3 i.MX 8ULP LPDDR3 design recommendations

Table 20. LPDDR3 routing recommendations

LPDDR3-800				
LPDDR3 signal	**Group**	**PCB + package prop delay**		**Considerations**
		Min	**Max**	
CK_t/CK_c	Clock	Short as possible	300 ps	Match the true/ complement signals within 2ps.
CAx	Address/ Command/ Control	CK_t - 75 ps	CK_t + 75 ps	
CKEx, CSx, ODT	Control	CK_t - 15 ps	CK_t + 15 ps	
DQS0_t/DQS0_c	Byte 0 - DQS	CK_t - 75 ps	CK_t	Match the true/ complement signals of DQS within 2ps.
DQ[7:0]/DM0	Byte 0 - Data	DQS0_t	DQS0_t +50 ps	
DQS1_t/DQS1_c	Byte 1 - DQS	CK_t - 75 ps	CK_t	
DQ[15:8]/DM1	Byte 1 - Data	DQS1_t	DQS1_t +50 ps	
DQS2_t/DQS2_c	Byte 2 - DQS	CK_t - 75 ps	CK_t	
DQ[23:16]/DM2	Byte 2 - Data	DQS2_t	DQS2_t +50 ps	
DQS3_t/DQS3_c	Byte 3 - DQS	CK_t - 75 ps	CK_t	
DQ[31:24]/DM3	Byte 3 - Data	DQS3_t	DQS3_t +50 ps	

The delay of the via transitions must be included in the overall calculation. This can be done in the Allegro tool by enabling the **Z-Axis Delay** in "Setup - Constraints - Modes".

NXP recommends to simulate your LPDDR3 implementation before fabricating PCBs.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

3.4.3.1 LPDDR3 routing example (i.MX 8ULP)

Figure 5 to Figure 8 show the placement and routing of LPDDR3 signals on X-8ULPLPD3-QA-15. The CLK and DQS signals are routed on the bottom layer to save routing space on the top layer and layer 3. The data byte lane 0 and data byte lane 3 signals are routed on the top layer. The data byte lane 1 and data byte lane 2 are routed on layer 3. The CA/CTL signals are routed on layer 12. This makes the signal travel on the via as short as possible to minimize via crosstalk.

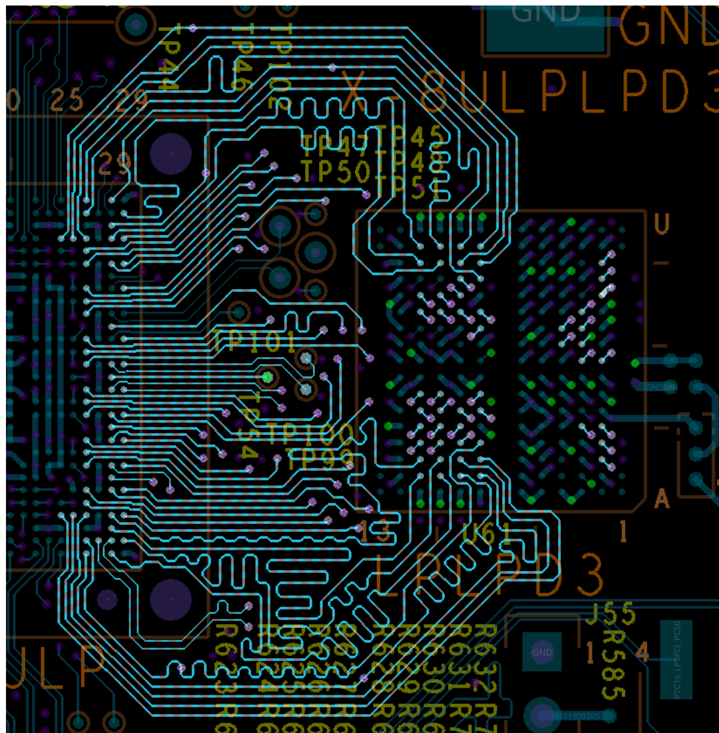

Figure 5. X-8ULPLPD3-QA-15 LPDDR3 routing (top layer)

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

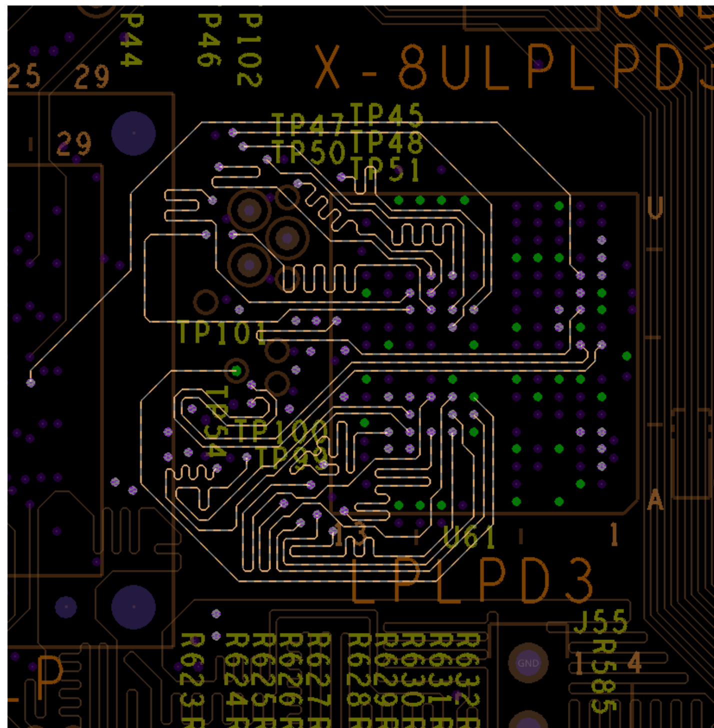

Figure 6. X-8ULPLPD3-QA-15 LPDDR3 routing (layer 3)

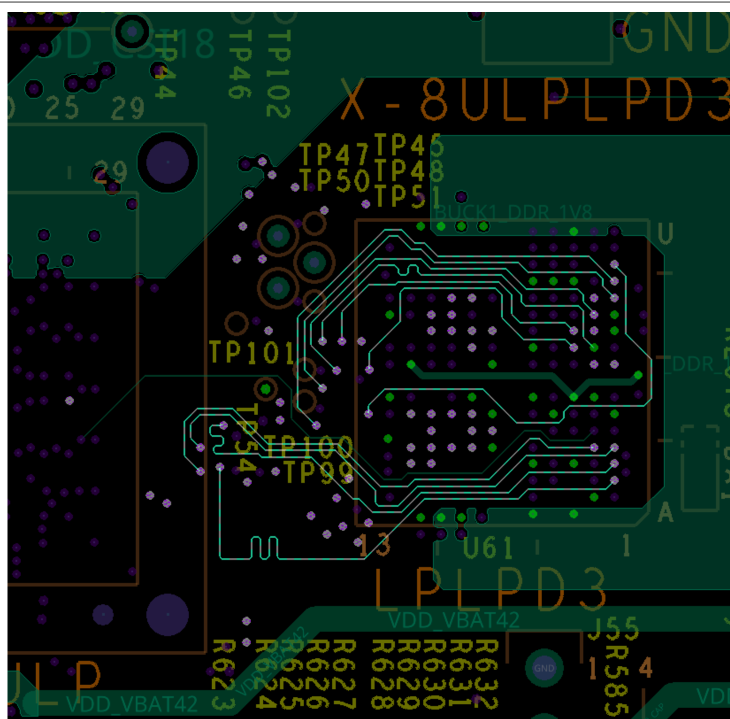

Figure 7. X-8ULPLPD3-QA-15 LPDDR3 routing (layer 12)

© 2023 NXP B.V. All rights reserved.

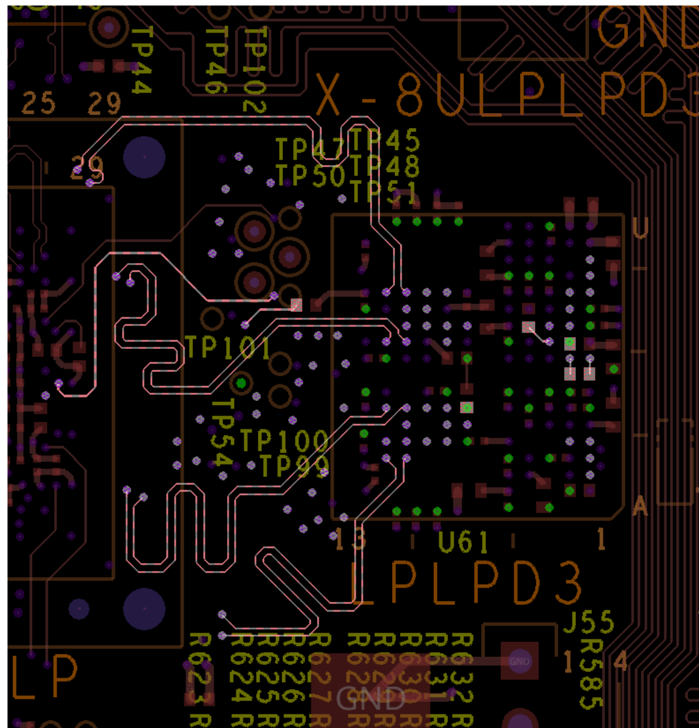

Figure 8. X-8ULPLPD3-QA-15 LPDDR3 routing (bottom)

3.4.4 i.MX 8ULP DDR SI simulation guide

The simulation architecture includes the DDR controller (the i.MX 8ULP processor), the PCB, and the DRAM device. The IBIS model for the i.MX 8ULP processor is available on the NXP website. The DRAM device IBIS model must be obtained from the memory vendor.

This section describes how to check the SI performance of the layout for a DDR design using the i.MX 8ULP.

- Firstly, perform the S-parameter extraction:
  - It requires a 2.5D full-wave extraction tool, such as PowerSI from Cadence.
  - Set the extraction bandwidth to 12 GHz.
  - Port reference impedance: 50 Ω for signal ports, and 0.1 Ω for power ports.
  - Coupled mode: Set the rise time to 20 ps and coupling coefficient to 1 %.
- Secondly, perform time domain simulation:
  - Stimulus pattern: 500-bit random code and different pattern for each signal within the same byte.
  - Ideal power.
  - The drive strength at the transmitter is 40 Ω, while the ODT at the receiver is 60 Ω.
  - Probe at the die.
  - Simulation at slow corner (worst case).
  - The Eye waveform is triggered by aligning with the timing reference (DQS/CLK).
  - See the appropriate JEDEC standards for the Rx Mask definition: JESD209-4 for LPDDR4 and LPDDR4x, JESD209-3 for LPDDR3.

When the simulation is done, find the simulated worst eye width and compare it with the following requirements to see if it can pass:

- For LPDDR4-1066:
  - DQ Write: Eye width @VREF ±70 mV should be over 850 ps.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

  - DQ Read: Eye width @VREF ±70 mV should be over 810 ps.
  - CA/ CS: Eye width @VREF ±87.5 mV should be over 1700 ps.
- For LPDDR4x-1066:
  - DQ Write: Eye width @VREF ±70 mV should be over 810 ps.
  - DQ Read: Eye width @VREF ±70 mV should be over 810 ps.
  - CA/ CS: Eye width @VREF ±87.5 mV should be over 1650 ps.

Figure 9 shows an example of simulated eye width of LPDDR4-1066 DQ write.

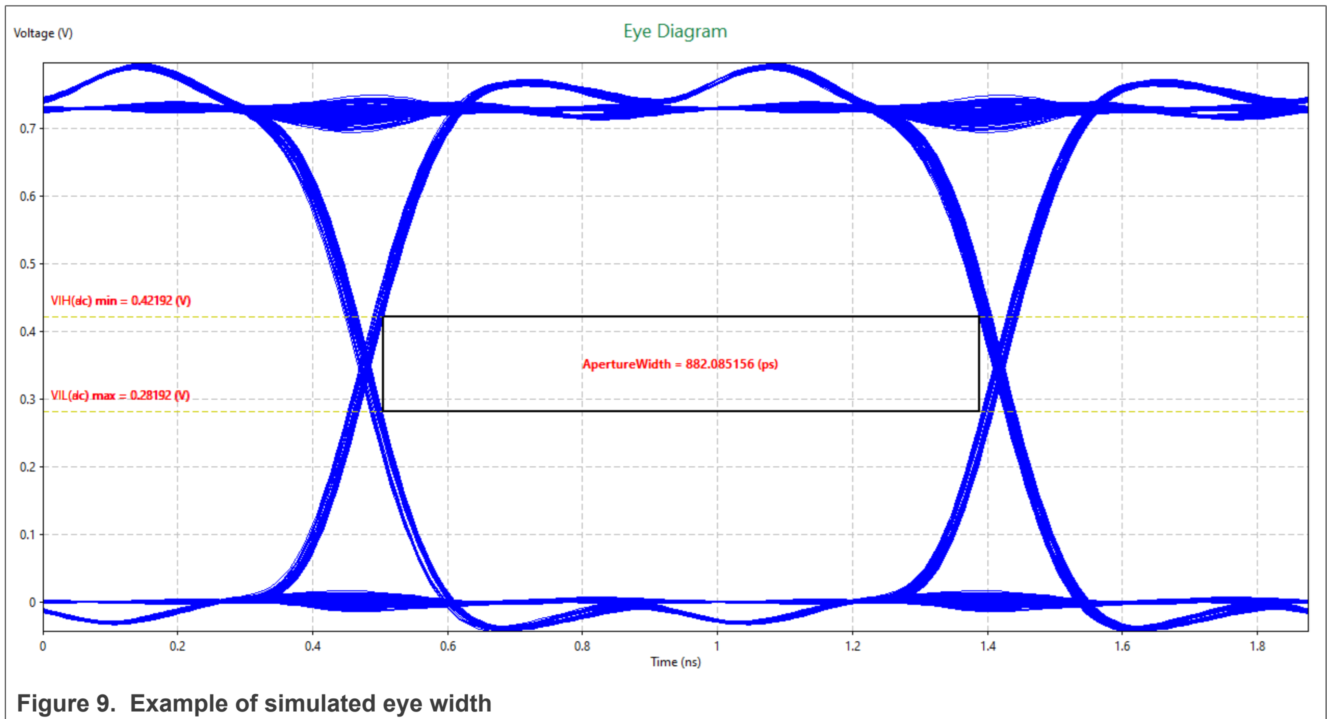

Figure 9. Example of simulated eye width

3.4.5 i.MX 8ULP DDR package delay

When performing the required delay matching for the LPDDR4/LPDDR4x/LPDDR3 routing, the bond wires within the i.MX 8ULP package must be accounted for and included in the match calculation. Table 21 lists the propagation/fly time from the die I/O to the package ball.

Table 21. i.MX 8ULP 15 x 15 package DDR package trace delays

Ball name	Delay (ps)	Ball name	Delay (ps)
DDR_A0	61.3	DDR_DQ11	65.8
DDR_A1	60.1	DDR_DQ12	65.8
DDR_A2	51.9	DDR_DQ13	66.1
DDR_A3	55.7	DDR_DQ14	59.1
DDR_A4	60.6	DDR_DQ15	65.3
DDR_A5	56.5	DDR_DQ16	55.7
DDR_A6	60.3	DDR_DQ17	64.0
DDR_A7	56.6	DDR_DQ18	65.8
DDR_A8	50.5	DDR_DQ19	77.1

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Table 21. i.MX 8ULP 15 x 15 package DDR package trace delays*...continued*

Ball name	Delay (ps)	Ball name	Delay (ps)
DDR_A9	56.1	DDR_DQ20	70.9
DDR_A10	72.2	DDR_DQ21	69.3
DDR_A11	67.1	DDR_DQ22	75.2
DDR_CK0_N	49.1	DDR_DQ23	75.5
DDR_CK0_P	49.5	DDR_DQ24	71.5
DDR_CK1_N	48.9	DDR_DQ25	69.5
DDR_CK1_P	51.1	DDR_DQ26	70.0
DDR_CKE0	49.8	DDR_DQ27	63.8
DDR_CKE1	60.0	DDR_DQ28	63.5
DDR_CS0_A_B	49.2	DDR_DQ29	60.3
DDR_CS0_B_B	54.4	DDR_DQ30	57.0
DDR_CS1_A_B	50.9	DDR_DQ31	61.8
DDR_CS1_B_B	53.9	DDR_DQS0_N	68.9
DDR_DM0	61.6	DDR_DQS0_P	70.4
DDR_DM1	63.1	DDR_DQS1_N	58.6
DDR_DM2	64.7	DDR_DQS1_P	57.3
DDR_DM3	62.4	DDR_DQS2_N	67.7
DDR_DQ0	57.2	DDR_DQS2_P	68.4
DDR_DQ1	66.9	DDR_DQS3_N	55.9
DDR_DQ2	59.5	DDR_DQS3_P	54.8
DDR_DQ3	72.9	DDR_DTO0	66.9
DDR_DQ4	68.7	DDR_DTO1	65.7
DDR_DQ5	66.5	DDR_ODT0	49.0
DDR_DQ6	78.1	DDR_ODT1	60.2
DDR_DQ7	69.1	DDR_PLL_TEST_N	57.9
DDR_DQ8	71.7	DDR_PLL_TEST_P	56.2
DDR_DQ9	65.1	DDR_RAM_RST_B	48.8
DDR_DQ10	67.4	DDR_ZQ	53.9

Table 22. i.MX 8ULP 9.4x9.4 package DDR package trace delays

NetName	Delay(pS)	NetName	Delay(pS)
DDR_A0	11.06	DDR_DQ9	31.19
DDR_A1	33.11	DDR_DQ10	30.02
DDR_A2	31.47	DDR_DQ11	30.42
DDR_A3	28.34	DDR_DQ12	24.89
DDR_A4	15.06	DDR_DQ13	18.41

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Table 22. i.MX 8ULP 9.4x9.4 package DDR package trace delays*...continued*

NetName	Delay(pS)	NetName	Delay(pS)
DDR_A5	28.94	DDR_DQ14	15.57
DDR_A6	42.32	DDR_DQ15	20.05
DDR_A7	31.66	DDR_DQ16	30.95
DDR_A8	38.82	DDR_DQ17	26.63
DDR_A9	25.74	DDR_DQ18	38.41
DDR_A10	25.56	DDR_DQ19	31.91
DDR_A11	16.28	DDR_DQ20	42.76
DDR_CK0_N	18.46	DDR_DQ21	37.5
DDR_CK0_P	19.18	DDR_DQ22	40.04
DDR_CK1_N	23.48	DDR_DQ23	42.39
DDR_CK1_P	25.68	DDR_DQ24	36.15
DDR_CKE0	24.06	DDR_DQ25	36.87
DDR_CKE1	28.64	DDR_DQ26	57.71
DDR_CS0_A_B	54.59	DDR_DQ27	32.5
DDR_CS0_B_B	29.64	DDR_DQ28	26.8
DDR_CS1_A_B	18.51	DDR_DQ29	23.99
DDR_CS1_B_B	25.27	DDR_DQ30	28.12
DDR_DM0	29.72	DDR_DQ31	19.47
DDR_DM1	21.99	DDR_DQS0_N	34.47
DDR_DM2	41.76	DDR_DQS0_P	35.09
DDR_DM3	29.4	DDR_DQS1_N	23.27
DDR_DQ0	33.91	DDR_DQS1_P	23.98
DDR_DQ1	29.3	DDR_DQS2_N	37.15
DDR_DQ2	41.07	DDR_DQS2_P	38.67
DDR_DQ3	30.66	DDR_DQS3_N	24.61
DDR_DQ4	28.85	DDR_DQS3_P	24.63
DDR_DQ5	27.66	DDR_DTO0	19.72
DDR_DQ6	28.98	DDR_DTO1	15.73
DDR_DQ7	26.23	DDR_ODT0	39.35
DDR_DQ8	28.34	DDR_ODT1	14.07

3.4.6 High-speed routing recommendations

The following list shows the routing traces for high-speed signals. The propagation delay and the impedance control should match to ensure correct communication with the devices:

- High-speed signals (DDR, RMII, MIPI, and so on) must not cross gaps in the reference plane.
- Avoid creating slots, voids, and splits in reference planes. Review via placements to ensure that they do not inadvertently create splits/voids (space the vias out to eliminate this possibility).

All information provided in this document is subject to legal disclaimers.
© 2023 NXP B.V. All rights reserved.

- Ensure that ground-stitching vias are present within 50 mils from signal-layer-transition vias on high-speed signals when transitioning between different reference ground planes.
- A solid GND plane must be directly under the crystals associated to components and traces.
- The clocks or strobes that are on the same layer must be placed at least 2.5x the height away from the reference plane spacing and adjacent traces to reduce crosstalk.
- All synchronous interfaces should have appropriate bus delay matching.
- The true and complementary signals of a differential pair must have the delay matched within 1 ps.

3.4.7 Reset architecture/routing

A reset button may be connected to the PMIC_RST_B pin of the PMIC (PCA9460) for development purposes. This allows all voltages to be put to their initial default power-on state when releasing the reset button. When you press and hold the button for more than 8 seconds, it could issue a PMIC cold reset with default PMIC settings. All power rails are recycled, except for the LDO_SNVS. During this time, the RESET0_b driven by the PMIC is kept asserted (low). This state lasts for several hundreds of milliseconds to provide enough time for the power supplies to be completely powered down. The power supplies start to ramp up again in the defined sequence. When all the power supplies reach their operating voltages, RESET0_b is de-asserted and the CPU may begin booting from the reset.

3.5 Trace impedance recommendations

See Table 23 when you are updating or creating constraints in the PCB design tool to set up the impedances/ trace widths.

Table 23. Trace impedance recommendations

Signal group	Impedance	PCB manufacturer tolerance (+/-)
All single-ended signals, unless specified	50 Ω single-ended	10 %
DDR DQS/CLK	100 Ω differential	10 %
USB differential signals	90 Ω differential	10 %
Differential signals, including Ethernet and MIPI (CSI and DSI)	100 Ω differential	10 %

3.6 Power connectivity/routing

Delivering clean and reliable power to the i.MX 8ULP internal power rails is critical to a successful board design. The PCB PDN should be designed to accommodate the maximum output current from each SMPS into the i.MX 8ULP supply balls. Table 24 lists the design goals for each high-current i.MX 8ULP power rail.

Table 24. i.MX 8ULP maximum current design levels

Supply input	Assumed maximum current (mA)
VDDQ_DDR	600 for LPDDR4 400 for LPDDR4x (TBD)
VDD_DIG0	500 (TBD)
VDD_DIG1 and VDD_DIG2	1000 (TBD)

3.6.1 i.MX 8ULP power distribution block diagram

There are companion PMICs that provide a low-cost and efficient solution for powering the i.MX 8ULP processor (for example, NXP PCA9460).

© 2023 NXP B.V. All rights reserved.

There are 3 types of the NXP PCA9460 processor: PCA9460A, PCA9460B, and PCA9460C. The default output of BUCK4 and LDO1 is different for each type of PCA9460. See the data sheet of NXP PCA9460 for details.

Figure 15 shows a block diagram of the power tree of the NXP MCIMX8ULP-EVK. It uses a PCA9460A PMIC to power ON the rails of the processor. It supports both LPDDR4 and LPDDR4x.

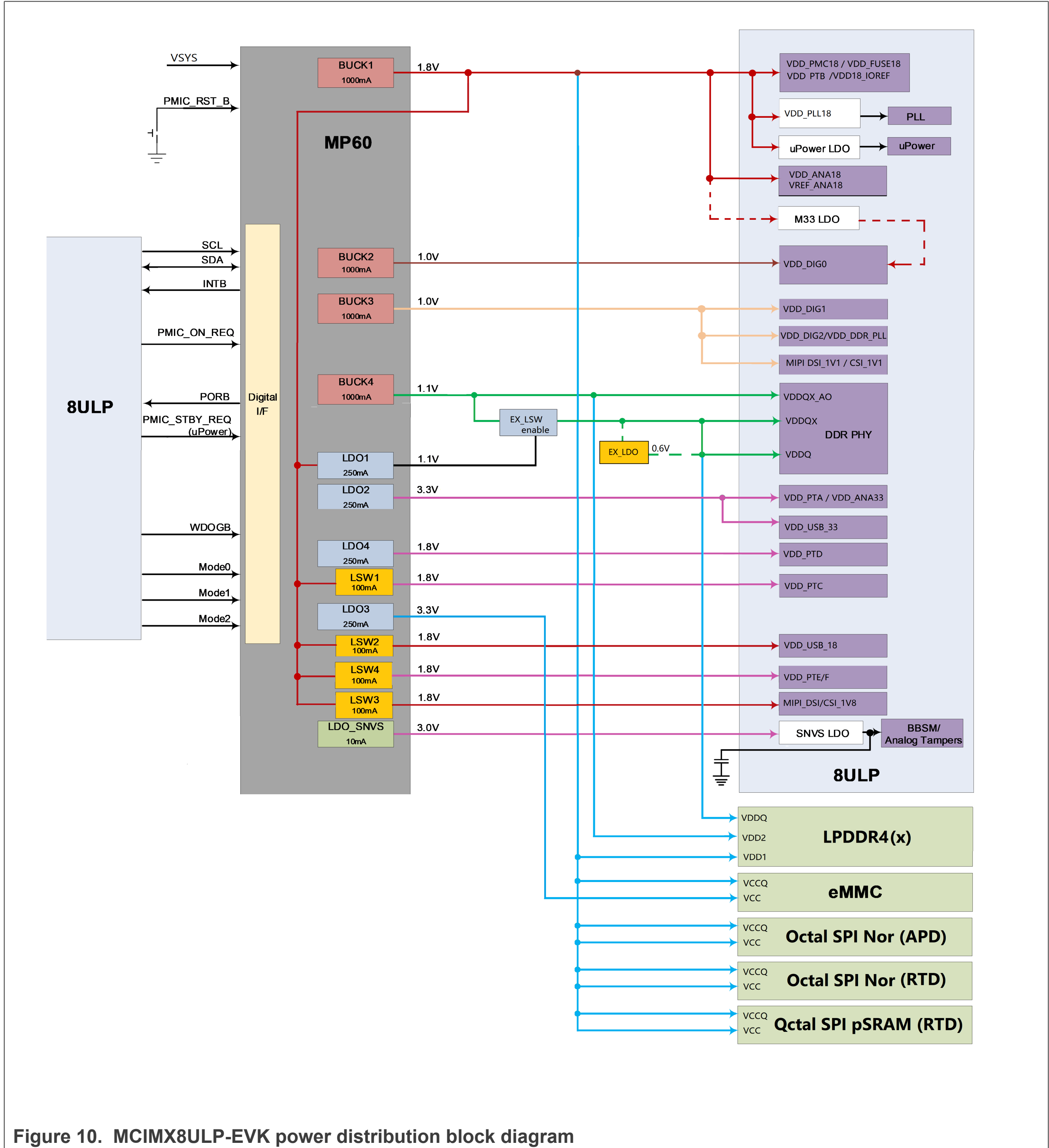

Figure 10. MCIMX8ULP-EVK power distribution block diagram

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

3.6.2 Power routing/distribution requirements

To design a good Power Delivery Network (PDN) is complicated. It includes the following:

1. Choose a good PCB stack-up (adequate copper thicknesses and layer assignments/utilization).
2. Optimize the placement and routing of the PDN. This includes good placement of the decoupling capacitors and connecting them to the power ground planes with as short and wide a trace as possible, because the increased inductance of a longer etch degrades the effectivity of the capacitor). Use the number/placement of capacitors on the NXP development platforms.
3. Optimize the DC IR drop. This involves using very wide traces/plane fills to route high-current power nets and ensure an adequate number of vias on the power net layer transitions. The neck down of fill areas should be minimized and the current density minimized. The maximum DC IR drop on a board should be 2 % (preferably 1 %) of the voltage rail. On a 1.1-V rail, the maximum voltage drop should be less than 0.022 V (preferably less than 0.011 V). See Table 25 for the DC IR drop requirement.
4. AC impedance check - the target impedance at different frequencies should be lower than the specified values. See Table 26 for the impedance targets and frequency for the specified power rail of an i.MX 8ULP PCB design.

Table 25. i.MX 8ULP DC IR drop requirements

Supply input	Nominal voltage (V)	Assumed maximum current (mA)	IR drop target	Corresponding power path resistance requirement (mΩ)
VDDQ_DDR	1.1/0.6	600/400 (TBD)	<2 %	< 3.6/<3 (TBD)
VDD_DIG0	1.0	500 (TBD)	<2 %	<40 (TBD)
VDD_DIG1 and VDD_DIG2	1.0[1]	1000 (TBD)	<1.5 %	< 15 (TBD)

5. The default output voltage of VDD_DIG1 and VDD_DIG2 is 1.0 V. The software changes it to 1.1 V in the U-Boot.

Table 26. i.MX 8ULP PDN target impedance

Supply input	< 20 MHz (mΩ)	20 - 100 MHz (mΩ)
VDDQ_DDR	15	45
VDD_DIG0	65	350
VDD_DIG1 and VDD_DIG2	20	90

3.7 USB connectivity

The i.MX 8ULP provides two complete USB2.0 interfaces and supports the following configurations (or any subset):

- Dedicated host or device using Type-A or Type-B connectors
- Dual role using Type-C connector

To implement a USB Type-C interface (UFP, DFP, or DRP), external hardware must be added to manage the two configuration channel IOs (CC1 and CC2) as well as monitor the plug orientation.

See the NXP development platform schematic for an example USB Type-C implementation.

3.8 uSDHC connectivity

The i.MX 8ULP provides 3 uSDHC interfaces and each uSDHC instance on each port has a different maximum frequency. See Table 27 for the uSDHC target maximum frequency.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Table 27. i.MX 8ULP uSDHC target maximum frequency

SDHC instance	Muxed location	Maximum frequency (MHz)
uSDHC0	PTD	200
uSDHC1	PTD	166
	PTE	100
	PTF	100
uSDHC2	PTD	166
	PTE	100
	PTF	100

The eMMC is usually connected to the uSDHC0 on the PTD.

The SD card slot usually supports both SD2.0 and SD3.0 and a uSDHC I/O voltage change is required to switch the timing from SD2.0 to SD3.0. However, the SDHC I/Os share the I/O power supply with other I/Os on the same port. To avoid changing the voltage level of other I/Os on the same port, use a level shift between the i.MX 8ULP and the SD card slot, such as NXP NVT4857UK, an SD 3.0-compliant bidirectional dual voltage level translator with auto-direction control.

4 Avoiding board bring-up problems

4.1 Introduction

This chapter describes how to avoid mistakes when bringing up a board for the first time. The recommendations below consist of basic techniques for detecting board issues and preventing/locating the three issues encountered: power, clocks, and reset.

4.2 Avoiding power pitfalls — current

Excessive current can damage the board. Use a current-limiting laboratory supply set to the expected main current draw (at most). Monitor the main supply current with an ammeter when powering up the board for the first time. You can use the supply's internal ammeter (if you have one). By monitoring the main supply current and controlling the current limit, any excessive current can be detected before a permanent damage occurs.

Before the board test, you can ohm out the board power rails to the ground to verify that there are no short circuits. Then, you can power on the board and there is no damage to the board and/or components.

4.3 Avoiding power pitfalls — voltage

To avoid incorrect voltage rails, create a basic table called "voltage report" before the board bring up/testing. The table helps to validate that all the supplies are reaching the expected levels.

To create a voltage report, list the following:

- Board voltage sources
- Default power-up values for the board voltage sources
- Best location on the board to measure the voltage level of each supply

Determine the best measurement location for each power supply to avoid a large voltage drop (IR drop) on the board. The drop causes inaccurate voltage values. The following guidelines help you to produce the best voltage measurements:

- Measure as close to the load as possible (in the case of the i.MX8 ULP processor).

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

- Make two measurements: the first after the initial board power-up and the second while running a heavy use case that stresses the i.MX8 ULP processor.

Ensure that the i.MX8 ULP power supply meets the DC electrical specifications listed in the chip-specific data sheet. See Table 28 for a sample voltage report table.

Note: *This report table is for the MCIMX8ULP-EVK. The sample voltage reports for the customer's PCBs are different from this, depending on the processor and the Power Management IC (PMIC) used and the assignment of the PMIC power resources.*

Table 28. Sample voltage report table

Source	Net name	Expected (V)	Measured (V)	Comment
DC jack input	PSU_5V0	5.0	-	Main supply for MCIMX8ULP-EVK
PCA9460_BUCK1	BUCK1_1V8	1.8	-	-
PCA9460_BUCK2	BUCK2_1V0	1.0	-	-
PCA9460_BUCK3	BUCK3_1V0	1.0/1.1[1]	-	-
PCA9460_BUCK4	BUCK4_1V1	1.1	-	-
PCA9460_LDO1	LDO1_1V1	1.1	-	-
PCA9460_LDO2	LDO2_3V3	3.3	-	-
PCA9460_LDO3	LDO3_3V3	3.3	-	-
PCA9460_LDO4	LDO4_1V8	1.8	-	-
PCA9460_LDO_SNVS	LDO5_3V0	3.0	-	-

1. The default output voltage of the PCA9460A BUCK3 is 1.0 V. The software changes it to 1.1 V in the U-Boot.

4.4 Checking for clock pitfalls

Problems with the external clocks are another board bring-up issue. Ensure that all the clock sources are running as expected.

The 24M_XTALI/24M_XTALO and the RTC clocks are the main clock sources for the 24-MHz and 32.768-kHz reference clocks.

When checking crystal frequencies, using an active probe is recommended to avoid excessive loading. A passive probe might inhibit the 24-MHz oscillators from starting up. Use the following guidelines:

- RTC clock is running at 32.768 kHz.
- 24M_XTALI/24M_XTALO is running at 24 MHz (used for the PLL reference).

4.5 Avoiding reset pitfalls

Follow these guidelines to ensure that you are booting correctly:

- During the initial power-on, while asserting the RESET0_b signal, ensure that the 24-MHz and 32.768-kHz clocks are active before releasing RESET0_b.
- Follow the recommended power-up sequence specified in the i.MX 8ULP data sheet.
- Ensure that the RESET0_b signal remains asserted (low) until all voltage rails associated with the boot-up are ON.

The BT0_CFG[0:15], BT1_CFG[0:15], and BOOT_MODE[0:1] balls and internal fuses control the boot. For a more detailed description of the boot modes, see the system boot chapter in the chip reference manual.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

4.6 Sample board bring-up checklist

The checklist incorporates the recommendations described in the previous sections. Blank cells should be filled in during the bring-up.

Table 29. Board bring-up checklist

Checklist item	Details	Owner	Findings and status
Note: The following items must be completed serially.			
1. Perform a visual inspection.	Check the major components to make sure nothing is misplaced or rotated before powering ON.		
2. Verify all i.MX 8ULP voltage rails.	Confirm that the voltages match the data sheet requirements. Be sure to check the voltages as close to the i.MX 8ULP as possible (like on a bypass capacitor). This reveals any IR drops on the board that could cause issues later. Ideally, all the i.MX 8ULP voltage rails should be checked, but see the guidance below for important rails to check for the i.MX 8ULP.		
	VDD_VBAT42, VDD_VBAT18_CAP, VDD_PMC18, VDDQ_DDR, VDD_DIG0, VDD_DIG1, and VDD_DIG2 are particularly important voltages and they must fall within the parameters provided in the i.MX 8ULP data sheet.		
3. Verify the power-up sequence.	Verify that power-on reset (RESET0_b) is deserted (high) after all power rails have come up and are stable. See the i.MX 8ULP data sheet for details about the power-up sequencing.		
4. Measure/probe the input clocks (32.768-kHz, 24-MHz, and others).	Without proper clocks, the i.MX 8ULP does not function correctly.		
5. Check the JTAG connectivity.	This is one of the most fundamental and basic access points to the i.MX 8ULP to allow the debug and execution of low-level code and probe/access the processor memory.		
Note: The following items may be worked on in parallel with other bring-up tasks.			
Access the internal RAM.	Verify the basic operation of the i.MX 8ULP in the system. Perform a basic test by performing a write-read-verify operation to the internal RAM. No software initialization is required to access the internal RAM.		
Verify the CLK_OUT0/1/2 outputs (measure and verify the default clock frequencies for the desired clock output options) if the board design supports the probing of clock-output balls.	This ensures that the corresponding clock and the PLLs are working. This step requires chip initialization (for example, via the JTAG debugger) to properly set up the IOMUX to output the clocks to the I/O balls and to set up the CGC0/1/2 to output the desired clock. See the chip reference manual for more details.		
Measure the boot mode frequencies. Set the boot configure switch for each boot mode and measure the following (depending on system availability): • SPI-NOR/SPI-NAND (probe the slave selection and measure the clock frequency).	This verifies the connectivity of signals between the i.MX 8ULP and the boot device and that the boot mode signals are set properly. See the “System Boot” chapter in the chip reference manual for details about the boot mode configurations.		

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Table 29. Board bring-up checklist*...continued*

Checklist item	Details	Owner	Findings and status
• eMMC/SD (measure the clock frequency).			
Run the basic DDR initialization and test the memory.	1. Assuming the use of a JTAG debugger, run the DDR initialization and open a debugger memory window pointing to the DDR memory map starting address. You can also do this by the i.MX8ULP DDR Stress Test Tool. 2. Try writing a few words and verify that they can be read correctly. 3. If not, recheck the DDR initialization sequence and whether the DDR has been correctly soldered onto the board. Recheck the schematic to ensure that the DDR memory has been connected to the i.MX 8ULP correctly.		

5 Using BSDL for board-level testing

5.1 BSDL overview

The Boundary Scan Description Language (BSDL) is used for board-level testing after the components are assembled. The interface for this test uses the JTAG pins. The definition is contained within IEEE Std 1149.1.

5.2 How BSDL works

A BSDL file defines the internal scan chain, which is the serial linkage of the IO cells, within a particular device. The scan chain looks like a large shift register, which provides a means to read the logic level applied to a pin or to output a logic state on that pin. Using JTAG commands, the test tool uses the BSDL file to control the scan chain so that device-board connectivity can be tested.

For example, when using an external ROM test interface, the test tool does the following:

1. It outputs a specific set of addresses and controls to the pins connected to the ROM.
2. It performs a read command and scans out the values of the ROM data pins.
3. It compares the values read with the known golden values.

Based on this procedure, the tool determines whether the interface between the two parts is connected properly and does not contain shorts or opens.

5.3 Downloading the BSDL file

The BSDL file for each i.MX processor is stored at the NXP website upon a product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.

5.4 Pin coverage of BSDL

Each pin is defined as a port within the BSDL file. You can open the file with a text editor (such as Wordpad) to review how each pin works. The BSDL file defines the following functions:

- PORT DESCRIPTION TERMS
- in = input only

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

- out = three-state output (0, Z, 1)
- buffer = two-state output (0, 1)
- inout = bidirectional
- linkage = OTHER (vdd, vss, analog)

The appearance of a “linkage” in a pin's file means that the pin cannot be used with a boundary scan. Usually, these are power pins or analog pins that cannot be defined by a digital logic state.

5.5 Boundary scan operation

See the following references for further information:

- The “System JTAG Controller (SJC)” chapter in the chip reference manual for the definitions of the JTAG interface operations.
- The “Fuse map” chapter in the chip reference manual for the fuse map tables.
- *Introduction to Boundary Scan of i.MX8/i.MX8X* (document AN13215)

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

6 Revision history

Table 30 shows the revisions done to this document.

Table 30. Revision history

Revision number	Date	Substantive changes
1	10 August 2023	Initial release

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

7 Legal information

7.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

7.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

7.3 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, μVision, Versatile — are trademarks and/or registered trademarks of Arm Limited (or its subsidiaries or affiliates) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved.

Contents

1 Overview ... 2
1.1 Device supported ... 2
1.2 Essential references ... 2
1.3 Supplementary references ... 2
1.3.1 General information ... 2
1.4 Related documentation ... 3
1.5 Conventions ... 3
1.6 Acronyms and abbreviations ... 3
2 i.MX 8ULP design checklist ... 5
2.1 Design checklist table ... 5
2.2 JTAG signal termination ... 13
2.3 Unused analog interfaces ... 13
3 i.MX 8ULP layout/routing recommendations ... 13
3.1 Introduction ... 13
3.2 Basic design recommendations ... 13
3.2.1 Placing decoupling capacitors ... 13
3.3 Stack-up and manufacturing recommendations ... 14
3.3.1 Stack-up recommendation (i.MX 8ULP) ... 14
3.3.2 Manufacturing recommendation (i.MX 8ULP) ... 14
3.3.3 EVK PCB stack-up (i.MX 8ULP) ... 15
3.4 DDR design recommendations ... 16
3.4.1 DDR connection information ... 16
3.4.2 LPDDR4/LPDDR4x/LPDDR3 design recommendations ... 16
3.4.2.1 i.MX 8ULP LPDDR4/LPDDR4x routing recommendations ... 17
3.4.2.2 LPDDR4/LPDDR4x routing example (i.MX 8ULP) ... 17
3.4.3 i.MX 8ULP LPDDR3 design recommendations ... 19
3.4.3.1 LPDDR3 routing example (i.MX 8ULP) ... 20
3.4.4 i.MX 8ULP DDR SI simulation guide ... 22
3.4.5 i.MX 8ULP DDR package delay ... 23
3.4.6 High-speed routing recommendations ... 25
3.4.7 Reset architecture/routing ... 26
3.5 Trace impedance recommendations ... 26
3.6 Power connectivity/routing ... 26
3.6.1 i.MX 8ULP power distribution block diagram ... 26
3.6.2 Power routing/distribution requirements ... 28
3.7 USB connectivity ... 28
3.8 uSDHC connectivity ... 28
4 Avoiding board bring-up problems ... 29
4.1 Introduction ... 29
4.2 Avoiding power pitfalls — current ... 29
4.3 Avoiding power pitfalls — voltage ... 29
4.4 Checking for clock pitfalls ... 30
4.5 Avoiding reset pitfalls ... 30
4.6 Sample board bring-up checklist ... 31
5 Using BSDL for board-level testing ... 32
5.1 BSDL overview ... 32
5.2 How BSDL works ... 32
5.3 Downloading the BSDL file ... 32
5.4 Pin coverage of BSDL ... 32
5.5 Boundary scan operation ... 33
6 Revision history ... 34
7 Legal information ... 35

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© 2023 NXP B.V. All rights reserved.

For more information, please visit: http://www.nxp.com

Date of release: 10 August 2023