Order this document by
DSP56651ADMUM/D
Rev. 1.1, 10/98

DSP56651ADM User's Manual

Motorola, Incorporated
Semiconductor Products Sector
6501 William Cannon Drive West
Austin TX 78735-8598

MOTOROLA

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Table of Contents

Chapter 1
Quick-Start Guide

Chapter 2
DSP56651ADM Technical Summary

Appendix A
DSP56651ADM Schematics

Appendix B
DSP56651ADM Bill of Materials

List of Tables

List of Figures

Chapter 1
Quick-Start Guide

The DSP56651 applications development module (DSP56651ADM) is designed to operate with the Motorola application development system (ADS). Use the DSP56651ADM with the Motorola ADS to facilitate the development, debugging, and testing of complex software applications and hardware products designed for the DSP56652. Detailed information about the Motorola ADS is provided in the Motorola *Digital Signal Processor Application Development System User's Manual* (order # DSPADSUM/AD).

Section 1.1 "What You Need to Supply for the DSP56651ADM," gives a summary description of the equipment you must supply to use the module.

Section 1.2 "Installation Procedure," describes installation instructions, including the following:

- Preparing the module for installation
- Installing the module
- Installing the software
- Testing the installation

Note: Detailed information about the design and operation of the DSP56651ADM is provided in this manual in Chapter 2 and Appendices A and B.

1.1 What You Need to Supply for the DSP56651ADM

To use the DSP56651ADM with the Motorola ADS (and the ISA interface card), you must supply the following host computer system:

- PC-compatible computer (Pentium–90 MHz) with the following:
  - — Windows95 or NT 4.0
  - — 32 Mbytes RAM
  - — One open 16-bit ISA expansion slot for host card

— One bank of free I/O addresses in the range of $100–$102, $200–202, or $300–$303

— CD-ROM drive

— Hard drive with 50 Mbytes of free disk space

— Mouse

1.2 Installation Procedure

Installation requires four basic steps:

1. Preparing the DSP56651ADM board
2. Installing the module
3. Installing the software
4. Testing the installation

1.2.1 Preparing the DSP56651ADM

Warning

Because all electronic components are sensitive to the effects of electrostatic discharge (ESD) damage, correct procedures should be used when handling all components in this kit and inside the supporting personal computer. Use the following procedures to minimize the likelihood of damage due to ESD.

Always handle all static-sensitive components only in a protected area, preferably a lab with conductive (anti-static) flooring and bench surfaces.

Always use grounded wrist straps when handling sensitive components.

Never remove components from anti-static packaging until required for installation.

Always transport sensitive components in anti-static packaging.

Locate the jumper blocks JP1–JP13 on the DSP56651ADM board, as shown in Figure 1-1. Table 1-1 describes the jumper group settings for use with the Motorola ADS. Read the technical summary in Chapter 2 ”DSP56651ADM Technical Summary” of this manual for additional information about the DSP56651ADM board and its components.

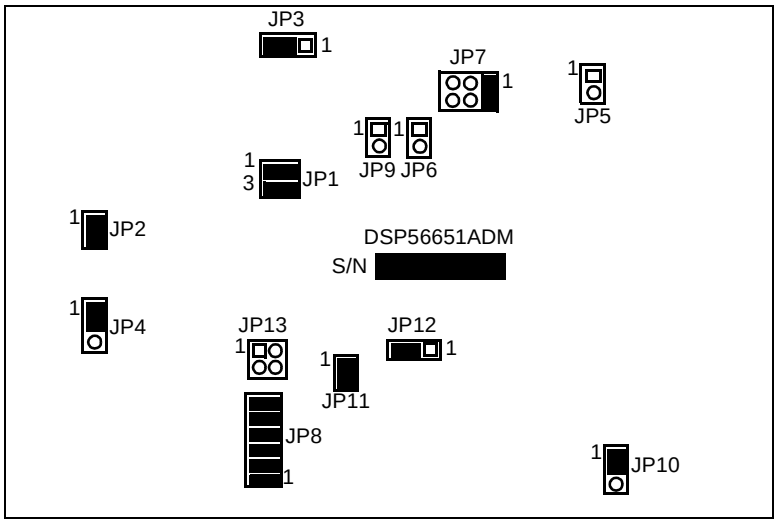

Figure 1-1. DSP56651ADM Jumper Quick Reference

Table 1-1. DSP56651ADM Default Jumper Options

Jumper Group	Comment	Jumper Connections
JP1	Selects $\overline{CS0}$ for emulation SRAM and CS4\ for FLASH	1–2 and 3–4
JP2	Selects $\overline{CS2}$ for FSRAM	1–2
JP3	Selects $\overline{MCU\_DE}$ at TMS1	2–3
JP4	Selects M∗CORE mode high (Boot from internal ROM)	1–2
JP5	Disable factory test mode	NC
JP6	Selects JTAG/OnCE signals on JTAG/OnCE connector	NC
JP7	Selects DSP56651 $\overline{CS3}$ for use by DUART	1–2
JP8	Selects DSP56651 SAP signals for use with MC145483 CODEC	1–2, 3–4, 5–6, 7–8, 9–10 and 11–12
JP9	Enable RS-232 level converter	NC
JP10	Selects +5VDC oscillator power	1–2
JP11	Selects use of on-board RESET logic	1–2
JP12	Selects FSRAM for 16-bit MODE accesses	2–3
JP13	Selects DSP56600 MODE A (Normal MDI boot)	NC

1.2.2 Installing the Module

Figure 1-2 shows the interconnection diagram for connecting the PC to the DSP56651ADM board. Using the instructions in the ADS user's manual, connect the command converter to the DSP56651ADM board. Power for the DSP56651ADM is supplied from an external 7–12 V AC /DC 500 mA power supply with a 2.5–mm female connector. Then connect the DSP Terminal Board to the DSP56651ADM Board via two ribbon cables. The 5-pin ribbon cable connects to the DSP Terminal's P1 connector and the DSP56651ADM's P6 connector. The18 pin ribbon cable connects to the DSP Terminal's P2 connector and the DSP56651ADM's P10 connector.

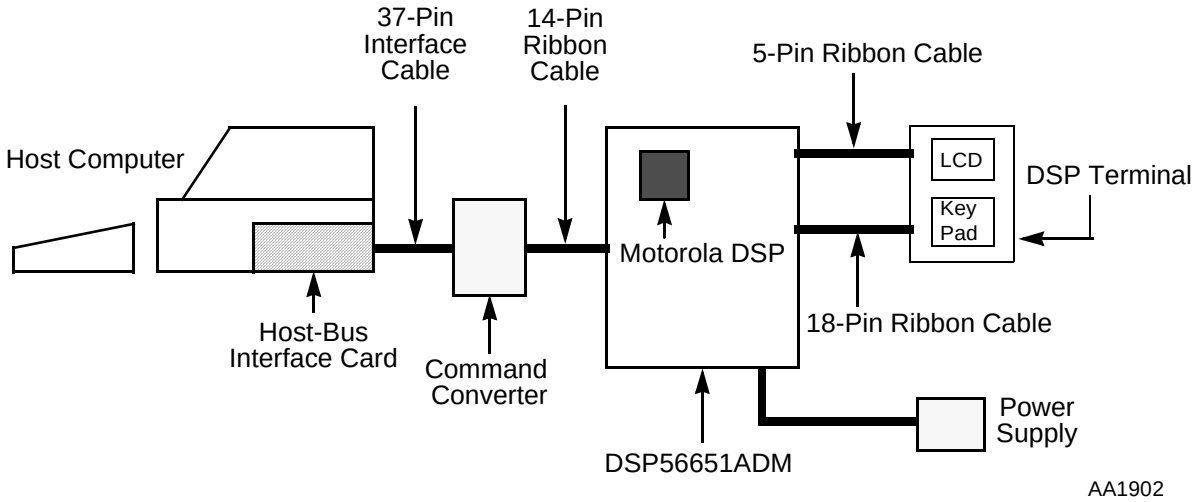

Figure 1-2. Application Development

1.2.3 Installing the Software

Refer to the Motorola *Digital Signal Processor Application Development System User's Manual* for detailed instructions about installation and use of the ADS software.

Refer to the *SDS User's Manual* for detailed Motorola information about installing the Single Step software.

Refer to the *DIAB User's Manual* for detailed information about installing the DIAB C Compiler software.

1.2.4 Testing the DSP56651ADM Installation

Refer to the Motorola *Digital Signal Processor Application Development System User's Manual* for detailed information regarding evaluation and testing of an installed ADS system.

Refer to the *SDS User's Manual* for detailed Motorola information regarding evaluation and testing of the Single Step software.

Refer to the *DIAB User's Manual* for detailed information regarding evaluation and testing of the DIAB C Compiler software.

Chapter 2
DSP56651ADM Technical Summary

The DSP56651ADM is designed as a versatile digital signal processor (DSP) development card that can be used with the Motorola ADS and can also be plugged into other cards to permit special user configurations. DSP56651 peripheral port connectors are located around the perimeter of the printed circuit board (PCB), allowing easy user access to all the DSP56651 signals, including V_{CC} (3.3 V), V_{CCQ} (2.4 V), and V_{SS} (GND). An overview description of the DSP56651ADM is also provided in the *DSP56651ADM Product Information (DSP56651ADMP/D)* included with this kit. The main features of the DSP56651ADM include the following:

- DSP56651 dual-core processor
  - — 32-bit RISC M•CORE
  - — 24/16-bit DSP56600 DSP
- External fast static RAM (FSRAM) memory
  - — 128K × 16-bit memory
  - — or 128K × 8-bit upper/lower byte memory
- 512K × 16-bit external FLASH memory
- 1 M x 16-bit FLASH emulation SRAM
- 13-bit linear CODEC with voice input and output jacks
- Socketed on-board 16.8 MHz oscillator for DSP56651 system clock
- Manual reset button S1
- Light emitting diode (LED) power indicator (LED1)
- Three LEDs for user DSP56600 debug operations (LED2–4)
- Three LEDs for user M•CORE debug operations (LED5–7)
- Five 20-pin logic analyzer connectors
- Buffered 50-pin external interface memory (EIM) connector
- Joint Test Action Group (JTAG) port connector for Motorola’s ADS that provides an enhanced development environment, including a high-speed data transfer port to a host PC ISA bus.

2.1 DSP56651

The DSP56651 is an emulation part, installed on the DSP56651ADM. Mounted in a 17 x 17, 1-mm pitch PBGA package, the DSP56651 is soldered on the component side of the DSP56651ADM board. The signals going to and from the DSP56651 part are used by the on-board memory/peripherals and routed to connectors to be used by off-board memory/peripherals. Two address/data buses are provided on the DSP56651ADM board: a high-speed address/data bus, connected directly to the DSP56651 part for memory interfacing and a buffered address/data bus, used by slower memory, peripherals, and external memory/peripheral interfaces. The buffering is provided to reduce the capacitive loading on DSP56651 address and data bus signals.

A full description of the DSP56651, including functionality and user information, is provided in the following documents included as a part of this kit (either as printed copies or on the documentation CD-ROM):

- *DSP56651 Technical Data* (DSP56651/D)–provides features list and specifications including signal descriptions, DC power requirements, AC timing requirements, and available packaging.
- *DSP56652 User's Manual* (DSP56652UM/AD)–provides detailed information about the on-chip components including the memory and I/O maps, peripheral functionality, and control and status register descriptions for each subsystem of the DSP56652, much of which is common to the DSP56651.
- *DSP56600 Family Manual* (DSP56600FM/AD)–provides a detailed description of the core processor, including internal status and control registers and a detailed description of the family instruction set.

Refer to these documents for detailed information about chip functionality and operation.

2.2 Memory

The DSP56651ADM uses the following external memory:

- Fast SRAM for external program/data memory, selectable as the following:
  - — 128K × 16-bit 12 nS memory, or
  - — 128K × 8-bit 12 nS memory in the upper or lower byte
- Fast FLASH and FLASH emulation memory for external program/data
  - — 512 K × 16-bit 90 nS FLASH memory
  - — 1 M × 16-bit 12 nS SRAM memory

Figure 2-1 DSP56651ADM Functional Block Diagram shows a functional block diagram of the DSP56651ADM including the memory devices.

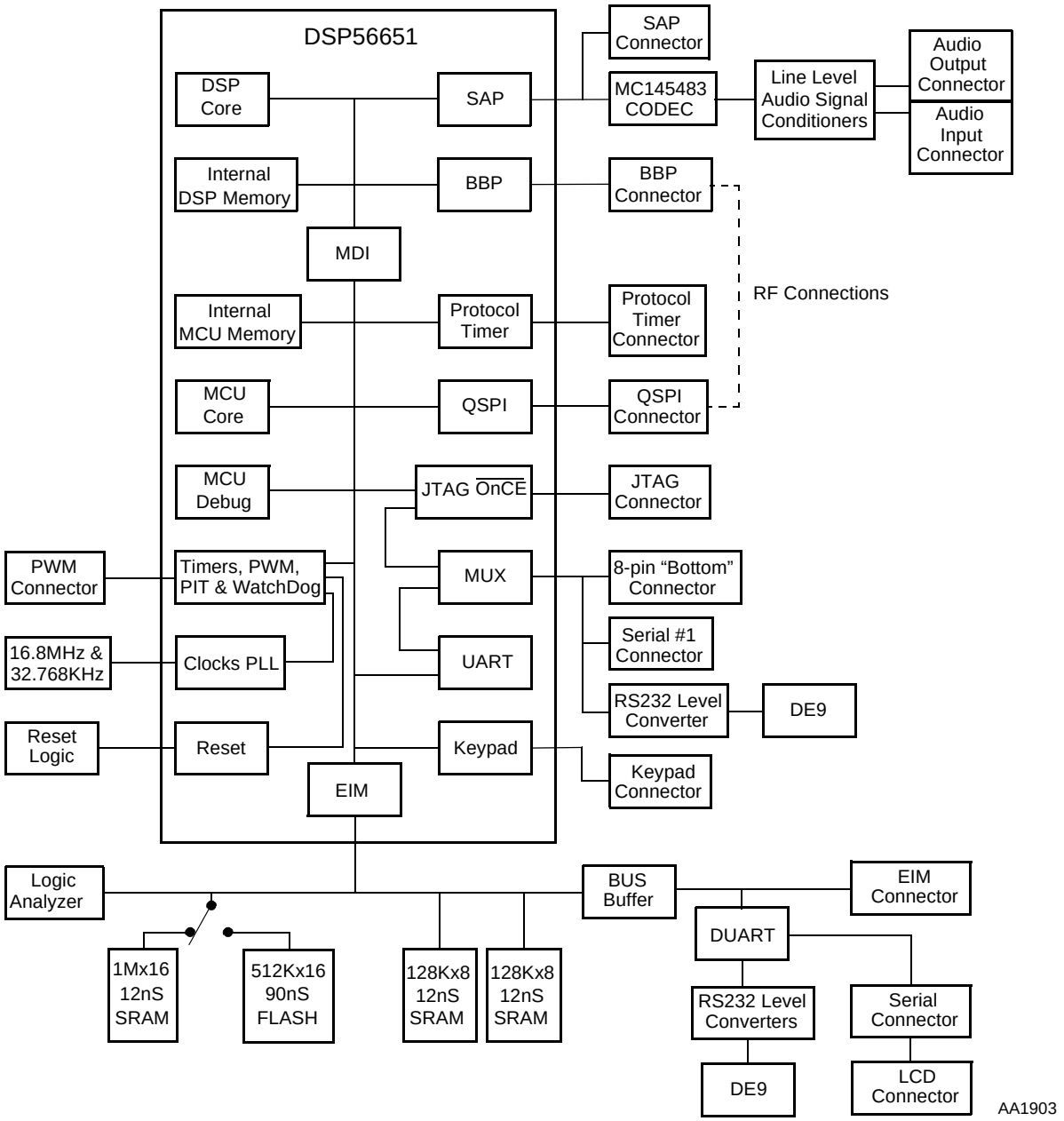

Figure 2-1. DSP56651ADM Functional Block Diagram

Table 2-1., "DSP56651ADM Chip Select," identifies which chip selects are associated with the external memories and peripherals along with the setting used by the CS control registers.

Table 2-1. DSP56651ADM Chip Select

Chip Select	Memory/Peripheral	CS Control Register
$\overline{CS0}$	FLASH	$F821
$\overline{CS0}$	SRAM	$1861
$\overline{CS1}$	Unused	—
$\overline{CS2}$	FSRAM	$0061
$\overline{CS3}$	DUART	$4CD1
$\overline{CS4}$	FLASH	$1861
$\overline{CS4}$	SRAM	$0061
CS5	Unused	—

2.2.1 Fast Static RAM (FSRAM) Memory Bank

The fast SRAM memory bank, 128K x 16-bit 12 nS or 128K x 8-bit 12 nS upper/lower byte, is connected to the DSP56651's $\overline{CS2}$. (See Figure 2-2 FSRAM Functional Block Diagram.) This memory bank uses two 128K × 8-bit 12 nS fast static RAMs, Motorola MCM6926A, labelled U7 and U8. U7 provides the low byte of memory, while U8 provides the high byte of memory. The on-board jumpers, JP2 and JP12, allow the operation and configuration of the FSRAM respectively. The on-board jumper JP2 allows $\overline{CS2}$ to enable the use of the on-board FSRAM. These memory chips can be configured to use the DSP56651's EIM 16-bit or 8-bit addressing mode. JP12 selects between the 16-bit or 8-bit FSRAM memory configurations. Refer to Table 2-2 and Table 2-3 for setting these jumpers.

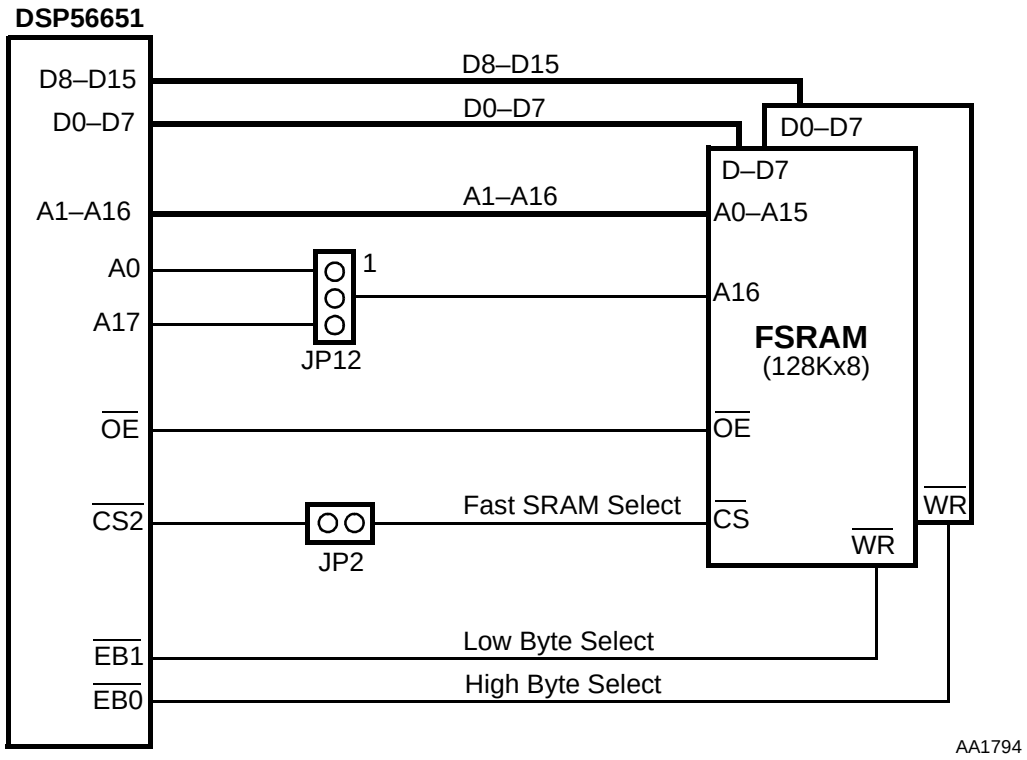

Figure 2-2. FSRAM Functional Block Diagram

Table 2-2. Fast SRAM Jumper Options

JP2	Options Selected
1–2	$\overline{CS2}$ used by 128K x 16-bit fast SRAM
OPEN	$\overline{CS2}$ available for use by off-board memory

Table 2-3. 8-Bit/16-Bit Memory Jumper Options

JP12	Options Selected	CS2 Control Register Value
1–2	Upper 8-bit memory operation	$0041
1–2	Lower 8-bit memory operation	$0051
2–3	16-bit memory operation	$0061

2.2.2 FLASH Memory Bank

The FLASH memory bank, 512K x 16-bits at 90 nS, is controlled by the DSP56651's $\overline{CS0}$ and $\overline{CS4}$ signals. (See Figure 2-3 FLASH/Emulation SRAM Functional Block Diagram.) This allows application code to be stored along with power-on boot code for use after a system reset. Because of the long program cycle time required to program the FLASH, programming the code into the FLASH during the code development and debug phases is not preferred. Therefore, a bank of SRAM, 1 M x 16-bits at 12 nS, is provided to allow for faster download/debug cycles. Through jumper JP1, the emulation SRAM and/or the FLASH can use the $\overline{CS0}$ and $\overline{CS4}$ signals. (See Table 2-4.) This allows both FLASH and emulation SRAM memory banks to be active at one time. Data/programs stored in SRAM can also be easily transferred to FLASH.

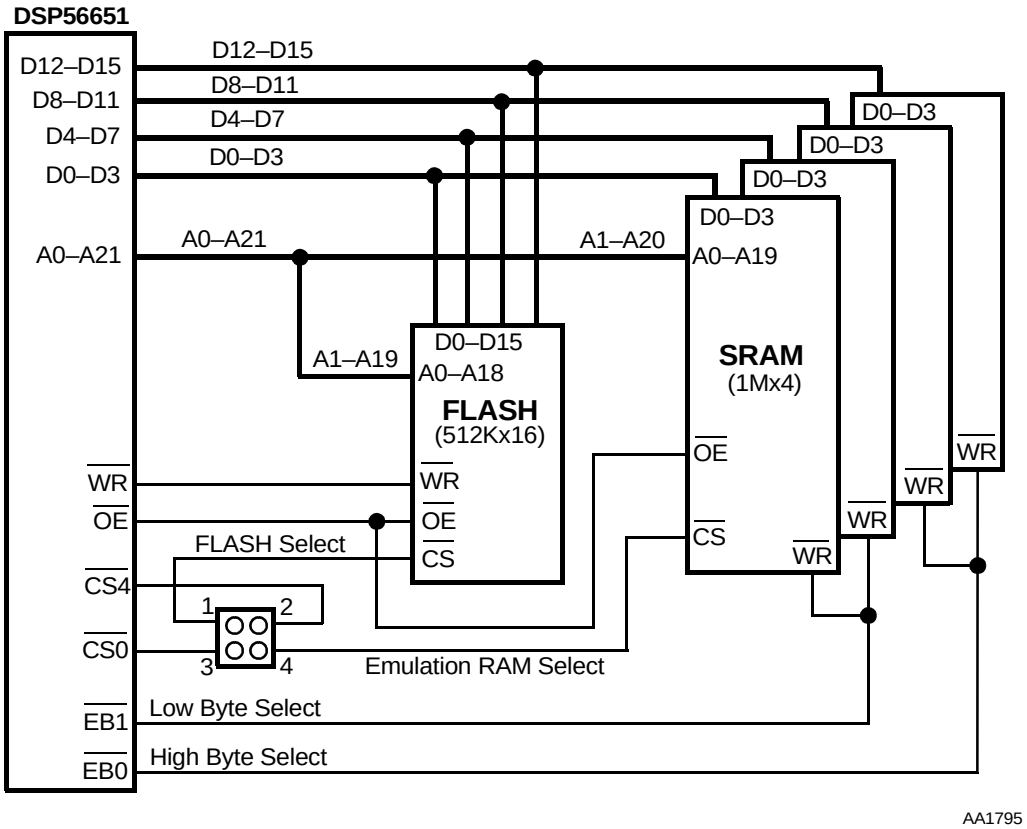

Figure 2-3. FLASH/Emulation SRAM Functional Block Diagram

Table 2-4. FLASH Jumper Options

JP1	FLASH Memory Banks Selections	CS0 Control Register Value	CS4 Control Register Value
1–3	FLASH @ $\overline{CS0}$, $\overline{CS4}$ available for use by off-board memory	$F821	—
3–4	SRAM @ $\overline{CS0}$, $\overline{CS4}$ available for use by off-board memory	$F861	—
1–2	FLASH @ $\overline{CS4}$, $\overline{CS0}$ available for use by off-board memory	—	$1861
2–4	SRAM @ $\overline{CS4}$, $\overline{CS0}$ available for use by off-board memory	—	$0061
1–3 & 2–4	FLASH @$\overline{CS0}$ and SRAM @ $\overline{CS4}$	$F821	$0061
1–2 & 3–4	FLASH @ $\overline{CS4}$ and SRAM @ $\overline{CS0}$	$F861	$1861

2.3 Voice Codec

The DSP56651ADM's analog section uses Motorola's MC145483 13-bit linear CODEC (installed at U15). Refer to the data sheet included with this kit for more information on the MC145483. The DSP56651ADM uses 1/8-inch jacks for the CODEC's line level input and output signals. The CODEC interfaces to the DSP via the DSP56651's serial audio port (SAP). (See Figure 2-4 Voice CODEC Functional Block Diagram and Table 2-5.) No glue logic is required. The codec clock and frame synchronization are provided by the SAP. Jumper JP8 allows the user to disconnect the on-board CODEC from the SAP port to allow users to connect their own CODEC to the DSP's SAP port.

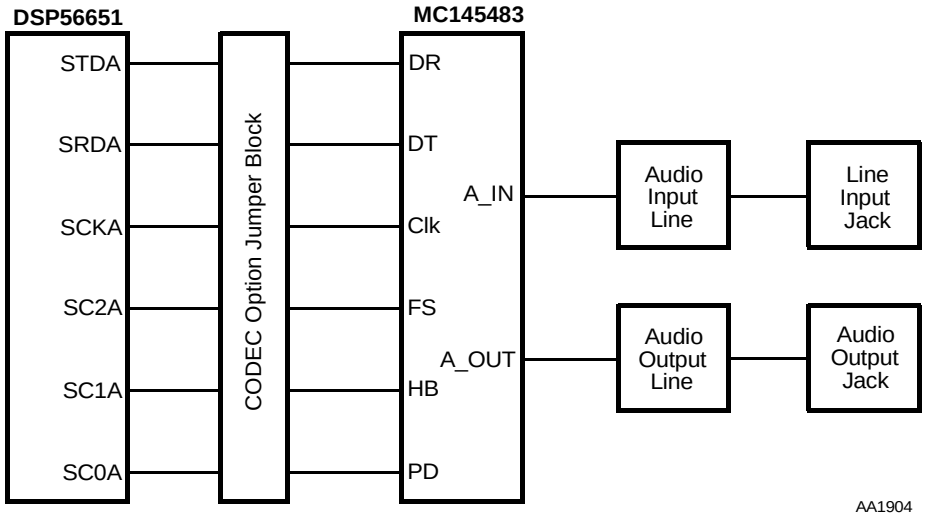

Figure 2-4. Voice CODEC Functional Block Diagram

Table 2-5. Voice CODEC Jumper Options

JP8	Voice CODEC Enabled	External User CODEC Enabled	DSP Signal Name
1–2	Jump	OPEN	SRDA
3–4	Jump	OPEN	STDA
5–6	Jump	OPEN	SCKA
7–8	Jump	OPEN	SC0A
9–10	Jump	OPEN	SC1A
11–12	Jump	OPEN	SC2A

2.3.1 Codec Jacks

P7 and P8 are stereo jacks that allow the user to send and receive analog signals to and from the on-board codec. P7 allows the user to apply an input signal to the on-board CODEC. The pinout of this connector is listed in Table 2-6.

Table 2-6. DSP56651ADM P7 Line-In Description

Connector	Signal
Barrel	ANALOG GND
Tip	LINE-IN
Ring	LINE-IN (optional)

P8 allows the user to send an output signal from the on board CODEC. The pinout of this connector is listed in Table 2-7.

Table 2-7. DSP56651ADM P8 Line-Out Description

Connector	Signal
Barrel	ANALOG GND
Tip	LINE-OUT
Ring	LINE-OUT (optional)

Note: P7 and P8 are stereo jacks. However, only mono audio capability is provided by the MC145483 Codec.

2.4 Debug Ports

The DSP56651ADM board provides the needed debug services required for efficient software and debugging via the OnCE port, bottom connector, on-board UART, and logic analyzer interface connections.

2.4.1 Boot Mode Selection

The DSP56651ADM provides two jumpers to select which mode to start the DSP56651 in after RESET, as shown in Table 2-8 and Table 2-9.

Table 2-8. M•CORE Boot MODE Jumper Options

JP4	Options Selected
1–2	Boot from internal ROM
2–3	Boot from FLASH memory bank

Table 2-9. DSP56600 Boot MODE Jumper Options

JP13	Options Selected
OPEN	MODE A: normal MDI boot
1–2	MODE B: MDI shared memory boot
3–4	MODE C: MDI messaging unit boot
1–2 & 3–4	MODE D: reserved

2.4.2 JTAG/OnCE

The DSP56651ADM provides a 14-pin JTAG/OnCE debug connector, which allows its use with existing 3.3 V command converter boards. See Figure 2-5 JTAG/OnCE Functional Block Diagram and Table 2-11.

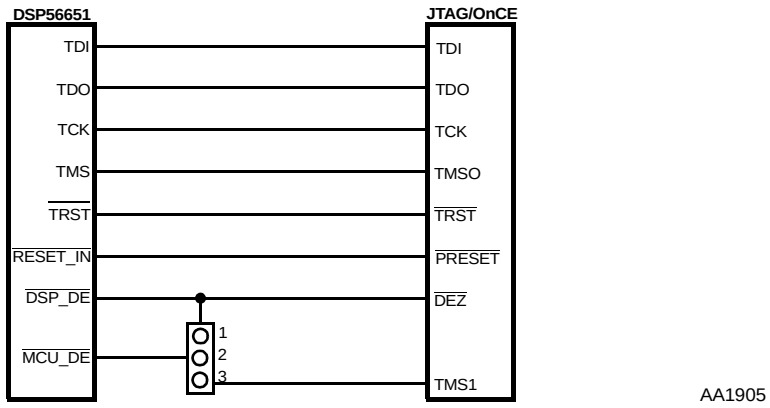

Figure 2-5. JTAG/OnCE Functional Block Diagram

As shown in Table 2-10, there are two jumper options for debug break control. One option allows the DSP or the MCU to cause the other processor to break. The other option allows the $\overline{\text{DSP\_DE}}$ signal to be routed to the OnCE $\overline{\text{DEZ}}$ signal, while the $\overline{\text{MCU\_DE}}$ signal can be routed to TMS1.

Table 2-10. JTAG/OnCE Jumper Options

JP3	Options Selected
1–2	MCU and DSP generate DEBUG breaks to each other
2–3	$\overline{\text{MCU\_DE}}$ used for TMS1
OPEN	$\overline{\text{DSP\_DE}}$ used for $\overline{\text{DEZ}}$ and TMS1 unused

Table 2-11. JTAG/OnCE Connector (P2) Pinout

Pin Number	Signal Name	Pin Number	Signal Name
1	TDI	2	GND
3	TDO	4	GND
5	TCK	6	GND
7	n/c	8	key pin
9	PRESET	10	TMS0
11	+3.3 V	12	TMS1
13	$\overline{\text{DEZ}}$	14	TRST

2.4.3 Bottom Connector

The DSP56651ADM provides a 14-pin “bottom” debug connector, which emulates the cellular phone handset’s bottom connector. (See Figure 2-6 Bottom Debug Connector Functional Block Diagram.) This connector provides one signal line for mux control. A jumper allows this mux control signal to be manually selected as a high or low signal. Also, provisions are provided that allow the external handset emulation board to override this manual selection. (See Table 2-12 and Table 2-13.)

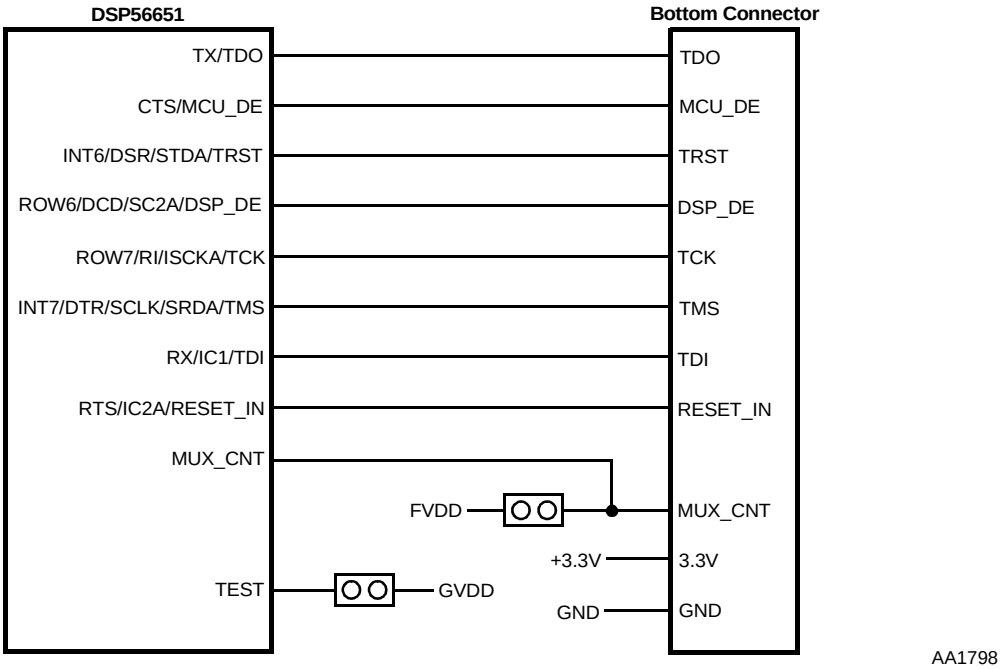

Figure 2-6. Bottom Debug Connector Functional Block Diagram

Table 2-12. MUX_CNT Jumper Options

JP6	Options Selected
1–2	Select JTAG/OnCE signals on bottom connector
OPEN	Select JTAG/OnCE signals on JTAG/OnCE connector

Table 2-13. Bottom Connector (P3) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	TDI	2	GND
3	TDO	4	GND
5	TCK	6	GND
7	n/c	8	MUX_CTL
9	Reset_In	10	TMS
11	+3.3 V	12	MCU_DE
13	DE	14	TRST

2.4.4 On-Board DUART

The DSP56651ADM buffers the signals from the on-board Dual UART, National's PC16552, to provide RS-232 level-compatible signals. These signals are connected to a 9-pin subminiature D-type connector. (See Figure 2-7 On-Board DUART Functional Block Diagram and Table 2-14.)

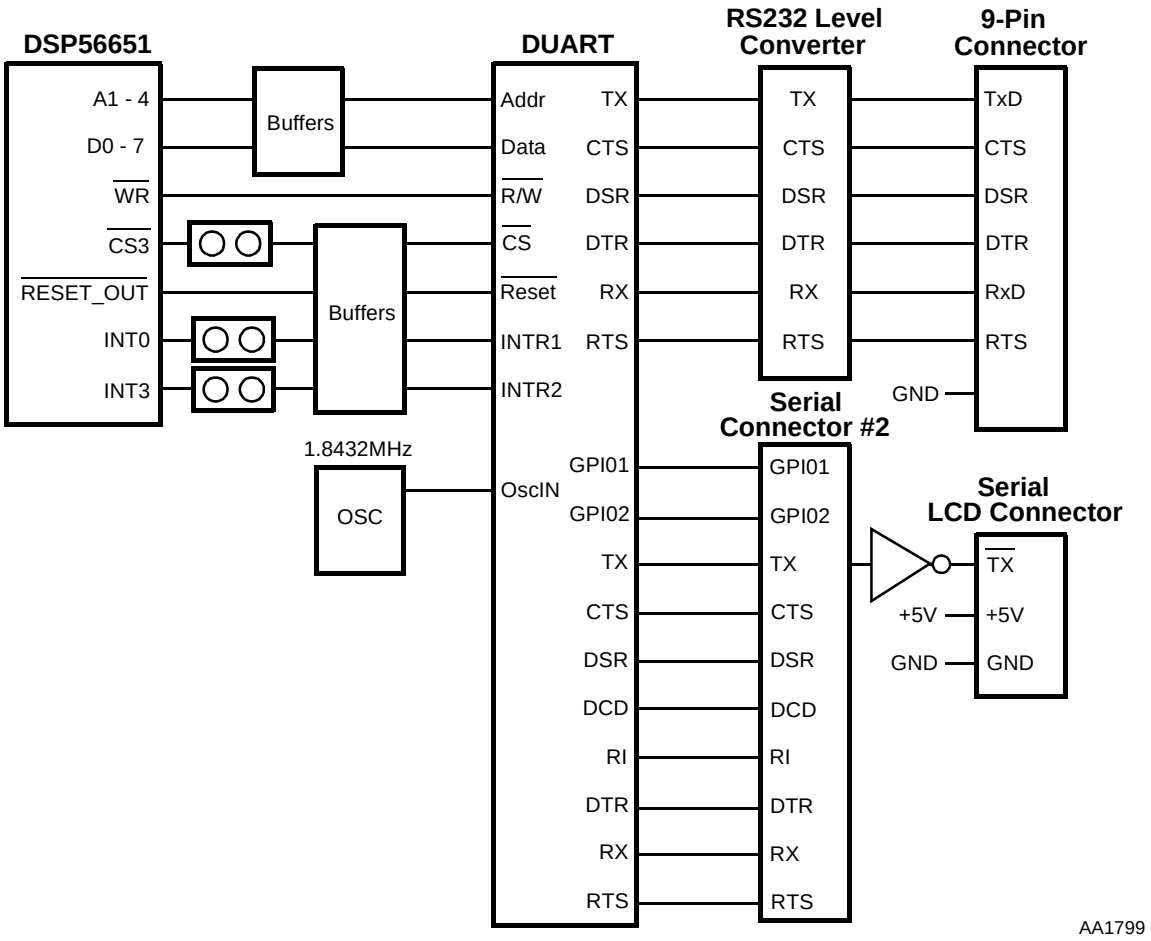

Figure 2-7. On-Board DUART Functional Block Diagram

Table 2-14 On-Board DUART Jumper Options

JP7	Options Selected	CS3 Control Register Value
1–2	Use $\overline{CS3}$ to select DUART	$4CD1
3-4	DUART INTR1 driving INT0	$4CD1
5-6	DUART INTR2 driving INT3	$4CD1

The RS-232 9-pin connector pin assignments are listed in Table 2-15.

Table 2-15. RS-232 Connector (P4) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	DCD	6	DTR
2	TxD	7	CTS
3	RxD	8	RTS
4	DSR	9	—
5	GND	—	—

The secondary UART port signal connector pin assignments are listed in Table 2-16.

Table 2-16. Secondary UART Port Connector (P5) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	GPIO1	2	GPIO2
3	TxD	4	RxD
5	RI	6	DCD
7	DTR	8	DSR
9	RTS	10	CTS

The serial LCD port signal connector pin assignments are listed in Table 2-17.

Table 2-17. Serial LCD Port Connector (P6) Pin Assignments

Pin Number	Signal Name
1	GND
2	+5 V
3	TxD
4	+5 V
5	GND

2.4.5 Logic Analyzer Interface

As shown in Figure 2-8 Logic Analyzer Interface Functional Block Diagram, the DSP56651ADM provides an interface connection for use with a logic analyzer.

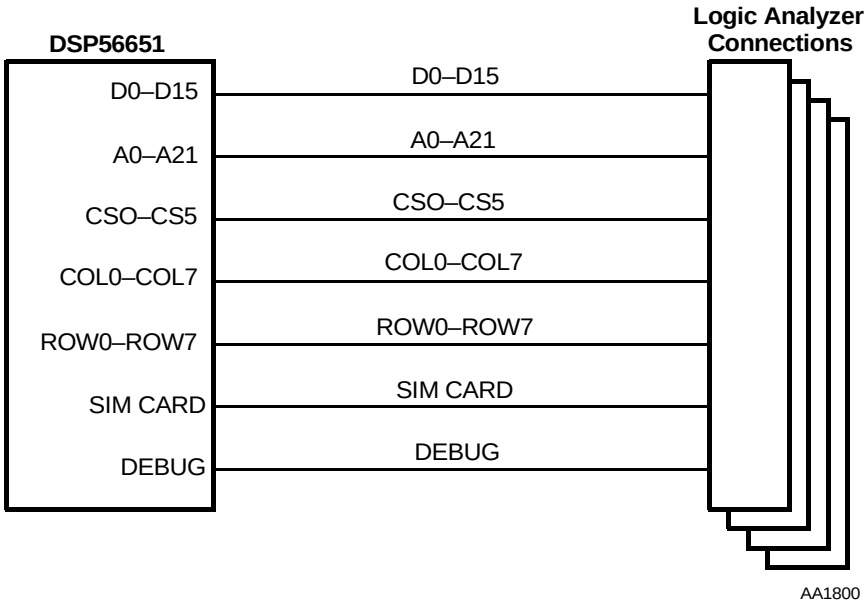

Figure 2-8. Logic Analyzer Interface Functional Block Diagram

An HP Logic analyzer probe interface is implemented. This interface uses five 20-pin 0.1 inch dual-inline headers, with pinouts specified in Table 2-18 through Table 2-22.

Table 2-18. Logic Analyzer Header #1 (P22) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	n/c	2	n/c
3	$\overline{WR}$	4	A15
5	A14	6	A13
7	A12	8	A11
9	A10	10	A9
11	A8	12	A7
13	A6	14	A5
15	A4	16	A3
17	A2	18	A1
19	A0	20	GND

Table 2-19. Logic Analyzer Header #2 (P20) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	n/c	2	n/c
3	CKOH	4	D15
5	D14	6	D13
7	D12	8	D11
9	D10	10	D9
11	D8	12	D7
13	D6	14	D5
15	D4	16	D3
17	D2	18	D1
19	D0	20	GND

Table 2-20. Logic Analyzer Header #3 (P24) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	n/c	2	n/c
3	CKO	4	CKO
5	RESET_IN	6	RESET_OUT
7	INT4	8	INT5
9	INT2	10	INT3
11	INT0	12	INT1
13	Spare	14	A21
15	A20	16	A19
17	A18	18	A17
19	A16	20	GND

Table 2-21. Logic Analyzer Header #4 (P21) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	n/c	2	n/c
3	CKO	4	CS5
5	CS4	6	CS3
7	CS2	8	CS1
9	CS0	10	OE
11	EB1	12	EB0
13	WR	14	SIZ1
15	SIZ0	16	PSTAT3
17	PSTAT2	18	PSTAT1
19	PSTAT0	20	GND

Table 2-22. Logic Analyzer Header #5 (P23) Pin Assignments

Pin Number	Logical Signal	Signal Name	Pin Number	Logical Signal	Signal Name
1	n/c	n/c	2	n/c	n/c
3	DSP_AT	MOD	4	DSP_ADDR15	PWR_EN
5	DSP_ADDR14	SIMRESET	6	DSP_ADDR13	SIMDATA
7	DSP_ADDR12	SENSE	8	DSP_ADDR11	SIMCLK
9	DSP_ADDR10	ROW4	10	DSP_ADDR9	ROW3
11	DSP_ADDR8	ROW2	12	DSP_ADDR7	ROW1
13	DSP_ADDR6	ROW0	14	DSP_ADDR5	COL5
15	DSP_ADDR4	COL4	16	DSP_ADDR3	COL3
17	DSP_ADDR2	COL2	18	DSP_ADDR1	COL1
19	DSP_ADDR0	COL0	20	GND	GND

2.4.6 DSP56651 UART

The DSP56651ADM buffers the signals from the DSP56651's UART port to provide RS-232 level-compatible signals. These signals are connected to a 9-pin subminiature D-type connector. (See Figure 2-9 DSP56651 UART Functional Block Diagram and Table 2-23.)

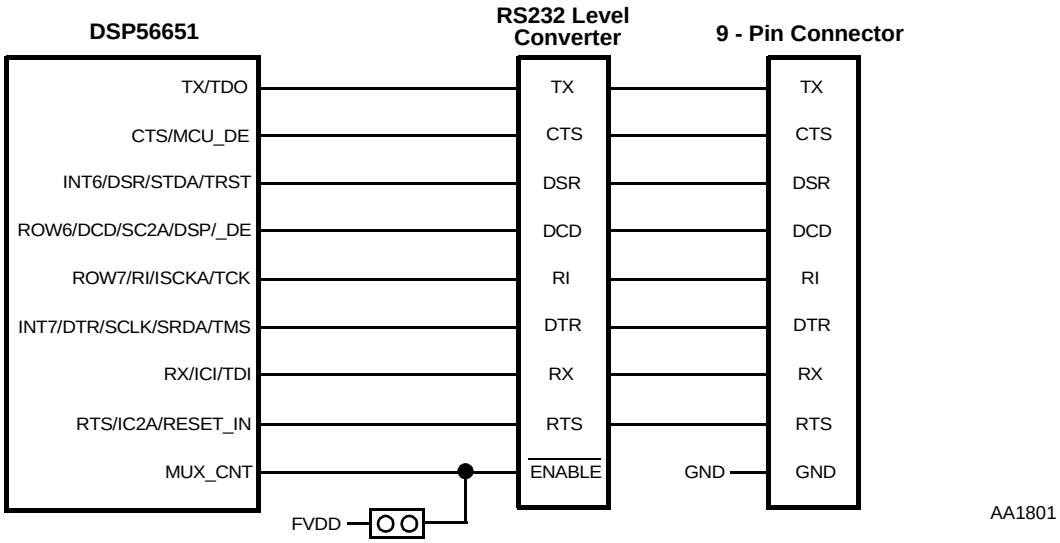

Figure 2-9. DSP56651 UART Functional Block Diagram

Table 2-23. DSP56651 UART Jumper Options

JP6	Options Selected
1–2	Disable DSP56651 UART operation
OPEN	Enable DSP56651 UART operation

The RS-232 9-pin connector pin assignments are listed in Table 2-24.

Table 2-24. RS-232 Connector (P19) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	DCD	6	DSR
2	TxD	7	RTS
3	RxD	8	CTS
4	DTR	9	RI
5	GND		

2.5 Power Supply

The DSP56651ADM is powered by an external 7–12 V AC/DC 500 mA power source through a two pin power connector. The power supply rectifies and regulates this input-supply voltage down to the DSP56651ADM board's specific supply voltages, (i.e. +5.0 VDC, +3.3 VDC and +2.4 VDC). (See Figure 2-10 Power Supply Functional Block Diagram for a functional block diagram and Table 2-25 for pin assignments.)

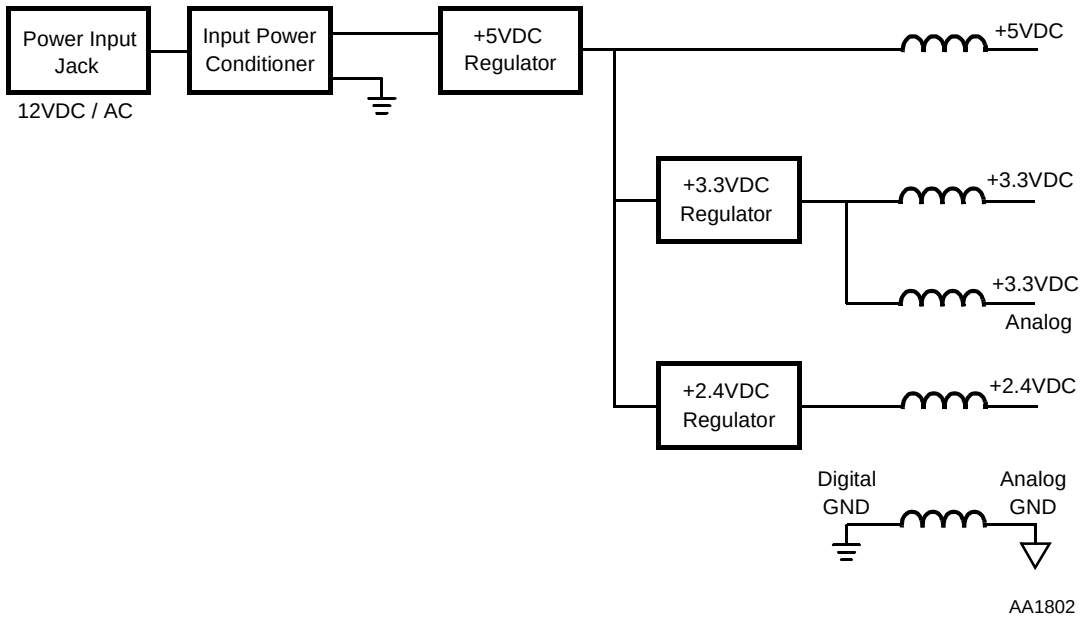

Figure 2-10. Power Supply Functional Block Diagram

Table 2-25. Input Power Pin Assignments

Pin	Signal Name
Inner Conductor	**+12 VDC/AC**
Outer Conductor	**GND**

2.6 Clock Sources

The DSP56651ADM provides two clock sources for the DSP56651, 16.8 MHz and 32.768 KHz. The 16.8 MHz oscillator is socketed to allow for easy frequency changes described and detailed in Figure 2-11 Clock Source Functional Block Diagram, Table 2-26, and Table 2-27. Provisions are provided via the oscillator jumper J10 to allow a user to use a +5 V or +3.3 V oscillator.

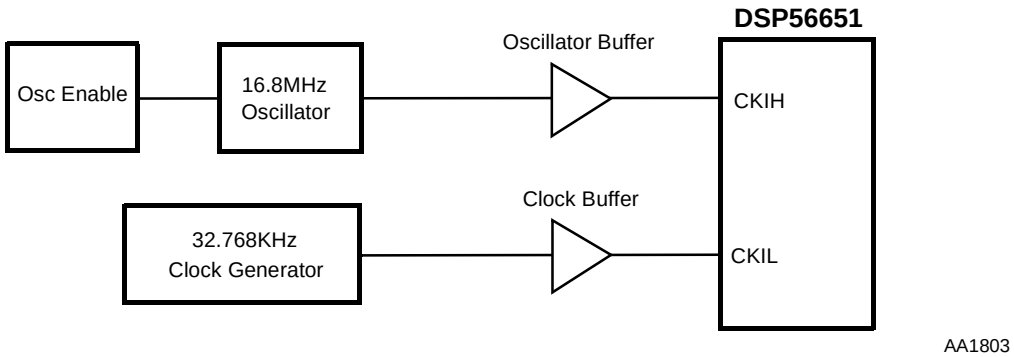

Figure 2-11. Clock Source Functional Block Diagram

Table 2-26. Oscillator Enable Jumper Options

JP10	Options Selected
1–2	Select +5 V Power for the Oscillator
2–3	Select +3.3 V Power for the Oscillator
OPEN	Oscillator Disabled

Table 2-27. Clocks, Resets & Power Connector (P11) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	CKIH	2	GND
3	CKOH	4	GND
5	CKIL	6	GND
7	CKO	8	GND
9	+3.3 V	10	STO
11	+5 V	12	+2.4 V
13	RESET_OUT	14	RESET_IN
15	EXTRST	16	DSP_IRQ

2.7 External Interface Memory

The DSP56651ADM provides an interface connection for use with external interface memory (EIM), (SRAM, FLASH, etc.) and/or peripherals (CODEC, LCD, etc.). This allows external hardware to be used in making a full-featured development environment. (Refer to Figure 2-12 External Memory Interface Functional Block Diagram for a functional block diagram and Table 2-28 for pin assignments.)

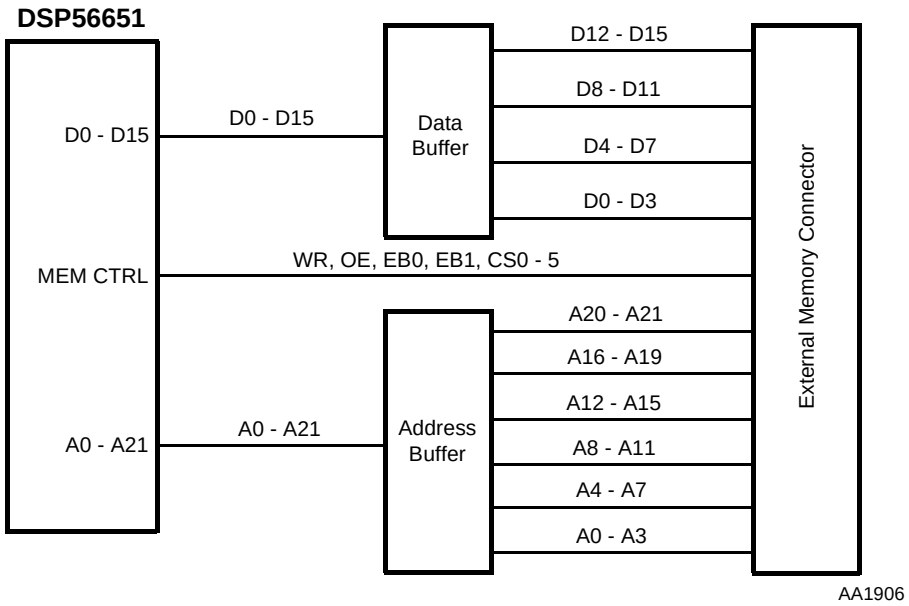

Figure 2-12. External Memory Interface Functional Block Diagram

Table 2-28. EIM (P9) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	D0	2	D1
3	D2	4	D3
5	D4	6	D5
7	D6	8	D7
9	D8	10	D9
11	D10	12	D11
13	D12	14	D13
15	D14	16	D15

Table 2-28. EIM (P9) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
17	A0	18	A1
19	A2	20	A3
21	A4	22	A5
23	A6	24	A7
25	A8	26	A9
27	A10	28	A11
29	A12	30	A13
31	A14	32	A15
33	A16	34	A17
35	A18	36	A19
37	A20	38	A21
39	CS0\	40	CS1\
41	CS2\	42	CS3\
43	CS4\	44	CS5
45	EB0\	46	EB1\
47	WR\	48	OE\
49	+5 V	50	GND

2.8 Keypad

The DSP56651ADM provides an interface connection for use with a keypad, diagrammed in Figure 2-13 Keypad Functional Block Diagram and Table 2-29.

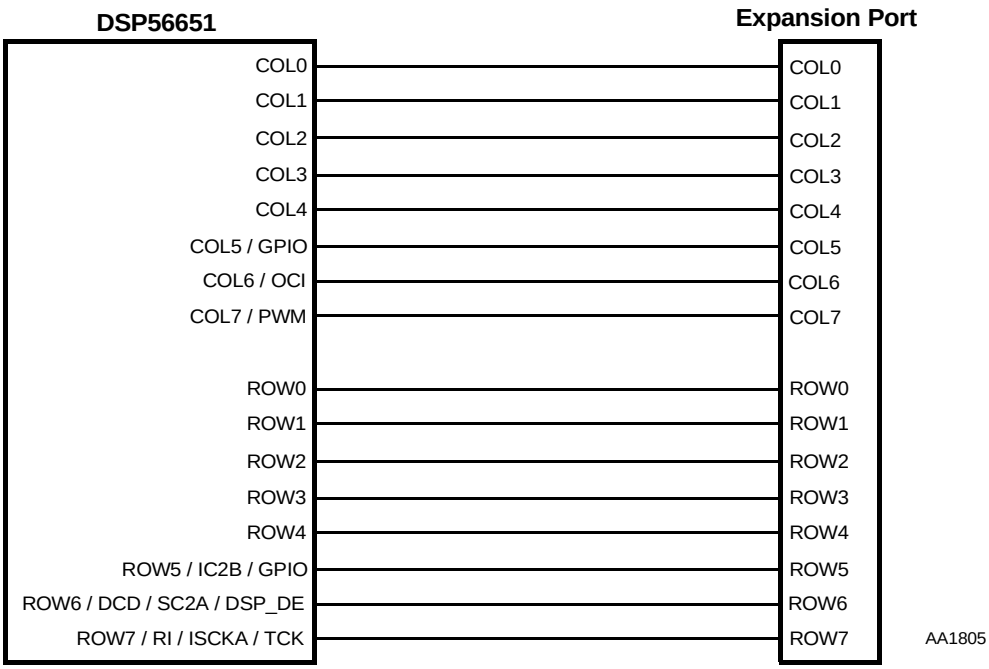

Figure 2-13. Keypad Functional Block Diagram

Table 2-29. Keypad Connector (P10) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	COL0	2	COL1
3	COL2	4	COL3
5	COL4	6	COL5
7	COL6	8	COL7
9	ROW0	10	ROW1
11	ROW2	12	ROW3
13	ROW4	14	ROW5
15	ROW6	16	ROW7
17	+3.3 V	18	GND

2.9 Baseband CODEC Serial Port Interface (BBP)

The DSP56651ADM provides an interface connection for use with an external baseband CODEC. Refer to Figure 2-14 BBP Functional Block Diagram for a functional block diagram and Table 2-30 for pin assignments.

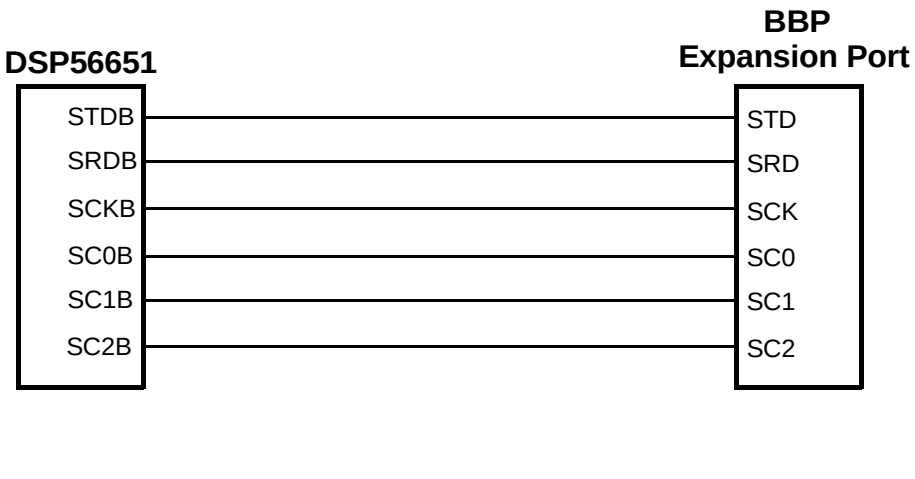

Figure 2-14. BBP Functional Block Diagram

Table 2-30. BBP Connector (P13) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	STD	2	SRD
3	SCK	4	SC0
5	SC1	6	SC2
7	RESET_OUT	8	+5 V
9	+3.3 VA	10	GND

2.10 Audio CODEC Serial Port Interface (SAP)

The DSP56651ADM provides an interface connection for use with an external audio CODEC. Refer to Figure 2-15 SAP Functional Block Diagram for functional block diagram and Table 2-31 for pin assignments.

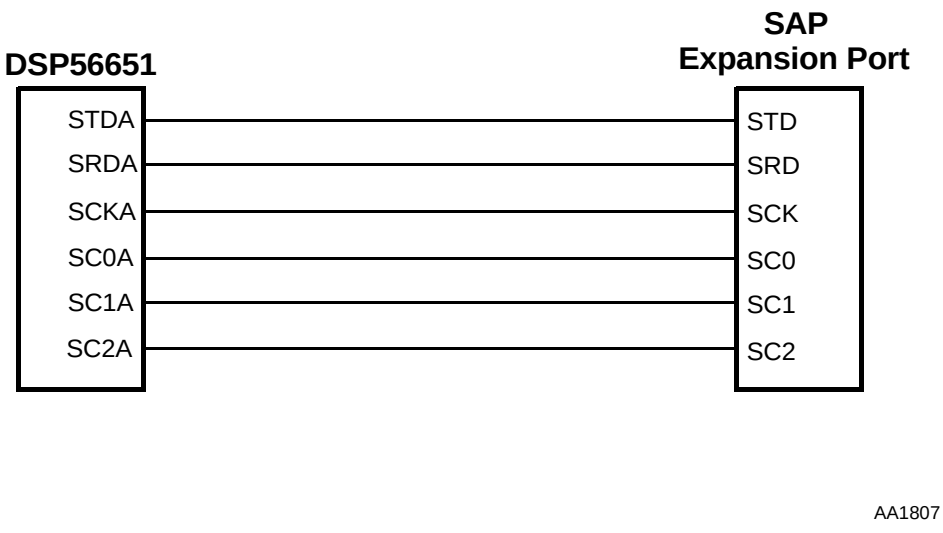

Figure 2-15. SAP Functional Block Diagram

Table 2-31. SAP Connector (P16) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	STD	2	SRD
3	SCK	4	SC0
5	SC1	6	SC2
7	RESET_OUT	8	+5 V
9	+3.3 VA	10	GND

2.11 Queued Serial Peripheral Interface (QSPI)

The DSP56651ADM provides an interface connection for use with an external SPI device. Refer to Figure 2-16 QSPI Functional Block Diagram for functional block diagram and Table 2-32 for pin assignments.

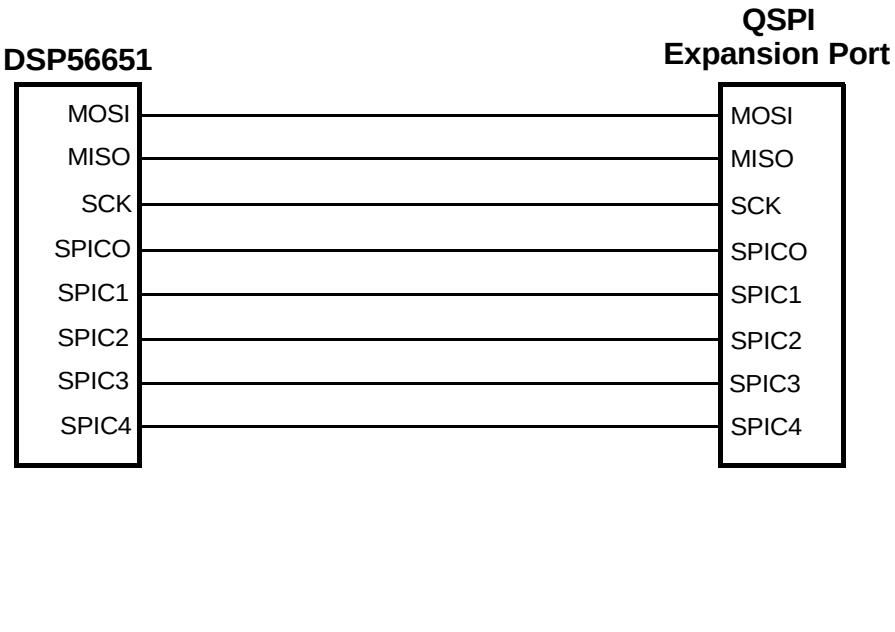

Figure 2-16. QSPI Functional Block Diagram

Table 2-32. QSPI Connector (P12) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	MISO	2	MOSI
3	SCK	4	SPIC0
5	SPIC1	6	SPIC2
7	SPIC3	8	SPIC4
9	+5 V	10	GND

2.12 Protocol Timer Interface

The DSP56651ADM provides an interface connection for use with the DSP56651's protocol timer. Refer to Figure 2-17 Protocol Timer Functional Block Diagram for functional block diagram and Table 2-33 for pin assignments.

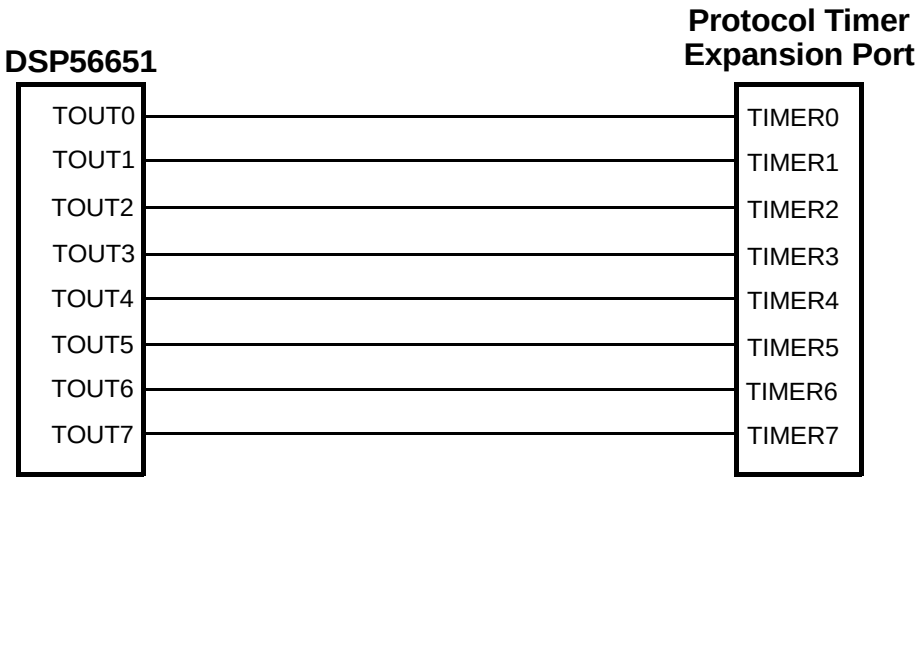

Figure 2-17. Protocol Timer Functional Block Diagram

Table 2-33. Protocol Timer Connector (P14) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	Timer0	2	Timer1
3	Timer2	4	Timer3
5	Timer4	6	Timer5
7	Timer6	8	Timer7
9	+3.3 V	10	GND

2.13 SIM Card Interface

The DSP56651ADM provides an interface connection for use with an external SIM Card. (See Figure 2-18 SIM Card Functional Block Diagram for the SIM card interface block diagram.) The SIM card connector pinout is shown in Table 2-34.

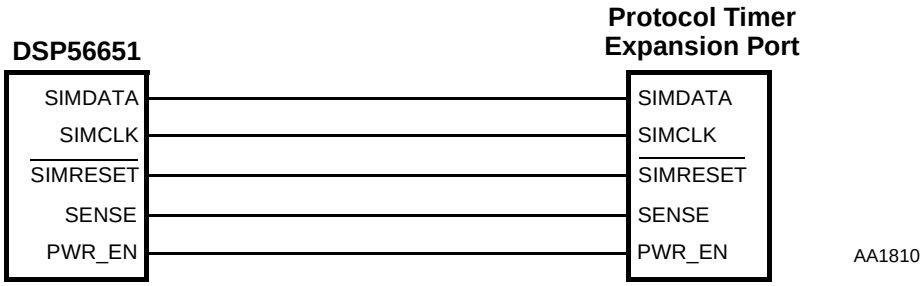

Figure 2-18. SIM Card Functional Block Diagram

Table 2-34. SIM Card Connector (P15) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	SIMCLK	2	SENSE
3	SIMDATA	4	SIMRESET
5	PWR_EN	6	key
7	+3.3 V	8	GND

2.14 DSP56651 Serial Port

The DSP56651ADM provides an interface connection for use of the DSP56651's UART port. See Figure 2-19 DSP56651 Serial Port Functional Block Diagram for the serial port interface block diagram. The serial port connector pinout is shown in Table 2-35.

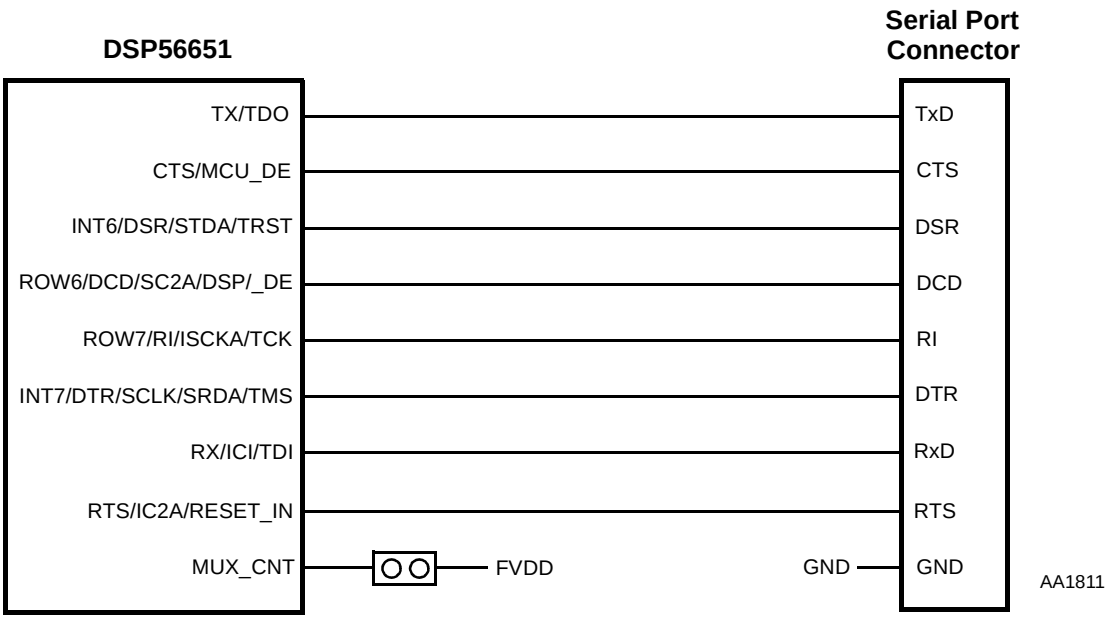

Figure 2-19. DSP56651 Serial Port Functional Block Diagram

Table 2-35. DSP56651 Serial Port Jumper Options

JP6	Options Selected
1-2	Disable DSP56651 serial port operation
OPEN	Enable DSP56651 serial port operation

The serial port connector pin assignments are listed in Table 2-36.

Table 2-36. DSP56651 Serial Port Connector (P18) Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	DCD	2	RxD
3	TxD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	GND

2.15 Reset Interface

The DSP56651ADM provides several reset input sources for use by the DSP56651 and off-board logic. See Figure 2-20 Reset Interface Functional Block Diagram for the serial port interface block diagram.

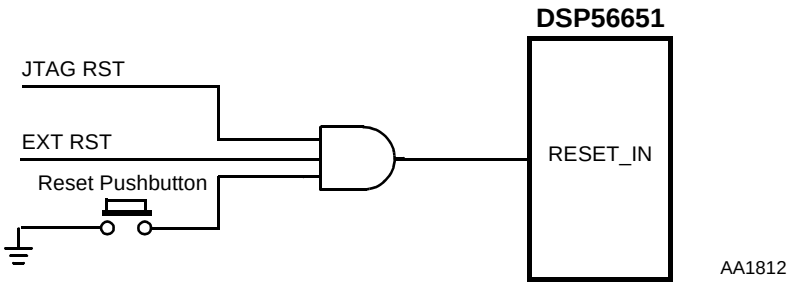

Figure 2-20. Reset Interface Functional Block Diagram

2.16 LED Indicators

Two banks of three on-board LEDs are provided on the DPS56651ADM along with a power indicator. (See Table 2-37 and Table 2-38) Power indicator LED1 shows when power is applied to the DSP56651ADM board. LED2, 3, and 4 are used by the DSP as debugging indicators. LED5, 6, and 7 are used by the MCU as debugging indicators.

Table 2-37. DSP Debugging Indicators

LED#	LED Color	LED Control Signal
LED2	Red	SC0A
LED3	Yellow	SC1A
LED4	Green	SC2A

Table 2-38. MCU Debugging Indicators

LED #	LED Color	LED Control Signal
LED5	Green	COL5
LED6	Yellow	COL6
LED7	Red	COL7

2.17 Test Points

Five on-board test points are provided to allow for voltage reference connections. These test points are located near the corners of the DSP56651ADM board and are connected to digital ground.

2.18 DSP Terminal Board

The DSP Terminal board provides twenty-one keys and a graphical LCD with alphanumeric capabilities. The keypad has four menu keys A, B, C, D, and a twelve key standard telephone keypad and up, down and select side keys. See Figure 2-21., "Terminal Keys Assignments," for the key layout assignment. The DSP Terminal can accept two different kinds of LCD modules. The first module, LCD1, has two modes of operation; an alphanumeric mode with a screen size of four lines by 16 characters and a graphical mode with 128 by 64 pixel resolution. The second module, LCD2, is an alphanumeric character based module with a screen size of four lines by 20 characters.

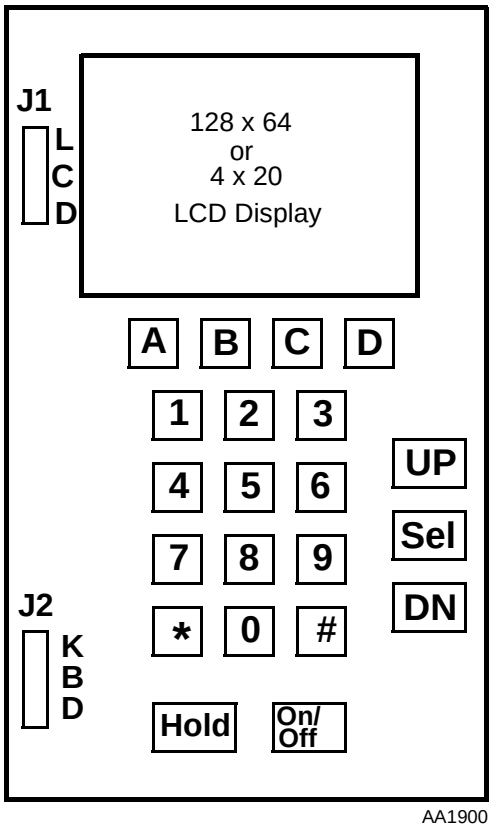

Figure 2-21. Terminal Keys Assignments

2.18.1 DSP Terminal Keypad Matrix

The DSP Terminal board contains twenty-one keys. These keys are organized in a matrix format of three rows by seven columns. Table 2-39., "DSP Terminal Key Layout," shows the relationship of each key to its row and column combination.

To connect the Keypad to the DSP56651ADM, use the provided 18 wire ribbon cable. Connect one end of the cable into connector J2 on the DSP Terminal and the other end of the cable into P10 on the DSP56651ADM. Both of these connectors are 2 x 9 Berg sticks. Table 2-40., "Keypad Connector Pin Assignments," shows the pin-out for J2.

Table 2-39. DSP Terminal Key Layout

	Column 6	Column 5	Column 4	Column 3	Column 2	Column 1	Column 0
Row 0	3	2	1	D	C	B	A
Row 1	*	9	8	7	6	5	4
Row 2	↑	⌑ Select	↓	ON/OFF	HOLD	#	0

Table 2-40. Keypad Connector Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	COL0	2	COL1
3	COL2	4	COL3
5	COL4	6	COL5
7	COL6	8	COL7
9	ROW0	10	ROW1
11	ROW2	12	ROW3
13	ROW4	14	ROW5
15	ROW6	16	ROW7
17	+3.3v	18	GND

2.18.2 DSP Terminal LCD Display

The DSP Terminal can accommodate two types of LCDs. However, only one LCD can be installed on the DSP Terminal board at one time. The graphic/alphanumeric LCD is provided with the kit. The first one is a graphical LCD with alphanumeric capabilities and the second one is an alphanumeric only LCD. The DSP56651ADM communicates serially with the LCD.

There are two methods of interfacing the DSP56651 with the LCD on the DSP Terminal. One method is by using the serial LCD Port Connector, P6, on the DSP56651ADM. This port interfaces directly with J1 on the DSP Terminal using the provided five wire ribbon cable. Table 2-41., "Serial LCD Connector (J1) Pin Assignments," shows the pin-out for J1. The other method is to use the Serial Port, P19, on the DSP56651 ADM. This port interfaces directly with the serial port on the LCD Module using a user supplied RS-232 9-pin serial cable. When this latter method is used, do not connect anything to J1.

Table 2-41. Serial LCD Connector (J1) Pin Assignments

Pin Number	Signal Name
1	GND
2	+5V
3	TxD
4	+5V
5	GND

Appendix A
DSP56651ADM Schematics

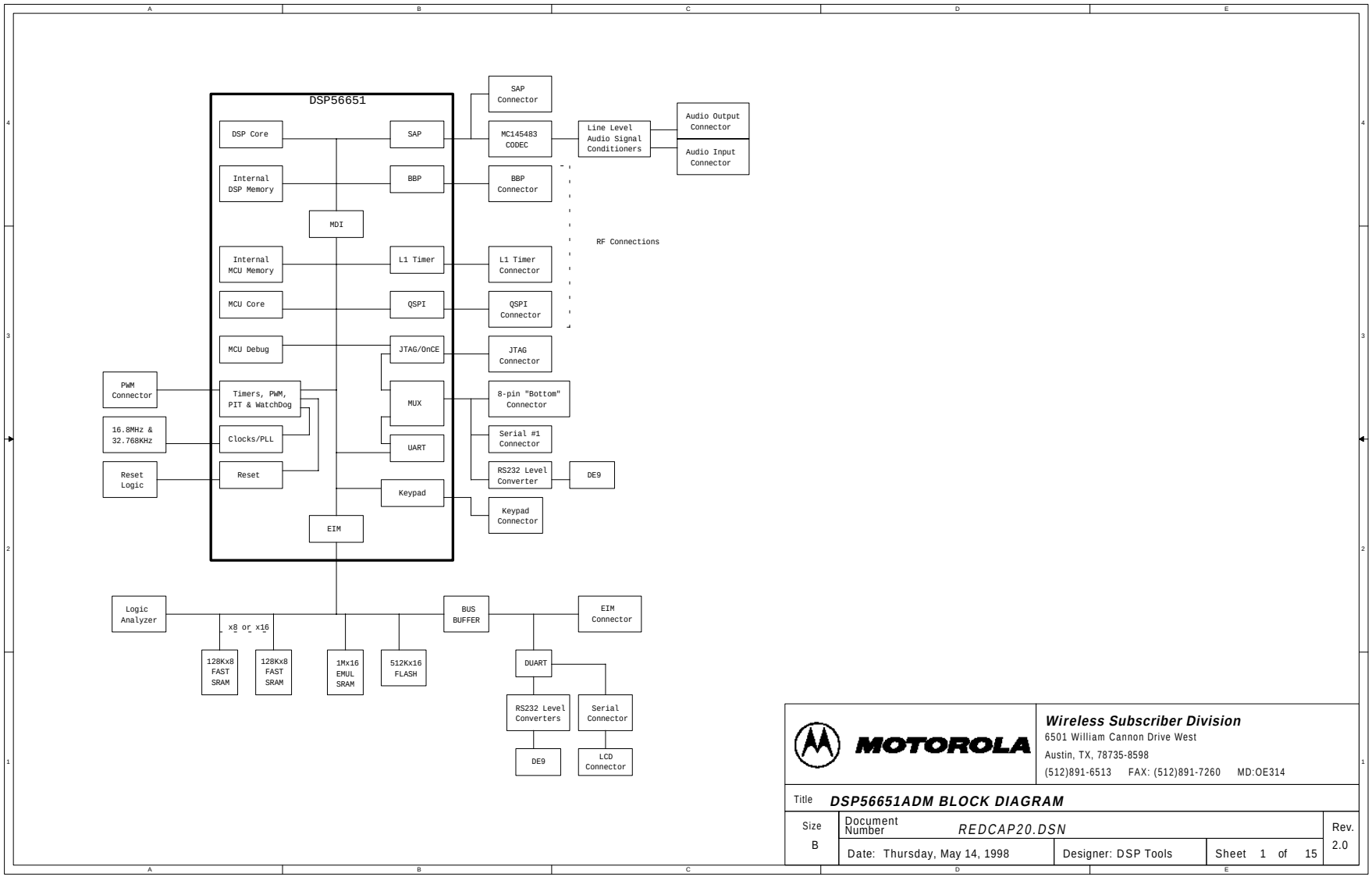

Figure A-1. DSP56651ADM Block Diagram

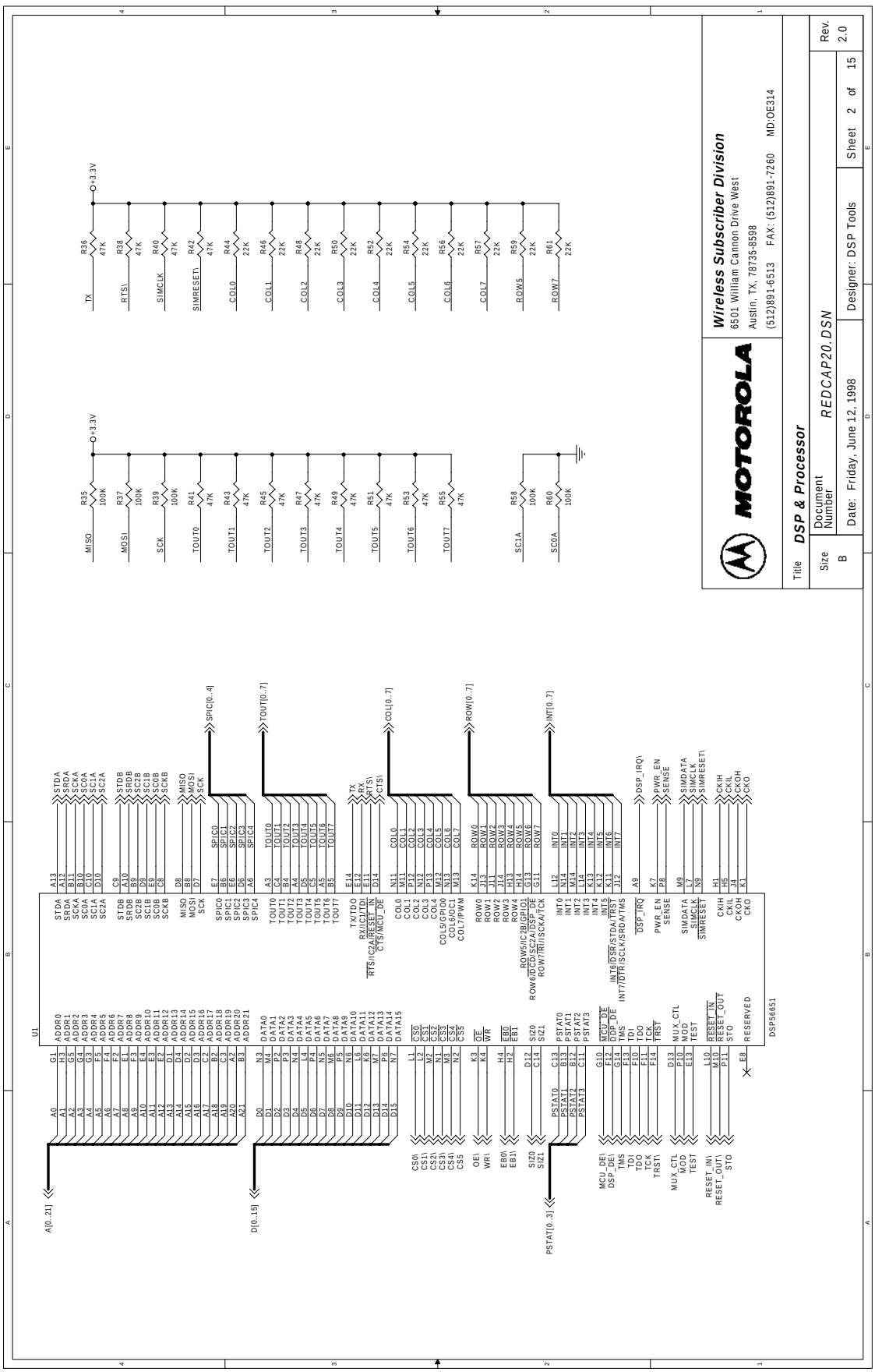

Figure A-2. DSP and Processor

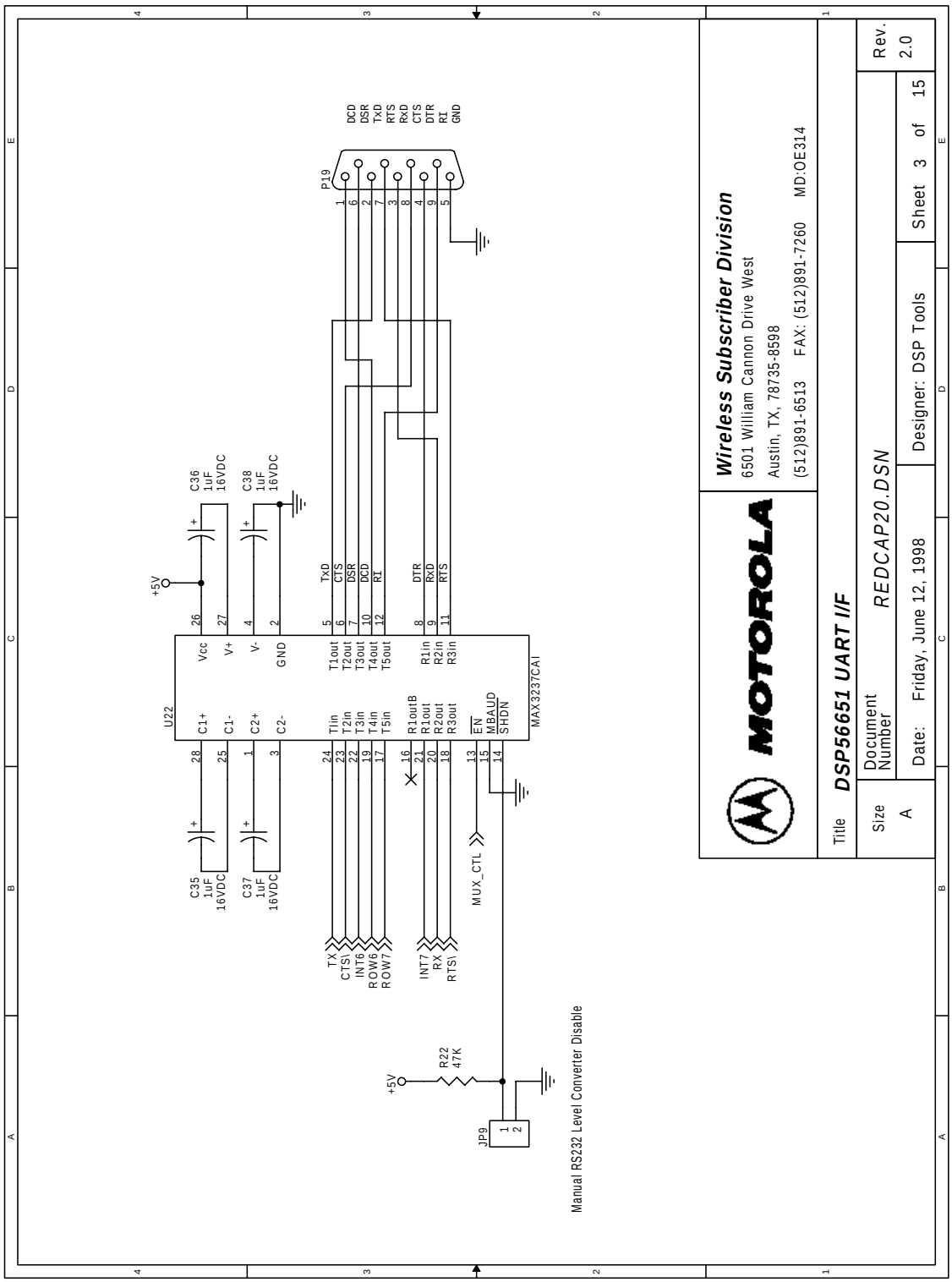

Figure A-3. DSP56651 UART I/F

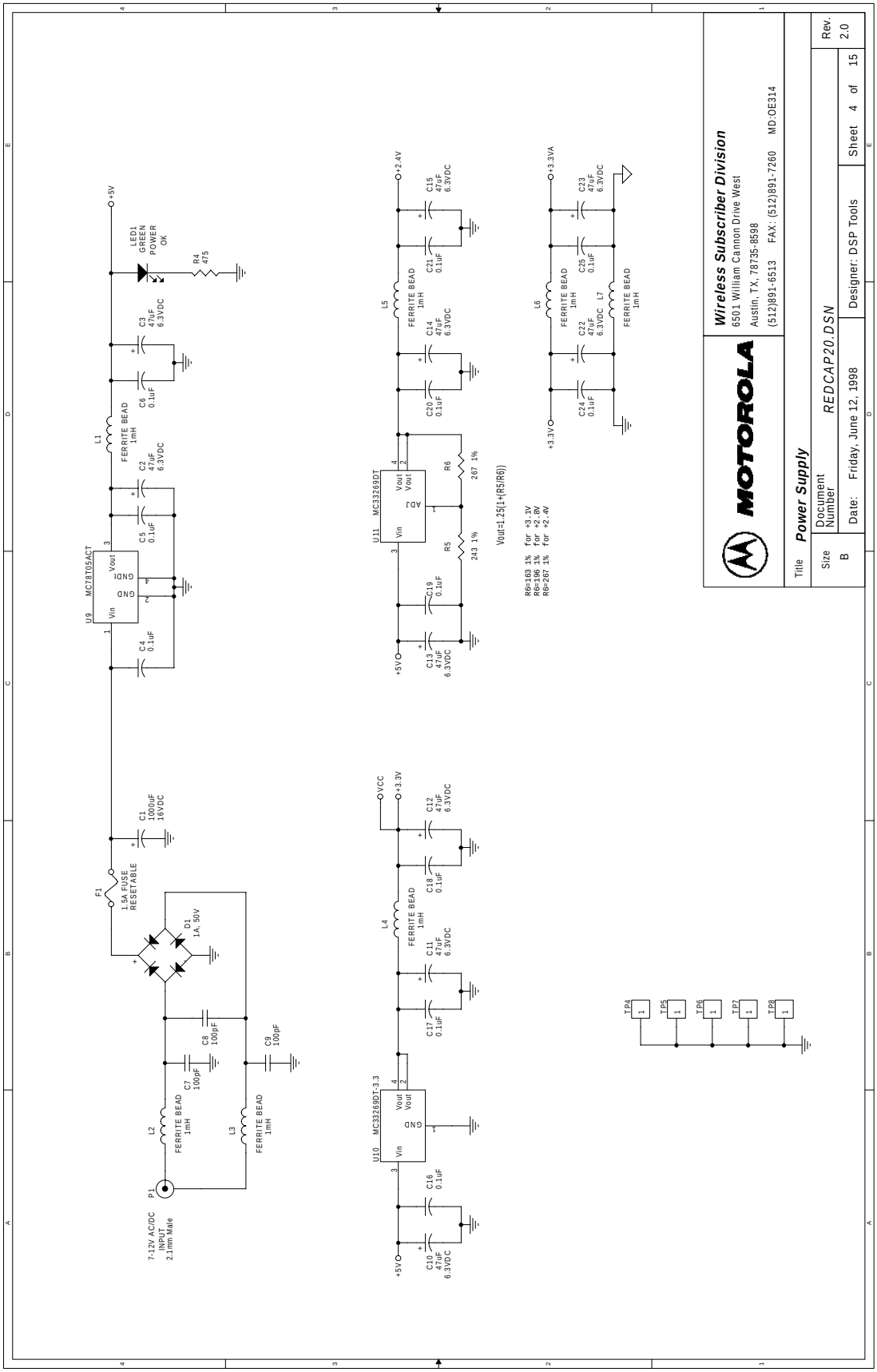

Figure A-4. Power Supply

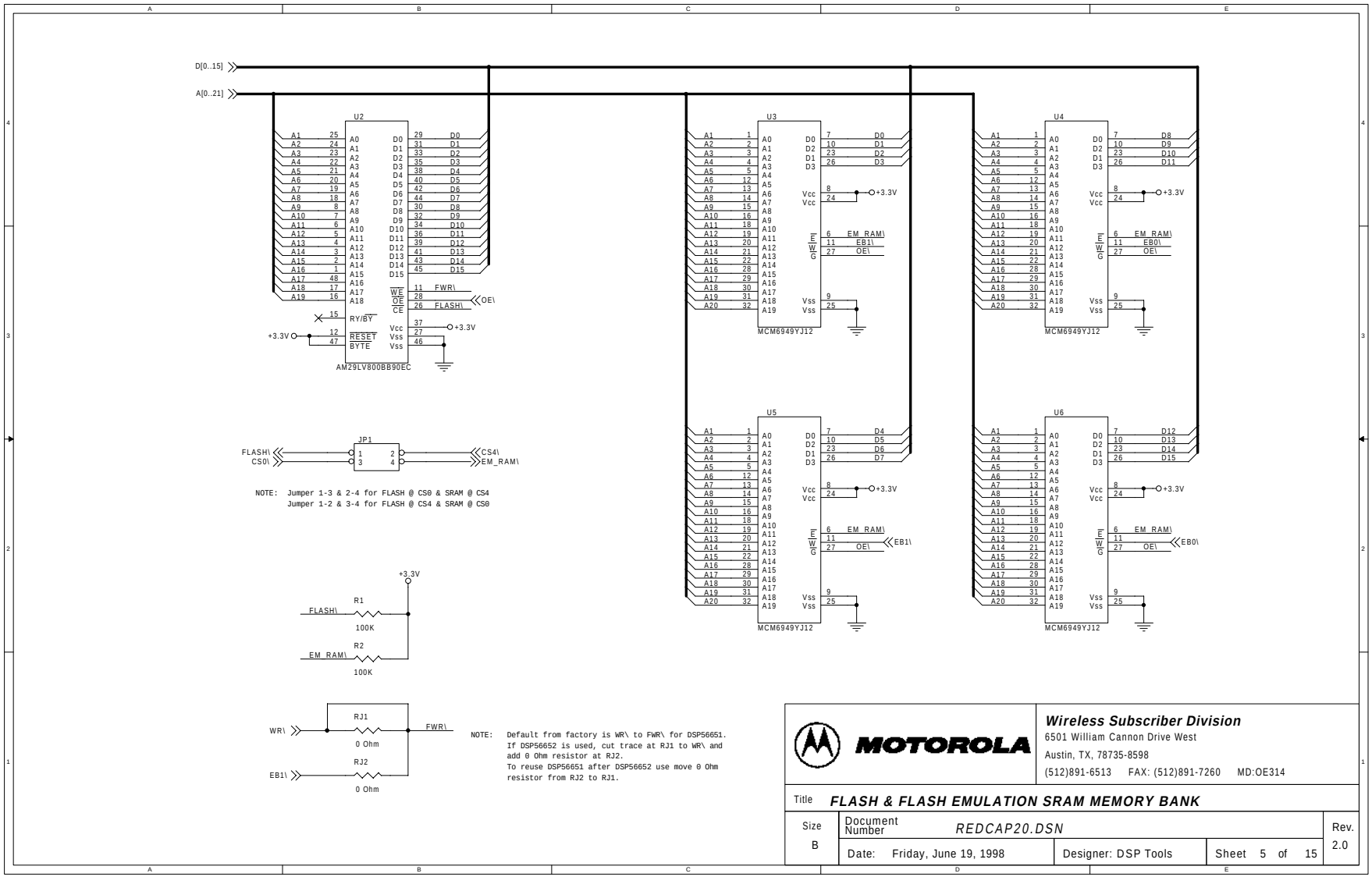

Figure A-5. Flash and Flash Emulation SRAM Memory Bank

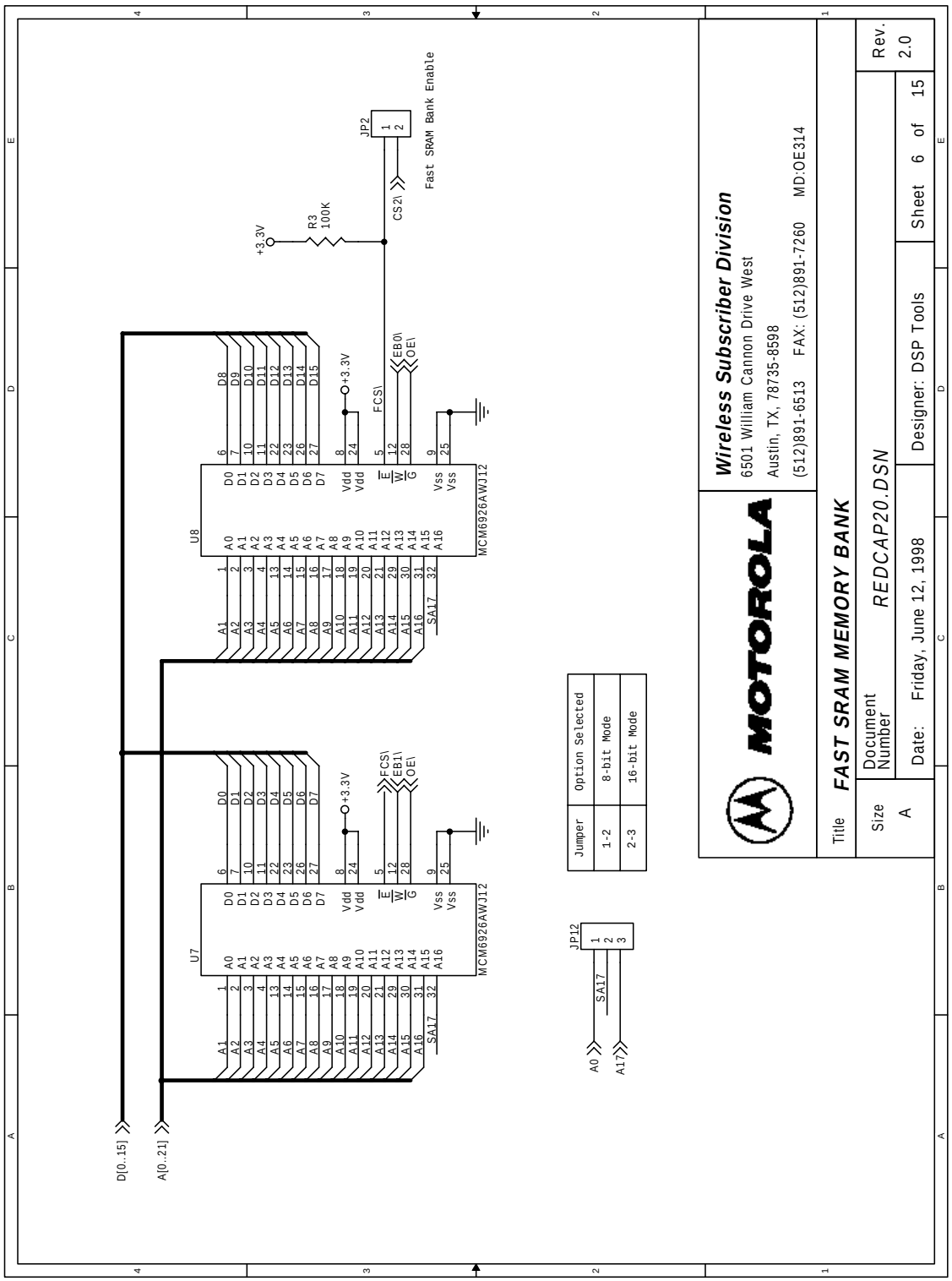

Figure A-6. Fast SRAM Memory Bank

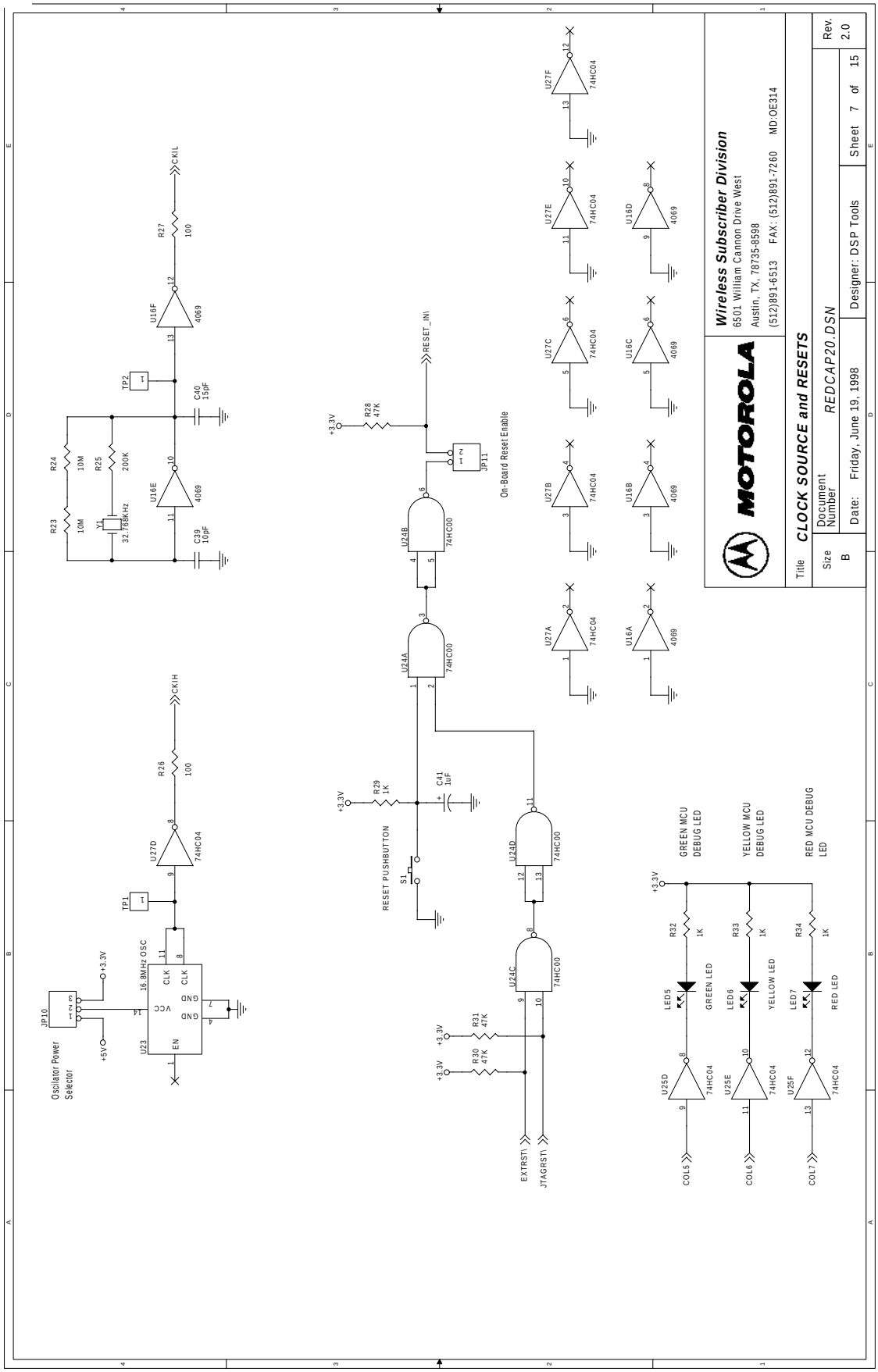

Figure A-7. Clock Source and Resets

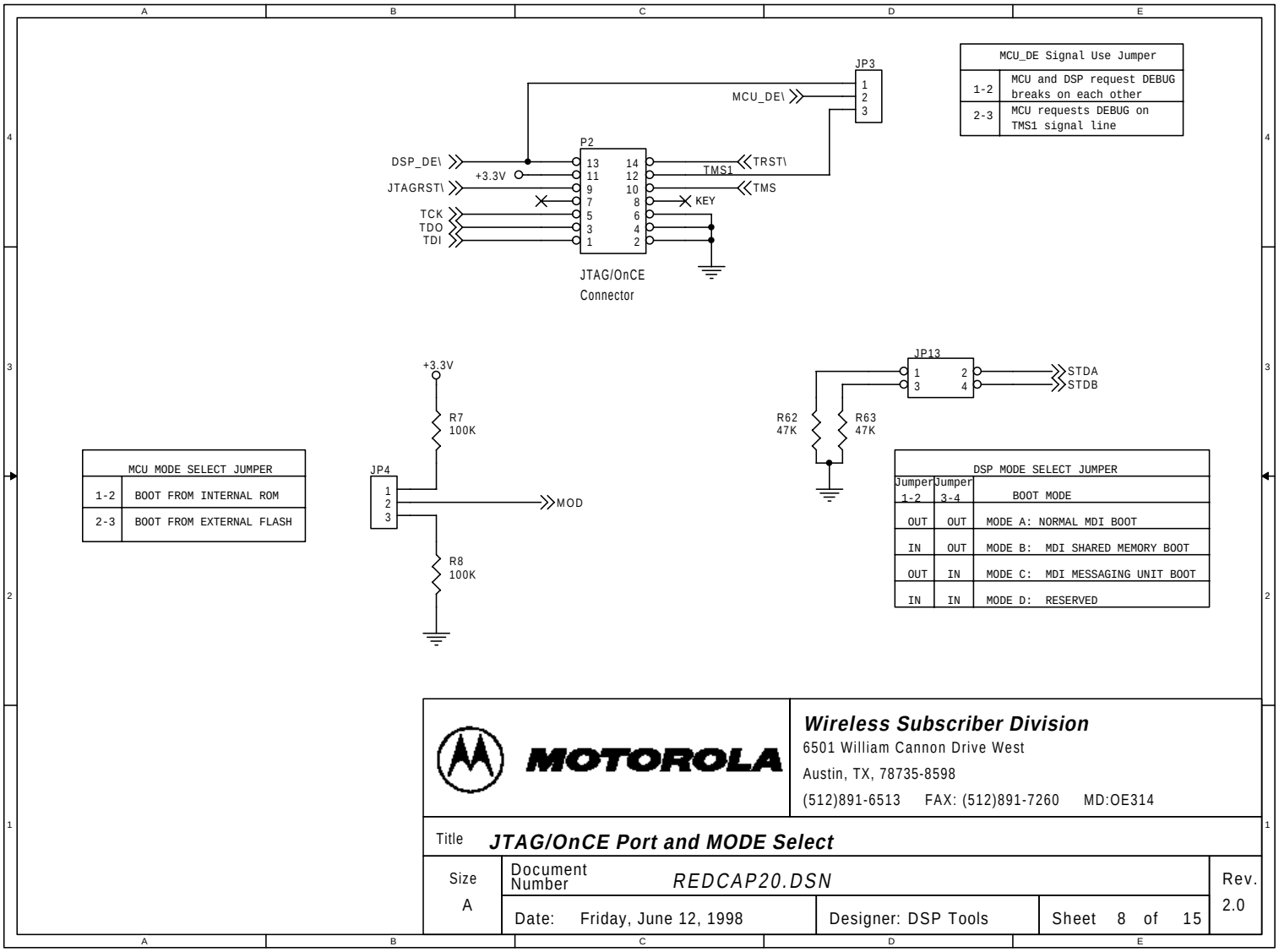

Figure A-8. JTAG/OnCE Port and MODE Select

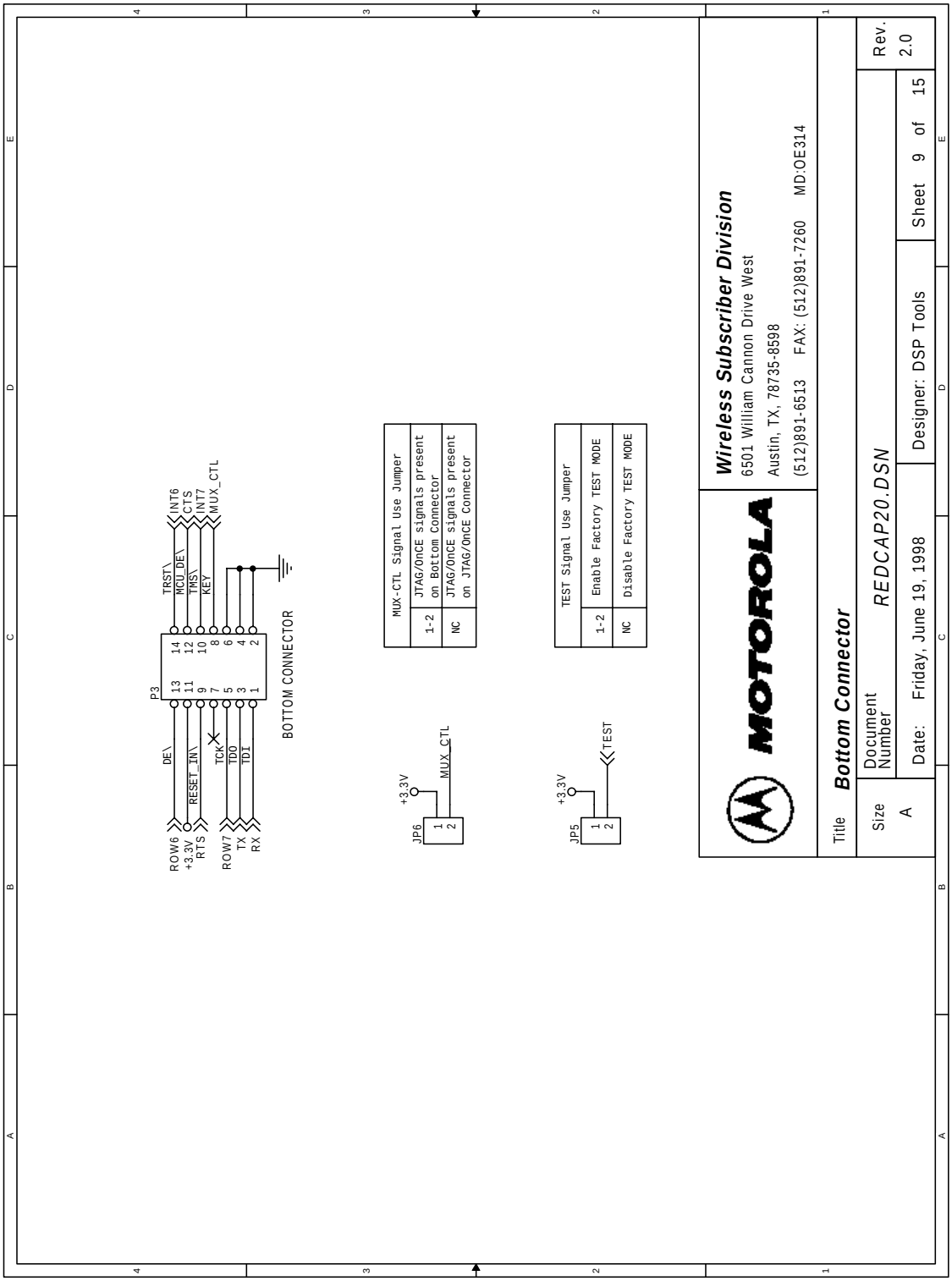

Figure A-9. Bottom Connector

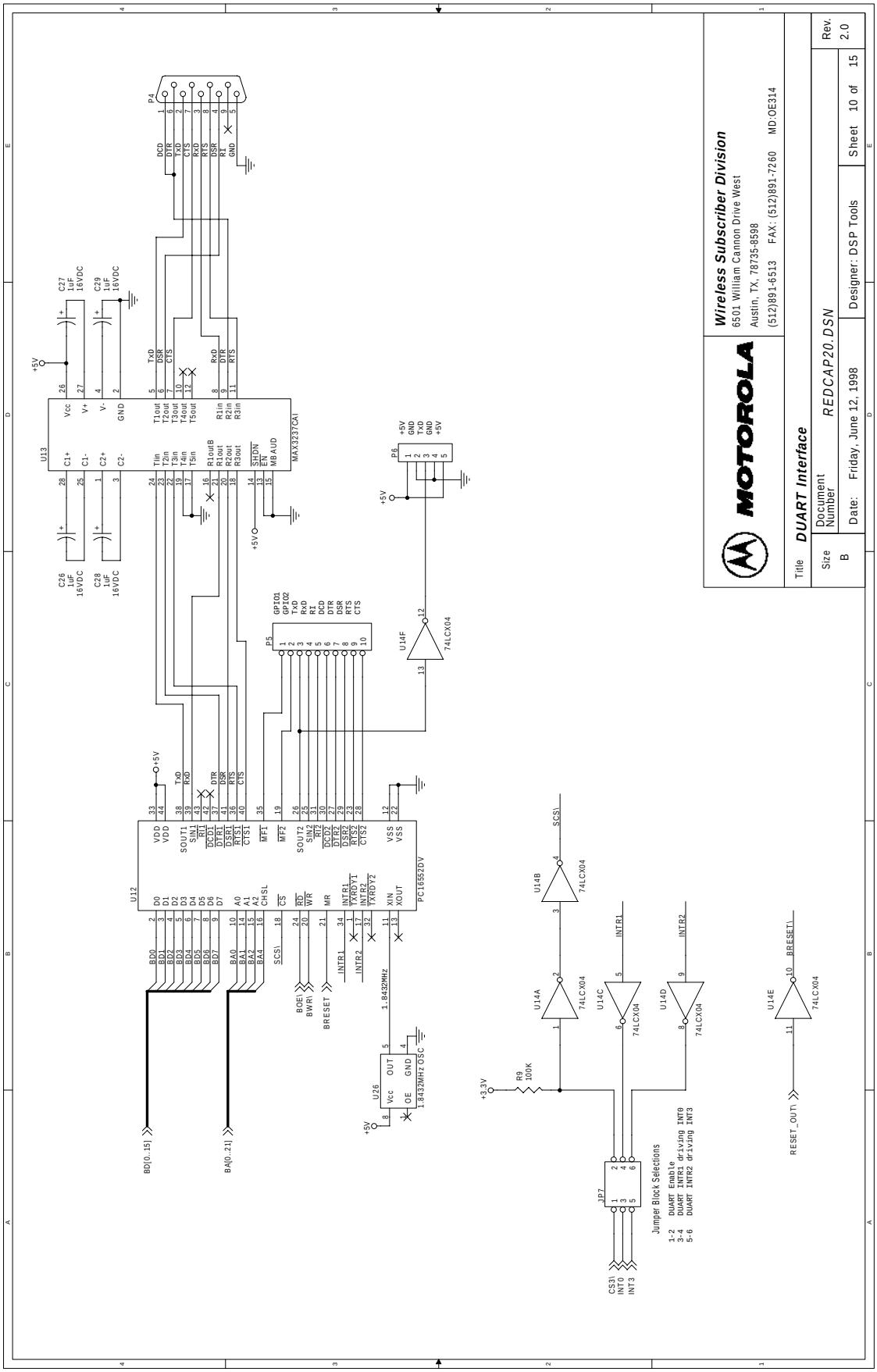

Figure A-10. DUART Interface

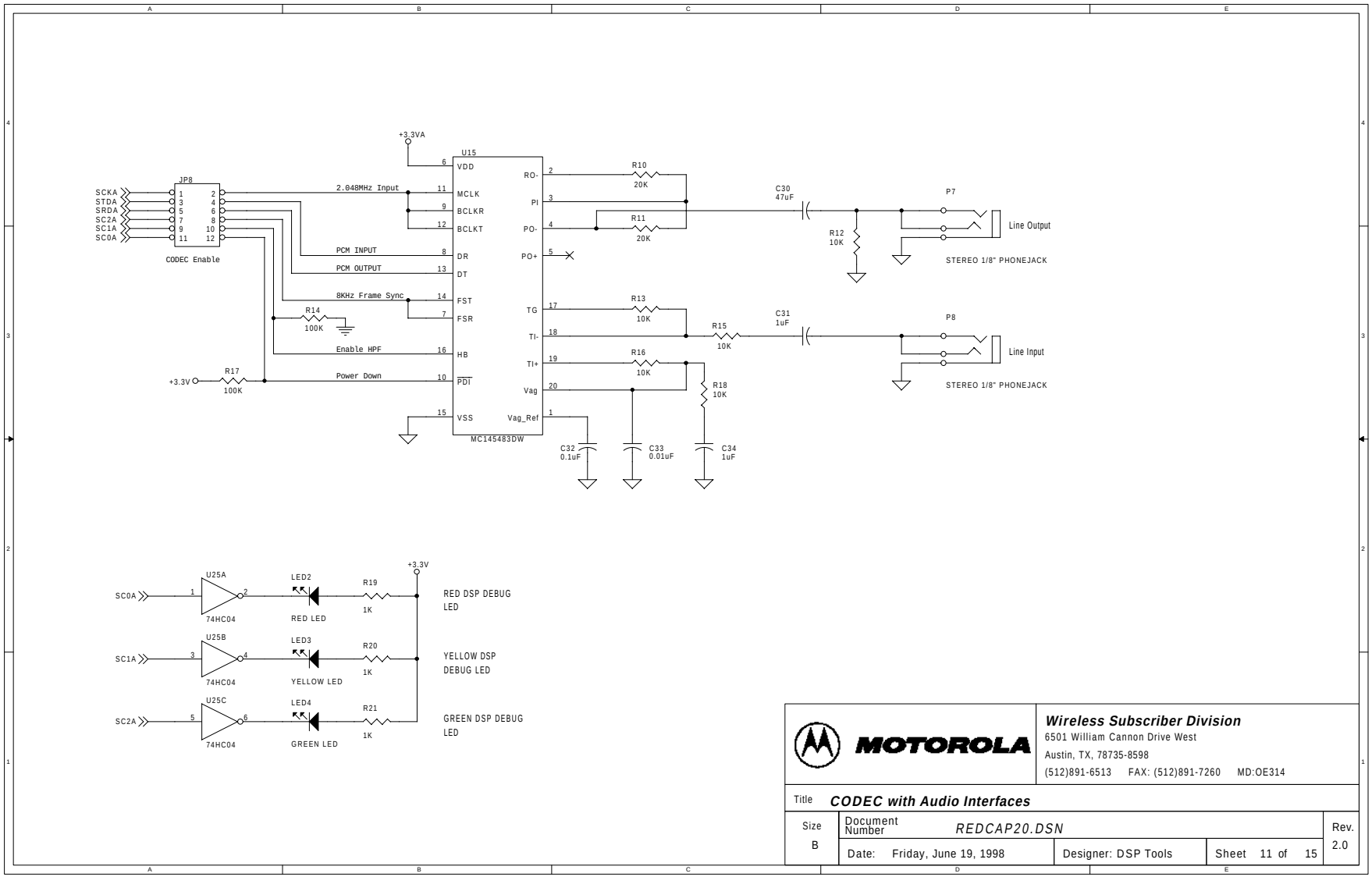

Figure A-11. CODEC with Audio Interfaces

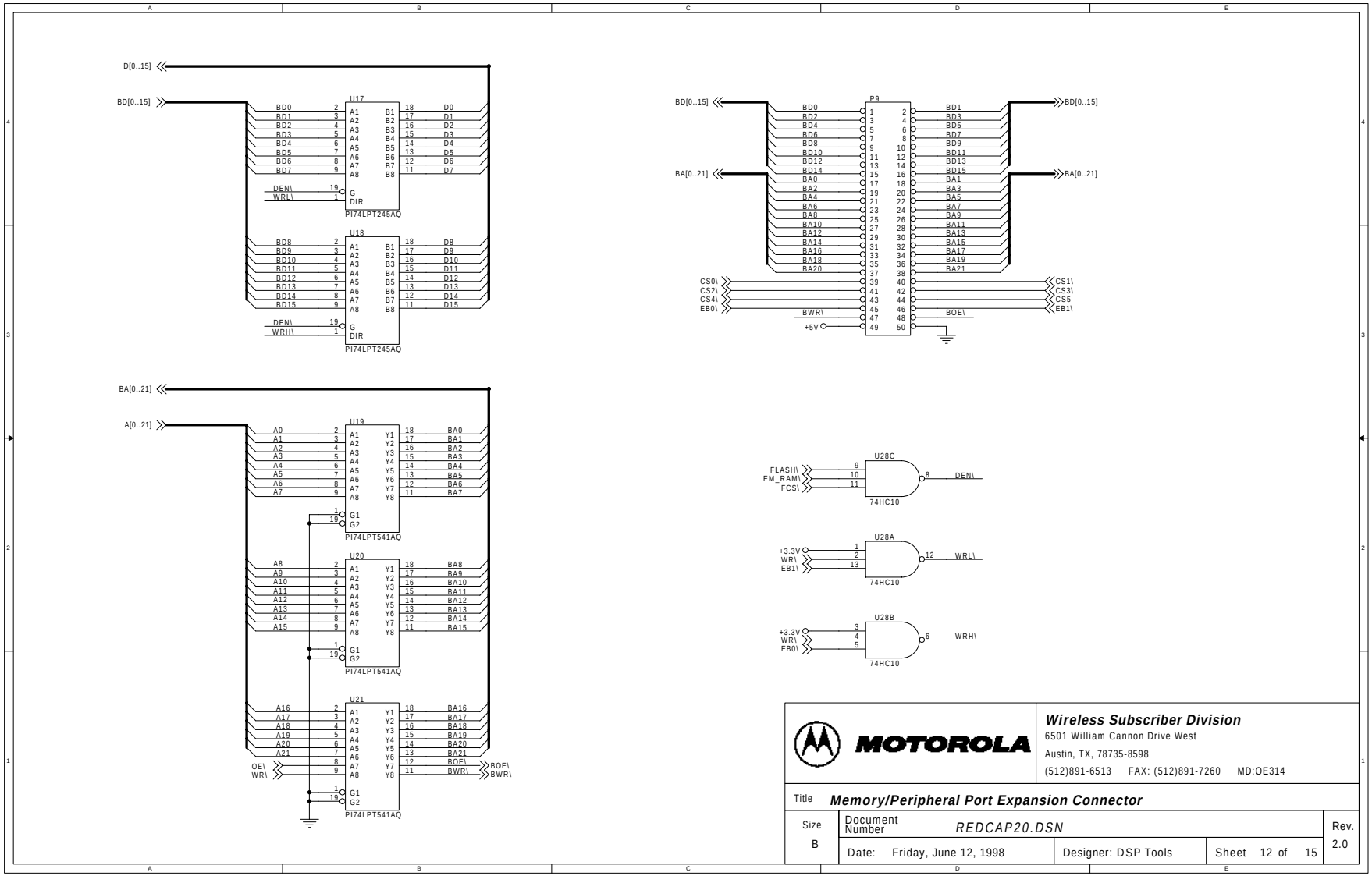

Figure A-12. Memory/Peripheral Port Expansion Connector

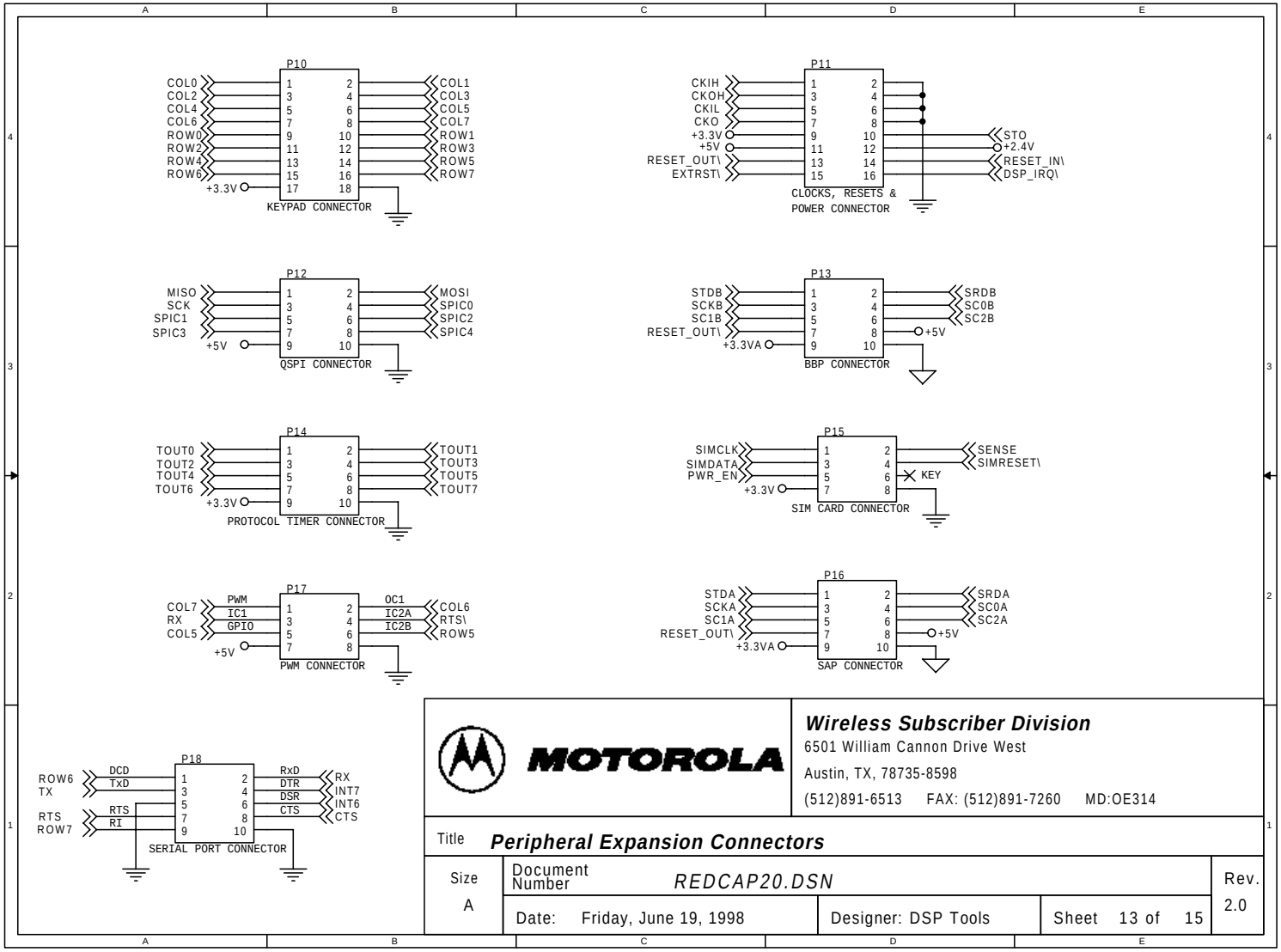

Figure A-13. Peripheral Expansion Connectors

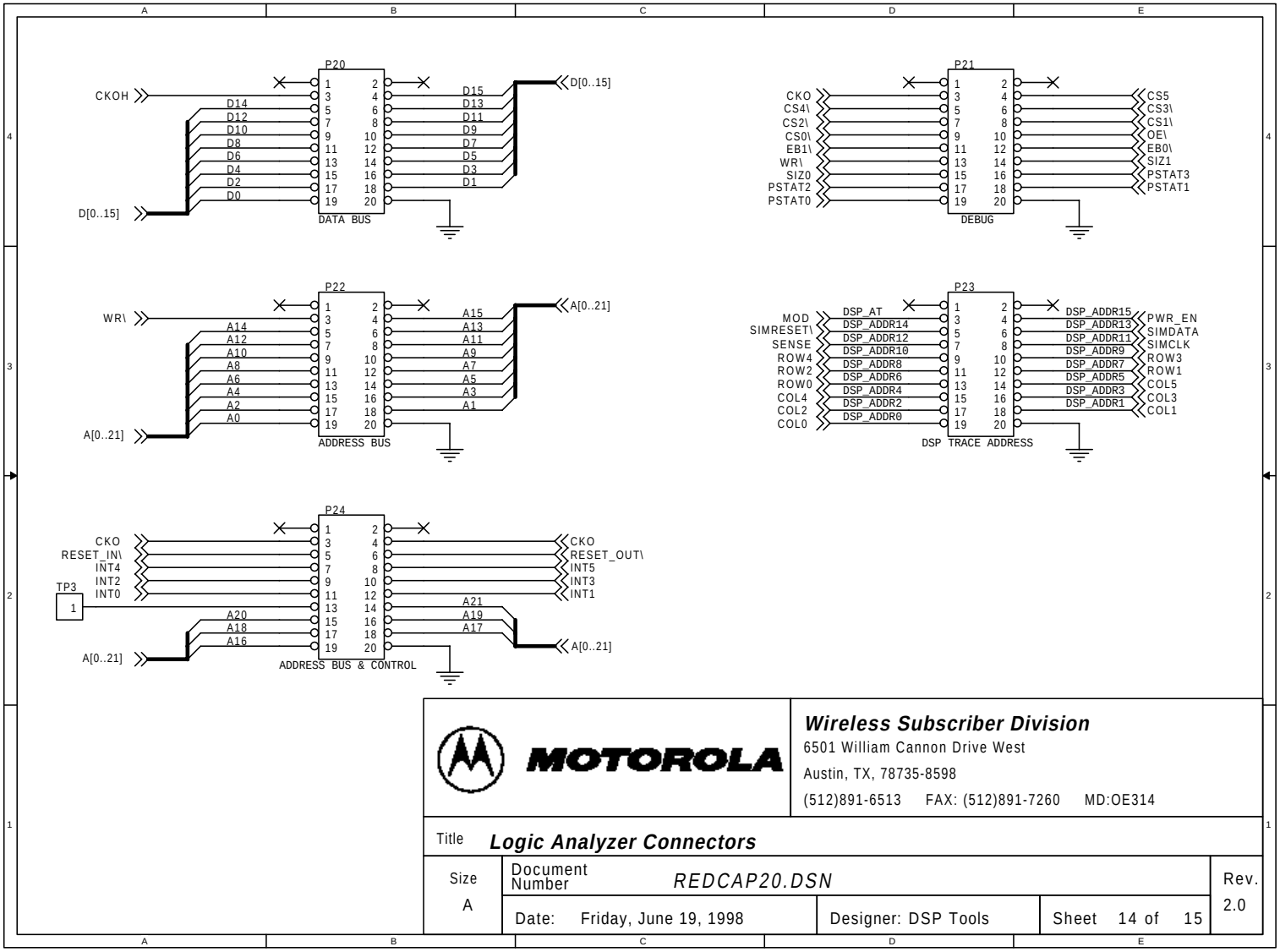

Figure A-14. Logic Analyzer Connectors

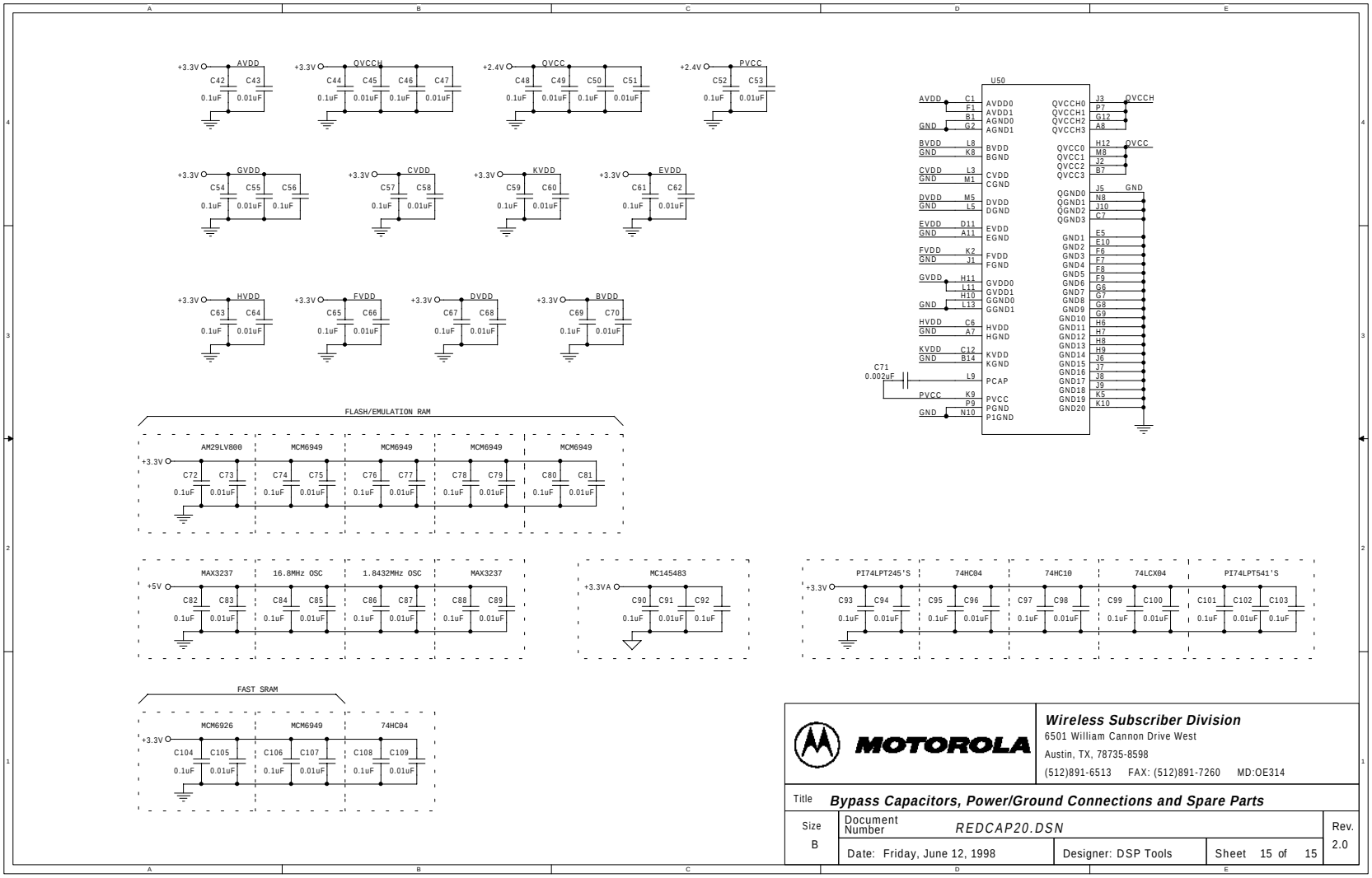

Figure A-15. Bypass Capacitors, Power/Ground Connections and Spare Parts

Appendix B
DSP56651ADM Bill of Materials

Table A-1. Electrical Parts List

Qty	Description	Ref. Designators	Vendor Part #
Integrated Circuits			
1	PC56651GC	U1	Motorola
1	AM29LV800BB90EC	U2	AMD
4	MCM6949YJ12	U3, U4, U5, U5	Motorola
2	MCM6926AWJ12	U7, U8	Motorola
1	MC78T05ACT	U9	Motorola
1	MC33269DT-3.3	U10	Motorola
1	MC33269DT	U11	Motorola
1	PC16552DV	U12	National
2	MAX3237EAI	U13, U22	Maxim
1	MC74LCX04D	U14	Motorola
1	MC145483DW	U15	Motorola
2	MC74HC04AD	U25, U27	Motorola
2	PI74LPT245AQ	U17, U18	Pericom
3	PI74LPT541AQ	U19, U20, U21	Pericom
1	16.8 MHz OSC	U23	FOX
1	MC74HC00D	U24	Motorola
1	1.8432 MHz OSC	U26	EPSON
1	MC14069UBD	U16	Motorola
1	MC74HC10D	U28	Motorola
Crystal			
1	32.768 KHz	Y1	ECS ECX-306

Qty	Description	Ref. Designators	Vendor Part #
Resistors			
13	100K Ω	R1-R3, R7-R9, R14, R17, R35, R37, R39, R58 & R60	Panasonic ERJ-6GEYJ104
1	475 Ω 1%	R4	Panasonic ERJ-6ENF4750
1	243 Ω 1%	R5	Panasonic ERJ-6ENF2430
1	267 Ω 1%	R6	Panasonic ERJ-6ENF2670
2	20K Ω	R10 & R11	Panasonic ERJ-6GEYJ203
5	10K Ω	R12, R13, R15, R16 & R18	Panasonic ERJ-6GEYJ103
7	1K Ω	R19–R21, R29, R32–R34	Panasonic ERJ-6GEYJ102
18	47K Ω	R22, R28, R30, R31, R36, R38, R40–R43, R45, R47, R49, R51, R53, R55, R62 & R63	Panasonic ERJ-6GEYJ473
2	10 M Ω	R23 & R24	YAGEO 106E
1	200K Ω	R25	Panasonic ERJ-6GEYJ204
2	100 Ω	R26 & R27	Panasonic ERJ-6GEYJ101
10	22K Ω	R44, R46, R48, R50, R52, R54, R56, R57, R59 & R61	Panasonic ERJ-6GEYJ223
Inductors			
7	1 mH FERRITE BEAD	L1–L7	Murata BL01RN1-A62
LEDs			
3	GREEN LED	LED1, LED4, LED5	Hewlett-Packard HSMG-C650
2	RED LED	LED2, LED7	Hewlett-Packard HSMS-C650
2	YELLOW LED	LED3, LED6	Hewlett-Packard HSMY-C650
Diode			
2	1 A, 50 V BRIDGE	D1	Vishay/Liteon DF005S
Fuses			
2	1.5 A, 35 V RESETABLE	F1	LittleFuse 2029L075
Capacitors			
1	1000 µF	C1	SKR102M1EJ21

Qty	Description	Ref. Designators	Vendor Part #
11	47 µF	C2, C3, C10–C15, C22, C23, C30	TCC47K6.3C
47	0.1 µF	C4–C6, C16–C21, C24, C25, C32, C42, C44, C46, C48, C50, C52, C54, C56, C57, C59, C61, C63, C65, C67, C69, C72, C74, C76, C78, C80, C82, C84, C86, C88, C90, C92, C93, C95, C97, C99, C101, C103, C104, C106, C108	MCCE104K2NR-T2
3	100 pF	C7–C9	MCCE101J2NO-T1
11	1 µF	C26–C29, C31, C34–C38, C41	TCC1K6.3A
33	0.01 µF	C33, C43, C45, C47, C49, C51, C53, C55, C58, C60, C62, C64, C66, C68, C70, C73, C75, C77, C79, C81, C83, C85, C87, C89, C91, C94, C96, C98, C100, C102, C105, C107, C109	MCCE103K2NR-T1
1	10 pF	C39	MCCE100D2N0-T1
1	15 pF	C40	MCCE150J2NO-T1
1	0.002 µF	C71	MCCE202K2NR-T1

Table A-2. Hardware Parts

Qty	Description	Ref. Designator	Vendor Part #
Jumpers			
2	2 × 2 Bergstick	JP1, JP13	Samtec TSW-1-2-07-S-D
5	2 × 1 Bergstick	JP2, JP5, JP6, JP9, JP11	Samtec TSW-1-2-07-S-S
4	3 × 1 Bergstick	JP3, JP4, JP10, JP12	Samtec TSW-1-3-07-S-S
1	3 × 2 Bergstick	JP7	Samtec TSW-1-3-07-S-D
1	6 × 2 Bergstick	JP8	Samtec TSW-1-6-07-S-D
Test Points			
8	1 × 1 Bergstick	TP1–TP8	Samtec TSW-1-1-07-S-S
Sockets			

Qty	Description	Ref. Designator	Vendor Part #
1	14-pin socket	U23	Assmann AR14-HZW
Connectors			
2	Stereo Phonejack	P7, P8	Switch Craft 35RAPC4BHN2
2	DE9F Connector	P4, P19	AMP 745781-4
2	7 x 2 RT Connector	P2, P3	Samtec TSW-1-7-07-S-D-RA
1	5 x 2 RT Connector	P5	Samtec TSW-1-5-07-S-D-RA
1	Power Connector	P1	Switch Craft RAPC-712
2	5 x 1 Connector	P6	Samtec TSW-1-5-07-S-S
1	25 x 2 RT Connector	P9	Samtec TSW-1-25-07-S-D-RA
1	9 x 2 RT Connector	P10	Samtec TSW-1-9-07-S-D-RA
1	8 x 2 RT Connector	P11	Samtec TSW-1-8-07-S-D-RA
1	5 x 2 RT Connector	P12–P14, P16, P18	Samtec TSW-1-5-07-S-D-RA
1	4 x 2 RT Connector	P15, P17	Samtec TSW-1-4-07-S-D-RA
1	10 x 2 Connector	P20–P24	Samtec TSW-1-10-07-S-D
Switches			
2	Momentary Pushbutton	S1	BOURNS 7914G-000ECT
Miscellaneous			
22	Shunt	SH1–SH22	Samtec SNT-100-BL-T
8	4–40 Nylon Screws	N/A	N/A
8	3/4” Nylon Standoffs	N/A	N/A

Index

M

O

P

Q

R

S

T

U

V