

---

## Table of Contents (Continued)

Paragraph Number	Title	Page Number
<b>SECTION 1</b>		
<b>DSP56166 OVERVIEW</b>		
1.1	INTRODUCTION .....	1-3
1.2	DSP5616 CORE BLOCK DIAGRAM DESCRIPTION .....	1-4
1.2.1.	Data Buses .....	1-4
1.2.2.	Address Buses .....	1-5
1.2.3.	Data ALU .....	1-6
1.2.4.	Address Generation Unit (AGU) .....	1-9
1.2.5.	Program Control Unit (PCU) .....	1-10
1.2.5.1.	Interrupt Priority Structure .....	1-10
1.2.5.2.	Interrupt Priority Levels (IPL) .....	1-13
1.2.5.3.	Exception Priorities within an IPL .....	1-13
1.3	MEMORY ORGANIZATION .....	1-13
1.4	EXTERNAL BUS, I/Os and ON-CHIP PERIPHERALS .....	1-14
1.4.1.	Memory Expansion Port (Port A) .....	1-15
1.4.2.	General Purpose I/O (Port B, Port C) .....	1-15
1.4.3.	RSSI0 and RSSI1 .....	1-16
1.4.4.	Timer .....	1-16
1.4.5.	Host Interface (HI) .....	1-16
1.5	OnCE .....	1-17
1.6	PROGRAMMING MODEL .....	1-17
1.6.1.	Data ALU .....	1-17
1.6.1.1.	Data ALU Input Registers (X1, X0, Y1, Y0) .....	1-18
1.6.1.2.	Data ALU Accumulator Registers (A2, A1, A0, B2, B1, B0) .....	1-18
1.6.2.	Address Generation Unit .....	1-20
1.6.2.1.	Address Register File (R0-R3) .....	1-20
1.6.2.2.	Offset Register File (N0-N3) .....	1-20
1.6.2.3.	Modifier Register File (M0-M3) .....	1-20
1.6.3.	Program Control Unit .....	1-20
1.6.3.1.	Program Counter (PC) .....	1-20
1.6.3.2.	Status Register (SR) .....	1-21
1.6.3.3.	Loop Counter (LC) .....	1-22
1.6.3.4.	Loop Address Register (LA) .....	1-22
1.6.3.5.	System Stack (SS) .....	1-22
1.6.3.6.	Stack Pointer (SP) .....	1-23

---

## Table of Contents (Continued)

Paragraph Number	Title	Page Number
1.6.3.7.	Operating Mode Register (OMR) .....	1-23
1.7	INSTRUCTION SET SUMMARY .....	1-26
1.7.1.	Instruction Groups .....	1-26
1.7.1.1.	Arithmetic Instructions .....	1-27
1.7.1.2.	Logical Instructions .....	1-28
1.7.1.3.	Bit Field Manipulation Instructions .....	1-28
1.7.1.4.	Loop Instructions .....	1-29
1.7.1.5.	Move Instructions .....	1-29
1.7.1.6.	Program Control Instructions .....	1-30
1.7.2.	Instruction Formats .....	1-30
1.7.3.	Addressing Modes .....	1-31
1.7.4.	Address Arithmetic .....	1-33
1.7.4.1.	Linear Modifier .....	1-33
1.7.4.2.	Reverse Carry Modifier .....	1-33
1.7.4.3.	Modulo Modifier .....	1-34

## SECTION 2 DSP56166 PIN DESCRIPTIONS

2.1	INTRODUCTION .....	2-3
2.2	ADDRESS AND DATA BUS (32 PINS) .....	2-3
2.3	BUS CONTROL (10 PINS) .....	2-3
2.4	INTERRUPT AND MODE CONTROL (4 PINS) .....	2-9
2.5	POWER, GROUND, AND CLOCK (30 PINS) .....	2-10
2.6	HOST INTERFACE (15 PINS) .....	2-11
2.7	16-BIT TIMER (2 PINS) .....	2-12
2.8	REDUCED SYNCHRONOUS SERIAL INTERFACES (RSSI0 AND RSSI1) AND PORT C (8 PINS) .....	2-13
2.9	ON-CHIP EMULATION (4 PINS) .....	2-14
2.10	ON-CHIP CODEC (7 PINS) .....	2-15

---

## Table of Contents (Continued)

Paragraph Number	Title	Page Number
---------------------	-------	----------------

---

### SECTION 3 OPERATING MODES AND MEMORY CONFIGURATION

3.1	INTRODUCTION .....	3-3
3.2	DSP56166 RAM BASED DESCRIPTION .....	3-3
3.2.1.	X Data Memory .....	3-3
3.2.2.	Program Memory .....	3-5
3.2.3.	Bootstrap ROM .....	3-5
3.2.4.	RAM Based DSP56166 Operating Modes .....	3-5
3.2.4.1.	Bootstrap Mode (Mode 0). .....	3-6
3.2.4.2.	Bootstrap Mode (Mode 1). .....	3-6
3.2.4.3.	Normal Expanded Mode (Mode 2). .....	3-7
3.2.4.4.	Development Mode (Mode 3). .....	3-7
3.2.5.	Bootstrap Mode .....	3-7
3.2.5.1.	Bootstrap ROM .....	3-7
3.2.5.2.	Bootstrap Control Logic .....	3-7
3.2.5.3.	Bootstrap Program .....	3-8
3.3	DSP56166 ROM BASED DESCRIPTION .....	3-10
3.3.1.	X Data Memory .....	3-10
3.3.2.	Program Memory .....	3-11
3.3.3.	ROM Based DSP56166 Operating Modes .....	3-12
3.3.3.1.	Single-chip Mode (Mode 0). .....	3-12
3.3.3.2.	Single-chip Mode (Mode 1). .....	3-12
3.3.3.3.	Normal Expanded Mode (Mode 2). .....	3-13
3.3.3.4.	Development Mode (Mode 3). .....	3-13

### SECTION 4 DSP56166 I/O INTERFACE

4.1	INTRODUCTION .....	4-3
4.2	I/O PORT SET-UP AND PROGRAMMING .....	4-3
4.2.1.	Port Registers .....	4-6
4.2.1.1.	Bus Control Registers (BCR and BCR2) .....	4-6
4.2.1.2.	Port B and Port C Registers .....	4-7

---

## Table of Contents (Continued)

Paragraph Number	Title	Page Number
<b>SECTION 5</b>		
<b>HOST INTERFACE</b>		
5.1	INTRODUCTION .....	5-3
5.2	HOST INTERFACE PROGRAMMING MODEL .....	5-5
5.3	HOST TRANSMIT DATA REGISTER (HTX) .....	5-5
5.4	RECEIVE BYTE REGISTERS (RXH, RXL) .....	5-5
5.5	TRANSMIT BYTE REGISTERS (TXH, TXL) .....	5-5
5.6	HOST RECEIVE DATA REGISTER (HRX) .....	5-6
5.7	COMMAND VECTOR REGISTER (CVR) .....	5-7
5.7.1.	CVR Host Vector (HV) Bits 0 through 4 .....	5-7
5.7.2.	CVR Reserved Bits – Bits 5 and 6 .....	5-7
5.7.3.	CVR Host Command Bit (HC) Bit 7 .....	5-9
5.8	HOST CONTROL REGISTER (HCR) .....	5-9
5.8.1.	HCR Host Receive Interrupt Enable (HRIE) Bit 0 .....	5-10
5.8.2.	HCR Host Transmit Interrupt Enable (HTIE) Bit 1 .....	5-10
5.8.3.	HCR Host Command Interrupt Enable (HCIE) Bit 2 .....	5-10
5.8.4.	HCR Host Flag 2 (HF2) Bit 3 .....	5-10
5.8.5.	HCR Host Flag 3 (HF3) Bit 4 .....	5-10
5.8.6.	HCR Reserved Control – Bits 5, 6, and 7 .....	5-11
5.9	HOST STATUS REGISTER (HSR) .....	5-11
5.9.1.	HSR Host Receive Data Full (HRDF) Bit 0 .....	5-11
5.9.2.	HSR Host Transmit Data Empty (HTDE) Bit 1 .....	5-11
5.9.3.	HSR Host Command Pending (HCP) Bit 2 .....	5-11
5.9.4.	HSR Host Flag 0 (HF0) Bit 3 .....	5-12
5.9.5.	HSR Host Flag 1 (HF1) Bit 4 .....	5-12
5.9.6.	HSR Reserved Status – Bits 5 and 6 .....	5-12
5.9.7.	HSR DMA Status (DMA) Bit 7 .....	5-12
5.10	INTERRUPT CONTROL REGISTER (ICR) .....	5-12
5.10.1.	ICR Receive Request Enable (RREQ) Bit 0 .....	5-12
5.10.2.	ICR Transmit Request Enable (TREQ) Bit 1 .....	5-13
5.10.3.	ICR Reserved bit – Bit 2 .....	5-13
5.10.4.	ICR Host Flag 0 (HF0) Bit 3 .....	5-13
5.10.5.	ICR Host Flag 1 (HF1) Bit 4 .....	5-14
5.10.6.	ICR Host Mode Control (HM1, HM0) Bits 5 and 6 .....	5-14
5.10.7.	ICR Initialize Bit (INIT) Bit 7 .....	5-15
5.11	INTERRUPT STATUS REGISTER (ISR) .....	5-15

---

## Table of Contents (Continued)

Paragraph Number	Title	Page Number
5.11.1.	ISR Receive Data Register Full (RXDF) Bit 0 . . . . .	5-16
5.11.2.	ISR Transmit Data Register Empty (TXDE) Bit 1 . . . . .	5-16
5.11.3.	ISR Transmitter Ready (TRDY) Bit 2 . . . . .	5-16
5.11.4.	ISR Host Flag 2 (HF2) Bit 3 . . . . .	5-17
5.11.5.	ISR Host Flag 3 (HF3) Bit 4 . . . . .	5-17
5.11.6.	ISR (Reserved Status) Bit 5 . . . . .	5-17
5.11.7.	ISR DMA Status (DMA) Bit 6 . . . . .	5-17
5.11.8.	ISR Host Request (HREQ) Bit 7 . . . . .	5-17
5.12	INTERRUPT VECTOR REGISTER (IVR) . . . . .	5-17
5.13	IVR HOST INTERFACE INTERRUPTS . . . . .	5-18
5.14	DMA MODE OPERATION . . . . .	5-18
5.14.1.	Host to DSP – Host Interface Action . . . . .	5-19
5.14.2.	Host to DSP – Host Processor Procedure . . . . .	5-19
5.14.3.	DSP to Host Interface Action . . . . .	5-20
5.14.4.	DSP to Host – Host Processor Procedure . . . . .	5-21
5.15	HOST PORT USAGE – GENERAL CONSIDERATIONS . . . . .	5-21
5.15.1.	Host Programmer Considerations . . . . .	5-21
5.15.2.	DSP Programmer Considerations . . . . .	5-23

## SECTION 6

### DSP56166 ON-CHIP SIGMA/DELTA CODEC

6.1	GENERAL DESCRIPTION . . . . .	6-3
6.2	CODEC BLOCK DIAGRAM . . . . .	6-4
6.3	ANALOG I/O DEFINITION . . . . .	6-5
6.4	INTERFACE WITH THE DSP5616 CORE . . . . .	6-6
6.4.1.	Interface Definition . . . . .	6-6
6.4.2.	On-chip Codec Programming Model . . . . .	6-7
6.4.3.	Codec Receive Register CRX . . . . .	6-8
6.4.4.	Codec Transmit Register CTX . . . . .	6-8
6.4.5.	Codec Control Register CCR0 . . . . .	6-8
6.4.5.1.	CCR0 Input Divider Bits (ED5-ED0) Bits 0-5 . . . . .	6-8
6.4.5.2.	CCR0 Codec Ratio Select Bits (CRS5-0) Bits 13-8 . . . . .	6-8
6.4.5.3.	CCR0 Reserved Bits 6-7 and 14-15 . . . . .	6-11
6.4.6.	Codec Control Register CCR1 . . . . .	6-11

---

## Table of Contents (Continued)

Paragraph Number	Title	Page Number
6.4.6.1.	CCR1 Audio Level Control Bits (VC3-VC0) Bits 0-3 . . . . .	6-11
6.4.6.2.	CCR1 Codec Loop Back Bit (CLB) Bit 7 . . . . .	6-12
6.4.6.3.	CCR1 Clock Select Bit (CLS) Bit 8 . . . . .	6-12
6.4.6.4.	CCR1 Mute Bit (MUT) Bit 10 . . . . .	6-12
6.4.6.5.	CCR1 Microphone Gain Select Bits (MGS1-0) Bits 11 and 12 . .	6-12
6.4.6.6.	CCR1 Input Select Bit (INS) Bit 13 . . . . .	6-13
6.4.6.7.	CCR1 Codec Enable Bit (COE) Bit 14 . . . . .	6-13
6.4.6.8.	CCR1 Codec Interrupt Enable Bit (COIE) Bit 15 . . . . .	6-13
6.4.6.9.	CCR1 Reserved Bits 4,5,6, and 9 . . . . .	6-13
6.4.7.	Codec Status Register COSR . . . . .	6-13
6.4.7.1.	COSR Codec Transmit Underrun Error FLag Bit (CTUE) Bit 0 .	6-13
6.4.7.2.	COSR Codec Receive Overrun Error Flag Bit (CROE) Bit 1 . . .	6-14
6.4.7.3.	COSR Codec Transmit Data Empty Bit (CTDE) Bit 2 . . . . .	6-14
6.4.7.4.	COSR Codec Receive Data Full Bit (CRDF) Bit 3 . . . . .	6-14
6.4.7.5.	COSR Reserved Bits 4-15 . . . . .	6-14
6.5	ON-CHIP CODEC GAIN AND FREQUENCY RESPONSE ANALYSIS .	6-16
6.5.1.	DC Gain and Frequency Response of the A/D Section . . . . .	6-16
6.5.2.	DC Gain and Frequency Response of the D/A Section . . . . .	6-21
6.5.2.1.	D/A Second Order Digital Interpolation Comb Filter . . . . .	6-21
6.5.2.2.	D/A Digital Modulator . . . . .	6-24
6.5.2.3.	D/A Butterworth Analog Low Pass Filter . . . . .	6-24
6.5.2.4.	Overall Frequency Response of the D/A Section . . . . .	6-25

## SECTION 7 16-BIT TIMER AND EVENT COUNTER

7.1	INTRODUCTION . . . . .	7-3
7.2	TIMER ARCHITECTURE . . . . .	7-3
7.3	TIMER COUNT REGISTER (TCTR) . . . . .	7-3
7.4	TIMER PRELOAD REGISTER (TPR) . . . . .	7-4
7.5	TIMER COMPARE REGISTER (TCPR) . . . . .	7-5
7.6	TIMER CONTROL REGISTER (TCR) . . . . .	7-6
7.6.1.	TCR Decrement Ratio (DC7-DC0) Bits 0-7 . . . . .	7-6
7.6.2.	TCR Event Select (ES) Bit 8 . . . . .	7-6
7.6.3.	TCR Overflow Interrupt Enable (OIE) Bit 9 . . . . .	7-6
7.6.4.	TCR Compare Interrupt Enable (CIE) Bit 10 . . . . .	7-7

---

## Table of Contents (Continued)

Paragraph Number	Title	Page Number
7.6.5.	TCR Timer Output Enable (TO2-TO0) Bits 11-13	7-7
7.6.6.	TCR Inverter Bit (INV) Bit 14	7-7
7.6.7.	TCR Timer Enable (TE) Bit 15	7-8
7.7	TIMER RESOLUTION	7-8
7.8	EVENT COUNTER TIMER DIAGRAMS	7-8

## SECTION 8 REDUCED SSI (RSSI0 and RSSI1)

8.1	INTRODUCTION	8-3
8.2	RSSI OPERATING MODES	8-3
8.3	RSSI CLOCK AND FRAME SYNC GENERATION	8-3
8.4	RSSI DATA AND CONTROL PINS	8-4
8.4.1.	Serial Transmit Data Pin — STD	8-6
8.4.2.	Serial Receive Data Pin — SRD	8-6
8.4.3.	Serial Clock — SCK	8-6
8.4.4.	Serial Frame Sync — SFS	8-6
8.5	RSSI RESET AND INITIALIZATION PROCEDURE	8-7
8.6	RSSI INTERFACE PROGRAMMING MODEL	8-8
8.7	RSSI TRANSMIT SHIFT REGISTER	8-10
8.8	RSSI TRANSMIT DATA REGISTER (TX)	8-10
8.9	RSSI RECEIVE SHIFT REGISTER	8-10
8.10	RSSI RECEIVE DATA REGISTER (RX)	8-10
8.11	RSSI CONTROL REGISTER A (CRA)	8-11
8.11.1.	CRA Prescale Modulus Select (PM7-PM0) Bits 0-7	8-11
8.11.2.	CRA Frame Rate Divider Control (DC2-DC0) Bits 8-10	8-12
8.11.3.	CRA Word Length Control (WL0, WL1) Bits 13 and 14	8-13
8.11.4.	CRA Prescaler Range (PSR) Bit 15	8-13
8.12	RSSI CONTROL REGISTER B (CRB)	8-13
8.12.1.	CRB Early/Late Frame Sync Bit (ELFS) Bit 2	8-14
8.12.2.	CRB Gated Clock (GCK) Bit 3	8-14
8.12.3.	CRB Frame Sync Direction (FSD) Bit 4	8-14
8.12.4.	CRB Clock Source Direction (SCKD) Bit 5	8-14
8.12.5.	CRB Clock Polarity Bit (SCKP) Bit 6	8-15
8.12.6.	CRB MSB/LSB Position Bit (SHFD) Bit 7	8-15
8.12.7.	CRB Frame Sync Length (FSL) Bit 8	8-15

## Table of Contents (Continued)

Paragraph Number	Title	Page Number
8.12.8.	CRB Frame Sync Invert (FSI) Bit 9 .....	8-15
8.12.9.	CRB RSSI Enable Bit (SSIEN) Bit 10 .....	8-15
8.12.10.	CRB RSSI Mode Select (MOD) Bit 11 .....	8-15
8.12.11.	CRB RSSI Transmit Enable (TE) Bit 12 .....	8-15
8.12.12.	CRB RSSI Receive Enable (RE) Bit 13 .....	8-16
8.12.13.	CRB RSSI Transmit Interrupt Enable (TIE) Bit 14 .....	8-16
8.12.14.	CRB RSSI Receive Interrupt Enable (RIE) Bit 15 .....	8-17
8.13	RSSI STATUS REGISTER .....	8-17
8.13.1.	RSSISR Transmit/Receive Frame Sync (TRFS) Bit 3 .....	8-17
8.13.2.	RSSISR Transmitter Underrun Error (TUE) Bit 4 .....	8-18
8.13.3.	RSSISR Receiver Overrun Error (ROE) Bit 5 .....	8-18
8.13.4.	RSSISR Transmit Data Register Empty (TDE) Bit 6 .....	8-18
8.13.5.	RSSISR Receive Data Register Full (RDF) Bit 7 .....	8-19
8.14	TIME SLOT REGISTER — TSR .....	8-19
8.15	NORMAL AND NETWORK OPERATING MODES .....	8-19
8.15.1.	Normal Mode Transmit .....	8-19
8.15.2.	Normal Mode Receive .....	8-20
8.15.3.	Network Mode .....	8-20
8.15.3.1.	Network Mode Transmit .....	8-21
8.15.3.2.	Network Mode Receive .....	8-22

## SECTION 9 DSP56166 ON-CHIP PLL

9.1	INTRODUCTION .....	9-3
9.2	ON-CHIP CLOCK SYNTHESIS CONTROL REGISTER PCR0 .....	9-4
9.2.1.	PCR0 Feedback Divider Bits (YD7-YD0) Bits 0-7 .....	9-4
9.2.2.	PCR0 Input Divider Bits (ID3-ID0) Bits 8-11 .....	9-5
9.2.3.	PCR0 Power Divider Bits (PD3-PD0) Bits 12-15 .....	9-5
9.3	ON-CHIP CLOCK SYNTHESIS CONTROL REGISTER PCR1 .....	9-5
9.3.1.	PCR1 Reserved Bits — Bits 0-9 .....	9-5
9.3.2.	PCR1 CLKO Select Bits (CS1-CS0) Bits 10 and 11 .....	9-5
9.3.3.	PCR1 Phase Select Bit (PS) Bit 12 .....	9-6
9.3.4.	PCR1 PLL Power Down Bit (PLLD) Bit 13 .....	9-6
9.3.5.	PCR1 PLL Enable Bit (PLLE) Bit 14 .....	9-6
9.3.6.	PCR1 Voltage Controlled Oscillator Lock Bit (LOCK) Bit 15 .....	9-7



---

## Table of Contents (Continued)

Paragraph Number	Title	Page Number
---------------------	-------	----------------

---

### APPENDIX A DSP56166 RAM BOOTSTRAP MODES

A.1.	INTRODUCTION.....	A-3
A.2.	BOOTSTRAP ROM.....	A-3
A.2.1.	Bootstrap Control Logic.....	A-3
A.2.2.	Bootstrap Firmware Program.....	A-4

### APPENDIX B DSP56166 APPLICATION EXAMPLES

### APPENDIX C DSP56166 PROGRAMMING SHEETS

C.1.	ADDRESSES.....	C-3
C.2.	INSTRUCTIONS.....	C-5
C.3.	CORE.....	C-18
C.4.	PLL.....	C-22
C.5.	TIMER.....	C-24
C.6.	CODEC.....	C-25
C.7.	GPI/O.....	C-27
C.8.	HOST.....	C-29
C.9.	RSSI.....	C-33

## Table of Contents (Continued)

Paragraph Number	Title	Page Number
---------------------	-------	----------------