# TN00006

## LPC1800 and LPC4300 MxMEMMAP memory map

**Rev. 1 — 30 November 2012** **Technical note**

### Document information

| Info | Content |
|---|---|
| **Keywords** | LPC1800, LPC4300, MxMEMMAP, memory map |
| **Abstract** | This technical note describes available boot addresses for the LPC1800 and LPC4300 memory map registers |

### Revision history

| Rev | Date | Description |
|---|---|---|
| 1 | 20121130 | Initial version. |

## Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

# 1. Introduction

The LPC1800 and LPC4300 MCUs both contain one or more registers called MxMEMMAP. These registers can be used to modify the MCU's memory map. They affect the instructions fetched when executing code and the local data read and written to by the instructions.

| Name | Access | Address offset | Description | Reset value | Reset value after EMC, UART0/3 boot | Reset value after USB0/1 boot | Reference |
|---|---|---|---|---|---|---|---|
| For LPC1800 family: | | | | | | | |
| M3MEMMAP | R/W | 0x100 | ARM Cortex-M3 memory mapping | 0x1040 0000 | 0x1000 0000 | 0x1000 0000 | Table 37 |
| For LPC4300 family: | | | | | | | |
| M4MEMMAP | R/W | 0x100 | ARM Cortex-M4 memory mapping | 0x1040 0000 | 0x1000 0000 | 0x1000 0000 | Table 44 |
| M0APPMEMMAP | R/W | 0x404 | ARM Cortex-M0 memory mapping | 0x2000 0000 | <tbd> | <tbd> | Table 54 |

The MxMEMMAP registers all have the same layout:

**Table 54. Memory mapping register (M0APPMEMMAP, address 0x4004 3404) bit description**

| Bit | Symbol | Description | Reset value | Access |
|---|---|---|---|---|
| 11:0 | | Reserved | 0 | - |
| 31:12 | M0APPMAP | Shadow address when accessing memory at address 0x0000 0000 | 0x2000 0000 | R/W |

The lower 12 bits are reserved and must be zero. The field consisting of the remaining bits 31:12 contains the high 20 bits of the address that will be shadowed into address 0. A simpler way to think of this is that the MxMEMMAP register contains an address, which must end in 0x000. Up to 256 MB of the information mapped at the specified memory region, will also appear at 0x00000000. This is called "shadowing" since the information appears both at its original address and at address 0x00000000.

Fig 1 contains an example of how this works on the LPC1850 when booting from external flash memory via the External Memory Controller (EMC).

**M3MEMMAP = 0x1C00 0000**

This chart shows how the boot ROM initializes M3MEMMAP when booting from external flash. By setting M3MEMMAP to 0x1C00 0000, external static memory chip select CS0 is remapped to the shadow area at 0x0000 0000. Despite the shadow area being 256 MB in size, the internal AHB SRAM located starting at 0x2000 0000 will not be shadowed.*

*The MEMMAP registers only affect the Instruction (I) and Data (D) buses on the M3/M4 cores, so memory with an address > 0x2000 0000 (on the Cortex System Bus) is not able to be shadowed unless it can be accessed by the System (S) bus.

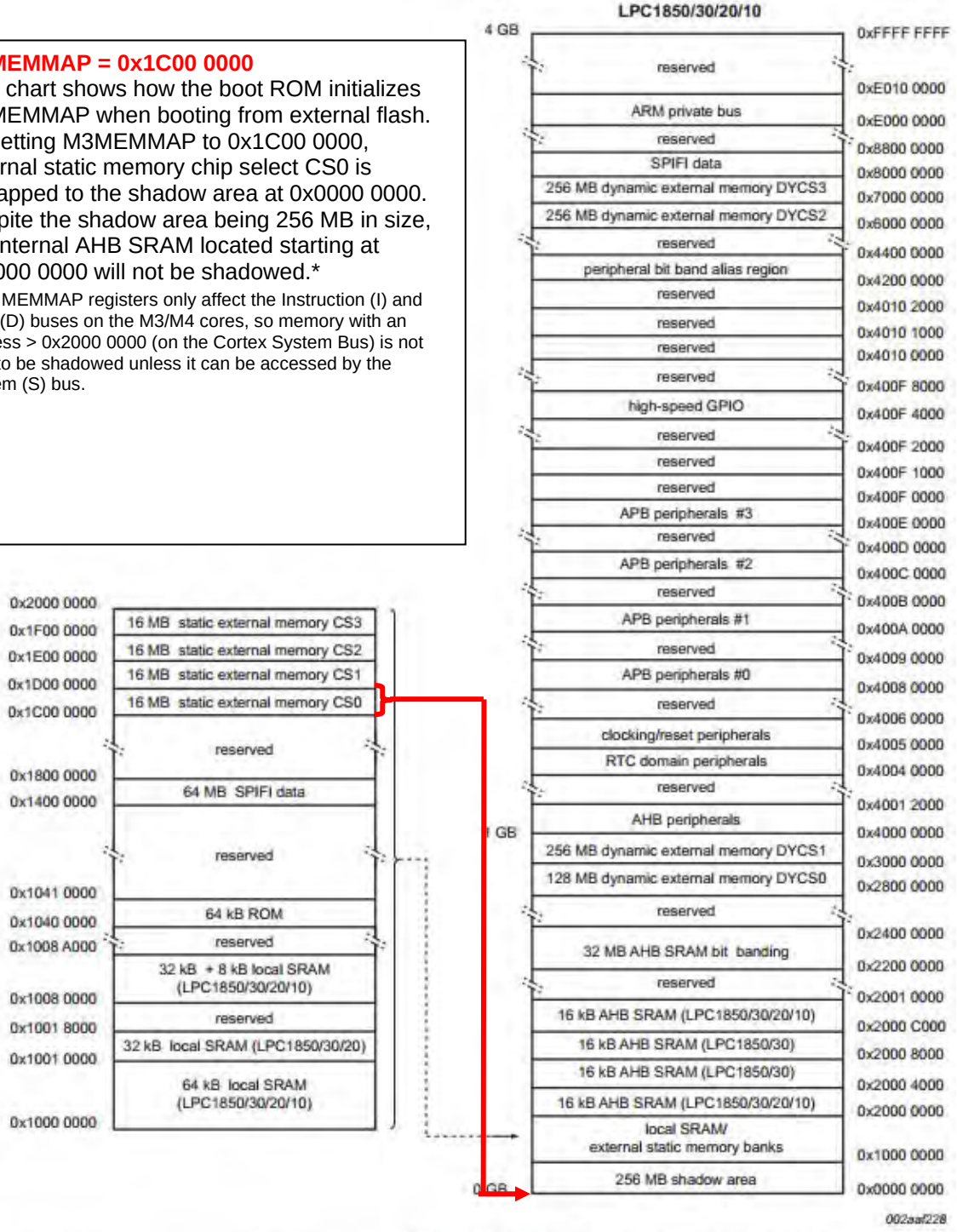


**Fig 3. System memory map - flashless parts LPC1850/30/20/10 (see Figure 4 for detailed addresses of all peripherals)**

**Fig 1. Example of shadowing**

## 1.1 MxMEMMAP FAQ

Q: What address should I build my code for?

A: The intention in providing the MxMEMMAP registers is to make it possible to build for a fixed address. Always building code for 0x0000 0000 could simplify booting from different memories since the code will be the same regardless of the address of the memory. Depending on your tool, it may be difficult to build for 0x0000 0000 because this could break the flash programming algorithms if the tool does not support relocating the code from linker address 0x0000 0000 to the flash memory area during programming.

Q: What if instead of linking for 0x0000 0000, I link my code for another address such as 0x1400 0000, which is SPIFI's lower memory region? Will the code still run?

A: Yes it will. When you build an image for the Cortex-Mx platforms, the first word in the image will be the stack location, and the second word will contain the address of the code's entry point. After mapping your code to 0x0000 0000, the ROM driver reads address 0x0000 0004 to get the code entry point. It then jumps to this address to start your program. If you build for 0x1400 0000, then the code entry point at 0x1400 0004 will be 0x14xx xxxx. This word is remapped to 0x0000 0004 and loaded by the boot ROM resulting in starting your code at 0x14xx xxxx. In this case, the shadow area would only be used by the boot ROM to read the stack pointer and start address, and would be ignored thereafter.

Q: What if I want to use many memories all containing different segments of code?

A: In this case, the shadow area can only represent one memory area and should be set up to point to your boot memory. Code for other memory areas such as DYCS0 (SDRAM) should be linked to the actual memory address, and not linked for 0x0000 0000.

Q: Is the ARM Cortex-M3/M4 VTOR register supported?

A: Yes. VTOR is supported and can be used to move the vector table out of the shadow region and locate it in another memory region. Upon boot, VTOR will be set to 0x0000 0000.

Q: Can on-board bus mastering peripherals such as USB, Ethernet, and DMA access the shadow region?

A: No. The MxMEMMAP mechanism only affects memories as seen by the Cortex-M3/M4 core's I and D or S buses or by the M0 core.

Q: What if I want to use a QSPI memory larger than 64 MB? Can I locate my code at 0 and map the upper SPIFI aperture at 0x8000 0000 to 0 using MxMEMMAP?

A: Yes. Since the SPIFI peripheral can be accessed by the System Bus (S), it will remap to 0x00000000. Other memories at address ranges > 0x20000000 that cannot be accessed by the System Bus (S) will not remap to 0x00000000.

## 1.2 LPC4300-specific FAQ

On the LPC4300, there are two MxMAP registers. M4MEMMAP controls the memory map for the Cortex-M4, and M0APPMEMMAP controls the memory map for the Cortex-M0. This means that the M0 and M4 can have different memory mapped into the shadow area. This means the code for both cores can be linked to 0x0000 0000 and stored in different memory areas.

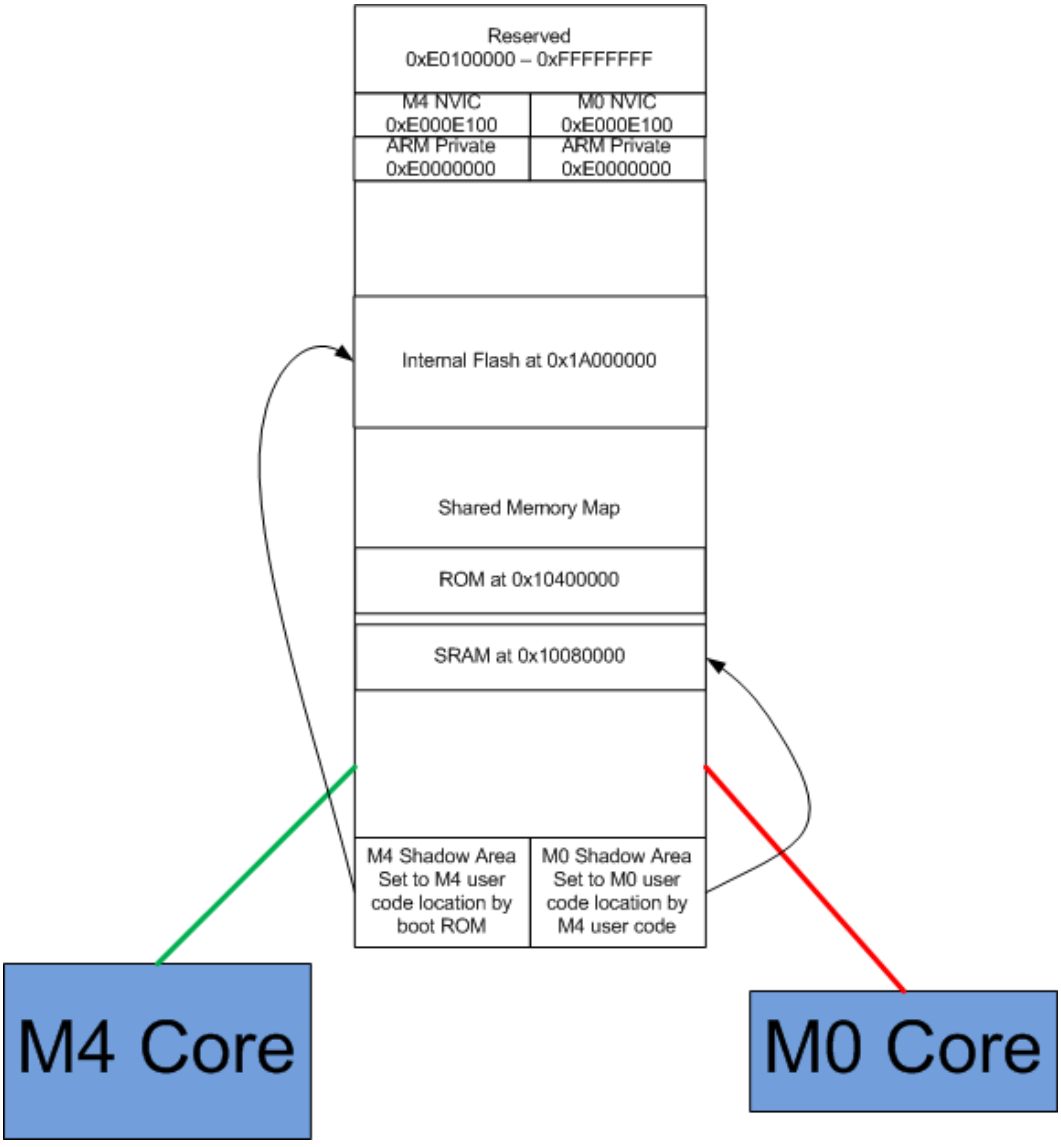


**Fig 2. MxMAP registers**

Q: How can the M0 and the M4 execute different code at the same address?

A: The MxMEMMAP registers only affect a single core in the MCU. The M4MEMMAP register does not affect the M0 or any peripherals. Neither does the M0MEMMAP register affect the M4 or any peripherals.

Q: Do I have to use M0APPMEMMAP when using the M0 core?

A: You must use M0APPMEMMAP. This is because when the M0 core is let out of reset, it will begin executing at 0x0000 0000. M0APPMEMMAP must be set up so that the M0 can fetch the correct stack pointer and code start address.

Q: Why isn't the VTOR register used?

A: There is a VTOR register on the M3 and M4 cores, but not on the M0 core. Since no VTOR is present on the Cortex-M0 core, the MxMEMMAP register was conceived as a way to remap memory on any Cortex-Mx core.

# 2. Legal information

## 2.1 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

## 2.2 Disclaimers

**Limited warranty and liability —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Evaluation products —** This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

## 2.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

# 3. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 30 November 2012**
**Document identifier: TN00006**