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Migrating from the P89V51Rx2 to P89CV51Rx2

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Document information

Info	Content
Keywords	P89V51Rx2, P89CV51Rx2
Abstract	This technical note details the differences between the P89V51Rx2 and P89CV51Rx2

Revision history

Rev	Date	Description
1	20110113	Initial version.

Contact information

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1. Introduction

The replacement of the P89V51Rx2 by the P89CV51Rx2 is possible as long as it's not in the DIL40 package. This note describes the differences between the two microcontrollers.

2. Reset

The P89V51Rx2 has a synchronous port reset. The port pins will have their initial state after startup from the oscillator. The P89CV51Rx2 does have a asynchronous port reset. The port pins will have their initial state when the reset becomes active. This is the same as for the P89C51Rx2.

3. Power-on startup

The P89V51RD2 with a bootrom code revision before V7 and P89V51RB/RC with bootrom code before revision V3 will have a delay of around 400 msec before the user program starts. In the delay the micro can enter ISP mode when the character "U" has been sent. RD2 micros with V7 and later and the RC2/RB2 micros with V3 and later can have this delay depending on the setting of the entry control . The P89CV51Rx2 will start without this delay. This micro enters ISP when PSENn = "0" during reset.

4. Internal auxiliary RAM

Bit 2 in AUXR register determines whether the internal or external auxiliary RAM is used. After reset the internal RAM has been selected (AUXR.2="0") . However for P89CV51Rx2 micros from revision B2 this has not been the case. The customer should modify the program after reset with the following (assembler) instruction: MOV 0x8E,#2. The present P89CV51Rx2 micros from revision B3 do not have this problem.

5. ISP entry control

The P89V51Rx2 can enter ISP mode in several ways depending on the revision of the bootrom code. The P89CV51Rx2 can only enter the ISP by making $\overline{PSEN}$ pin "LOW". This is the same way as for the P89C51Rx2 micros in the past.

In applications where external program memory has been used, this pin should not be "LOW" during and just after reset has been released.

Users who are using the enhanced ISP control features of the later P89V51Rx2 must change the application in such a way that $\overline{PSEN}$ pin becomes the ISP control pin.

The ISP entry is back to address 0xFC00. The ISP routine uses data RAM addresses 0x30-0x3D and bit place 0x20.1 and RAM buffer from address 0x80.

6. ISP commands

The P89CV51Rx2 does not support the following commands: Reset serial number (0x7), Verify serial number (0x8), Write serial number (0x9), Display serial number (0xA) and Reset and run code (0xB).

7. IAP mode

The P89CV51Rx2 has the same bootloader entry point as the P89C51Rx2. Because of the difference with the P89V51Rx2 the application software must be modified to the new IAP entry and the new boot enable bit location. The IAP routine also uses register R2 and data address 0x30.

Description	89CVRx2	89V51Rx2
Boot block	0xE00-0xFFFF	0-0x1FFF
Boot enable bit	AUXR1.5 (enboot)	FCF.0 (BSEL)
IAP entry address	0xFFF0	0x1F00

For erase and program command the oscillation frequency in R0 is needed (e.g., R0=11 for a frequency of 11.052 MHz). The P89V51Rx2 does not need this information.

8. Parallel programming

The P89CV51Rx2 cannot be programmed with the same algorithm as the P89V51Rx2. Please contact your programmer manufacturer for the correct algorithm.

9. Code memory bank selection

The memory bank switch between bootrom and user memory has also been changed. In the P89V51Rx2 you can switch between bootcode block (1) and user code block (0) with SWR and BSEL bit in FCF register. This does not exist in the P89CV51Rx2. You can switch between bootrom code memory and user memory with "enboot" bit in register AUXR1.

10. Secondary bootloader

When you are using a secondary bootloader a jump must be programmed in block 1 of the flash memory in the P89V51Rx2. This is not necessary in the P89CV51Rx2. You can use the boot vector register of the P89CV51Rx2 (see data sheet).

11. Security

The P89V51Rx2 has the serial number feature to prohibit entry of the ISP mode. The P89CV51Rx2 does not have this feature.

The P89V51Rx2 also has one security bit. When this bit is set a parallel programmer cannot read, erase or program the microcontroller. This bit will be cleared after a total chip erase.

The P89CV51Rx2 has three security bits like the P89C51Rx2.

The P89CV51Rx2 can be secured on the same level as the P89V51Rx2. For more detail see the data sheet of the P89CV51Rx2.

12. Clock control

The CPU clock bit for running in 6-clock of 12-clock mode that is back to register CKCON (0x8F) bit 0 in the P89CV51Rx2. This bit is only active when the FX clock mode bit, that can be programmed via ISP or Programmer, has erased. This is 12-clock mode. For peripheral settings see data sheet.

13. Software reset

The P89V51Rx2 can be reset in software by setting bit 2 in FCF (0xB1) register. This is not possible with the P89CV51Rx2.

14. Watchdog

The P89CV51Rx2 has the watchdog mechanism of the P89C51Rx2 with one watchdog register WDRST on address 0xA6. The P89V51Rx2 has a mechanism with two watchdog registers on addresses 0xC0 and 0x85.

The watchdog part of the program must be rewritten. To enable the watchdog of the P89CV51Rx2 the user must write the sequence 0x1E and 0xE1 to WDRST and must write this sequence to WDRST again within 16383 machine cycles to prevent a watchdog overflow followed by a watchdog reset.

15. Hardware

No problems are expected by changing from P89V51Rx2 to P89CV51Rx2. Both micros have the same pinning. The $\overline{EA}$ pin of the P89CVRx2 is 12 V tolerant. However, it is not advisable to put this voltage on the pin in normal operation. The tolerance is for (ISP) programming an application designed for the old P89C51RX+ microcontroller.

16. Emulation

Both micros are supporting the emulation according to the "enhanced hooks" principle. They do not support the emulation according to the "hook" principle like the P89C51Rx2.

17. Power consumption

The power consumption in operational mode @12 MHz of the P89CV51Rx2 (max 11.5 mA) is less than the P89V51Rx2 (max 23 mA). All the other values are the same.

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