Sandpoint
Reference Platform Errata

Board Revision Level	**X2**
Errata Revision Level	**G**

Revision History

Version	Date	Changes
A	1999 Feb 17	Initial errata.
B	1999 Feb 24	Updated power errata; slots
	1999 Apr 20	Test clock errata noted; no change to revision.
C	1999 May 20	Add IDSEL rework.
D	1999 Jun 18	PPMC issues; cleanup.
E	1999 Aug 10	Added 64-bit slot issues.
F	1999 Oct 28	IOCS16* and IDE issue.
G	1999 Nov 04	Errata #7 revised -- not optional, it is mandatory for COP support.

Table 1: Summary of Sandpoint Errata

#	Type	Problem	Impact	Work-Around	Affects	Rev
1	CAD	The placement of all the slots is incorrect. The expected order, from the PMC outward is: 1, 2, 3, 4. The actual order is: 2, 1, 4, 3.	Slots misidentified. This is significant for operating modes 3&4, which treat slot 4 specially; and for some OSes which expect an ethernet card in slot 2 specifically.	Re-label slots and modify documentation. For X3: reposition slots.	X2	A
2	Design	The Winbond PCIRST* signal conflicts with the PCIRST* signal from the reset controller.	Possible chip damage or loss of s/w reset capability.	Lift pin 22 of U8. This prevents the Winbond from asserting software reset. For X3: route Winbond PCIRST through PAL merge logic.	X2	A
3	CAD/ Design	The VSB filter capacitor is placed too far from the header and SuperI/O part.	Cannot turn power on with switches.	On the bottom of the board, under J23 (ATX power connector) attach a capacitor between pins 7 (GND) and pin 9 (VSTBDY). Capacitor value may be 1.0uF Non-pol to 33uF tantalum (value is not critical). For X3: Move capacitor closer to power supply header.	X2	B
4	Design	The test clock jumper select does not work. The test clock jumper grounds TCLK_SEL, which has an internal pull-down, so the jumper changes nothing..	Cannot supply test clocks.	1. Connect a jumper from J33 pin 1 to J34 pin 1 when using an external clock, if no jumper is used in J34. Alternately connect to J29 pin 26 (chassis header) or any available 3.3V power point. For X3: Connect TCLK_SEL to +3.3V or change to pulldown.	X2	B

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#	Type	Problem	Impact	Work-Around	Affects	Rev
5	Spec issue	If the MPC8240 or MPC107, as a PCI master/host, issues a configuration cycle which results in its own IDSEL being asserted, will hang or behave erratically.	System failure.	SW: On Sandpoint systems, do not issue configuration cycles to device 12. HW: 1. Remove R71 2: Connect wire from R71 pad (nearest J12) to J12 pin 21. For X3: If SYSCON asserted, disconnect AD12 from IDSEL on PMC slot.	X2	C
6	PPMC Spec changes	PPMC VITA spec changes propose that PCI arbitration be removed.	Incompatible in mode 0/1.	Do not install VITA-compatible PPMC boards on Sandpoint or vice-versa. For X3: Allow PCI arbitration separately from interrupt/SYSCON selection. Another switch?	X2	D
7	PPMC Spec changes / COP failure	PPMC VITA spec changes propose that system that PPMCs may reset the target system by asserting J2-60 low. COP debuggers expect to be able to reset the target system. In addition, the Winbond may lock up if a PCI transaction is interrupted by resetting only the PCI master (MPC8240 or MPC107) and not the Winbond target.	COP debuggers may not be able to control target system.	1.Connect a wire from TP1 (near PMC connector J12 pin 60) to Reset switch S2 (near chassis header) pin 2 (pin 2 is directly opposite pin 1, on a square pad). For X3: Merge J2-60 with on-board reset logic in the PAL.	X2	G
8	Cleanup	Hard to configure, switches all over the place.	None	None. For X3: 1. Replace scattered slide switches with SMT DIP switches. 2. Use PAL to invert INT selectively.	X2	D

Table 1: Summary of Sandpoint Errata

#	Type	Problem	Impact	Work-Around	Affects	Rev
9	Design	The 64-bit PCI slots are wired and keyed for 3.3V operation, but the Sandpoint is a 5V environment. The slots should have been univerally keyed and VIO connected to 5V.	Cards used in 64-bit PCI slots must operate at 3.3V and tolerate 5V signalling (from the Winbond and PMC). Cards which cannot tolerate 5V signals may be damaged.	Use only universal cards in the 64-bit slots. Universal PCI cards have two notches cut into the gold-plated connector area. For X3: 1. Connect VIO to 5V. 2. Change slot type to universal.	X2	E
10	Design	IOCS16* is connected to the IDE disk drives. This can cause system failures under heavy interrupt loads.	IDE disk activity during interrupt activity may cause hangs.	1. Cut IOCS16* to IDE disks and connect to ground. See detailed drawing. For X3: permanent connection.	X2	F

Errata 7: Target System Reset

Overview:

COP in-circuit emulators may not be able to reliably gain control of the target system if the reset command issued to the PPMC card does not also reset the motherboard (Sandpoint). The cause is apparently due to interrupting a PCI transaction the Winbond before completion. If the Winbond is not reset, the system will lock up until a global reset is issued.

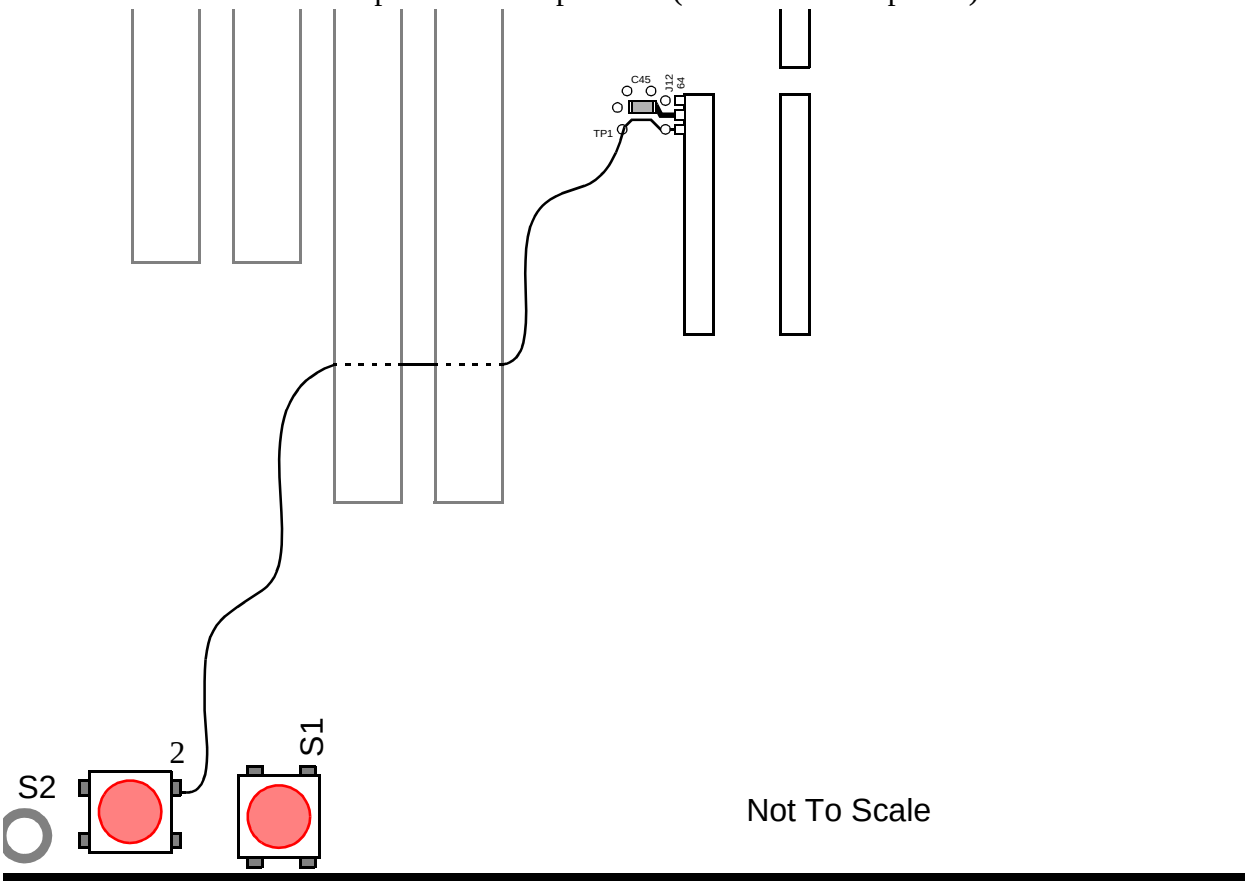
The latest VITA specification has added a pin to the PPMC connector for just such a purpose. The rework adds this function.

(Note: Some older PPMC cards may also require some rework).

Work-arounds:

The work-around is to connect the new SYSRST* function to the reset switch pin.

1. Connect a wire to pin 2 of S2 to pad TP1 (connects to J12 pin 60).



Errata 10: IDE IOCS16* FIX

Overview:

The ISA signal IOCS16* is connected to the IOCS16* pin of the IDE disk drive cables. This can cause problems with interactions between the Winbond PIC and the IDE disk controller during periods of heavy interrupt activity, depending upon the nature and timing of interrupts.

The failure is intermittent but repeatable on certain OSs, the exact nature of the problem is under investigation.

Work-arounds:

The work-around is to permanently wire IOCS16* to ground, putting the device in 16-bit transfer mode.

1. Cut trace between RN58 pin 3 and via.
2. Connect RN58 pin 3 to C91 left side or to via.
3. Cut trace between RN64 pin 3 and via.

4 Connect RN64 pin 3 to C91 left side or to via..