

SPF5024CMBAYES – NXP Standard

Configuration report for PF5024-B OTP program ID: AY rev A

Rev. 1.0 - 1/11/2022

Report

1 General description

The PF5024 is a power management integrated circuit (PMIC) featuring multiple high efficiency buck regulators designed to operate as a stand alone regulator or as a companion chip to a larger PMIC.

Built-in one time programmable memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states.

Note: Electrical characteristics are maintained in the PF5024 data sheet

2 Features and benefits

- Up to four high efficiency buck converters
- Watchdog timer/monitor
- Voltage Monitoring circuit to fit ASIL B safety level
- One time programmable device configuration
- 3.4 MHz I2C communication interface
- Integrated Functional Safety to fit ASIL B systems
- 40-pin QFN package with wettable flank and exposed pad

3 Applications

- Automotive Infotainment
- High - End Industrial

4 Ordering information

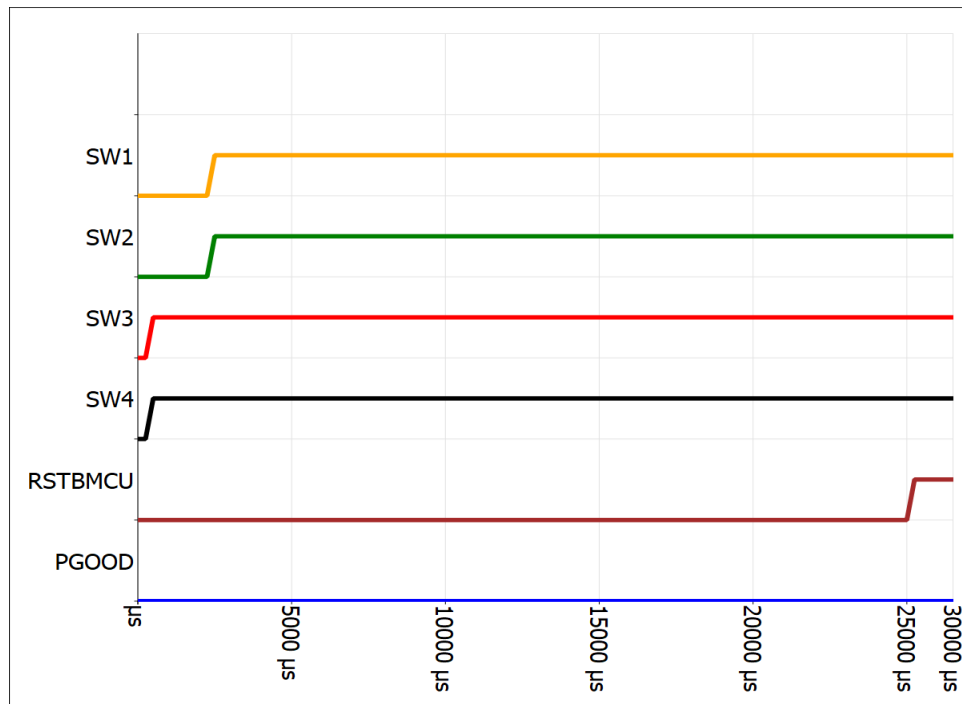
Table 1. Ordering information

Type number ^[1]	Package		
	Name	Description	Version
SPF5024CMBAYES	HVQFN40	HVQFN40, plastic, thermally enhanced very thin quad flat pack; non-leaded wettable flank, 40 terminals; 0.5 mm pitch; 6 mm x 6 mm x 0.85 mm body	SOT618-14

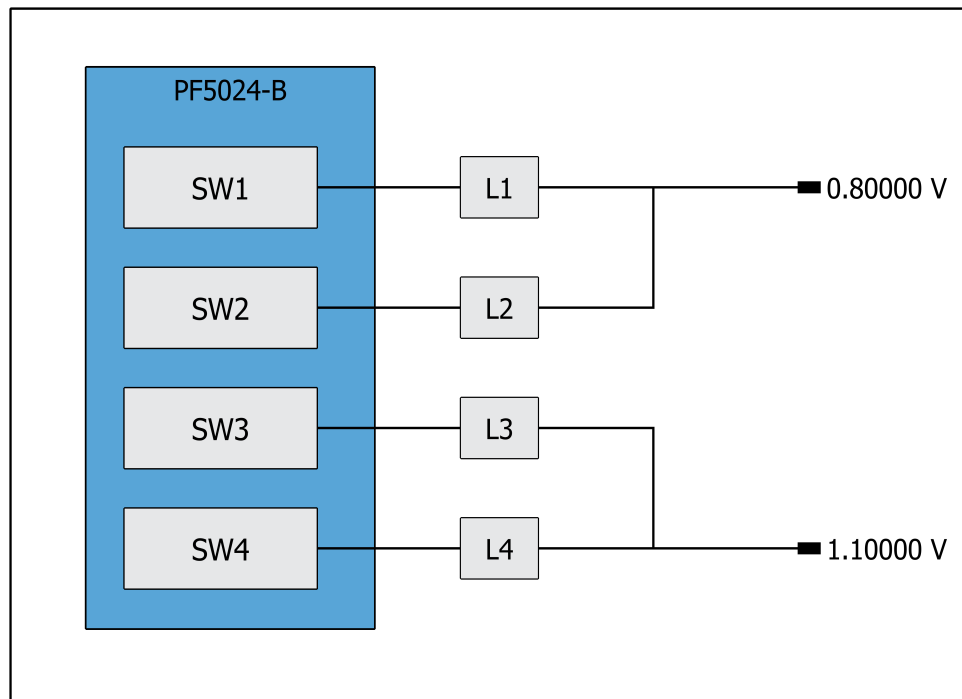
[1] To order parts in tape and reel, add the R2 suffix to the part number.



5 Power-up sequence summary



6 Hardware configuration diagram



7 OTP configuration

See PF5024 datasheet for parametric details. The OTP configuration summary for AY sequence ID is provided in Tables below.

Table 2. Device OTP configuration

Functional block	Feature	OTP selection
I2C Settings	I2C address	0x08
	I2C CRC	Enabled
VIN OV lockout	VIN_OVLO Mode	Enabled
	VIN_OVLO shutdown	Device shuts down upon a VIN_OVLO
	VIN_OVLO debounce	100 μ s
Power good	PG check on power up	PG not checked at power up
	PG active mode	PGOOD mode
PWRON control	Power on event detection	Level sensitive mode
	PWRON debounce	32 ms
	TRESET time	2 s
	TRESET behavior	PMIC shuts down after push button pressed
STANDBY control	STANDBY polarity	Active High
EWARN timer	EWARN delay	100 μ s
XFAIL pin	XFAIL operation	Enabled
WDI control	WDI reset type	Hard WD Reset
	WDI polarity	Rising edge of WDI
	WDI detection in standby	Disabled in STBY
WD timer control	WD timer	WD Timer Disabled
	WD clear window	Cleared within a 50%
	WD window duration	1024 ms

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	WD expire number	Event on step 7
	Maximum WD event counter	15 Events
	WD detection in standby	Disabled in STBY
Frequency control	Nominal switching frequency	2.500 MHz
	Switching Mode	PWM
	FSYNC mode	SYNCOUT
	SYNCIN range	2000KHz to 3000KHz
	SYNCOUT operation	Disabled
	Frequency spread spectrum	Enabled
	FSS range	+/-5%

Table 3. OTP fault management configuration

Functional block	Feature	OTP selection
Fault management	Fault timer	Disabled
	Maximum fault counter	Disabled

Table 4. Sequencer OTP configuration

Functional block	Feature	OTP selection
Power up sequencing	Sequence TBASE	250 μ s
	RESETBMCU sequence slot	Slot 100
	PGOOD sequence slot	OFF
	SW1 sequence slot	Slot 9
	SW2 sequence slot	Slot 9
	SW3 sequence slot	Slot 1
	SW4 sequence slot	Slot 1
Power down sequencing	Power down mode	Group power down
	RESETBMCU Power down	Group 4

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	PGOOD Power down group	Group 2
	SW1 Power down group	Group 2
	SW2 Power down group	Group 2
	SW3 Power down group	Group 4
	SW4 Power down group	Group 4
	RESETBMCU group delay	100 μ s
	Group 1 power down delay	250 μ s
	Group 2 power down delay	250 μ s
	Group 3 power down delay	250 μ s
	Group 4 power down delay	250 μ s
	Power down delay	5.0 ms
	VTT power down	High impedance

Table 5. Regulator OTP configuration

Functional block	Feature	OTP selection
SW1	Output voltage	0.80000 V
	Current limit	4.5 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	DVS ramp	3.91 mV/ μ s
	Switching phase	45°
	Output inductor	1 μ H (Default)
	PGOOD mode	Enabled
	SW1 WD Bypass	Reset on WDI
	SW1 OV Bypass	OV protection enabled

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	SW1 UV Bypass	UV protection enabled
	SW1 ILIM Bypass	ILIM protection enabled
	SW1 Transconductance	65 umho
	SW1 multi-phase selector	SW1/2 dual phase
SW2	Output voltage	0.80000 V
	Current limit	4.5 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	DVS ramp	3.91 mV/μs
	Switching phase	90°
	Output inductor	1 μH (Default)
	VTT mode	Disabled
	PGOOD mode	Enabled
	SW2 WD Bypass	Reset on WDI
	SW2 OV Bypass	OV protection enabled
	SW2 UV Bypass	UV protection enabled
	SW2 ILIM Bypass	ILIM protection enabled
	SW2 Transconductance	65 umho
SW3	Output voltage	1.10000 V
	Current limit	4.5 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	DVS ramp	3.91 mV/μs
	Switching phase	135°

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	Output inductor	1µH (Default)
	PGOOD mode	Enabled
	SW3 WD Bypass	Reset on WDI
	SW3 OV Bypass	OV protection enabled
	SW3 UV Bypass	UV protection enabled
	SW3 ILIM Bypass	ILIM protection enabled
	SW3 Transconductance	65 umho
SW4	Output voltage	1.10000 V
	Current limit	4.5 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	DVS ramp	3.91 mV/µs
	Switching phase	180°
	Output inductor	1µH (Default)
	PGOOD mode	Enabled
	SW4 WD Bypass	Reset on WDI
	SW4 OV Bypass	OV protection enabled
	SW4 UV Bypass	UV protection enabled
	SW4 ILIM Bypass	ILIM protection enabled
	SW4 Transconductance	65 GM
	SW4 multi-phase selector	SW3/4 dual phase
ASIL B functional safety	Fail safe state	FS state Disabled
	Max FS counter	1 Event
	FS self-clear timer	1 Minute

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	Bandgap comparator	Interrupt on BG fault
	I2C secure write	Disabled
PROGRAM ID	Program ID High	A
	Program ID Low	Y

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