Errata

MVPX2ERR/D
Rev. D, 3/2002

MVP X2 Multiprocessor
Evaluation System
Errata

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MVP

1 Introduction

This document describes the known errata and limitations of the MVP reference platform. In all cases, if an errata has a workaround, it is applied to the system before shipped to customers.

The errata revision (“A”, “B”, etc.) is updated every time a new problem is found and systems have been shipped. If your current system is a “MVP X2 rev ‘A’”, then it has all rev “A” fixes, but no rev “B” fixes.

The errata should be applied to the published schematics to determine the correct wiring of the MVP X2 system (i.e. after changes are applied).

Lastly, note that some errata are not true errors but requests for minor modifications to improve the system. These errata are not performed but may be rolled into possible future revisions of the system, if any.

ERRATA

Table 1: Summary of MVP Errata

#	Err	Sev	Problem	Cause	Work-Around	Rev
1	DES	TBD	Inputs to Galileo MPP ports are not 5V tolerant. So sPCIINT, sPCIREQ and SIOINT should be buffered.	Unknown. Not 100% sure this is true -- check w/Galileo.	1. None. X3: Buffer inputs with 5->3V buffers.	A
2	DES	-	~~Clock pins to secondary/5V PCI devices should be 5V.~~ Actually, 3.3V meets VOH of 2.0V.	~~Use of 3.3V clock driver.~~	~~1. None.~~ ~~X3: Buffer outputs with 3->5V buffers.~~	A
3	DES	TBD	FWE* should not be connected to flash; DCS0/2 are used to control flash writes, through MMM FPGA.	Incomplete change from X1.	1. Lift U33 pin 3. X3: U33 pin 3 to MMM FPGA. but nowhere else. May not be needed at all.	A
4	DOC	Min	Direction of ports on page 9 is incorrect.	Changed definition, needed to replace ports.	1. N/A X3: FWE is an output (to flash).	A
5	CAD	Min	Dual serial port header protrudes into gasket area.	Was supposedly moved.	1. None. X3: Move connector backward.	A
6	CAD	Min	C320 is on the bottom of the board.	Too high; should be on the top of the board.	1. Install C320 on the top of the board anyway. Pins are visible between C219 and dual DB9 header X3: Move to top of board.	A
7	D+C	Maj	U29 supplies power to USB ports but is far away.	Did not denote power supply as needing heavy traces.	1. None. X3: Relocate U29 to near USB header (J20). Use 100mil traces between U29 and J20; 6mil is acceptable between U29 and U18 (VIA SIO).	A
8	CAD	Min	LEDs are irregularly spaced and partially under a PCI slot.	None.	1. None. X3: Relocate LEDs and resistors to blank area where metallization copyright is currently located. Also, group the LEDs by function.	A

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#	Err	Sev	Problem	Cause	Work-Around	Rev
9	CAD	TBD	High- and low-side FETs are far apart, and L and R are far apart. Not optimal placement.	None.	1. None X3: Exchange placement of Q2/Q4 w/L1/L2, resp.	A
10	TBD	Min	J17/J18 are hard to access.	None.	1. None X3: Relocate further away, out of congested route area. Change so both have the same orientation. Change to keyed, shrouded headers.	A
11	TBD	Maj	No clocks.	Documentation appears to say it is not needed.	1. Install R4. X3: Connect SYSCLK to TCLK. Delete resistor?	A
12	DES	Maj	AD[27:19] have changed definitions for configuration options. The new defaults need pulldowns. According to Galileo, only AD23 is critical.	Changed pin definitions.	See details on page 12. X3: Change AD[27:25] & AD[23:19] to pulldowns. Change AD24 to pullup/pull-down option (use reserved switch).	A
13	CAD	Min	Mounting hole MH9 is offset.	Layout error.	1. None. X3: Reposition MH9 to correct location.	A
14	TBD	TBD	Soft power switch does not work.	TBD.	1. Install jumper across PSON pins on the chassis header. X3: TBD.	A
15	DES	Min	COP signals pulled to OVDD instead of VCC_3.3	Wrong component used.	1. None X3: Change to VCC_3.3 pullup variant.	A
16	DES	Min	QACK* not buffered. If COP controller pulls high, it will pull to 3.3V and violate OVDD limitations.	Don’t use QACK.	1. Remove or cut pin 2 of J11 and J12. X3: Disconnect QACK*.	A

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#	Err	Sev	Problem	Cause	Work-Around	Rev
17	CAD	Min	Ferrites positioned far from J20/J22. Less effective.	Layout issue.	1. None X3: Move closer to connector. Insure power ferrites have 50 mil traces.	A
18	CAD	Min	TS/AACK/TA test point not on top of board.	Layout issue.	1. None X3: All TP's with property "TOP" must be on the top of the board.	A
19	TBD	Maj	Galileo arbiter GT_BR* function to BR1* pin.	Rev A changed.	1. TBD X3: Connect GT_BR* to new pin.	A
20	DES	Min	R160 (second CPU interrupt) resistors still listed as no_stuff.	Missed change.	1. Stuff R160 w/0 ohm resistor. X3: Delete it.	A
21	MFG	Maj	Y1 seems to be a random values.	TBD	1. Insure Y1 is a 48 MHz oscillator. X3: Check P/N accuracy.	A
22	DES	Min	IDSEL resistor is in CBE path instead of sAD[20] path. Also, it should be 10 ohms.	Unknown?	1. None X3: Move to IDSEL path and change value.	A
23	CAD	Min	"Service Interrupt" silkscreen occluded by mounting hole.	None.	1. None X3: Rename to 'Service'.	A
24	-	-	Internal arbiter now preferred.	None.	1. Install R161-R166 (0 ohm). 2. Do not program arbiter FPGA (or erase it). X3: Delete No_stuff from R161-R166.	A
25	-	-	Preferred V'ger power supply is 1.65V.	Changed for better Fmax.	(replaced with errata #47) X3: Delete No_stuff from R152/R179 No_stuff R175/R178.	A

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#	Err	Sev	Problem	Cause	Work-Around	Rev
26	-	-	Separate switches must be moved to switch between MPX and 60X bus mode.	-	None. X3: Use MMM to drive active high and active low MPXBus signals to CPU and discovery using one switch.	A
27	-	-	MPC7450 symbol bodies reveal unsupported functions.	Spec change.	None. X3: Update symbols.	A
28	DES	Min	Cannot probe inter-CPU interrupt traces.	-	None. X3: Add test points.	A
29	DES	TBD	BADR not buffered to flash, could have incorrect timing relative to buffered address signals.	TBD	None. X3: Buffer BADR equivalent to latched addresses.	A
30	SCH	Min	Flash address confusing.	-	None. X3: Describe addressing with notes.	A
31	-	-	Cannot see some silk screen labels due to heatsink or other causes.	-	None. X3: Relocate U1/U2 labels (“Primary” and “Secondary” to outside of heatsink area.	A
32	-	-	Silk screen generally too large (Tyco changed to insure high yield)	-	None. X3: Force PCB vendor to print as-is? Disclaim rejection of s/s misprints?	A
33	-	-	Cannot tell which DIMM socket is first.	-	None. X3: Add symbolic labels for DIMMs (DIMM #1/First, etc). Shrink existing outline if needed.	A
34	-	-	Fan sinks not using standard 3-pin header.	-	None. X3: Use standard PC fans (+12V, GND, Tach).	A

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#	Err	Sev	Problem	Cause	Work-Around	Rev
35	-	-	Some components are non-standard (0603) and should have been.	-	None. X3: Change: R240 R249	A
36	-	-	Some reports of sensitivity to noise on ARTRY, particularly when L1 is active.	-	None. X3: Investigate. Possibly allow for stronger pullup (500-2K) if noise is found and/or cache problems are found.	A
37	DES	Min	Inductors for CPU core supplies are shown as 25A, worrying customers.	Availability of high-current inductors limited choices.	None. X3: Put a note, perhaps find a smaller inductor.	A
38	DES	Min	None. ECC pins are scrambled on the GT64260 schematic symbol, but this does not affect operation in ECC/RMW modes as GT allows bit-repositioning.	Unknown.	None. X3: Fix schematic symbol.	A
39	-	-	Add GBL* to the Mictor header list.	-	None. X3: Add to spare Mictor pins.	A
40	DES	Maj	Ethernet not working.	Center tap reference was not moved to TDTAP when port was converted from switch- to NIC-mode.	See details on page 13. If errata #44 workaround is implemented, skip. X3: Move tap reference from RDTAP to TDTAP.	B
41	CAD	Maj	C302 and C133 should both be 1.0 uF ceramic caps. C133 is not, allowing excessive noise into the switcher.	Packaging error.	1. Connect 1.0uF ceramic across or in place of C133. X3: Correct component.	B
42	D+C	TBD	No bulk capacitors located at ATX power entry area for +12V, -12V.	Oversight.	1. Connect radial 100uF >=20V electrolytic capacitor under board J8 from pins 10 (+) to pin 7 (GND). X3: Add bulk capacitance at ATX power connector area. Also add near PCI slots.	B

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#	Err	Sev	Problem	Cause	Work-Around	Rev
43	?	?	Transient corruption of RTC and NVRAM in VIA component.	-	Under investigation. X3: Add bulk capacitance near VIA as well.	B
44	LIB	MAJ	Ethernet won't work reliably on 10baseT. Works on 100baseT.	The NPI 6120-37 is actually a 100baseFX transformer, not appropriate for 10baseT	1. None. X3: Replace with Pulse H1102.	B
45	DES	MAJ	Second CPU will not run/run well over 600 MHz due to poor placement of power supply filtering capacitors.	-	See details on page 15. X3: Add additional tantalum capacitors to the opposite side of CPU #2.	B
46	DES	MAJ	Second CPU will not run/run well over 600 MHz due to excessive voltage drop over current sense resistor.	Incorrectly believed 0.005 was close enough to 0.0028. At these current ratings, it isn't. Recheck math.	1. Remove R217. Replace with very heavy wire or copper braid. 2. Remove R218. Replace with very heavy wire or copper braid. X3: See #45.	B
47	DES	MAJ	Second CPU will not run/run well over 600 MHz due to excessive voltage drop over current sense resistor.	-	1. Boost VCore by 0.050 V from 1.65V to 1.70 V to compensate for losses across sense resistors (even when replaced with wire): R179, R180, R181 - Nostuff R178-R177 - Stuff 0 ohms/wire R153-R176,R152 - Nostuff R175, R174 - Stuff 0 ohms/wire X3: Review layout; insure sufficient power vias allow for attachment to VCore pins. Don't via down from top layer to attach power.	B
48	?	?	Multiprocessing synchronization of timebases would be easier with an MPP-pin-controlled TBEN connection.	-	1. Use software HID0.TBEN. X3: Use one spare MPP pin to control TBEN in common to all CPU's.	B

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#	Err	Sev	Problem	Cause	Work-Around	Rev
49	DES	MAJ	No USB power	-1/-2 parts differ only in polarity of enable signal used. Wrong component used.	Do either: 1. Replace U29 with Micrel MIC2526-1 or: 1. Lift U29 pins 1 and 4. 2. Connect lifted pins 1 and 4 to U29 pin 6 (ground) X3: Change part or change enables .	C
50	DES	MIN	IDE disk not functional	DA(2:0) connected incorrectly.	1. Lift U18 pins 67 and 70. 2. Connected lifted pin 67 to pad under 70. 3. Connect lifted pin 70 to pad under 67. (or cut traces before pads and crosswire -- whichever is convenient). X3: Rotate DA(2:0) bus.	C
51	DES+ COMP	MAJ	MPC972 is not process-enhanced to do 133 MHz, despite claims.	Chip too slow? Filter?	TBD	C
52	DES	-	Move USB sense to other GPIO pins so internal I2C may be used.	-	None. X3: Move connections.	C
53	DES + CHIP	MIN	Oscillator requires 2 10pF caps.	No VIA documentation.	None. X3: Add caps.	C
54	DES	MIN	Need to be able to reset NVRAM.	-	None. X3: Add grounded jumper to VBAT.	C
55	TBD	-	ROM LED doesn’t seem to track activity correctly.	TBD	TBD.	C
56	DES	MIN	Cannot wire-OR DASP* from IDE drivers, need diode merge.	Error.	None. X3:	C

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#	Err	Sev	Problem	Cause	Work-Around	Rev
57	MIN	-	Preferred GT clock arrangement is TCLK, with SYSCLK grounded.	None.	None. X3: Ground SYSCLK.	C
58	CHIP	TBD	CSTIMING is tristated for >=2 clocks after reset; requires external pullup.	Chip errata.	1. Add 10K pullup to OVDD; OR 1. Enable pullup in FPGA. X3: Add pullup.	C
59	CAD	MAJ	Slots are in wrong order!	Layout error.	1. None X3: Put slots in correct order.	C
60	-	-	No need to buffer COP to OVDD, standard required COP to do that.	Unclear spec.	None. X3: Remove COP signals from FPGA path, except for reset signals to be merged.	C
61	DES	TBD	IDE pullups need tweaking for ATA66	None.	None. X3: Adjust per IDE spec.	C
62	DES	TBD	SPKR should be pulled down.	None.	1. Set bits in S/W. X3: Add pulldown.	C
63	CAD	Maj	Slots are numbered wrong. What should be 1-2-3-4 is in fact 2-1-4-3.	Slots follow the order of schematic sheets, left-to-right progressing with each page. In addition, slots follow increasing IDSEL numbers.	1. None. Just confusing. Possibly add label to slots. X3: Reorder slots per spec.	C
64	-	-	Slots should start numbering at AD16 per some interpretations of PCI spec.	Open. True?	None. X3: Reorder slots.	C
65	DES	Maj	VCCA filter for MPC961C should be 270 ohms when used at 3.3V.	Misread spec; 10-15 ohm is only for 2.5VIO.	1. Replace R240 (10ohm) with 270 ohm. 2. Update BOM. X3: Change component.	C
66	CAD	Min	Label IDE slots as Primary/Secondary	None.	None. X3: Label slots.	C

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#	Err	Sev	Problem	Cause	Work-Around	Rev
67	Des	Min	Port92 reset inoperable.	Port92 strobes INIT, not PICRST.	None. X3: Incorporate INIT as reset term.	C
68	Des	Maj	Erratic memory clock stability.	VCCA is hardwired to 3.3V, bypassing filter.	1. Tbd. X3: Remove extra VCC3.3 power.	C
69	Des	Maj	IDE Data bus is backwards	Sigh.	1. None, software? Twisty cable? X3: Fix..	C
70	CAD	Avg	AT Keyboard is supposed to be bottom, as noted on schematic and UM.	Geometry of dual DIN6 wrong.	1. None. X3: Fix geometry.	C
71	Des	-	Add SMI# to CPU SMI*?	None.	1. None. X3: Investigate.	C
72	Des	-	Use X5R for AVDD caps, not Y5V.	None.	1. None. X3: Investigate.	C
73	Des	Maj	IDE chip select paris are reversed.	What's the point, I give up.	1. None. X3: DCSxA is the primary chip selects, DCSxB is the secondary..	C
74	Des	Maj	Corruption of NVRAM and RTC.	VIA PWRGD not driven by MMM due to lack of PWRGD from power supply.	1. Cut trace exiting pin 138 of U6 (Via). 2. Connect wire from pin 138 to U23 pin 2 (5V reset). 3. Lift U23 pin 1. 4. Connect U23 pin 1 to J8 pin 8 (pwrgood) X3: As above.	D
75	CAD	Min	PCI clock traces not shortened.	PCI clock traces should be pre-emptively shortened by 1.5" to allow for PCI card clock trace length.	1. None. X3: Investigate.	D

Table 1: Summary of MVP Errata

#	Err	Sev	Problem	Cause	Work-Around	Rev
76	D+M	TBD	BVSEL and L3VSEL resistors not correct.	No_Stuff property missing.	1. Insure that R169, R170, R8 and R151 are not populated. X3: Correct options.	E

Errata 12: Configuration Level

OVERVIEW

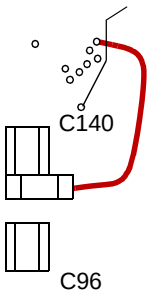
The configuration option for GT64260A has changed.

WORKAROUND

1. On the top of the board, cut the trace exiting RN52 pin 1.
2. On the bottom of the board, beneath RN52, attach as shown:

A) Connect a 4.7K 0805 or larger resistor to C140. The left side of C140 is connected to the resistor, but not the right side.

B) Connect a wire from the right side of the resistor to the via shown:



Errata 40: Transformer rewire

OVERVIEW

The bias power is on the wrong pin.

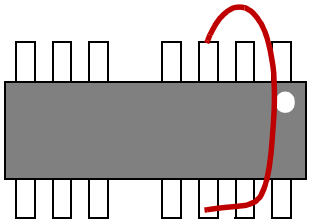
DO NOT PERFORM THIS ERRATA IF ERRATA CORRECTION #44 IS IMPLEMENTED.

WORKAROUND

1. Rework transformers as shown

   A) Lift T1/T2 pin 14

   B) Connect T1/T2 pin 3 to pad under pin 14, using 20-26 gauge wire.



NOTE: T1 and T2 have different orientations.

NOTE: T1 and T2 are considered to be 16-pin devices, despite the missing pins.

Errata 44: Transformer replacement

OVERVIEW

The ethernet transformers are incorrect.

WORKAROUND

1. Remove transformers T1 and T2.

2 Attach Pulse Engineering H1102 transformers in place, using short wires between the transformer and the pad, as in the following list:

PCB PAD	H1102 PIN
1	1
3	2
2	3
8	16
6	15
7	14
16	6
14	7
15	8
9	11
11	10
10	9

NOTE: T1 and T2 have different orientations.

NOTE: T1 and T2 PCB pads are considered to be 16-pin devices, despite the missing pins.

Errata 46: CPU2 Power Supply Fix

OVERVIEW

Lack of bypass capacitors on one side of CPU #2 limits Fmax.

WORKAROUND

1. Add capacitors across C126 and C310 on the bottom of the board beneath U2. Connect either:

   A) two 600-800 uF 6-10V OSCON capacitors, or

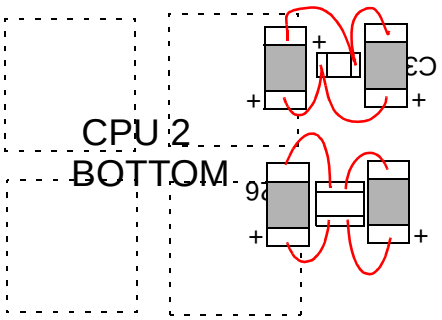
   B) four 470 uF 6-10V tantalum capacitors.

2) Connect as shown for either type, observing capacitor polarity.

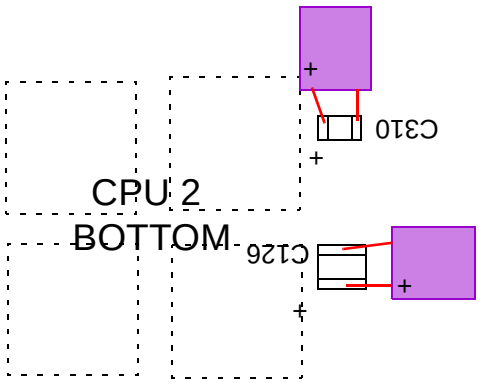
   A) C126 ground is to the right/toward the PCI slots.

   B) C310 ground is towards the bottom (toward U1).

With Tantalum caps:



With OSCON caps:



Version	Date	Changes
A	2001 Oct 04	Initial Errata
B	2001 Nov 28	Updates
C	2001 Dec 12	Added USB power issue, IDE, VCCA.
C	2002 Feb 25	Added errata #44 workaround details.
D	2002 Mar 20	Added RTC/NVRAM fix.

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