Product Type	Integrated Communication Processor
Freescale Part #	MPC184VF
Name	Eos
Package	252 MAP BGA

		Max Key Size (bits)
Algorithms	DES (ECB, CBC)	56
	3DES (ECB, CBC)	168 (3-keys)
	AES (ECB, CBC, CTR, CCM)	256
	ARC-4	128
	MD-5+ HMAC	(up to 512 bit keys)
	SHA-1+ HMAC	(up to 512 bit keys)
	SHA-256+ HMAC	(up to 512 bit keys)
	RSA Digital Signature	2048-bit operands
	RSA Digital Verify	2048-bit operands
	ECC Digital Signature	512-bit field or modulus size
	ECC Digital Verify	512-bit field or modulus size
	RNG	On chip 32-bit

Target Applications :
DSLAMs, Broadband Gateways, mid-range routers, wireless access points, telecom equipment

Export Control Info:
Harmonized Tariff (US): 8542.31.0000
ENC Status: Restricted. US EAR part 740.17(b)(2)
ECCN: 5A002
CCAT: G026024

Overview:
The MPC184 is a memory-mapped device designed to interface to 32-bit PCI busses, or the 8xx bus of processors implementing the PowerQUICC 1 architecture. The MPC184 is capable of acting as a bus master, or as a bus slave. With the MPC184 in slave mode, an application being executed on a host processor can accelerate cryptographic functions by writing instructions, keys, and data to the MPC184, and reading the result. Alternately, the MPC184 can act as a bus Master. In this mode, the host processor determines which cryptographic function needs to be performed on a block of data, and creates a descriptor (in system memory) which describes the function to perform, and the location of the data in memory. The host writes a pointer to the descriptor directly to the MPC184, and the MPC184 fetches all additional instructions and data required to complete a high level cryptographic function. Upon completion of processing, the MPC184 writes the permuted data back to memory. The MPC184 is expected to achieve 200+ public key exchanges per second, and ~300Mbps 3DES throughput..