

### 1 General description

The PF8250 is a power management integrated circuit (PMIC) designed for high performance i.MX 8 and S32V based applications. It features seven high efficiency buck converters and four linear regulators for powering the processor, memory and miscellaneous peripherals. It meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 2 qualified.

Built-in one time programmable memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states.

Note: Electrical characteristics are maintained in the PF8150\_PF8250 data sheet

### 2 Features and benefits

- Up to seven high efficiency buck converters
- Four linear regulators with load switch options
- RTC supply and coin cell charger
- Watchdog monitoring
- Independent OV/UV monitoring circuits
- One-time programmable device configuration
- 3.4 MHz I2C communication interface
- 56-pin 8 x 8 QFN package
- AEC-Q100 grade 2 qualified
- Safety mechanisms to fit ASIL B applications

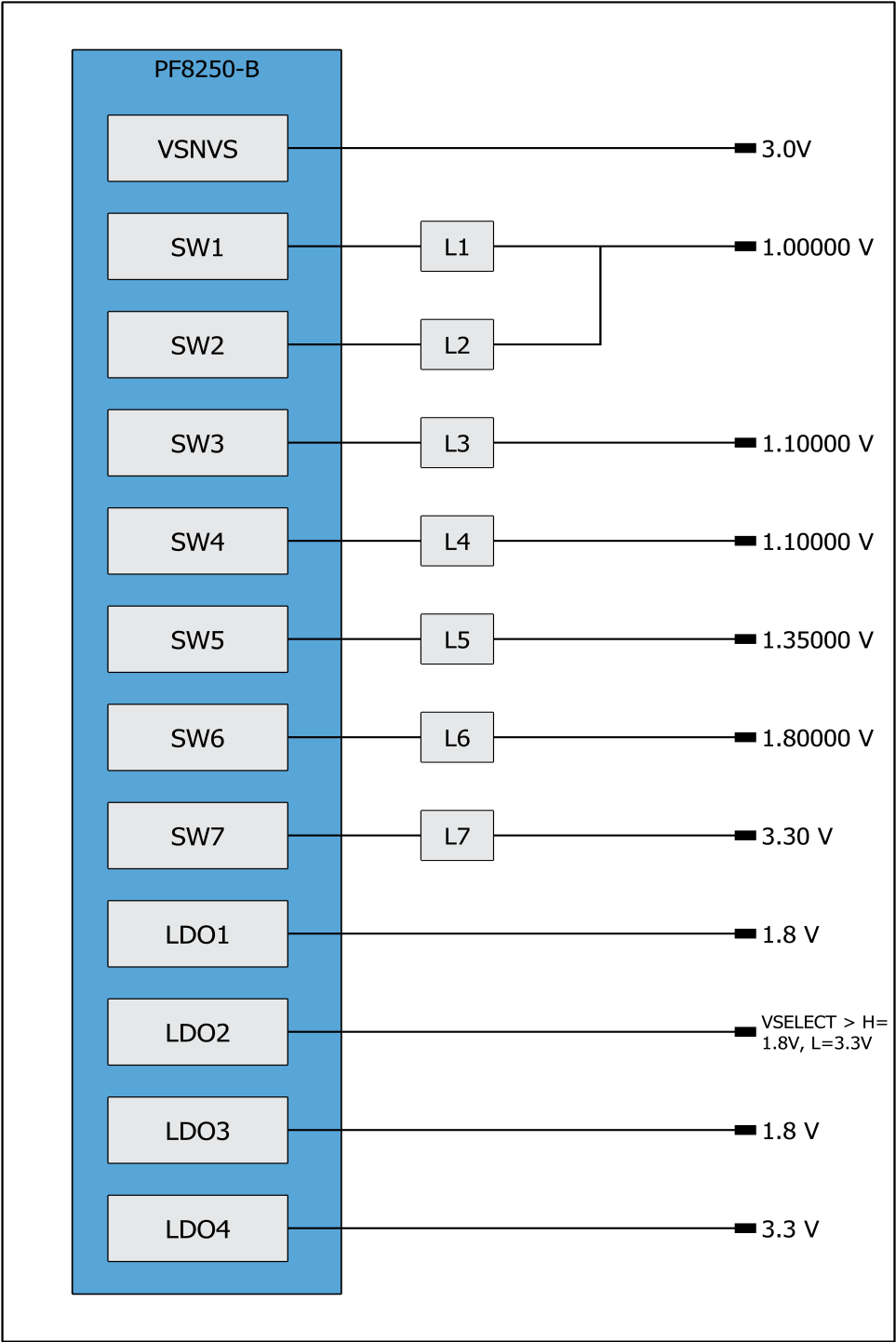
### 3 Applications

- Automotive Infotainment
- High-end consumer and industrial





6 Hardware configuration diagram



## 7 OTP configuration

See PF8150\_PF8250 data sheet for parametric details. The OTP configuration summary for DF (sequence ID) is provided in Tables below.

Table 2. Device OTP configuration

Functional block	Feature	OTP selection
System configuration	I2C Address	0x08
	I2C CRC	Enabled
	I2C Secure Write	Secure Write Disabled
	VIN OVLO Monitor	VIN_OVLO Enabled
	VIN OVLO Debounce	100µs
	VIN OVLO Shutdown	VIN_OVLO Shutdown Disabled
	Maximum Fault Count	Disabled
	Fault Timer	DISABLED
	Fail Safe State	FailSafe Disabled
	Fail-safe Maximum Count	15
	Fail-safe OK Timer	60 min
Watchdog monitoring	WDI Mode	Hard WD Reset
	WDI Polarity	WD event detected on rising edge
	WDI In Standby	WDI event Disabled in Standby
	WD Counter	WD Timer Disabled
	WD Counter In Standby	WD Timer Disabled in Standby
	WD Clear Window	Clear within 100% of window
	Maximum Time Out Steps	7
	WD Duration	1024 ms
	Maximum WD Event	15

## Configuration report for PF8250-B OTP program ID: DF rev A

Clock management	Switching Frequency	2.5 MHz
	SYNCIN Range	2000KHz to 3000KHz
	SYNCIN Operation	Disabled
	SYNCOUT Operation	Disabled
	Frequency Spread Spectrum	Frequency Spread Spectrum Disabled
	FSS Range	FSS Range set to 5%
COINCELL Control	Coin Cell Charging Voltage	3.0 V

Table 3. I/Os configuration

Functional block	Feature	OTP selection
I/O Configuration	PWRON Mode	Level Sensitive
	PWRON Debounce	32 msec
	PWRON Reset Mode	Shut down >TRESET
	TRESET Delay	2 sec
	STANDBY Polarity	STANDBY Active High
	PGOOD Pin Mode	PGOOD Indicator
	OV/UV Check On Power Up	PGOOD monitoring on PWRUP disabled
	EWARN Time	5ms
	XFAILB Operation	XFAILB Operation Enabled
	FSOB Soft Fault Event	Event does not assert FSOB
	FSOB Hard Fault Event	Event does not assert FSOB
	FSOB WDI Event	Event does not assert FSOB
	FSOB WDC Event	Event does not assert FSOB
	FSOB Operating Mode	Active Safe State Disabled

## Configuration report for PF8250-B OTP program ID: DF rev A

Table 4. Sequencer configuration

Functional block	Feature	OTP selection
SW configurations	SW1 Multiphase Selector	SW1/2 Dual Phase
	SW4 Multiphase Selector	SW3/4 Single Phase
	SW5 Multiphase Selector	SW5/6 Single Phase
	Default SW Operation	SW Regulators Default in PWM mode
	SW6 VTT Mode	VTT Mode Disabled
	VTT Discharge Mode	VTT Output Disable in HI-Z
	Bandgap Monitor Reaction	BGMON shutdown Bypassed
Power-up sequence	Sequencer Time Base	250 $\mu$ s
	SW1 Sequence	Slot 0
	SW2 Sequence	Slot 0
	SW3 Sequence	OFF
	SW4 Sequence	OFF
	SW5 Sequence	Slot 2
	SW6 Sequence	Slot 2
	SW7 Sequence	Slot 2
	LDO1 Sequence	Slot 0
	LDO2 Sequence	Slot 2
	LDO3 Sequence	OFF
	LDO4 Sequence	OFF
	RESETBMCU Sequence	Slot 20
	PGOOD Sequence	Slot 20
Power down sequence	Power Down Mode	Mirror power up sequence

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	SW1 Power Down Group	Group 4 (1st)
	SW2 Power Down Group	Group 4 (1st)
	SW3 Power Down Group	Group 4 (1st)
	SW4 Power Down Group	Group 4 (1st)
	SW5 Power Down Group	Group 4 (1st)
	SW6 Power Down Group	Group 4 (1st)
	SW7 Power Down Group	Group 4 (1st)
	LDO1 Power Down Group	Group 4 (1st)
	LDO2 Power Down Group	Group 4 (1st)
	LDO3 Power Down Group	Group 4 (1st)
	LDO4 Power Down Group	Group 4 (1st)
	RESETBMCU Power Down Group	Group 4 (1st)
	PGOOD Power Down Group	Group 4 (1st)
Power Down Delays	Group 1 Power Down Delay	120 µs
	Group 2 Power Down Delay	120 µs
	Group 3 Power Down Delay	120 µs
	Group 4 Power Down Delay	120 µs
	RESETBMCU Group Delay	10 µs
	Power Down Delay	5 ms

Table 5. Switching regulators

Functional block	Feature	OTP selection
SW1	SW1 Output Voltage	1.00000 V
	SW1 DVS Ramp	7.813/5.208 mV/µs
	SW1 UV Threshold	93%

## Configuration report for PF8250-B OTP program ID: DF rev A

	SW1 OV Threshold	107%
	SW1 Current Limit	4.5 A
	SW1 Inductor	1 $\mu$ H
	SW1 Phase	0°
	SW1 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW1 WD Bypass	Regulator reacts upon a Watchdog
	SW1 OV Bypass	OV Protect Enabled
	SW1 UV Bypass	UV Protect Enabled
	SW1 ILIM Bypass	ILIM Fault Bypassed
SW2	SW2 Output Voltage	1.00000 V
	SW2 DVS Ramp	7.813/5.208 mV/ $\mu$ s
	SW2 UV Threshold	93%
	SW2 OV Threshold	107%
	SW2 Current Limit	4.5 A
	SW2 Inductor	1 $\mu$ H
	SW2 Phase	225°
	SW2 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW2 WD Bypass	Regulator reacts upon a Watchdog
	SW2 OV Bypass	OV Protect Enabled
	SW2 UV Bypass	UV Protect Enabled
	SW2 ILIM Bypass	ILIM Fault Bypassed
SW3	SW3 Output Voltage	1.10000 V
	SW3 DVS Ramp	7.813/5.208 mV/ $\mu$ s
	SW3 UV Threshold	93%

## Configuration report for PF8250-B OTP program ID: DF rev A

	SW3 OV Threshold	107%
	SW3 Current Limit	4.5 A
	SW3 Inductor	1 $\mu$ H
	SW3 Phase	0°
	SW3 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW3 WD Bypass	Regulator reacts upon a Watchdog
	SW3 OV Bypass	OV Protect Enabled
	SW3 UV Bypass	UV Protect Enabled
	SW3 ILIM Bypass	ILIM Fault Bypassed
SW4	SW4 Output Voltage	1.10000 V
	SW4 DVS Ramp	7.813/5.208 mV/ $\mu$ s
	SW4 UV Threshold	93%
	SW4 OV Threshold	107%
	SW4 Current Limit	4.5 A
	SW4 Inductor	1 $\mu$ H
	SW4 Phase	225°
	SW4 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW4 WD Bypass	Regulator reacts upon a Watchdog
	SW4 OV Bypass	OV Protect Enabled
	SW4 UV Bypass	UV Protect Enabled
	SW4 ILIM Bypass	ILIM Fault Bypassed
SW5	SW5 Output Voltage	1.35000 V
	SW5 DVS Ramp	7.813/5.208 mV/ $\mu$ s
	SW5 UV Threshold	93%

## Configuration report for PF8250-B OTP program ID: DF rev A

	SW5 OV Threshold	107%
	SW5 Current Limit	4.5 A
	SW5 Inductor	1 $\mu$ H
	SW5 Phase	45°
	SW5 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW5 WD Bypass	Regulator reacts upon a Watchdog
	SW5 OV Bypass	OV Protect Enabled
	SW5 UV Bypass	UV Protect Enabled
	SW5 ILIM Bypass	ILIM Fault Bypassed
SW6	SW6 Output Voltage	1.80000 V
	SW6 DVS Ramp	7.813/5.208 mV/ $\mu$ s
	SW6 UV Threshold	93%
	SW6 OV Threshold	107%
	SW6 Current Limit	2.6 A
	SW6 Inductor	1 $\mu$ H
	SW6 Phase	90°
	SW6 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW6 WD Bypass	Regulator reacts upon a Watchdog
	SW6 OV Bypass	OV Protect Enabled
	SW6 UV Bypass	UV Protect Enabled
	SW6 ILIM Bypass	ILIM Fault Bypassed
SW7	SW7 Output Voltage	3.30 V
	SW7 UV Threshold	93%

## Configuration report for PF8250-B OTP program ID: DF rev A

	SW7 OV Threshold	107%
	SW7 Current Limit	2.6 A
	SW7 Inductor	1 $\mu$ H
	SW7 Phase	270°
	SW7 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW7 WD Bypass	Regulator reacts upon a Watchdog
	SW7 OV Bypass	OV Protect Enabled
	SW7 UV Bypass	UV Protect Enabled
	SW7 ILIM Bypass	ILIM Fault Bypassed

Table 6. LDO regulators

Functional block	Feature	OTP selection
LDO1	LDO1 Output Voltage	1.8 V
	LDO1 UV Threshold	93%
	LDO1 OV Threshold	107%
	LDO1 PGOOD Control	Reg. is part of AND function to control PGOOD
	LDO1 WD Bypass	Regulator reacts upon a Watchdog
	LDO1 Mode	Normal Mode
	LDO1 OV Bypass	OV Protect Enabled
	LDO1 UV Bypass	UV Protect Enabled
	LDO1 ILIM Bypass	ILIM Fault Bypassed
LDO2	LDO2 Output Voltage	3.3 V
	LDO2 UV Threshold	93%
	LDO2 OV Threshold	107%
	LDO2 PGOOD Control	Reg. is part of AND function to control PGOOD

## Configuration report for PF8250-B OTP program ID: DF rev A

	LDO2 WD Bypass	Regulator reacts upon a Watchdog
	LDO2 Mode	Normal Mode
	LDO2EN Hardware Control	I2C Control Only
	VSELECT Hardware Control	LDO2 set by VSELECT. Low=3.3V / High=1.8V
	LDO2 OV Bypass	OV Protect Enabled
	LDO2 UV Bypass	UV Protect Enabled
	LDO2 ILIM Bypass	ILIM Fault Bypassed
LDO3	LDO3 Output Voltage	1.8 V
	LDO3 UV Threshold	93%
	LDO3 OV Threshold	107%
	LDO3 PGOOD Control	Reg. is part of AND function to control PGOOD
	LDO3 WD Bypass	Regulator reacts upon a Watchdog
	LDO3 Mode	Normal Mode
	LDO3 OV Bypass	OV Protect Enabled
	LDO3 UV Bypass	UV Protect Enabled
	LDO3 ILIM Bypass	ILIM Fault Bypassed
LDO4	LDO4 Output Voltage	3.3 V
	LDO4 UV Threshold	93%
	LDO4 OV Threshold	107%
	LDO4 PGOOD Control	Reg. is part of AND function to control PGOOD
	LDO4 WD Bypass	Regulator reacts upon a Watchdog
	LDO4 Mode	Normal Mode
	LDO4 OV Bypass	OV Protect Enabled
	LDO4 UV Bypass	UV Protect Enabled

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	LDO4 ILIM Bypass	ILIM Fault Bypassed
VSNVS	VSNVS Output Voltage	3.0V

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