CBTV24DD12

12-bit bus switch/multiplexer for DDR4-DDR3-DDR2 applications

Rev. 1 — 28 August 2014 Product brief

1. General description

CBTV24DD12 is designed for 1.8 V/2.5 V/3.3 V supply voltage operation and it supports Pseudo Open Drain (POD), SSTL_12, SSTL_15 or SSTL_18 signaling and CMOS select input levels. This device is designed for operation in DDR4, DDR3 or DDR2 memory bus systems, with speeds up to 3200 MT/s.

The CBTV24DD12 has a 1 : 2 switch or 2 : 1 multiplex topology and offers a 12-bit wide bus. Each 12-bit wide A-port can be switched to one of two ports B and C, for all bits simultaneously. Each port is non-directional due to the use of FET switches, allowing a multitude of applications requiring high-bandwidth switching or multiplexing.

The selection of the port is by a simple CMOS input (SELect). Another CMOS input (ENable) is available to allow all ports to be disconnected. The SEL0, SEL1 and $\overline{EN}$ input signals are designed to operate transparently as CMOS input level signals up to 3.3 V.

CBTV24DD12 uses NXP's proprietary high-speed switch architecture providing high bandwidth, very little insertion loss, return loss, and very low propagation delay, allowing use in many applications requiring switching or multiplexing of high-speed signals. It is available in a 3.0 mm × 8.0 mm TFBGA48 package with 0.65 mm ball pitch, for optimal size versus board layout density considerations. It is characterized for operation from −10 °C to +85 °C.

2. Features and benefits

2.1 Topology

- 12-bit bus width
- 1 : 2 switch/MUX topology
- Bidirectional operation
- Simple CMOS select pins (SEL0, SEL1)
- Simple CMOS enable pin ($\overline{EN}$)

2.2 Performance

- 3200 MT/s throughput
- 7.4 GHz bandwidth (for both single-ended and differential signals)
- Low ON insertion loss
- Low return loss
- Low crosstalk
- High OFF isolation

- POD_12, SSTL_12, SSTL_15 or SSTL_18 signaling
- Low R_{ON} (8 Ω typical)
- Low ΔR_{ON} (<1 Ω)

2.3 General attributes

- 1.8 V/2.5 V/3.3 V supply voltage operation
- Very low supply current (600 μA typical)
- ESD robustness exceeds 2.5 kV HBM, 1 kV CDM
- Available in TFBGA48 package, 3.0 mm × 8.0 mm × 1 mm size, 0.65 mm pitch, Pb-free/Dark Green

3. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
CBTV24DD12ET	V2412	TFBGA48	plastic low profile fine-pitch ball grid array package; 48 balls; body 3 × 8 × 1 mm; 0.65 mm pitch	SOT1365-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
CBTV24DD12ET	CBTV24DD12ETY	TFBGA48	Reel 13” Q1/T1 *Standard mark SMD dry pack	4500	T_{amb} = −10 °C to +85 °C

4. Functional diagram

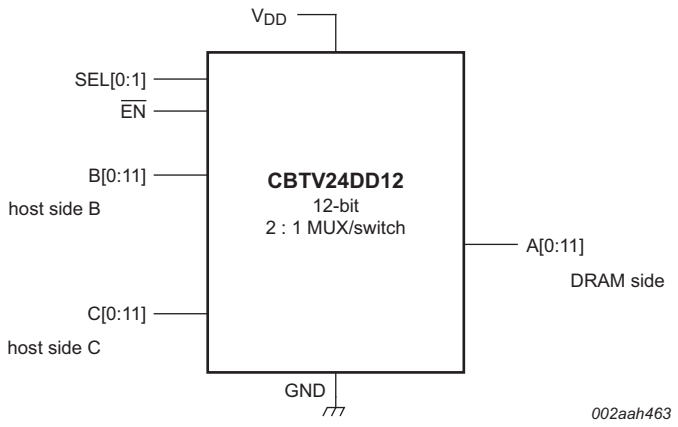
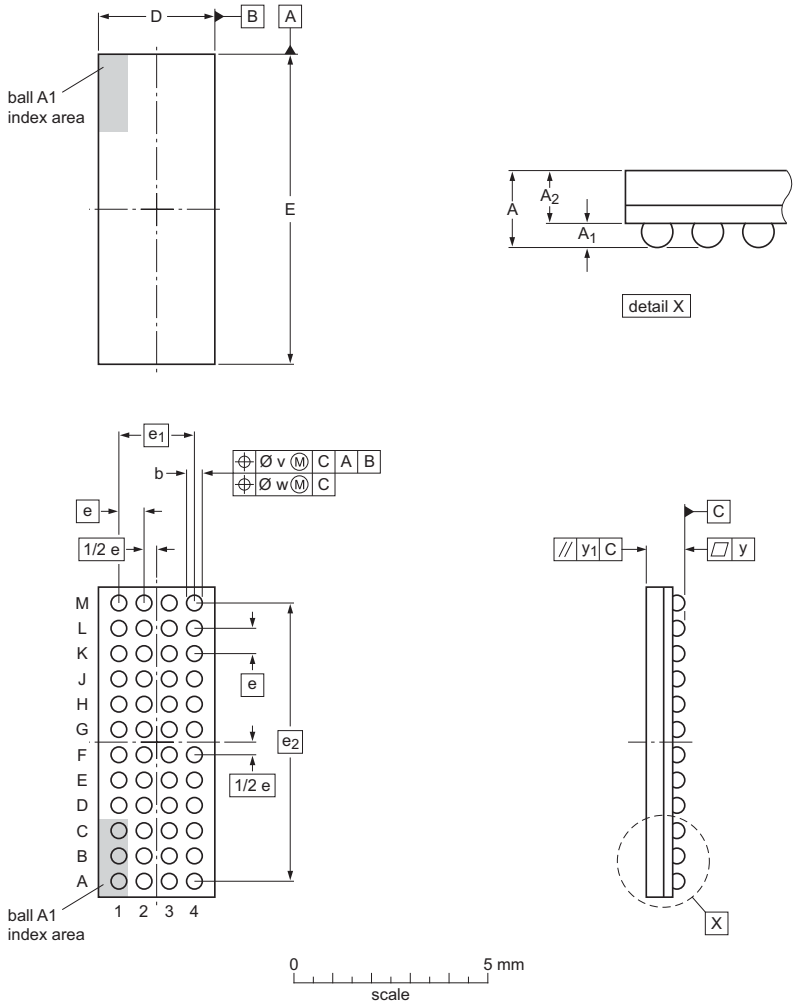


Fig 1. Functional diagram

5. Package outline

TFBGA48: plastic low profile fine-pitch ball grid array package; 48 balls **SOT1365-1**



Dimensions

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.05	0.35	0.73	0.45	3.1	8.1							
	nom	0.98	0.30	0.68	0.40	3.0	8.0	0.65	1.95	7.15	0.15	0.05	0.08	0.1
	min	0.88	0.25	0.63	0.35	2.9	7.9							

sot1365-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1365-1	- - -	- - -	- - -			~~14-01-03~~ 14-08-12

Fig 2. Package outline TFBGA48 (SOT1365-1)

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