Altimus X3B Evaluation Board Errata

Rev. F, 9/2005

1 Overview

This document describes the known errata and limitations of the Altimus PrPMC card for the Sandpoint reference platform. In all cases, if an errata has a workaround, it is applied to the system before shipped to customers.

The errata revision (“A”, “B”, etc.) is updated every time a new problem is found and systems have been shipped. If your current system is a “Altimus X3B rev ‘A’”, then it has all rev “A” fixes, but no rev “B” fixes.

The errata should be applied to the published schematics to determine the correct wiring of the PrPMC+Sandpoint system (i.e. after changes are applied).

Lastly, note that some errata are not true errors but requests for minor modifications to improve the system. These errata are not performed but may be rolled into possible future revisions of the system, if any.

ERRATA

Table 1: Summary of Altimus Errata

#	Type	Problem	Impact	Work-around	Rev
1	Design	No pullup on $\overline{\text{CHKSTP\_IN}}$. Processor immediately check-stops.	CPU halts.	Add pullup between COP header J9 pin 8 and R79 pin 1 (side not connected to J9). X4: Add 10K pullup to COP $\overline{\text{CHKSTP\_IN}}$ port.	A
2	Design	SDRAM BA0/BA1 pins swapped.	None. Banks open 'wrong' banks.	None X4: Correct, if only for clarity.	A
3	Design	MPC107 $\overline{\text{SRESET}}$ output is overdriven by COP buffer. Contention when MPC107 asserted $\overline{\text{SRESET}}$.	Software SRESET* assertion may be unreliable.	None X4: Add $\overline{\text{SRESET}}$ terms to PAL or add open-drain driver to buffered $\overline{\text{COP\_SRESET}}$.	A
4	Design	Pin 5 of COP is not $\overline{\text{QREQ}}$	None.	None X4: Delete $\overline{\text{QREQ}}$ from pin 5.	A
5	Chip	$\overline{\text{MCP}}$ pin is not driven to BVDD levels.	For 2.5V configured devices (MPC7410), excessive voltage may be applied.	None (inaccessible). X4: Route $\overline{\text{MCP}}$ through voltage level buffer U11.	B
6	Design	MPC107 AVDD/LAVDD not connected to 2.5V.	Could cause erratic behaviour, though strangely enough none has been seen. MPC107 PLL voltage may be relatively insensitive.	1. Rotate R56 and R57 such that pad 1 remains attached and pad 2 is disconnected (or use soldermask tape, etc). For R56 (near tantalum C35), pin 2 is near the gold via and 'R56' label. For R57, pin 2 is near R57 s/s (R57 is near tantalum C49). 2. Connect R56 and R57 pads 2 to C35 pin 1 ("+"). X4: Connect R56 and R57 to VCC_2.5.	B
7	CAD DB	LED geometry does not match schematic symbol (cathode is not pin 1) NOTE: the silkscreen is correct. This refers only to Gerber file info not normally seen by customers.	Assembly house would always install LEDs backwards.	1. Install LED's 'backwards'. X4: Delete and reinstall LED symbols to use new geometry.	B
8	ENG	$\overline{\text{QACK}}$ always asserted.	Power management may be difficult.	1. Lift U11 pin 23. 2. Connect U11 pin 26 to pad under U11 23. X4: Delete COP buffer.	C

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#	Type	Problem	Impact	Work-around	Rev
9	ENG	COP buffer not needed.	COP tools must drive only with OVDD.	1. None. X4: Delete COP buffer.	C
10	ENG	In 32-bit bus mode, tlbsync instructions causes hang.	$\overline{\text{TLBISYNC}}$ permanently asserted in 32-bit bus mode.	CUSTOMER/TEST ONLY - NOT DONE BY DEFAULT 1. For customers who wish to implement 32-bit bus mode on the MPC75X, connect wire from R89 pin 1 to CPU_HRST* (R13 pin 2 et. al.). X4: Assert $\overline{\text{TLBISYNC}}$ with $\overline{\text{HRESET}}$ using 0-ohm option resistor.	C
11	DOC	L2OVDD table not accurate for all 360BGA processors.	None.	1. Expand table to include CPU type. X4: Fix schematic notes.	-
12	ARCH	If arbitration is disabled on Sandpoint, SYSCON* is deasserted,and interrupts cannot be received via IRQ0*. SYSCON* should not control whether arbitration is enabled on the PMC.	In Sandpoint PrPMC mode, interrupts cannot be received on IRQ0*.	1. Place a solder ‘blob’ on U2 pins 13 and 14. X4: Connect IRQ0* and INTA#.	D
13	Design	Interrupts not receivable on IRQ0* (in spite of errata #12) when not in SYSCON* mode, which is true on SPX# systems with serial numbers >= 6000, or when SYSCON is not selected.	Lack of interrupts on IRQ0*.	1. Add a wire or solder-bridge across U2 (QS3384) pins 12, 13 and 14. Note: For SPX3 systems <= 5999: Select MPMC mode on the MPMC and SPX3 (SYSCON LED should be active). For X4: Connect INTA# to IRQ0# with no QS involvement (new standard method).	E
14	Device/ Design	The MPC7410 will drive L2ADDR[17] (normally unused) high in 1MB private memory mode or with 2MB L2 configured as half cache, half private memory, it will drive L2ADDR[17] high for the private memory accesses. MPC755-equipped Altimus boards do not need this rework.	Private-memory modes do not work for some modes/sizes (cache works fine).	For MPC7410: 1. On the top of the board, between the processor and the SRAMs, cut the trace shown on the detail view. 2. Change R67 to 22 ohms. This disconnects CA17 from the processor, and R67 pulls CA17 low. For X4: Disconnect CA17.	F

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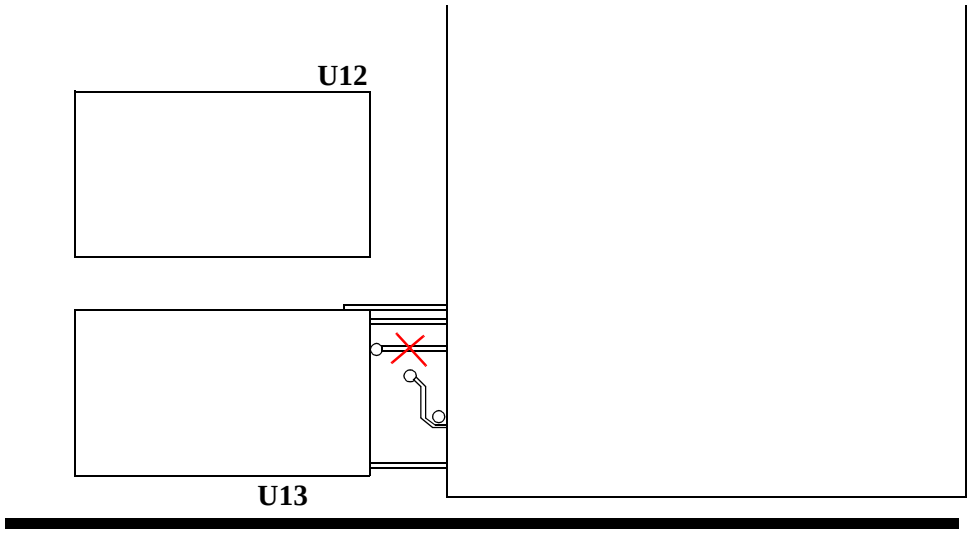
15	Design	The unused cache control signals $\overline{\text{ADV}}$, $\overline{\text{ADSP}}$, $\overline{\text{SW}}$ and $\overline{\text{SE2}}$ should be pulled up to VCACHEIO, not VCACHE.	None; VCACHE is always high (3.3V or 2.5V) enough to register as an unasserted signal.	1. None. For X4: Connect the $\overline{\text{ADV}}$ etc pullup to VCACHEIO.	

Errata 14 Details



Version	Date	Changes
A	2001 Jun 03	Initial Errata
	2002 Jan 03	Updates
B	2002 Jul 25	Added #6, #7
C	2003 Jan 23	Added #8-#11
D	2003 Jan 28	Added #12.
	2003 Jun 5	Corrected #8; pin should be 26, not 25.
E	2003 Jul 15	Added #13.
	2004 Feb 11	Clarify #10, #13.
F	2004 Oct 19	Added #14, #15.
	2005 Sep 25	Clarify #14.

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	2004 Dec 15	Clarified #15